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S.E. Sem. III [CMPN]

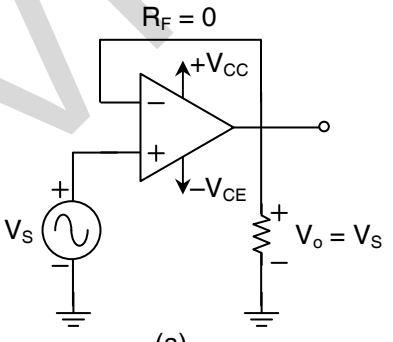
Electronic Circuits and Communication Fundamentals

Prelim Question Paper Solution

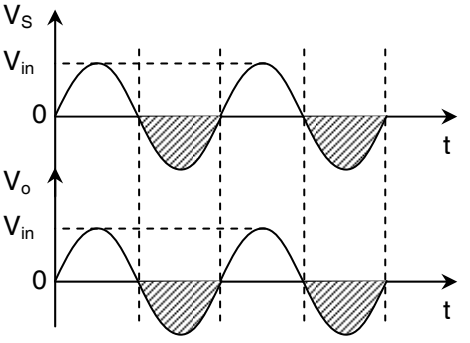
1. (a) Comparison between BJT and FET

	BJT	FET
1)	BJT is a bipolar device, both majority and minority carriers take place in electrical conduction.	FET is an unipolar device, electron current in N–channel and hole current in P–channel.
2)	BJT is current operated device, it is a current controlled current source.	FET is voltage operated device, it is a voltage controlled current source.
3)	BJT has high g_m, and hence provides large gain	FET has low g_m and hence provides low gain.
4)	BJT has low input resistance (Ω–kΩ) ∴ input junction is forward biased.	FET has high input resistance (MΩ) ∴ input junction is reverse biased.
5)	Thermal runaway is possible in BJT. ∴ I_C increases when temperature increases.	Thermal runaway is not possible in FET. ∴ I_D decreases when temperature increases.
6)	BJT can be operated with low values of supply voltage (3 – 10) V	FET requires large supply voltage (> 10) V
7)	BJT is noisy in operation.	FET is less noisy in operation.
8)	Requires large area while fabrication of IC's.	Requires less area while fabrication of IC's.
9)	Less susceptible to damage while handling.	More susceptible to damage while handling.
10)	Very complex biasing circuits required to provide stability.	Biasing circuits are less complex when compared to that of BJT.
11)	Cannot be used as a voltage variable resistance	It can be used as a voltage variable resistance

1. (b) VOLTAGE-FOLLOWER



(a)

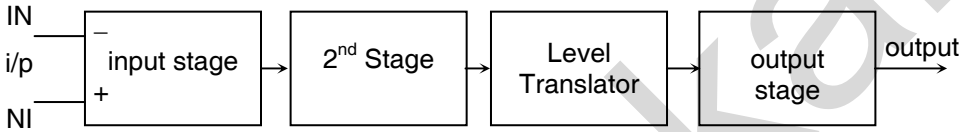


When $R_1 = \infty$ and $R_F = 0$ the non-inverting amplifier gets converted into a voltage follower or unity gain amplifier. When non-inverting amplifier is configured so as to obtain a gain of 1, it is called as voltage follower or unity gain non-inverting buffer.

The schematic diagram for voltage follower is a shown below. The voltage follower configuration in figure (a) is obtained by short circuiting R_F and open circuiting R_1 connected in usual non-inverting amplifier configuration in figure (a).
Thus all the output is feedback to inverting input of OP-AMP.
Therefore the gain of feedback circuit i.e. B = 1

1. (c) OPERATIONAL AMPLIFIER

Block diagram

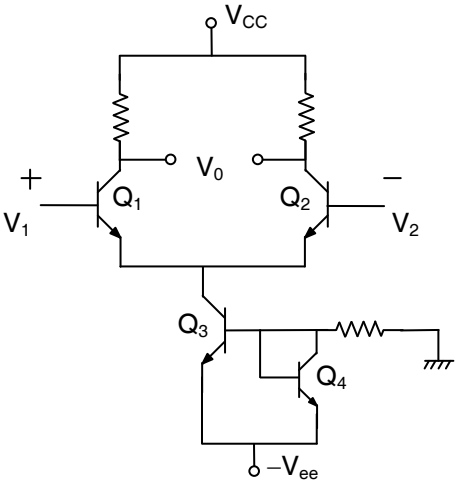


dual i/p balanced o/p diff. amplifier | dual i/p unbalanced o/p diff. amplifier | emitter follower with constant current bias | Complementary symmetry class AB amplifier

The input stage is a dual input balanced output high gain differential amplifier, and has a very high input resistance. This is done by making use of darlington connection or by FET as input stage. The output of the 1st differential amplifier is used to drive dual input unbalanced output differential amplifier. Because of direct coupling, the dc voltage at the output of intermediate stage is above ground potential. Therefore a level shifter is used at the output of 2nd stage to shift the dc level at the output of the intermediate stage down to zero with respect to ground. The level translator is an emitter follower using constant current bias. The final stage is a push pull complementary symmetry amplifier, which increases the output voltage swing and increases the current supplying capability of op–amp.

First stage : Consists of transistors, which form the first differential amplifier stage, using constant current bias provided by transistor at the emitter and associated resistances. This 1st stage has inverting and non-inverting input and hence can be driven with two input's or a single input. The 1st stage establishes.

i) high input resistance
ii) high voltage gain
iii) rejects common signals
iv) eliminates drift
v) provides high CMRR



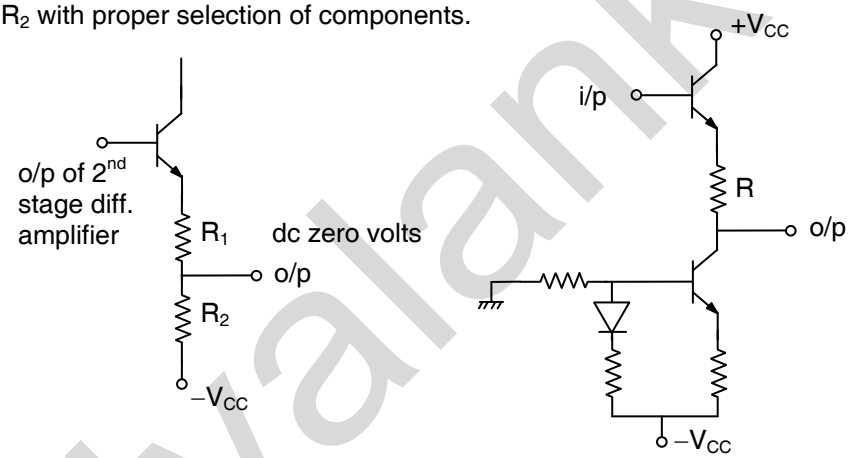
Second Stage : The second differential amplifier is driven from the output of first differential amplifier and uses an emitter bias. This will also amplify the signals. Because of direct coupling used, the dc potential at the collector is well above ground. Hence even if there is no input there is a dc signal output. This is undesirable because it reduces the output swing.

Level Translator

Because of direct coupling used.

i) dc level at the emitter rises from stage to stage. This increase in dc level tend to shift the operating point of succeeding stage and hence limits the output voltage swing and distort the output signal.

ii) This will lead to error in dc signals, when used for dc applications. Hence a level shifting stage is included to shift the output dc level at the second stage down to zero level. The output of the second differential stage is fed to an emitter follower stage with constant current bias. Hence a positive voltage at the collector of second stage can produce zero volts at the junction of R_1 and R_2 with proper selection of components.



1. (d) Need of Modulation in Communication

1) Reduction in the height of antenna :

For the efficient transmission of the signal, the height of antenna should be atleast $\lambda/4$, where λ is the wavelength of the wave and it is the distance traveled by the wave in one cycle duration and $\lambda = c/f$, where 'c' is the velocity of light = 3×10^8 m/s and 'f' is the frequency of the signal to be transmitted.

Consider the baseband signal with f = 15 kHz so $\lambda = \frac{3\times10^8}{15\times10^3} = 20$ kM.

Therefore, minimum length of antenna is $\lambda/4$ = 5kM. This is not practicable. Now if we modulate above signal with carrier frequency 10MHz, then

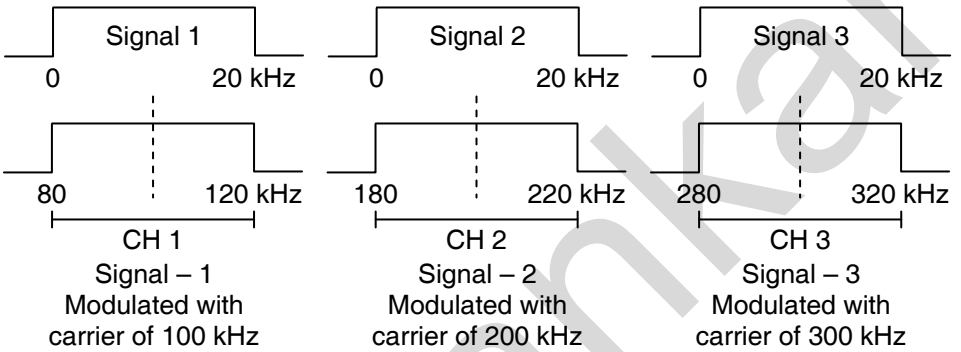
$$\lambda = \frac{c}{f} = \frac{3\times10^8}{10\times10^6} = 30 \text{ m}$$

So minimum height of antenna $= \lambda/4 = 7.5$ m which is practicable.

2) Avoid mixing of signals :

If the baseband signals are transmitted without modulation by more than one transmitter. Since, all the signals are in the same frequency range, i.e. 20Hz to 20KHz. So all the signals get mixed together and the receiver cannot separate them from each other. So baseband signals are modulated with different carrier then they will occupy different slots in frequency domain as shown in figure.

Thus, modulating signal by different carrier frequencies avoids the mixing of the signals.



3) Increases the range of communication :

The frequency of the baseband signal is low. Therefore it cannot travel by long distance. When such signals are transmitted, they get heavily attenuated. The attenuation of signal reduces with increase in frequency of transmitted signal and they can travel larger distance. The modulation process upshift the frequency of the signal to be transmitted. Therefore, it increases the range of communication.

4) Allows multiplexing of signals :

Multiplexing means transmission of two or more signals simultaneously over the same carrier and this is possible only with modulation.

5) Improves quality of reception :

With FM and digital modulation techniques like PCM, the effect of noise can be reduced to great extent. This improves quality of reception.

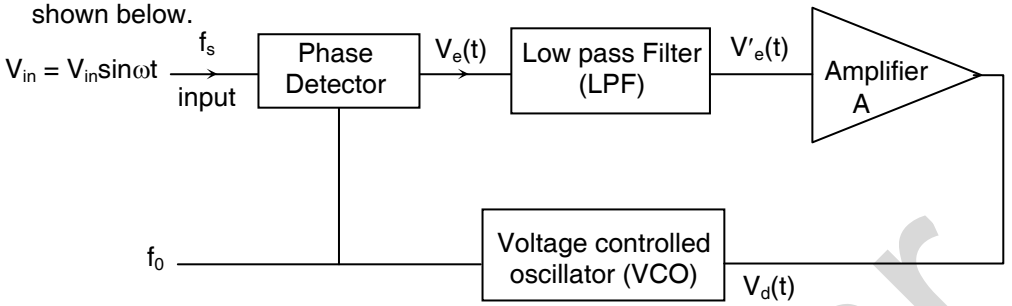
1. (e) PHASE LOCKED LOOP

A phase locked loop (PLL) is defined as a control mechanism by which the frequency and phase of the incoming signal is synchronised with the frequency and phase of the VCO.

The phase locked loop consists of three blocks.

(i) Phase detector
(ii) Low pass filter
(iii) Voltage controlled oscillator

The amplifier may or may not be a part of PLL. The block diagram of PLL is shown below.



The PLL passes through three modes of operation to go into lock condition.
Before the application of the input, the VCO operates at a frequency depending upon the external resistance and capacitor. This is called the free running frequency f_0' of the VCO. This mode of operation of the PLL is called the **free running mode**.

On the application of an external input V_{in} sin ω_s t, the output of the phase detector, has the sum and difference frequency components. [$f_s + f_0$ and $f_s \sim f_0$].

The phase detector compares the input frequency f_s with the feedback frequency f_0. The output of the phase detector is proportional to the phase difference 'θ' between f_s and f_0. The output of the phase detector has a dc component, called the error voltage ($V_e(t)$).

The low pass filter passes the low frequency component [$f_{in} \sim f_0$] and blocks the high frequency component. ($f_{in} + f_0$) and error voltage $V_e'(t)$ is obtained and is give as the control input to the VCO so that the frequency of the VCO approaches the frequency of the incoming signal. This mode of operation when the VCO frequency changes and approaches the incoming signal frequency is called the **Capture mode**.

When the two inputs to the phase detector are equal, the output of the phase detector has an error voltage which is just sufficient to keep the VCO operate at the frequency of the incoming signal f_s. This mode of operation is the **Lock mode**.

The design of VCO should be such that $f_{in} + f_0$ and $f_s \sim f_0$ component are significantly apart. The action of the loop is to make 'θ' take just that value which is required to generate the DC control voltage necessary to change value to f_{in}.

This allows the PLL to track any frequency changes of the input signal, once lock has been acquired.

1. (f) Comparison between TDM and FDM

	TDM	FDM
1)	Total available time is divided into several user	Total frequency bands are divided into several users

2)	Transmission of two or more signals on the same path, but at different times.	A multiplex system for transmitting two or more signals over a common path by using a different frequency band for each signal.
3)	TDM imply partitioning the bandwidth of the channel connecting two nodes into finite set of time slots	The signals multiplexed come from different sources/transmitters.
4)	TDM system requires commutator and de-commutator.	FDM system requires an adder and separator.
5)	TDM system sends synchronization pulses between two set of messages.	FDM system maintains guard band between two frequencies.

2. (a) **Find I_D**

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2$$

But $V_{GS} = V_g - I_D R_S$

$$= \frac{R_2}{R_1+R_2} \times V_D - I_D R_s$$

$$= \frac{110}{910+110} \times 20 - (0.51)\, I_D$$

$\therefore \quad V_{gs} = 2.157 - 0.51\, I_D$

$$I_D = 10\left[1-\frac{(2.157-(0.51)I_D)}{-3.5}\right]^2 = 10\left[\frac{3.5+2.157-(0.51)I_D}{3.5}\right]^2$$

$$= \frac{10}{12.25}\,[5.657 - (0.51)\, I_D]^2$$

$\therefore \quad 12.25\, I_D = 10\,[5.657 - 0.51\, I_D]^2$

$$= 32 - 5.77\, I_D + 0.26\, I_D^2$$

$\therefore \quad 32 - 6.995\, I_D + 0.26\, I_D^2 = 0$

$$\therefore \quad I_D = \frac{6.995 \pm \sqrt{(6.995)^2 - (4\times 32\times 0.26)}}{2\times 0.26}$$

$$= \frac{6.995 \pm 3.956}{0.52}$$

$= 21.06$ mA or 5.84 mA

I_D should be smaller than I_{DSS}.

$\therefore \quad I_D = 5.84$ mA

Find V_{GS}

$V_{GS} = 2.157 - 0.51\, I_D$

$= 2.157 - 0.51 \times 5.84$

$= -0.8236$ V

Find V_G

$$V_G = \frac{R_2}{R_1+R_2}\times V_{DD} = \frac{110}{910+110}\times 20 = 2.157 \text{ V}$$

Find V_S and V_D

$V_S = 0.51\ I_D \qquad = 0.51 \times 5.84$

$= 2.98\ V$

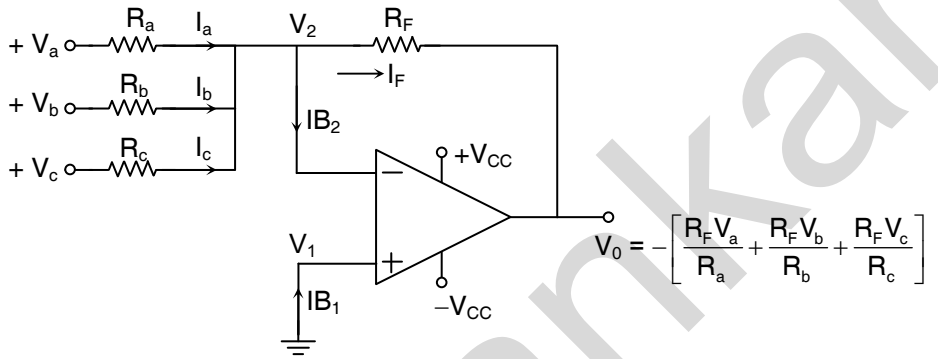
Find V_{DS}

$V_{DS} = V_D - V_S \qquad = 7.152 - 2.98$

$= 4.172\ V$

2. (b) Op–Amp Adder

Inverting Configuration



Above figure shows the inverting amplifier with three inputs V_a, V_b & V_c. Depending upon relationship between the feedback resistor R_F and input resistors R_a, R_b and R_c. The circuit can be used either summing amplifier, scaling amplifier, or averaging amplifier.

Apply KCL at node V_2.

$$I_a + I_b + I_c = I_{B2} + I_F$$

$$I_{B2} = 0$$

$$I_a + I_b + I_c = I_F$$

$$\frac{V_a - V_2}{R_a} + \frac{V_b - V_2}{R_b} + \frac{V_F - V_2}{R_c} = \frac{V_2 - V_0}{R_F}$$

Since R_i and A of OP-AMP are ideally infinite. So $I_{B2} = 0$, $V_1 = V_2 = 0$ (Virtual ground).

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_F}{R_c} = \frac{-V_0}{R_F}$$

$$V_0 = -\left[\frac{R_F}{R_a}V_a + \frac{R_p}{R_b}V_b + \frac{R_F}{R_c}V_c\right] \qquad \ldots (A)$$

If in the above circuit, $R_a = R_b = R_c = R$, then the circuit will be

$$V_0 = -\frac{R_F}{R}\,[V_a + V_b + V_c]$$

This means that the output voltage is equal to negative sum of all the inputs times gain of the circuit. Hence the circuit is called as summing amplifier.

Obviously when the gain of the circuit is 1. i.e. $R_a = R_b = R_c = R_F = R$, then the output voltage is equal to sum of all input voltages.

i.e. $V_0 = -(V_a + V_b + V_c)$

Scaling or Weighted Amplifier

If each input voltage is amplified by a different factor, in other words weighted differently at the output. Then the circuit is called as scaling or weighted amplifier. This condition can be accomplished if R_a, R_b and R_c are different in values. Thus output voltage of summing amplifier is

$$V_0 = -\left[\frac{R_F}{R_a}V_a + \frac{R_p}{R_b}V_b + \frac{R_F}{R_c}V_c\right] \qquad \text{where } \left[\frac{R_F}{R_a} \neq \frac{R_p}{R_b} \neq \frac{R_F}{R_c}\right]$$

Average Amplifier

The above circuit can be used as averaging amplifier in which the output voltage is equal to the average of all the input voltage. This is accomplished by using all input resistance of equal values

i.e. $R_a = R_b = R_c = R$

In addition, the gain by which each input is amplified must be equal to 1 over the number of inputs

i.e. $\frac{R_F}{R} = \frac{1}{n}$ where n = number of inputs.

Thus if there are three inputs, then $\frac{R_F}{R} = \frac{1}{3}$.

$$V_0 = -\left[\frac{V_a + V_b + V_c}{3}\right]$$

3. (a) AMPLITUDE MODULATION

Amplitude Modulation (AM) is the process in which the amplitude of high frequency carrier signal in proportion with the instantaneous value of modulating signal.

Waveform for an AM wave

Modulating signal

$$V_m = V_m \cos \omega_m t$$

Carrier Signal

$$V_C = V_c \cos \omega_c t$$

The AM wave expressed by following expression.

$$V_{AM} = A \cos (2\pi f_C t)$$

where $A = V_C + V_m$

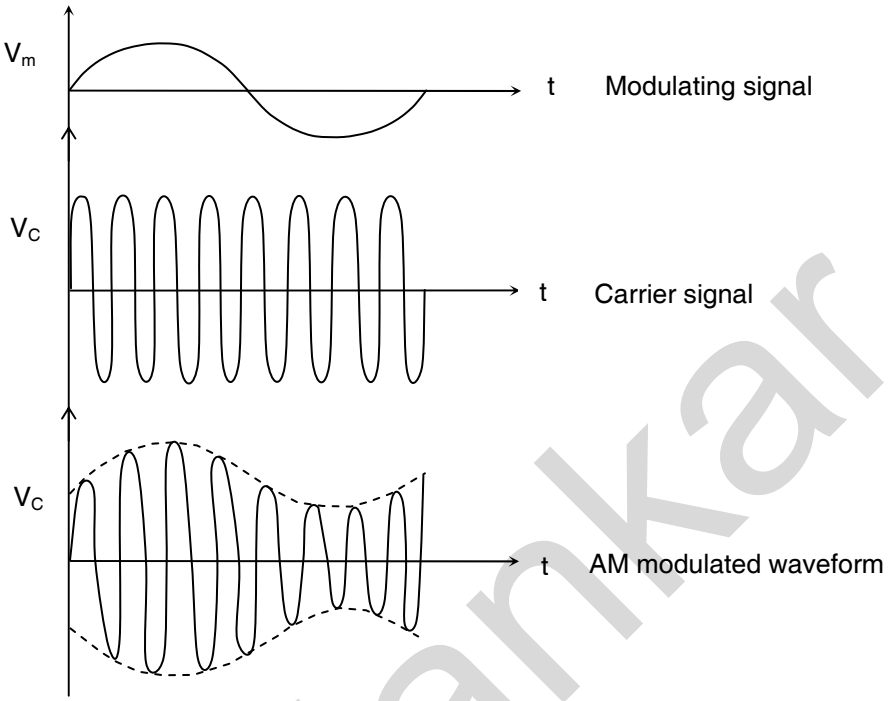
$= V_C + V_m \cos \omega_m t$

$\therefore \quad V_{AM} = (V_C + V_m \cos\omega_m t) \cos \omega_C t$

$= V_C \cos \omega_C t + V_m \cos \omega_m t \,.\, \cos \omega_C t$

$= V_C \left[1 + \frac{V_m}{V_C}\cos\omega_m t\right] \cos \omega_C t$

$= V_C [1 + m \cos \omega_m t] \cos\omega_C t$ where Modulation index (m) = $\frac{V_m}{V_C}$



Total transmitted power

AM frequency spectrum contain following spectral components.

$$V_{AM} = \underbrace{V_C \cos \omega_C t}_{\text{Carrier Wave}} + \underbrace{\frac{mV_C}{2}\cos(\omega_c + \omega_m)t}_{\text{USB}} + \underbrace{\frac{mV_C}{2}\cos(\omega_c \,.\, \omega_m)t}_{\text{LSB}}$$

Total power in AM

$$P_L = P_C + P_{LSB} + P_{USB}$$

$$P_L = \frac{V_C^2}{R} + \frac{V_{LSB}^2}{R} + \frac{V_{USB}^2}{R}$$

$$P_C = \frac{\left(V_C/\sqrt{2}\right)^2}{R} = \frac{V_C^2}{2R}$$

$$P_{LSB} = P_{USB} = \frac{E_{SB}^2}{R}$$

$$= \left(\frac{mV_C}{2-\sqrt{2}}\right)^2 \Big/ 2 = \frac{m^2V_C^2}{8R}$$

$$\therefore \quad P_L = \frac{V_C^2}{2R} + \frac{m^2V_C^2}{8R} + \frac{m^2V_C^2}{8R}$$

$$= \frac{V_C^2}{2R}\left(1 + \frac{m^2}{4} + \frac{m^2}{4}\right)$$

$$P_L = \left(1 + \frac{m^2}{2}\right)P_C$$

3. (b) Super Heterodyne Receiver

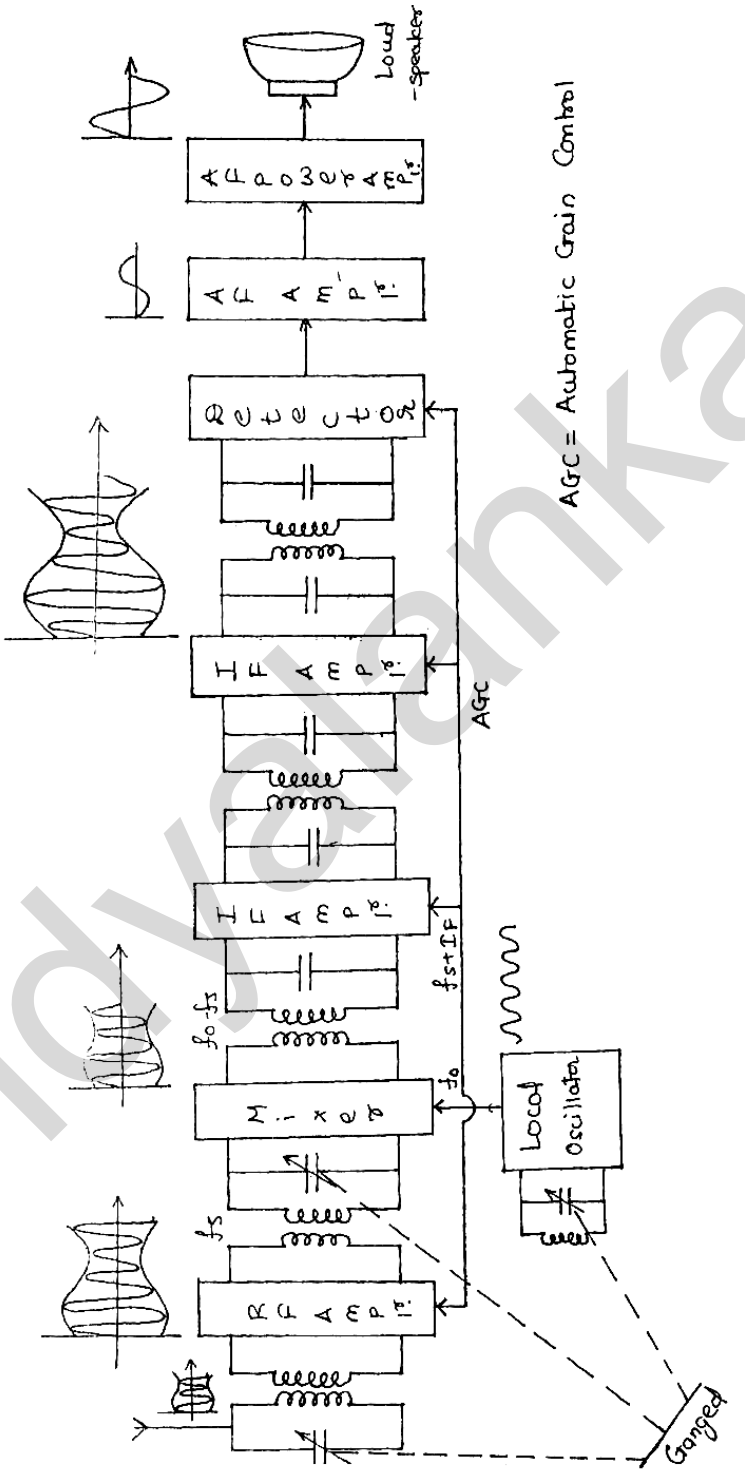
The features of heterodyne receiver is that all incoming radio frequency signals called intermediate frequency by using heterodyne process.

In this receiver, the received signal frequency is mixed with the local oscillator frequency f_0. The local oscillator is an LC oscillator which produce sinusoidal oscillations of frequency f_0. The frequency of local oscillator depends on the values of L & C of associated tuned circuit. The signal frequency f_s and signal f_0 gives to the mixer circuit. Mixer is a non-linear circuit. It will produce the output which contain different frequency component such as f_s, f_0, $f_0 \pm f_s$, harmonics of input frequencies and the IC components. The inputs tank circuit of IF amplifier is tuned to $f_0 - f_s$ which is always 455 KHz and is known as Intermediate frequency I_f. To get I_f always = 455 KHz, the local oscillator should be tuned such that whatever may be input signal frequency f_s, local oscillator frequency f_0 should be always 455 KHz, more than f_s. AM wave with 455 KHz is amplified to the desired level by 2 or 3 I_f amplifier and then it is fed to the detector which detects a taken out the AF information from the AM wave. This audio frequency signal is then amplified by voltage and power amplifier so that it can drive the loudspeaker.

Advantages of Superheterodyne R_x over TRF R_x

1) Since, major part of gain of receiver is provided by IF amplifiers which are tuned to 455 KHz, the neutralization capacitor can be easily designed for fixed IF. Thus unwanted feedback, eliminated and hence, it eliminates the possibility of instability at high frequency side of tuning range.
2) Since IF amplifier are tuned at fixed frequency. Therefore, the bandwidth remains constant and the adjacent channel does not pick up by the receiver. Thus we get better selectivity.
3) Gain of receiver is provided by IF amplifier and IF amplifier has constant bandwidth. Therefore the gain provided by IF amplifier is also constant over the tuning range of AM broadcasting.
4) Number of capacitors which are to be tuned simultaneously are less, hence easy to manufacture or tune.

Block diagram of Superheterodyne Receiver

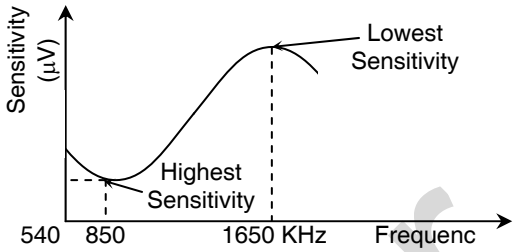


Characteristics of Receiver

1) Sensitivity

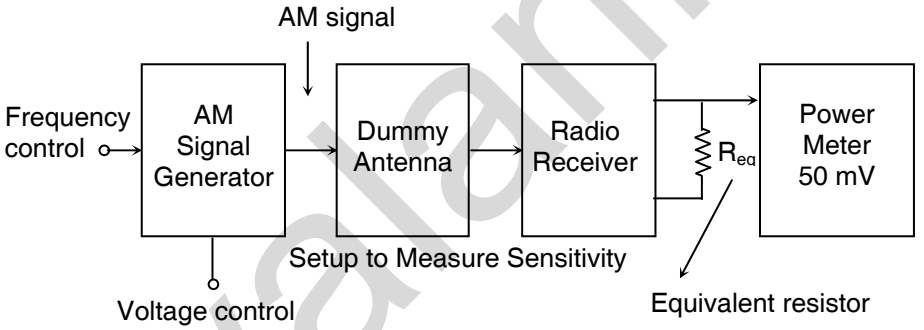
It is the ability of the receiver to receive weak signal and it is defined as the amount of input voltage required for the receiver to produce standard output power (50 mV) at its output.

Sensitivity is expressed in μV or dB below 1V. The typical sensitivity curve is as shown :



From the curve it is seen that radio receiver is most sensitive at 850 KHz as the frequency increases, the gain of receiver decreases. Therefore more input voltage required to produce standard output. Therefore at high frequency, the sensitivity of receiver is less. The sensitivity of receiver depends on the gain of RF and IF amplifier.

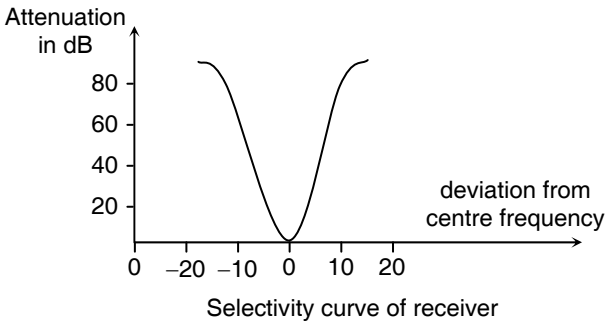
Sensitivity Measurement



While measuring sensitivity, the receiver source and load must be standardised so that variation is the measurement and do not affect the output. For this purpose actual antenna is replaced by dummy antenna which is LC tuned circuit and the load is not loudspeaker but its resistor.

A standard input AM signal at 30% modulation and FM = 400 Hz is applied to receiver through the dummy antenna. The input is varied by using voltage control to get standard output power of 50 mV across the load. The input in μV of carrier voltage is a measure of sensitivity.

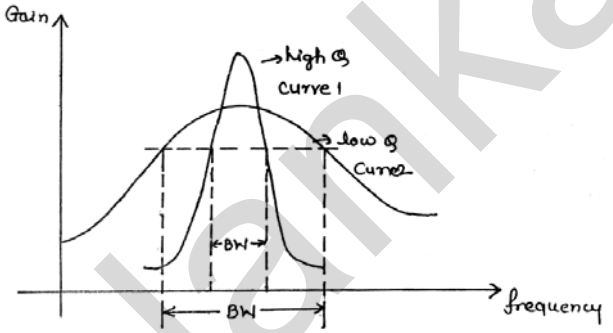
2) Selectivity



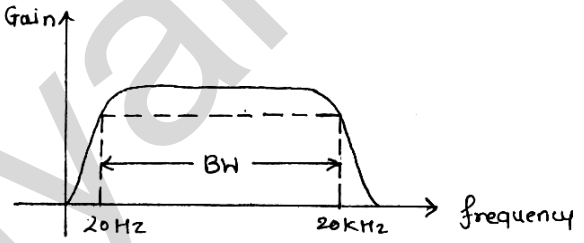
Selectivity of receiver is defined as the ability of the receiver to select desired signal or channel and reject unwanted signal or adjacent channel. The selectivity curve of receiver is as shown above. When the receiver receives the frequency signal at which receiver is tuned (centre frequency). It will provide maximum gain/zero attenuation but as the input signal frequency deviates from the centre frequency the gain of receiver decreases i.e. attenuation increases.

Selectivity depends on the sharpness of the resonance curve of the tuned circuit used in receiver. Therefore, sharper resonance curve, better the selectivity. It depends on Q of the LC tank circuit. Higher the Q less is the BW and better is selectivity.

Resonance curve of tuned circuit



3) Fidelity

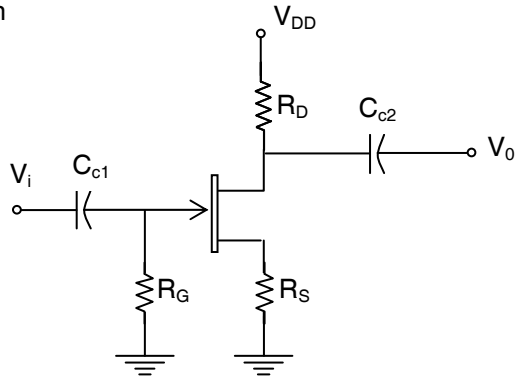


Fidelity Curve

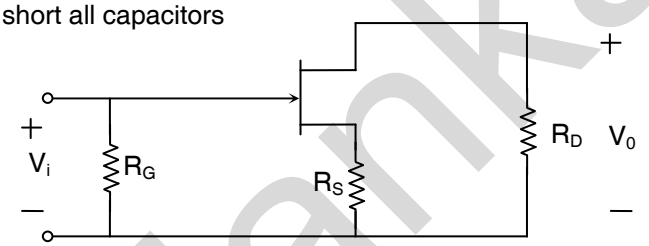
It is the ability of receiver to reproduce all the modulating frequency equally i.e. receiver must provide constant gain for all modulating frequencies. Since, AF amplifies amplify the AF signal, the fidelity depend on the frequency response of AF amplifier. The typical diagram of fidelity curve is as shown. High fidelity is essential in order to reproduce good quality music faithfully i.e. without distortion. For this, it is essential to have constant gain of AF amplifier over audio frequency range.

4. (a) CS amplifier with R_S Unbypassed

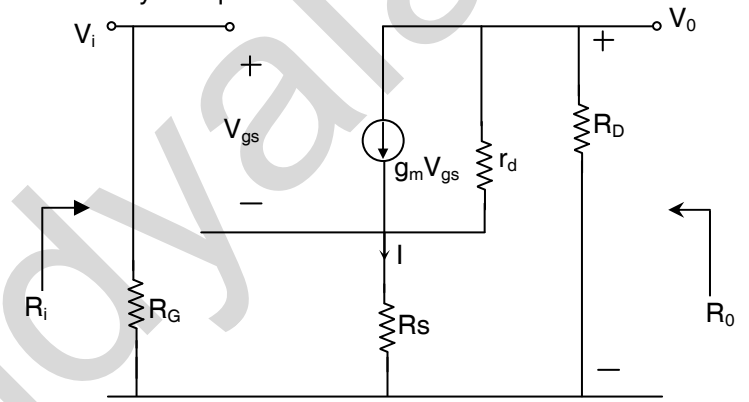
(a) Circuit diagram



(b) ac equivalent circuit
Short V_{DD} and short all capacitors



(c) Replace JFET by its equivalent



(d) To find Voltage gain $A_V = V_0/V_i$

$$V_0 = -I \cdot R_D = -g_m V_{gs} \frac{r_d}{r_d + R_D + R_S} R_D$$

$$= -\frac{\mu V_{gs}}{r_d + R_D + R_S} R_D \qquad (\because \mu = g_m r_d)$$

$$V_i = V_{gs} + I R_S = V_{gs} + g_m V_{gs} \frac{r_d}{r_d + R_D + R_S} R_S$$

$$= V_{gs}\left(1 + \frac{\mu R_S}{r_d + R_D + R_S}\right) = V_{gs}\left(\frac{r_d + R_D + R_S(1+\mu)}{r_d + R_D + R_S}\right)$$

$$\therefore \quad A_v = -\frac{\mu R_D}{r_d + R_D + R_S(1+\mu)}$$

(e) To find Input impedance R_i

$R_i = R_G$

(f) To Find Output impedance R_0

$R_0 = [r_d + R_S (1 + \mu)] \,||\, R_D$

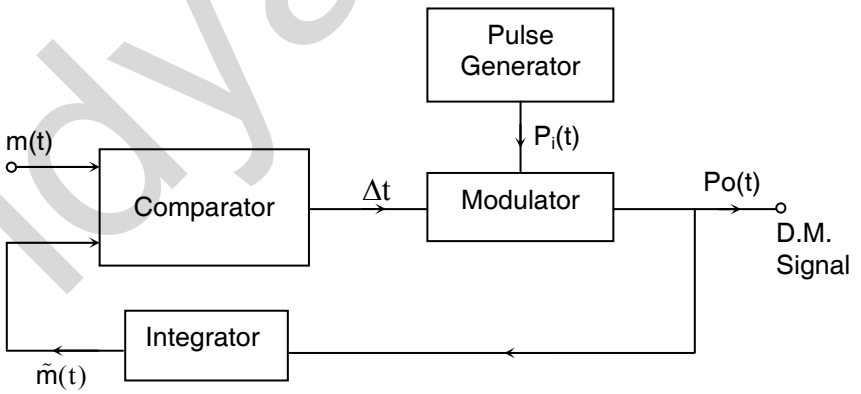
Results (with r_d)	Results (without r_d)
$A_v = \frac{-\mu R_D}{r_d + R_D + R_S(1+\mu)}$ where $\mu = g_m r_d$	$A_v = \frac{-g_m R_D}{1 + g_m R_S}$
$R_i = R_G$	$R_i = R_G$
$R_0 = [r_d + R_S (1 + \mu)] \,||\, R_D$	$R_0 = R_D$

Note : If the load R_L is given, replace R_D with (R_D || R_L)

4. (b) Delta Modulation

Delta modulation is also a digital modulation system. In delta modulation just one bit is sent per sample, to indicate whether the present sample is larger or smaller than the previous sample. Thus in delta modulation, the modulated signal carries information not about the signal samples but about the difference between successive samples. If the difference is +ve or –ve a +ve or –ve pulse respectively is generated in the modulated signal. Thus D.M. carries the information about the derivative of m (t) and hence the name is delta modulation. Thus integration of delta modulated signal m (t) will be an approximation of m (t).

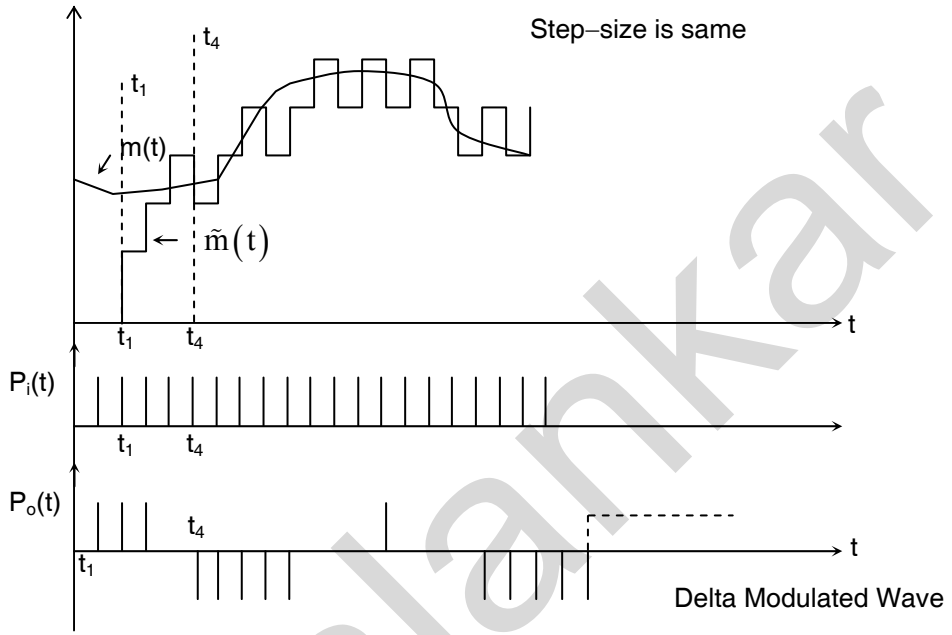
The block diagram of the delta modulator is shown below.



The pulse generator produce a pulse train $P_i(t)$ of positive pulses. The modulator receives $P_i(t)$ and $\Delta(t)$, the output of differential amp. The modulator output $P_o(t)$ is the product of input pulse train $P_i(t)$ and +1 or –1 depending upon the polarity of Δt. $P_o(t)$ is positive pulse if Δt is +ve and it is –ve pulse if Δt is –ve. The magnitude of Δt has no role in deciding $p_o(t)$. The output of modulator is applied to an integrator whose o/p is $\tilde{m}(t)$.

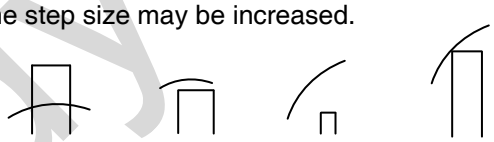
The input signal m (t) and the integrator output $\tilde{m}(t)$ is compared in difference amp. Whose output is $\Delta(t) = m(t) - \tilde{m}(t)$.

Following fig. explains the operation of delta modulator.



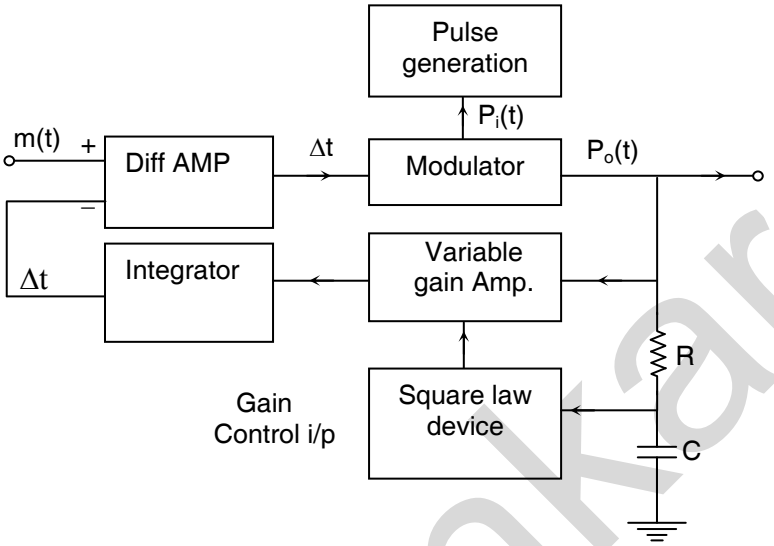
Adaptive Delta Modulation

The slope overload error of delta modulation can be overcome by changing step size. To avoid slope overload error, if the signal variations are less than the step size, the step size may be reduced and if the signal variations are greater than the step size, the step size may be increased.

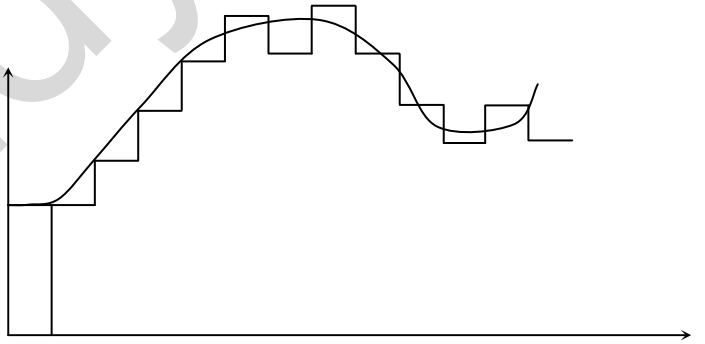


So the delta modulation system which adjust step size according to signal variation is known as Adaptive delta modulation.

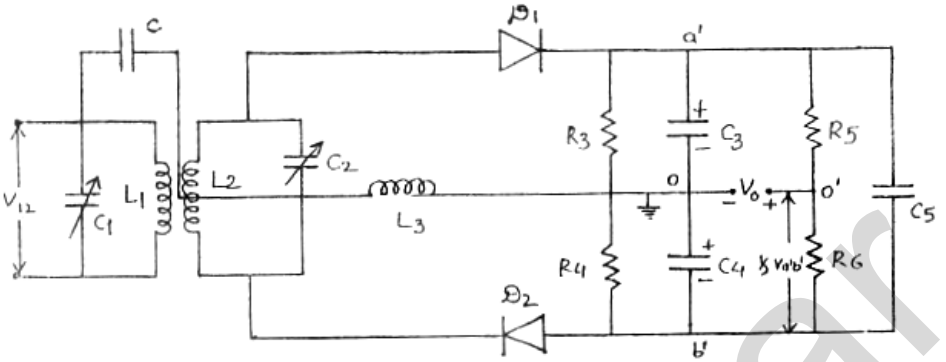
Following figure shows the block diagram of adaptive delta modulation



In adaptive delta modulation, a variable gain amp is used before integrator with P_o (t) as its input. The gain of this amp. depends on the gain control input, which is obtained by integrating P_o (t) in R.C. network and then passing the integrator o/p through a square law device under the slope overload condition $P_0(t)$ is a long sequence of either positive or negative pulses. The R.C. integrator integrates these pulses. Thus the o/p this integrator is either of a large positive or negative value. The square law device o/p is of a large +ve value ($(-)^2$ or $(+)^2$) irrespective of whether the i/p is +ve or –ve. Thus the gain control input of the variable gain amp. is large and its gain increases. Hence the step size increases, which can be take care of the slope–overload (positive or negative). When the signal variations are within step size, P_0 (t) is a sequence of alternative +ve and –ve pulses. The R.C. integral o/p in this case is zero, hence the gain control i/p of the variable gain amp. is also zero. Then the gain of variable gain amp. decreases, resulting in a reduced step size. It is shown below.



5. (a) RATIO DETECTOR



Ratio detector have inbuilt amplitude limiting. Therefore its output does not respond to amplitude variation of FM wave.

i) Diode D_2 is reversed in ratio detector such that terminal O is positive w.r.t. terminal b′ as shown in figure. $V_{a'b'} = V_{a'0} + V_{b'0}$. In Foster Seelay discriminator it is the difference voltage.

ii) Because of the capacitor C5 connected at the output, the voltage Va′b′ always remains constant. Hence, output is taken between O and O′. Hence, the output is given by

$$V_{b'0} + V_0 - \frac{1}{2}V_{a'b'} = 0$$

$$\therefore \quad V_0 = \frac{1}{2}V_{a'b'} - V_{b'0}$$

$$= \frac{V_{a'0} + V_{b'0}}{2} - V_{b'0}$$

$$\therefore \quad V_0 = \frac{1}{2}\left(V_{a'0} - V_{b'0}\right)$$

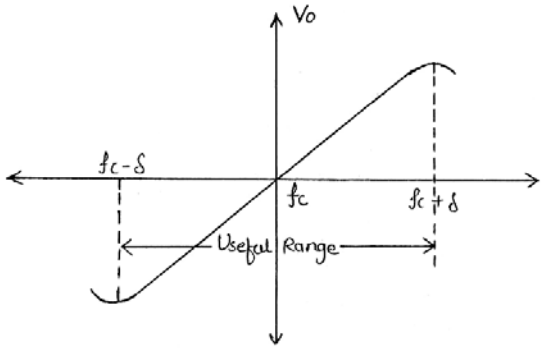
Above equation shows that the output of ratio detector varies similar to that of foster seeley discriminator but its magnitude reduced to half.

Working :

i) When $f_{in} = f_c$.
The input voltage to both diodes are same. Therefore the output voltages $V_{a'0}$ and $V_{b'0}$ of both diodes are identical. Hence resultant output voltage is zero.

ii) When $f_{in} > f_c$.
The secondary circuit becomes inductive. Hence output of diode D1 i.e. $V_{a'0}$ is greater than $V_{b'0}$. Therefore resultant output voltage increases positively.

iii) When $f_{in} < f_c$.
The secondary circuit becomes capacitive. Hence, output of diode i.e. $V_{b'0}$ is greater than $V_{a'0}$. Hence, resultant output voltage increases negatively, as shown below.



Amplitude Limiting

Case 1: When the amplitude of FM wave (V_{12}) is constant, the capacitance C_5 is charge up to the potential $V_{a'b'}$. Therefore, this is constant dc voltage. When V_{12} is constant, there will be no current either to charge or discharge the capacitor C_5 i.e. it provide it infinite impedance. The load of D_1 and D_2 are R_3 and R_4.

Case 2: If V_{12} tries to increase current through diodes increases. Thus current through load R_3 and R_4 increases. However voltage across the load remains constant because voltage across C_5 does not change instantaneously. Now the situation is that current through diode has been increased but voltage across load has not change means load has to decreases but load is fixed (R_3 and R_4). Therefore, the effect is that Q of secondary winding decreases because of this effective load acting on the IF amplifier decreases. Therefore gain of IF amplifier which driving ratio detector decreases. Hence input to ratio detector decreases i.e. increase in V_{12} is compensated.

Case 3: If input V_{12} tries to decrease, the current through diode decreases but the voltages across load will not change due to presence of capacitor C_5. Hence, load impedance has to increase but it is constant. Therefore, the effect is that the Q of secondary winding increases which in turn increases the effective load acting on IF amplifier. Therefore the gain of IF amplifier increases, hence input of ratio detector increases. Thus, the decrease in V_{12} is compensated.

Thus, ratio detector varies the gain of IF amplifier, by changing the damping or Q of its tuned circuit. This maintain constant output voltage even through amplitude of FM wave changes.

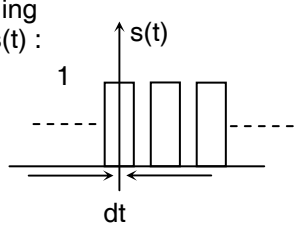
Advantages & Applications :

i) It's advantages over foster seeley detector is that it will provide amplitude limiting as well as voltage suitable for AGC.
ii) Foster Seelay detector output is more linear than ratio detector. Hence, it is used in high quality FM receivers.
iii) It provide better FM demodulation as well as amplitude limiting. Hence, widely used in TV receivers, for second section.

5. (b) SAMPLING THEOREM

→ Types of sampling
- Impulse sampling → s(t) Impulse train
- Natural sampling } → s(t) Pulse train
- Flat top sampling }

→ FDR of Impulse sampling
Fourier expansion of s(t) :



→ $s(t) = A_0 + \sum_{n=1}^{\infty} A_n \cos \omega_n t + \sum_{n=1}^{\infty} B_n \sin \omega_n t$

where $A_0 = \frac{1}{T_S} \int_{-T_S/2}^{T_s/2} s(t).dt$

$$A_n = \frac{2}{T_S} \int_{-T_S/2}^{T_s/2} s(t).\cos n\omega_s t.dt$$

$$B_n = \frac{2}{T_S} \int_{-T_S/2}^{T_s/2} s(t).\sin n\omega_s t.dt$$

We calculate Fourier series for the above mentioned sample :

$$\therefore \quad A_0 = \frac{1}{T_S} \int_{-dt/2}^{dt/2} 1.dt$$

$$\therefore \quad A_0 = \frac{1}{T_S} [dt]_{-dt/2}^{dt/2}$$

$$\therefore \quad A_0 = \frac{1}{T_S} \left[\frac{dt}{2} + \frac{dt}{2} \right]$$

Hence $A_0 = \frac{dt}{T_S}$

$$A_n = \frac{2}{T_s} \int_{-dt/2}^{dt/2} 1.\cos n\omega_s t.dt$$

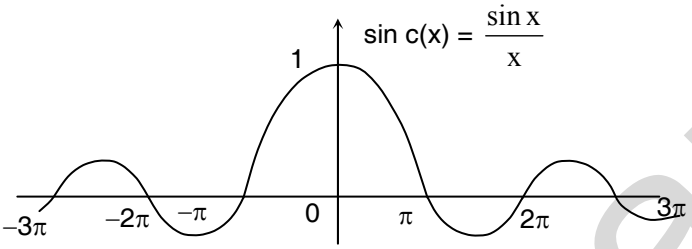
$$\therefore \quad A_n = \frac{2}{T_S} \left[\frac{\sin n\omega_s t}{n\omega_s} \right]_{-dt/2}^{dt/2}$$

$$\therefore \quad A_n = \frac{2}{nT_s\omega_s} \left[\frac{\sin n\omega_s dt}{2} + \frac{\sin n\omega_s dt}{2} \right]$$

$$\therefore \quad A_n = \frac{2dt}{2T_s} \cdot \frac{2\sin n\omega_s \, dt/2}{n\omega_s dt/2}$$

$$\therefore \quad A_n = \frac{2dt}{T_s} \cdot \frac{\sin n\omega_s\, dt/2}{n\omega_s dt/2}$$

$$\text{Hence} \quad A_n = \frac{2dt}{T_s} \cdot \text{sinc}\left[n\omega_s \frac{dt}{2}\right]$$



Since s(t) is impulse train at $\to 0$

$$\lim_{dt \to 0} \frac{\sin n\omega_s\, dt/2}{n\omega_s dt/2} = 1$$

Now due to property of Fourier series since s(t) is real and even function.
Hence $B_n = 0$

Now the representation becomes :

$$s(t) = \frac{dt}{T_s} + \sum_{n=i}^{\infty} \frac{2dt}{T_s} \cdot \text{sinc}\left[\frac{n\omega_s dt}{2}\right] \cos n\omega_s t$$

When s(t) is an impulse train we obtain

$$\frac{\sin n\omega_s\, dt/2}{n\omega_s\, dt/2} = 1$$

$$\text{Hence} \quad s(t) = \frac{dt}{T_s} + \frac{2dt}{T_s} \sum_{n=1}^{\infty} \cos n\omega_s t$$

$\to$ The sampled signal becomes :

$$s(t).m(t) = \frac{dt}{T_s} m(t) + \frac{2dt}{T_s} m(t) \sum_{n=1}^{\infty} \cos n\omega_s t$$

$$= \frac{dt}{T_s} m(t) + \frac{2dt}{T_s} m(t) \cos \omega_s t + \frac{2dt}{T_s} m(t) \cos 2\omega_s t + \frac{2dt}{T_s} m(t) \cos 3\omega_s t + \frac{2dt}{T_s} m(t). \cos 4\omega_s t + \ldots\ldots\ldots$$

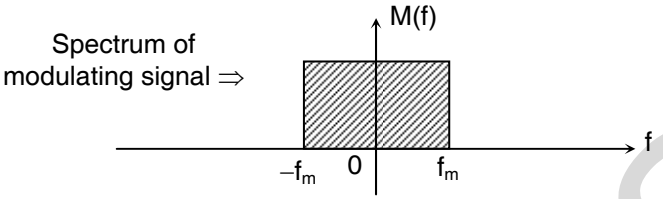
$\to$ Now using Fourier transform

$$m(t) \quad \xleftrightarrow{F} \quad M(f)$$

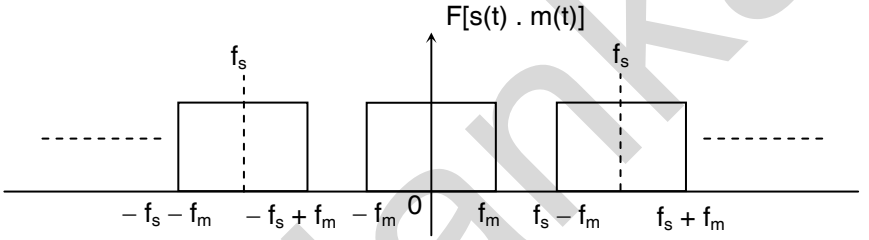
$$m(t). \cos \omega_c t \quad \longleftrightarrow \quad \frac{1}{2}[M(f - f_c) + M(f + f_c)]$$

→ Hence Frequency domain

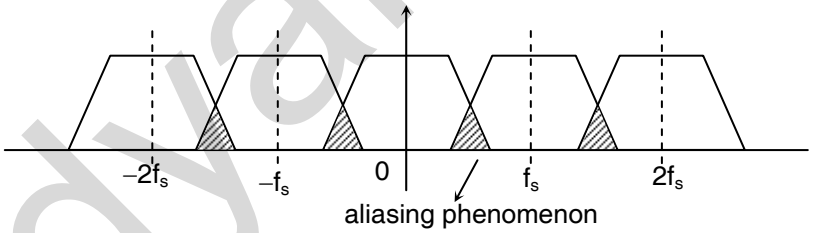
$$F[s(t).m(t)] = \frac{dt}{T_s}M(f) + \frac{dt}{T_s}[M(f-f_s) + M(f+f_s)] + \frac{dt}{T_s}[M(f-2f_s) + M(f+2f_s)] + ...$$



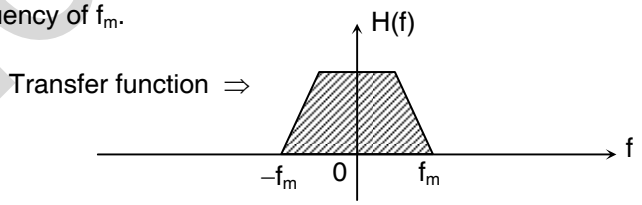
→ Frequency spectrum becomes



When $f_s < 2f_m$ the adjacent spectrum will overlap with one spectrum resulting in distortion of signal called aliasing.



→ To recover the sampled signal back we need a low pass filter with sharp cut-off frequency of f_m.



6. (a) Comparison between PAM, PWM, PPM :

	Parameter	PAM	PWM	PPM
1)	Information contained in	Amplitude Variation	Width Variation	Position Variation
2)	Bandwidth Requirement	low	high	high
3)	Noise immunity	low	high	high

4)	Transmitted Power	Varies with amplitude & pulses	Varies with variation in width	Remains constant
5)	Need to transmitt synchronization pulses	not needed	not needed	necessary
6)	Complexity of generation & detection	Complex	Easy	Complex

6. (b) An ideal op–amp exhibits the following electrical characteristics.

(a) Infinite voltage gain
(b) Infinite input resistance R_i, so that any signal source can drive it and there is no loading of the preceding stage.
(c) Zero output resistance R_0, so that output can drive an infinite number of other devices.
(d) Zero offset voltage, hence can be direct coupled.
(e) Infinite BW, so that frequencies from 0 to ∞ Hz can be amplified without attenuation.
(f) Infinite CMRR, so that common mode noise is zero.
(g) Infinite slew rate, so that output voltage changes simultaneously with input.

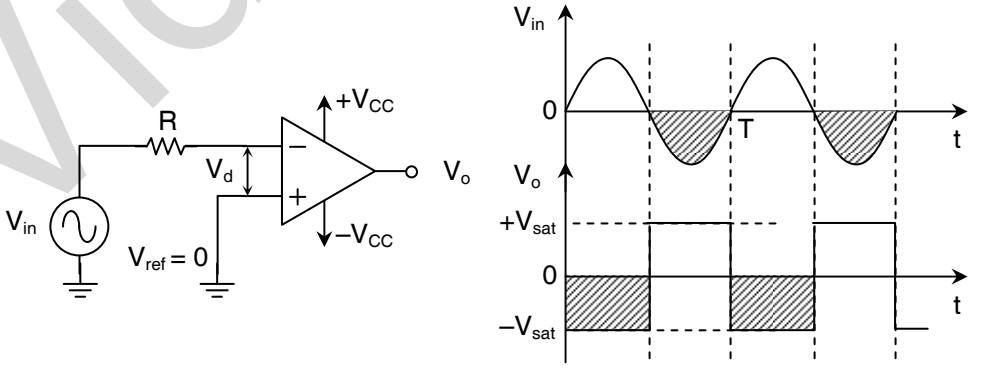
6. (c) Zero Crossing Detectors

Zero crossing detector is nothing but the basic comparator circuit with a zero reference voltage applied to the non-inverting terminal.

Circuit Operation : Refer to waveforms, when the input sinewave crosses zero and becomes +ve at instant t = 0, the differential input voltage V_d becomes negative and output voltage will swing to $-V_{(sat)}$.

When the sinewave again crosses zero and becomes negative at instant t = T/2, the differential input voltage becomes +ve and output voltage will swing to $+V_{(sat)}$ as now the (+) terminal is more +ve than the (–) terminal. The zero crossing detector thus switches its output from one state to other every time when the input voltage crosses zero.

The ZCD is also known as sinewave to square wave converter.



Input and Output voltage waveforms

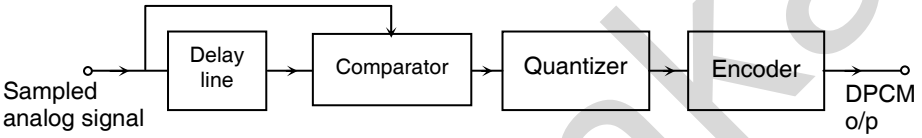
6. (d) PCM

In PCM the modulating signal is first sampled [Sampling freq. must be > 2 fm]. Then quantization process takes place.

Differential PCM (DPCM)

In DPCM, instead of quantizing each sample, the difference between two successive samples is quantized, encoded and transmitted as in PCM. This is particularly useful in voice transmission, because in this case two successive samples do not differ much in amplitude. Thus the difference signal is much less in amplitude than the actual amplitude and, hence, less number of bits per code are reduced, resulting in a reduced bit rate. Thus B.W. required in this case is less than the P.C.M.

The block diagram of D.P.C.M. is shown below



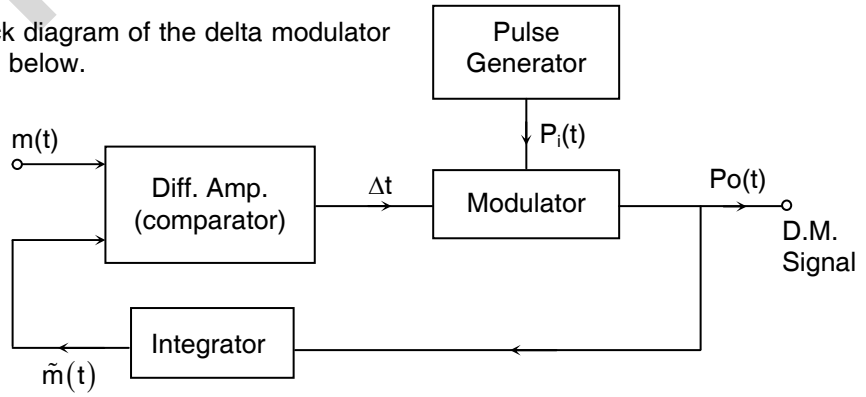
The signals are sampled in usual way and these samples are passed through delay line to a comparator circuit which also gets the sampled signal i/p. The comparator o/p corresponds to the difference between the two successive samples. The difference is then quantized and converted into a P.C.M. in the usual way.

The disadvantage of D.P.C.M. is that the modulator and demodulator circuit are more complicated than P.C.M.

Delta Modulation

Delta modulation is also a digital modulation system. In delta modulation just one bit is sent per sample, to indicate whether the present sample is larger or smaller than the previous sample. Thus in delta modulation, the modulated signal carries information not about the signal samples but about the difference between successive samples. If the difference is +ve or –ve a +ve or –ve pulse respectively is generated in the modulated signal. Thus D.M. carries the information about the derivative of m (t) and hence the name is delta modulation. Thus integration of delta modulated signal m (t) will be an approximation of m (t).

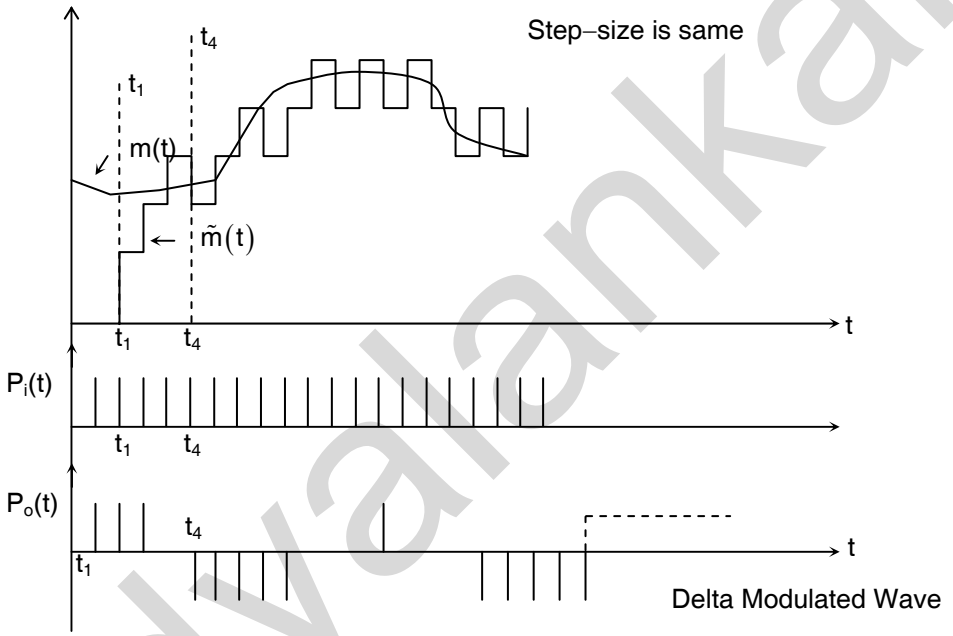
The block diagram of the delta modulator is shown below.



The pulse generator produce a pulse train $P_i(t)$ of positive pulses. The modulator receives $P_i(t)$ and $\Delta(t)$, the output of differential amp. The modulator output $P_o(t)$ is the product of input pulse train $P_i(t)$ and +1 or −1 depending upon the polarity of Δt. $P_o(t)$ is positive pulse if Δt is +ve and it is −ve pulse if Δt is −ve. The magnitude of Δt has no role in deciding $p_o(t)$. The output of modulator is applied to an integrator whose o/p is $\tilde{m}(t)$.

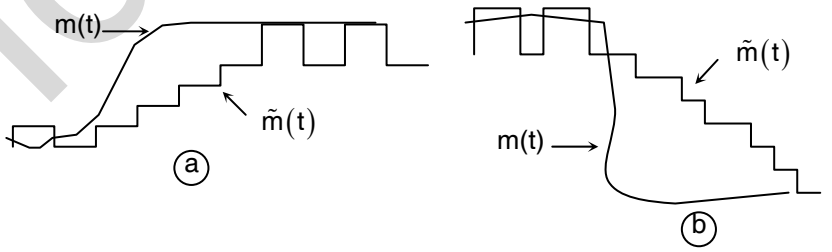
The input signal m (t) and the integrator o/p $\tilde{m}(t)$ is compared in difference amp. Whose output is $\Delta(t) = m(t) - \tilde{m}(t)$.

Following figure explains the operation of delta modulator.



Limitation of Delta Modulation

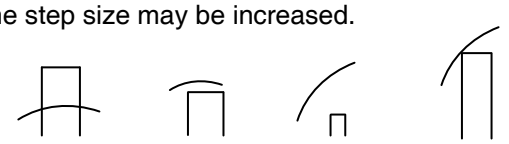
If m(t) changes too fast then $\tilde{m}(t)$ cannot follow m(t) as shown below.



In fig. (a) slope of m (t) is greater than slope of $\tilde{m}(t)$ hence $\tilde{m}(t)$ is enable to follow m(t). Similarly in (b) slope of m(t) is more negative than slope of $\tilde{m}(t)$. In both cases recovered waveform will be distorted. Then D.M. system is said to be slope overloaded.

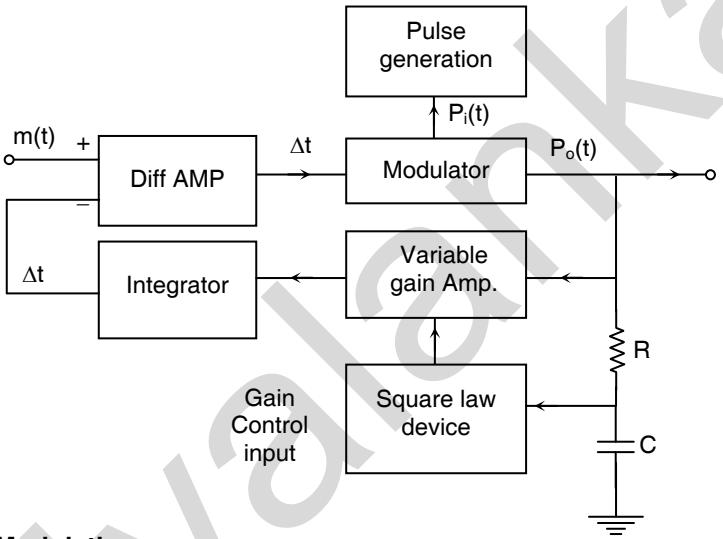
Adaptive Delta Modulation

The slope overload error of delta modulation can be overcome by changing step size. To avoid slope overload error, if the signal variations are less than the step size, the step size may be reduced and if the signal variations are greater than the step size, the step size may be increased.



So the delta modulation system which adjust step size according to signal variation is known as Adaptive delta modulation.

Following Figure shows the block diagram of adaptive delta modulation



6. (e) Phase Modulation

If the phase of carrier signal is varied in accordance with the amplitude of modulating signal, then the resulting wave is said to be phase modulated. Here, the phase deviation is proportional to amplitude of modulating signal

$\therefore$ Phase deviation $= \theta$

$\theta \propto$ modulating signal

$\therefore \quad \theta = K_p V_m \cos w_m t$

where K_p = phase deviation sensitivity

The maximum value of phase deviation is

$$\theta_{max.} = K_p V_m$$

The instantaneous phase of PM wave is

$$\psi = \omega_c t + \theta = \omega_c t + K_p V_m \cos \omega_m t$$

The equation of PM wave is

$$e(t) = A \sin \psi$$

$$= A \sin (\omega_c t + K_p V_m \cos \omega_m t)$$

$\therefore \quad e(t) = A \sin (\omega_c t + M_p \cos \omega_m t) \qquad (\because A = VC)$

where $MP = K_p V_m$

MP is modulation index of phase modulation and it is proportional to amplitude of modulating signal and it is independent of frequency of modulating signal.

Bandwidth of PM :

The instantaneous phase of PM is

$$\psi = \omega_c t + K_p \cos \omega_m t$$

the instantaneous frequency is

$$W_i = \frac{d\psi}{dt}$$

$$= \frac{d}{dt}[\omega_c t + k_p v_m \cos \omega_m t]$$

$$= \omega_c - K_p V_m \omega_m \sin \omega_m t$$

$$Wi = \omega c - \delta$$

So maximum value of frequency deviation is PM is

$$\delta_{max.} = K_p V_m \omega_m$$

Frequency deviation in PM is $\propto$ to amplitude as well as frequency of modulating signal as per Carson rule bandwidth require for PM is

$$BW = 2(\delta + f_m)$$

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