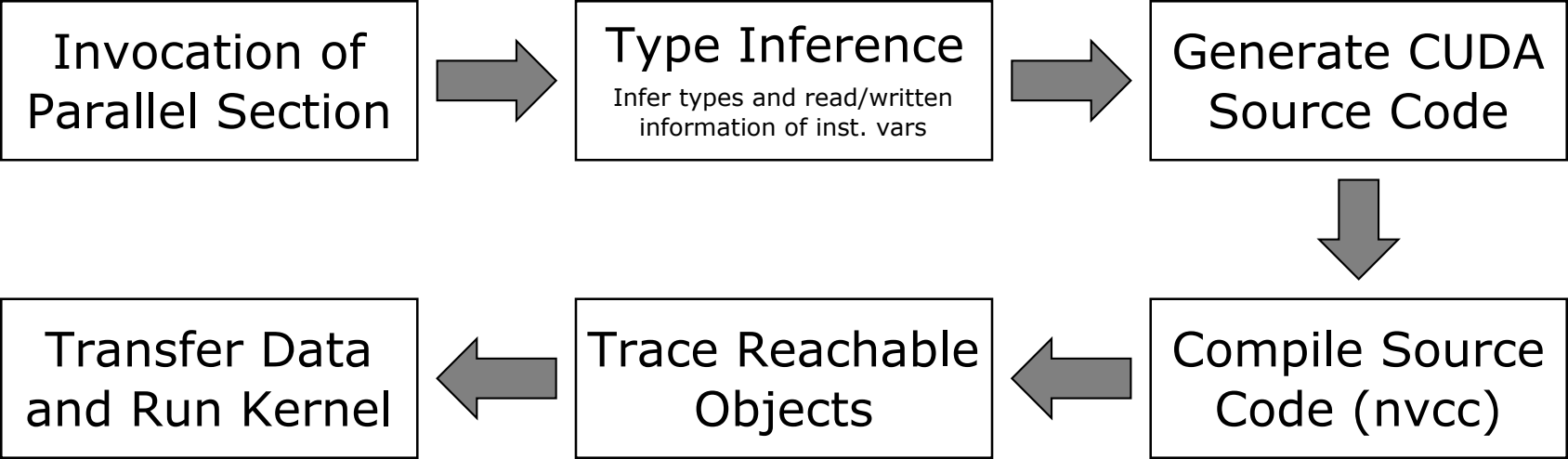
Invocation of Parallel Section
Type Inference
Infer types and read/written information of inst. vars
Generate CUDA Source Code
Compile Source Code (nvcc)
Trace Reachable Objects
Transfer Data and Run Kernel