Background

The digital audio platform has two clocks, 22.5792 MHz and 24.576 MHz. At any time, one of the clocks is active depending on the desired audio sample rate (44.1 kHz vs. 48/96/192 kHz). The board has to perform this 2:1 muxing and distribute the selected clock to the 4 DAC or ADC modules (over about 12" or 300 mm of PCB) and to an FPGA that buffers the audio samples. The proposed design converts the selected single-ended oscillator output to differential; each module needs to convert back to single-ended.

Phase noise in the clock is one of the error sources in A/D or D/A conversion, in addition to the converter itself and the analog interface (filtering and/or I/V conversion). The measurements in this document illustrate the performance differences between oscillators and quantify the performance impact of the platform's clock distribution. The intent is to make other hobbyists comfortable using the platform even if they have concerns about phase noise, and to provide data for component selection choices.

Device under test

The prototyping setup consists of two boards: a clock source and clock receiver. On the digital audio platform, both of these components will be interchangeable; the main PCB only has differential traces between the source and each module (which contains a receiver).

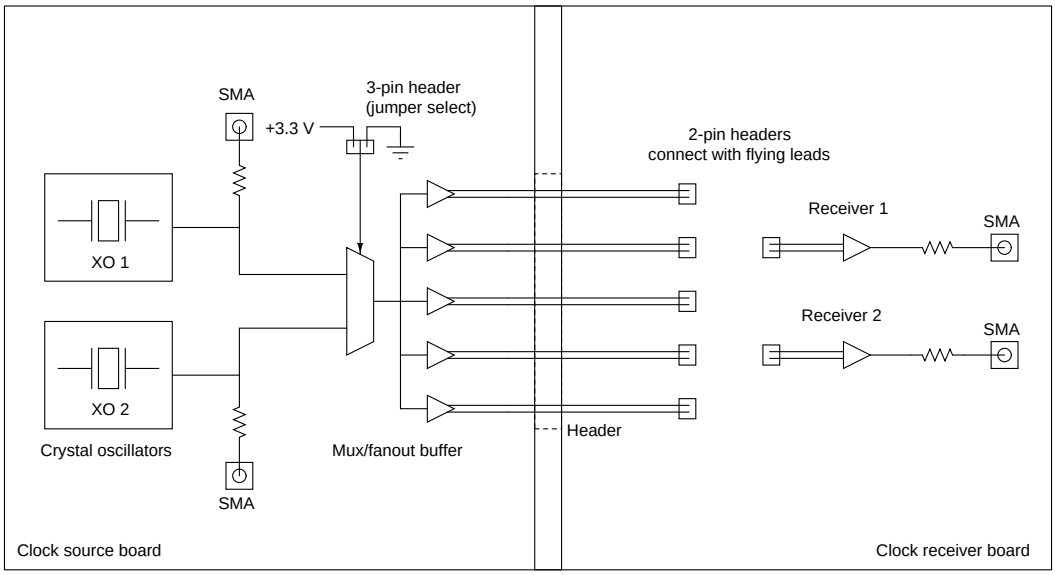

Figure 1: Setup for phase noise measurements.

There are two interchangeable clock source boards:

- **Clock source A** uses a 74-series mux (SN74LVC1G3157) and standard LVDS transmitters (FIN1031, FIN1001) to drive differential outputs. It is populated with two crystal oscillators (selectable by jumper):
  1. Epson SG-210STF (2.5x2.0 mm SMD), 22.5792 MHz.
     Specified phase noise is -145 dBc/Hz at 1 kHz offset.
  2. Crystek CCHD-957 (14x9 mm SMD), 22.5792 MHz.
     Specified phase noise is -149 dBc/Hz at 1 kHz offset. (-97 dBc/Hz at 10 Hz offset)

  This board is powered by a UA78M33 regulator. It is meant to represent a "low cost" stuffing option for the clock source, regardless of which oscillators are used.

- **Clock source B** uses an ADCLK948 to perform muxing and drive differential outputs. Its oscillators are:
  1. Crystek CCHD-957 (14x9 mm SMD), 24.576 MHz.
     Specified phase noise is -149 dBc/Hz at 1 kHz offset. (-98 dBc/Hz at 10 Hz offset)
  2. Tentlabs XO (11x11 mm DIP), 11.2896 MHz.
     Specified phase noise is -151 dBc/Hz at 1 kHz offset. (-93 dBc/Hz at 10 Hz offset)

  This board is powered by an ADM7154 regulator with a 330 μF tantalum cap for reference bypass. It is meant to represent a "high performance" (high cost) stuffing option for the clock source.

Each clock source board has 5 differential clock outputs routed to a 32-pin 0.1"-pitch header that connects to a socket on the clock receiver board. (These outputs are named CLK0, CLK1, CLK2, CLK3, and CLKF.)

There are two receivers (differential to single-ended converters) on the clock receiver board:

- **Clock receiver A** uses a DS90LV12 LVDS receiver powered by a UA78M33 regulator. It is meant to represent a "low cost" option for DAC/ADC modules.
- **Clock receiver B** uses an AD9515 LVPECL receiver powered by an ADM7154 regulator. It is meant to represent a "high performance" (high cost) option for DAC/ADC modules.

Each of these receivers has a 2-pin 0.1" header for differential input and is AC coupled by 10 nF capacitors. Meanwhile, the 5 outputs of the clock source board are routed (over traces from 3.5" to 12" in length) to 2-pin 0.1" headers. This is meant to capture the effect of different routing lengths (to the 4 modules and FPGA) that are expected on the final boards. One of these headers can be connected to each receiver using jumper wires or zero-ohm resistors.

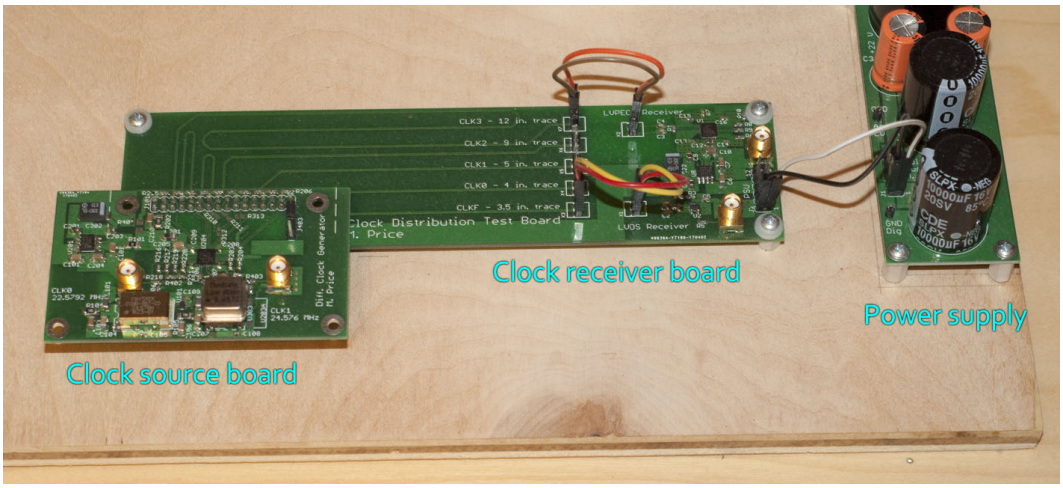

Figure 2: Photo of setup for phase noise measurements.

Results

I am fortunate to work for a company that has test equipment including a phase noise analyzer. I did not experiment thoroughly with the test setup, but I don't believe the phase noise results presented here are close to the floor of the analyzer.

Measurements made with clock source A had large high-frequency spurs, mostly above 1 MHz but with one as low as 84 kHz. The amplitude of these spurs varied, and in some cases they dominated the integrated jitter calculations. This made it hard to evaluate the relative performance of different oscillator, trace, and receiver combinations. So, for the following analysis, I used software post-processing to remove the large spurs (peaks of approximately 6 dB or more). I still need to trace and eliminate the cause of the spurs, and verify that real-world performance is comparable

Oscillator	Jitter	Excess jitter	
		Receiver A	Receiver B
Crystek CCHD-957	1.726 ps	0.427 ps	0.529 ps
	0.196 ps, >100 Hz		
Epson SG-210STF	0.876 ps	0.510 ps	0.189 ps
	0.267 ps, >100 Hz		

Table 1: RMS jitter for clock source A and excess jitter from each receiver.

to the filtered results presented here. (Because the spurs were present in the clocks measured at the oscillator outputs, I believe the issue is related to the power supply or ground configuration. In particular, I may have incorrectly configured the ADM7154 regulator used on source A, since source B uses the same PCB layout and doesn't have the same problem.)

Source and receiver combinations

Figure 3 compares the 2 oscillators on clock source A (low-cost option) with large spurs removed. Table 1 shows the integrated RMS jitter for each oscillator, as well as the excess jitter introduced by the LVDS transmitter in conjunction with either of the two receiver options. The jitter is computed by integrating the post-processed (i.e. spurs removed) phase noise from 10 Hz to 5 MHz.

It isn't clear why some of the measurements with the Crystek oscillators show higher close-in phase noise than the others. It's possible that the sweeps were performed when the power supplies were still settling, or that there was some other mistake in the measurement procedure. To work around this, I integrated excess jitter from one measurement to the next only at the frequencies at which phase noise was higher in the "excess" measurement. This is based on my understanding that it is not possible to "subtract" jitter. I also integrated jitter starting at 100 Hz instead of 10 Hz, so you can see how much of the jitter is from the low end of the audio band–in this case, most of it.

It is hard to compare the CCHD-957 oscillator to the SG-210STF due to the low frequency anomalies with the Crystek. But on clock source A, these two oscillators deliver similar performance with the CCHD-957 having a somewhat lower phase noise (except for a hump from 10–50 kHz) at higher frequencies.

The difference between the two receiver options is apparent in this plot also. Receiver B introduces about 6 dB of extra phase noise starting at 1 kHz. (Notice that for the SG-210STF the phase noise plot with receiver B has the same hump as the CCHD-957 visible above 10 kHz, though it doesn't appear in the direct measurement. Why?) Receiver A has a larger effect, degrading the phase noise by 10–20 dB starting around 300 Hz. The phase noise introduced by receiver A is large enough to mask the differences between the two oscillators. When integrated, the jitter added by receiver A is about 0.5 ps, and the jitter added by receiver B is about 0.2 ps. TODO: Investigate why the integrated excess jitter for the CCHD-957 is wonky.

Figure 4 and table 2 show similar results for source B, which compares the Tentlabs XO and another Crystek CCHD-957. On this board, both oscillators perform much better at low frequencies. The CCHD-957 is around -105 dBc/$\sqrt{\text{Hz}}$ at 10 Hz offset and -135 dBc/$\sqrt{\text{Hz}}$ at 100 Hz offset (better than the datasheet performance), for a total of 0.124 ps RMS jitter. The Tentlabs XO is almost as good at low frequencies, but has a higher "floor" at moderate to high frequencies, though it still integrates out to less than 1 ps RMS. With the Tentlabs XO, it is hard to see the difference between the two receiver options. With the CCHD-957, receiver B brings the floor up by about 6 dB at high frequencies; you can see this effect starting as low as 100 Hz due to the lower noise in the direct measurement. As before, receiver A adds more broadband phase noise: about 0.4 to 0.5 ps RMS jitter. (There is a scaling difference on the phase noise plot due to the difference in oscillator frequencies; that's why the CCHD-957 with receiver A is about 3 dB higher than the Tentlabs XO with receiver A, even though its RMS jitter is lower.)

It looks like the oscillators on clock source B perform better than those on clock source A, probably due to the lower noise power supply. Again, keep in mind that I used post-processing to remove high-frequency spurs, so these

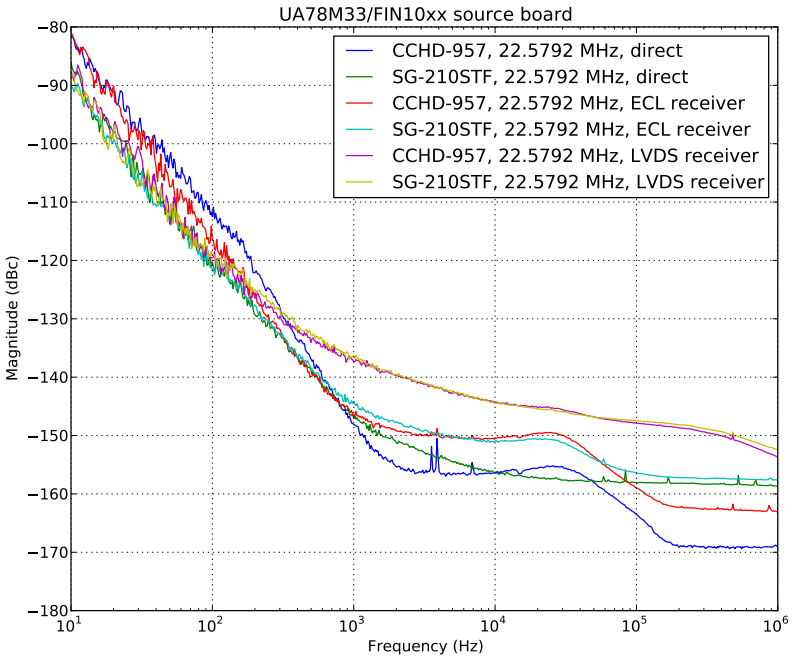

Figure 3: Comparison of oscillators on clock source A, with three measurement options: at the oscillator, using receiver A (LVDS), and using receiver B (ECL).

Oscillator	**Jitter**	**Excess jitter**	
		Receiver A	Receiver B
Crystek CCHD-957	0.124 ps	0.403 ps	0.132 ps
Tentlabs XO	0.842 ps	0.504 ps	0.217 ps

Table 2: RMS jitter for clock source B and excess jitter from each receiver.

measurements will need to be repeated once that problem is fixed.

Trace lengths

One question is whether the length of the trace matters, and if it does, does that depend on the source/receiver combination? To investigate, I compared the 5 available traces with all 4 source/receiver combinations, using the Crystek oscillators. These results are summarized in table 3, with phase noise plots and discussion thereafter.

Figure 5 shows a comparison of trace lengths for source A and receiver A, with the direct measurement shown for reference (note again that the higher close-in phase noise is probably an anomaly). Very little difference is apparent in the phase noise spectra, and table 3 bears this out with integrated excess jitter (attributed to the source/receiver chain) in a very narrow range of 0.412–0.427 ps RMS.

Figure 6 combines source A with receiver B. It is clear that receiver B introduces less phase noise than receiver A above 300 Hz. However, the close-in phase noise does seem to depend on the trace length, with the longer traces (9” or 12”) shifted up by 4–6 dB. It’s possible that this is just a measurement anomaly similar to the higher close-in phase noise in the direct measurement. However, it does indicate the possibility that the trace length may have an impact on this source/receiver combination. This may be because the LVDS transmitter, with its relatively low drive strength

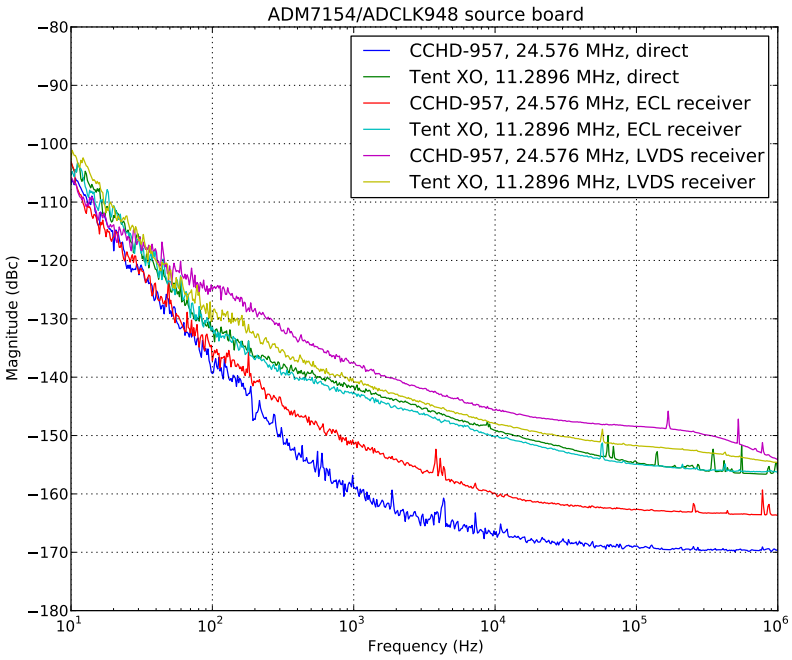

Figure 4: Comparison of oscillators on clock source B, with three measurement options: at the oscillator, using receiver A (LVDS), and using receiver B (ECL).

(3.5 mA), is unable to drive the capacitance of the longer traces without a slew rate degradation at the receiver. (Keep in mind that these measurements involved extra 0.1" headers and 5" long flying leads in addition to the differential traces between source and receiver, so the situation is likely to improve in the final design.)

Figure 7 combines source B with receiver A. There is a small (1–2 dB) broadband phase noise difference between the traces. However, it's unclear if this is due to the trace length or some other aspect of the PCB layout. The excess jitter varies from 0.427–0.629 ps RMS. The degraded close-in phase noise with the CLK3 trace is probably an anomaly.

Figure 8 shows the results with source B and receiver B (the most expensive option). Phase noise performance doesn't appear to be affected by trace length. TODO: Investigate why the integrated excess jitter for CLKF is so high.

Power supply and vibration sensitivity

In addition to the trace length, I did a couple other experiments to investigate the behavior of the CCHD-957 oscillators. Figure 9 shows the apparent effect of different power supply regulators on the oscillator outputs (before the transmitter). Two of the traces were taken with clock source A, and one with clock source B. (Note that the clock frequencies are different, but the difference is small enough to avoid drastically scaling the phase noise spectra.) For one of the measurements, I disconnected the output of the UA78M33 regulator and connected the low noise power supply built into the phase noise analyzer. This improved the results, especially in the range between 3–100 kHz. (Maybe the phase noise humps seen with clock source A are related to the UA78M33 regulator?) In general, it appears that the CCHD-957 is sensitive to power supply noise.

I was also curious about the affect of vibration on the oscillator. I wasn't able to create any noticeable spurs by stimulating the source board with my voice, which means that the CCHD-957 isn't egregiously sensitive to vibration. However, I was able to see a difference in the phase noise spectrum when I rapidly tapped on the table beneath the

Source	Trace	Excess jitter	
		Receiver A (LVDS)	Receiver B (ECL)
Source A (LVDS)	CLKF (3.5”)	0.412 ps	0.137 ps
Source A (LVDS)	CLK0 (4”)	0.418 ps	0.142 ps
Source A (LVDS)	CLK1 (5”)	0.425 ps	0.189 ps
Source A (LVDS)	CLK2 (9”)	0.421 ps	0.869 ps
Source A (LVDS)	CLK3 (12”)	0.427 ps	0.611 ps
Source B (ECL)	CLKF (3.5”)	0.629 ps	0.283 ps
Source B (ECL)	CLK0 (4”)	0.427 ps	0.153 ps
Source B (ECL)	CLK1 (5”)	0.462 ps	0.154 ps
Source B (ECL)	CLK2 (9”)	0.465 ps	0.142 ps
Source B (ECL)	CLK3 (12”)	0.545 ps	0.145 ps

Table 3: Excess jitter for different trace lengths.

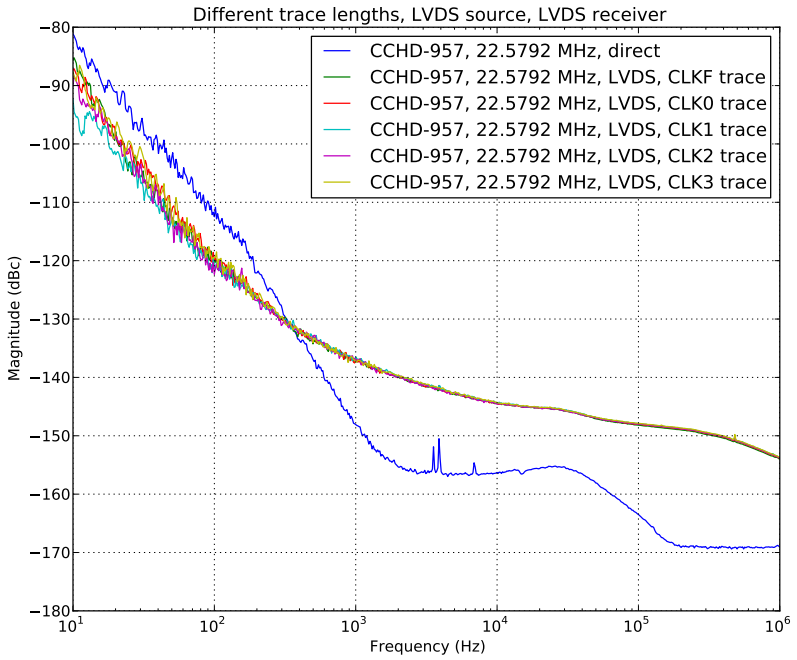

Figure 5: Comparison of differential trace lengths for Crystek 22.5792 MHz oscillator on source board A, with receiver A.

PCBs. Figure 10 shows this effect, with the spur-removal postprocessing disabled. The excess jitter from the vibrations mixing into the oscillator output is 0.069 ps, smaller than the impact of the clock distribution circuits evaluated above.

Conclusion

These measurements examined the impact of supply regulators, oscillators, differential transmitters and receivers, and PCB traces on phase noise performance. Of the 3 oscillators tested, the Crystek CCHD-957 has the lowest phase noise. (There are probably better oscillators but I didn’t try them; finding the best oscillator wasn’t the main goal here.) It is quite sensitive to power supply noise but (unscientifically speaking) not sensitive to small amounts of

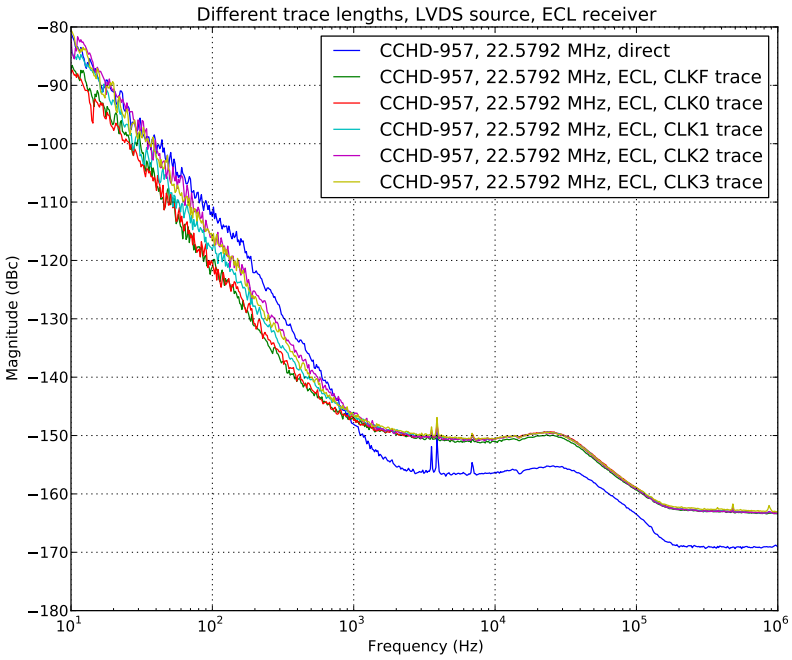

Figure 6: Comparison of differential trace lengths for Crystek 22.5792 MHz oscillator on source board A, with receiver B.

vibration. Purpose-built LVPECL clock distribution chips introduced less phase noise than their LVDS counterparts; this difference was more pronounced in the receiver than in the transmitter. It appears that either LVDS or LVPECL schemes can tolerate 12” long differential traces.

Finally, even with the best components tested, differential clock distribution does degrade the performance of a good oscillator like the CCHD-957. The excess phase noise is mostly at 1 kHz and higher offsets, and integrates out to around 0.15 ps RMS (assuming 5 MHz bandwidth). This may be an unavoidable price to pay for synchronizing multiple DAC/ADC modules to a single oscillator across a physically large PCB. I cannot predict whether this difference will be measurable or subjectively noticeable in an audio application.

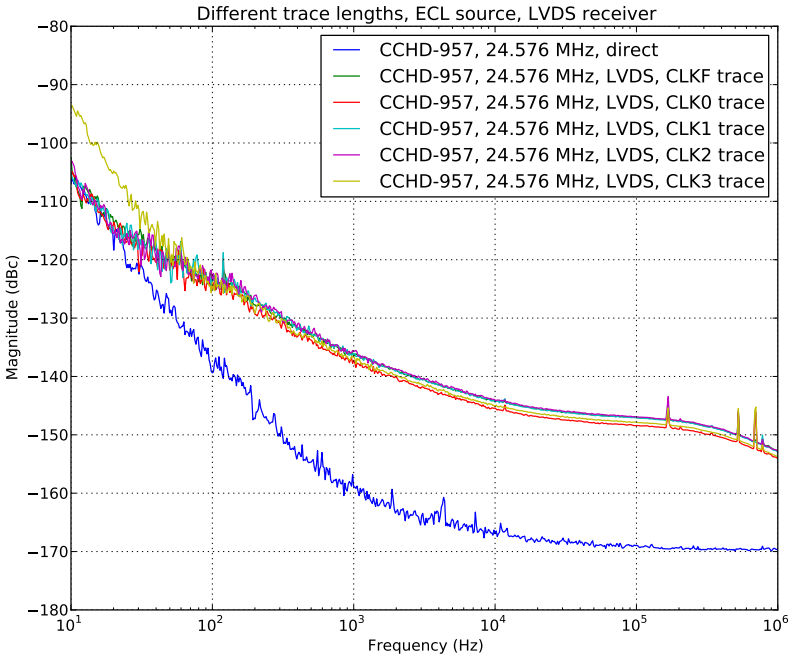

Figure 7: Comparison of differential trace lengths for Crystek 24.576 MHz oscillator on source board B, with receiver A.

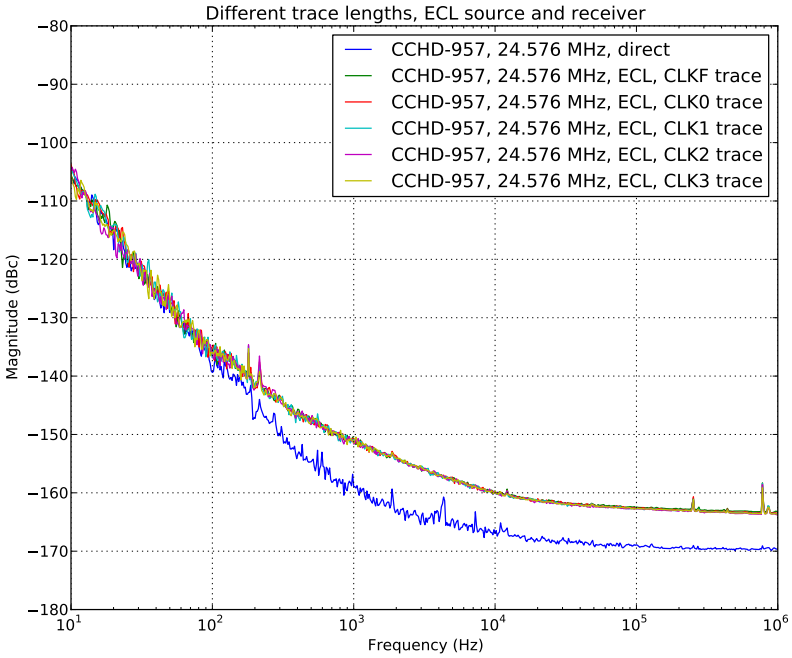

Figure 8: Comparison of differential trace lengths for Crystek 24.576 MHz oscillator on source board B, with receiver B.

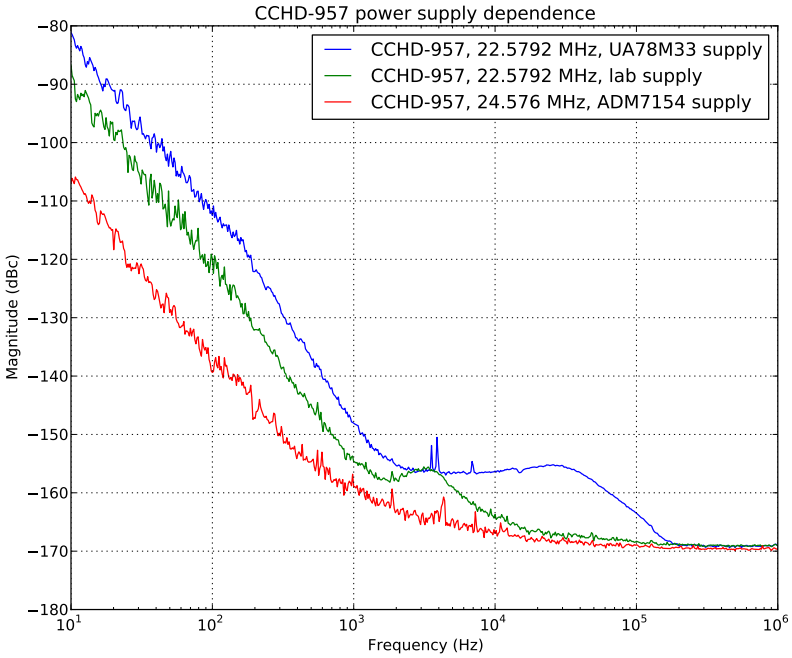

Figure 9: Comparison of supply regulation options for Crystek oscillators, measured at the oscillator.

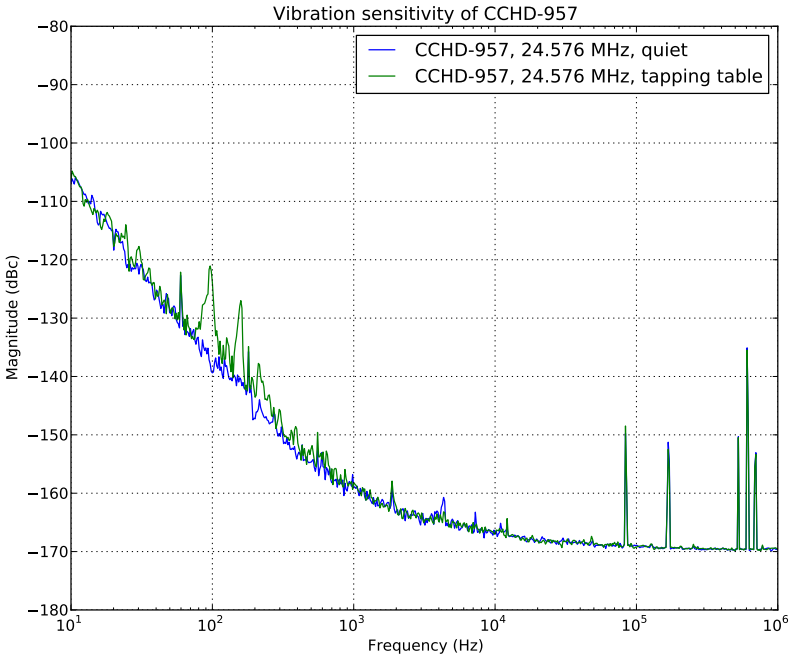

Figure 10: Effect of vibration (table tapping) on Crystek 24.576 MHz oscillator on source board B, measured at the oscillator.