

M. Price 10/6/2017

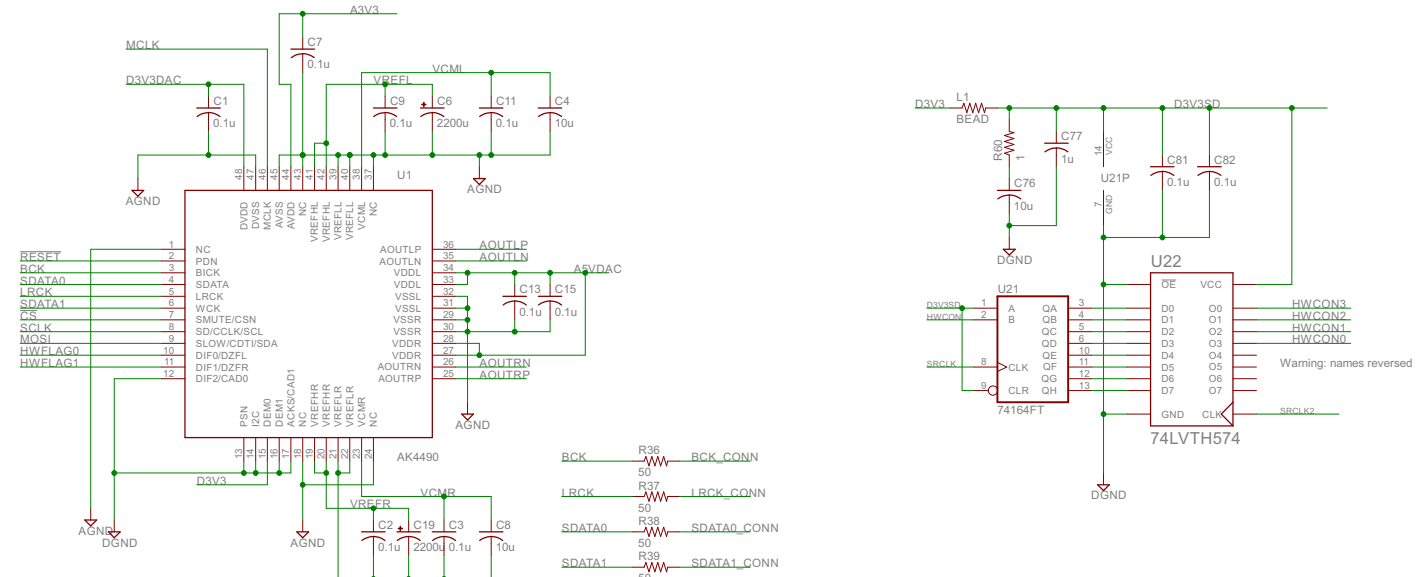
The diagram illustrates the pin connections for the J1L and J1R headers. The J1L header (left) is connected to pins 1L through 20L. The J1R header (right) is connected to pins 1R through 20R. The connections are as follows:

- J1L Header:**
 - Pin 1: AP15V
 - Pin 2: AGND
 - Pin 3: AGND
 - Pin 4: AN15V
 - Pin 5: AGND
 - Pin 6: AP5V
 - Pin 7: DP3V3
 - Pin 8: DGND
 - Pin 9: BCK
 - Pin 10: DGND
 - Pin 11: LRCK
 - Pin 12: SDATA0
 - Pin 13: SDATA1
 - Pin 14: SDATA2
 - Pin 15: SDATA3
 - Pin 16: DGND
 - Pin 17: CS
 - Pin 18: MOSI
 - Pin 19: MISO
 - Pin 20: DGND
- J1R Header:**
 - Pin 1: AP15V
 - Pin 2: AGND
 - Pin 3: AGND
 - Pin 4: AN15V
 - Pin 5: AGND
 - Pin 6: AP5V
 - Pin 7: DP3V3
 - Pin 8: DGND
 - Pin 9: BCK
 - Pin 10: DGND
 - Pin 11: LRCK
 - Pin 12: CHAN
 - Pin 13: SCLK
 - Pin 14: SRCLK
 - Pin 15: SRCLK2
 - Pin 16: RESET
 - Pin 17: DGND
 - Pin 18: MCLKN
 - Pin 19: MCLKP
 - Pin 20: DGND

The diagram also shows connections for AGND, DGND, and MOD-V2.

The image displays several circuit diagrams for power management ICs, organized into sections:

- 5 V supply for VDDL:** A schematic for the LT3042DD (U15) configured as a precision current source. It uses a 4.7uF capacitor (C17), a 4.7uF capacitor (C18), and a 43.9K resistor (R3) to set the current. The output is connected to the IN/UV, PG, and SET pins. The OUTS pin is connected to the A5VDAC pin. The GND pins are connected to AGND. A 22 ohm / 2200 uF reference filtering network is shown.
- 5 V supply for VREFLIR:** A schematic for the LT3042DD (U16) configured as a precision current source. It uses a 4.7uF capacitor (C83), a 4.7uF capacitor (C84), and a 43.9K resistor (R6) to set the current. The output is connected to the IN/UV, PG, and SET pins. The OUTS pin is connected to the A5VREF pin. The GND pins are connected to AGND. A 22 ohm / 2200 uF reference filtering network is shown.
- 5 V supply for output buffers - preregulator to keep thermal load off ADP7142:** A schematic for the ADP7142 (U3) configured as a preregulator. It uses a 4.7uF capacitor (C12), a 100uF capacitor (C29), and a 10uF capacitor (C5) to filter the input. The output is connected to the IN pin. The EN pin is connected to the A5V pin. The SENSE/ADJ pin is connected to the A5V pin. The GND pins are connected to AGND.
- 5 V supply for output buffers:** A schematic for the ADP7182 (U4) configured as a negative voltage regulator. It uses a 4.7uF capacitor (C31), a 10uF capacitor (C2), and a 10uF capacitor (C70) to filter the input. The output is connected to the IN pin. The EN pin is connected to the A5V pin. The GND pins are connected to AGND.
- 3.3 V supply for AK4490 AVDD:** A schematic for the ADM7160 (U5) configured as a 3.3V voltage regulator. It uses a 1uF capacitor (C16), a 1uF capacitor (C10), and a 220uF capacitor (C20) to filter the input. The output is connected to the IN pin. The EN pin is connected to the A3V3 pin. The GND pins are connected to AGND.
- 3.3 V supply for AK4490 DVDD:** A schematic for the ADM7160 (U11) configured as a 3.3V voltage regulator. It uses a 1uF capacitor (C78), a 1uF capacitor (C79), and a 1uF capacitor (C79) to filter the input. The output is connected to the IN pin. The EN pin is connected to the D3V3DAC pin. The GND pins are connected to AGND.
- ADM7154 (3.3 V) - powers LVPECL receiver:** A schematic for the ADM7154 (U8) configured as a 3.3V voltage regulator. It uses a 1uF capacitor (C71), a 1uF capacitor (C43), a 1uF capacitor (C45), a 1uF capacitor (C41), a 1uF capacitor (C35), and a 1uF capacitor (C42) to filter the input. The output is connected to the IN pin. The EN pin is connected to the D3V3_FCL pin. The GND pins are connected to DGND.



Uses ADA4899-1 wide bandwidth op amp

