Audio clock distribution prototyping - Phase noise measurement plan

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**Background**

I work for Analog Devices (Cambridge, MA), but this is a hobby project not sanctioned by the company. In other words, low priority.

In my spare time, I’m making a board that allows up to 4 audio DAC/ADC modules to be plugged in with a standardized interface. Each module can be either 2-channel or 8-channel. The intent is to support various audio system configurations (digital crossover/equalization, music recording, multichannel, etc.) and facilitate experimentation. The design will be open sourced after I test a complete prototype.

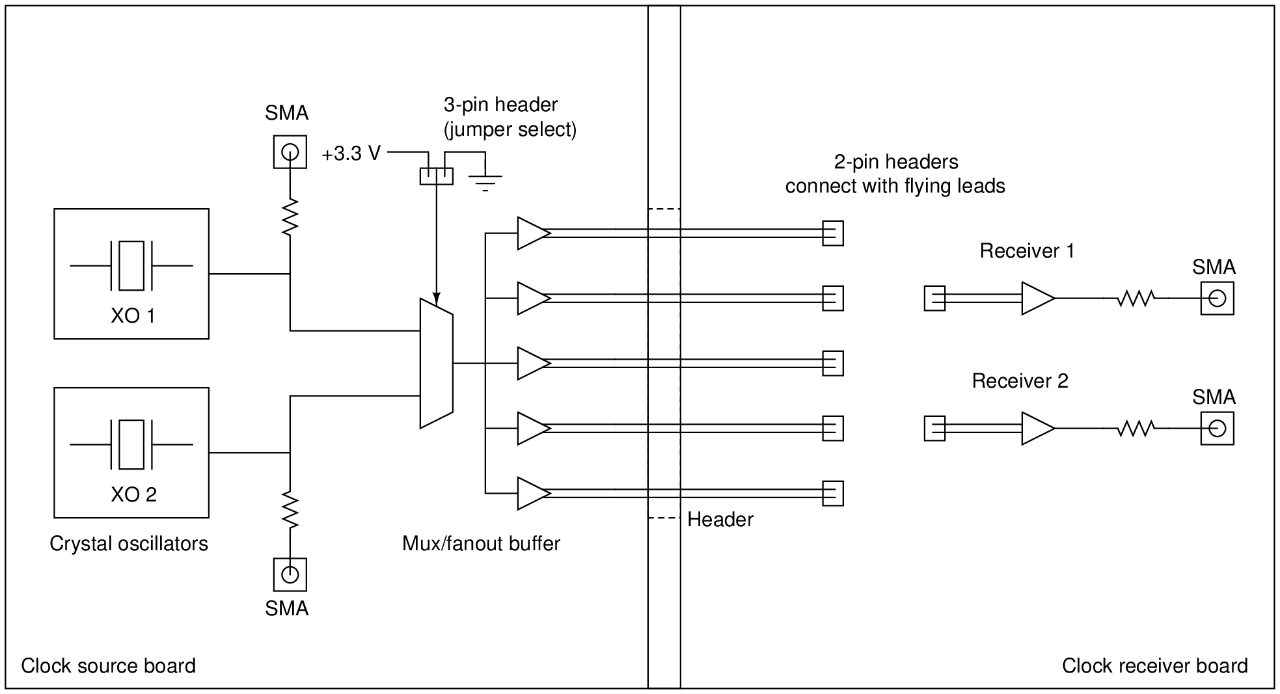
The system has two clocks, 22.5792 MHz and 24.576 MHz. At any time, one of the clocks is active depending on the desired audio sample rate (44.1 kHz vs. 48/96/192 kHz). The board has to perform this 2:1 muxing and distribute the selected clock to the 4 modules (over about 12” or 300 mm of PCB) and to an FPGA that buffers the audio samples.

Audio enthusiasts can be particular about the quality of the clocks provided to their DAC/ADC chips. Phase noise in the clock is one of the error sources, in addition to the converter itself and the analog interface (filtering and/or I/V conversion). Some audio DAC designs employ high performance oscillators (positioned in proximity to the DAC chip), extensive supply filtering, and/or mechanical isolation to minimize phase noise. The errors are small, and I’m not very experienced with the subjective impacts. However, I would like to ensure that my clock distribution does not significantly degrade the performance of the oscillator, or at least quantify the degradation if it is measurable. The intent is to make other hobbyists comfortable using the platform even if they have concerns about phase noise.

Another intent of this measurement is to teach myself about the impact of board-level design choices, which is why I constructed options to evaluate different oscillators and clock distribution parts. The options are listed below.

**Device under test**

The prototyping setup consists of two boards: a clock source and clock receiver.



There are two interchangeable clock source boards:

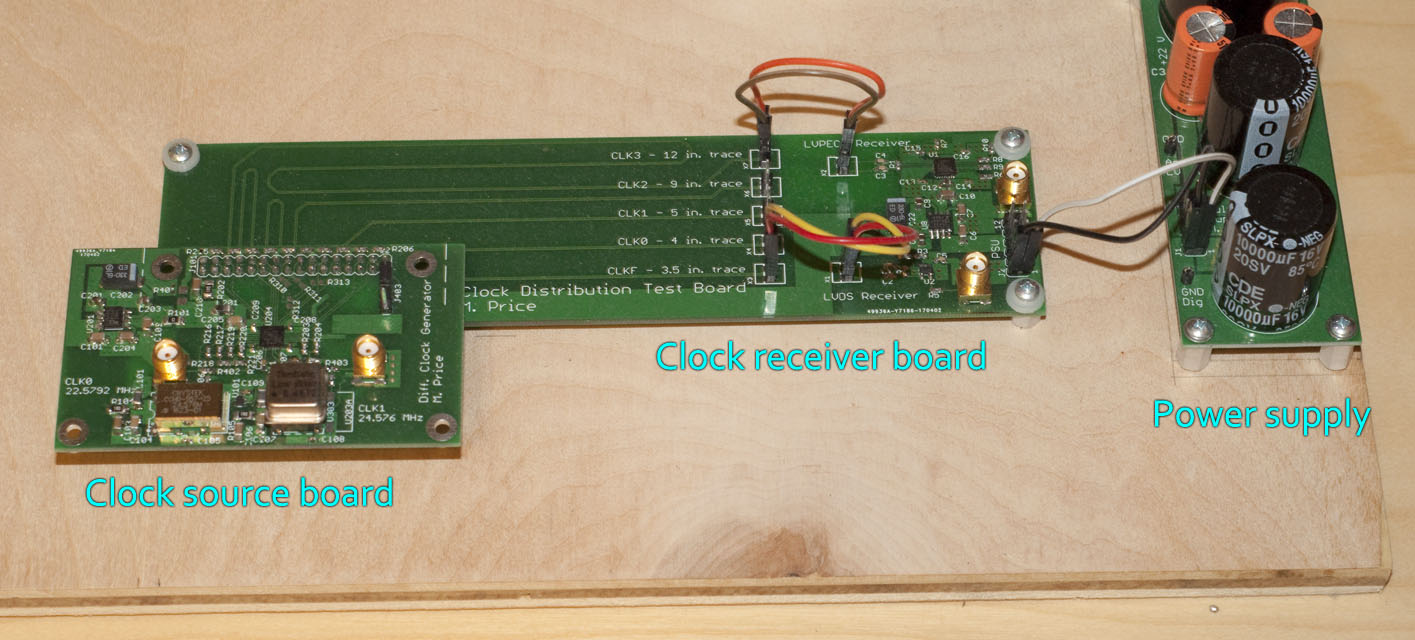
* One clock source uses a 74-series mux and standard LVDS transmitters to drive differential outputs. It is populated with two crystal oscillators (selectable by jumper):
  1. Epson SG-210STF (2.5x2.0 mm SMD), 22.5792 MHz.  
     Specified phase noise is -145 dBc/Hz at 1 kHz offset.
  2. Crystek CCHD-957 (14x9 mm SMD), 22.5792 MHz.  
     Specified phase noise is -149 dBc/Hz at 1 kHz offset. (-97 dBc/Hz at 10 Hz offset)
* The other clock source uses an ADCLK948 to perform muxing and drive differential outputs. Its oscillators are:
  1. Crystek CCHD-957 (14x9 mm SMD), 24.576 MHz.  
     Specified phase noise is -149 dBc/Hz at 1 kHz offset. (-98 dBc/Hz at 10 Hz offset)
  2. Tentlabs XO (11x11 mm DIP), 8.4672 MHz.  
     Specified phase noise is -151 dBc/Hz at 1 kHz offset. (-93 dBc/Hz at 10 Hz offset)

Each clock source board has 5 differential clock outputs routed to a 0.1”-pitch header that connects to a socket on the clock receiver board. (These outputs are named CLK0, CLK1, CLK2, CLK3, and CLKF.)

There are two receivers (differential to single-ended converters) on the clock receiver board:

* One uses a standard LVDS receiver.
* The other uses an AD9515.

Each of these receivers has a 2-pin 0.1” header for differential input and is AC coupled by 10 nF capacitors. Meanwhile, the 5 outputs of the clock source are routed (over traces from 3.5” to 12” in length) to 2-pin 0.1” headers. One of these can be connected to each receiver using jumper wires or zero-ohm resistors.



QUESTION: Any obvious problems with this design?

QUESTION: Would this DUT require metal shielding to obtain the desired performance?

QUESTION: Each SMA connector is connected to its CMOS output pin through series resistance. Is the value of the resistor important? If so, what should it be?

**Measurements so far**

I confirmed that the boards are functional: 3.3 V single-ended clock outputs appear with the right frequency for each oscillator.

TODO: Test with a 50 ohm load and/or attenuator.

SAFETY WARNING: The linear PSU has exposed connections that carry high voltages, including the 120 V AC input. To minimize risk, no one should reach into the open chassis while it’s powered on, or touch it except to switch the power off. Also, the filter capacitors retain charge after AC power is removed. Any changes to power supply connections must be made carefully (this should not be necessary as part of the phase noise measurements).

**Measurement plan**

Equipment:

* Prototyping chassis with PSU and clock boards installed
* Phase noise analyzer with appropriate reference source
* SMA cables and attenuators as needed
* SPL meter for vibration sensitivity tests

QUESTION: What attenuator configuration should be used for a 3.3 V single-ended source?

QUESTION: What reference sources (VCO) are available and which should be used? The E5505 manual shows that the 8662/3A has better close-in performance than other sources, but the numbers still seem high compared to the crystal oscillator specifications (maybe because the frequencies are different).

The frequency offset range of interest is from 10 Hz to half the oscillator frequency (a constant limit between 1-4 MHz for all tests would be fine). I would ideally like to obtain measurement files on a USB stick (or, failing that, images of the spectrum display for each measurement).

I envision that some setup adjustments (and possibly revisions to the DUT hardware) may be required to get the best measured performance.

*Part 1: oscillators*

The first set of measurements is to capture the differences between the three available types of oscillators. The clock receivers are not connected or used. We only observe the 3.3 V CMOS output directly from the oscillator.

1. Install clock source board 1. Place the oscillator select jumper on pins 1-2. Connect the phase noise analyzer to SMA connector J401. Power up the PSU and capture the phase noise spectrum.
2. Power down the PSU. Move the oscillator select jumper to pins 2-3. Move the phase noise analyzer to SMA connector J402. Power up the PSU and capture the phase noise spectrum.
3. Power down the PSU. Disconnect the phase noise analyzer and remove the clock source board. Repeat steps 1-2 with clock source board 2.

QUESTION: Do crystal oscillators need to warm up?

*Part 2: receivers*

The second set of measurements is to measure the added phase noise introduced by clock distribution (single-ended to differential conversion and back).

QUESTION: Should this be performed as a residual measurement or just two separate absolute measurements? I’m currently assuming that they are separate absolute measurements.

1. Install clock source board 1. Place the oscillator select jumper on pins 1-2. Connect the header for the CLK3 trace (X7) to the header for receiver 1 (X1). Connect the phase noise analyzer to SMA connector X9. Power up the PSU and capture the phase noise spectrum.
2. Power down the PSU. Move the oscillator select jumper to pins 2-3. Power up the PSU and capture the phase noise spectrum.
3. Power down the PSU. Move the differential wire connection from X1 to X2 to use receiver 2. Move the phase noise analyzer to SMA connector X8. Repeat steps 1-2 to capture phase noise spectra of the two oscillators on clock source board 1 using receiver 2.
4. Power down the PSU. Remove clock source board 1 and install clock source board 2. Repeat steps 1-3 to capture phase noise spectra of the two oscillators on clock source board 2 using both receivers.

*Part 3: impact of trace length*

One combination of oscillator/driver/receiver should be chosen (probably the best performing one). Then the phase noise measurement will be repeated for each of the 5 available clock outputs.

*Part 4: vibration sensitivity*

To get an imprecise estimate of vibration sensitivity, I would like to repeat the phase noise measurement of one oscillator/driver/receiver combination in the presence of sound. An arbitrary broadband source (probably my voice) will be adjusted to sound levels (measured near the clock source board) of 70, 80, and 90 dB.

**Post-processing**

The phase noise spectra are fairly self-explanatory so there isn’t much to do. I figured I would make some overlay plots of the phase noise with/without the distribution network, and compute the integrated jitter over a certain bandwidth (say, 10 Hz to 1 MHz). But I’ll take any suggestions.