

Recommended Design Rules and Strategies for BGA Devices

User Guide

UG1099 (v1.0) March 1, 2016

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/2016	1.0	Initial Xilinx release.

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General BGA and PCB Layout Overview

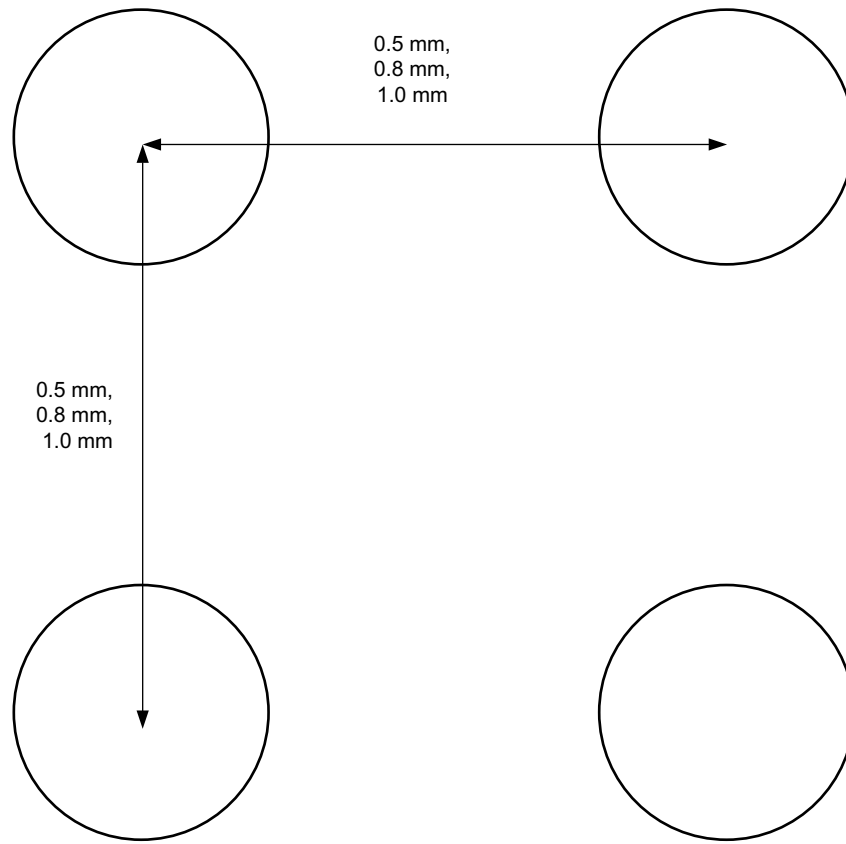
Introduction

Xilinx® UltraScale™ architecture, 7 series, and 6 series devices come in a variety of packages that are designed for maximum performance and maximum flexibility. Three pitch sizes are available for these packages: 1.0 mm, 0.8 mm, and 0.5 mm. In general, as the pitch size decreases, the challenges for PCB routing increase as there is less room to route traces and vias between package balls. This guide illustrates various methods for successful design regardless of pitch size.

Note: Throughout this guide, various specifications and estimates are given regarding PCB pricing, costs, and technology. As PCB manufacturing technology is constantly advancing, it is highly advised to consult with your PCB manufacturer to fully understand their capabilities regarding the information presented here.

Pitch Size

Pitch size is defined as the distance between consecutive balls on a BGA package, measured from center to center, as shown in [Figure 1-1](#).



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Figure 1-1: Definition of Pitch Size

BGA Landing Pads

Xilinx recommends using Non Solder Mask Defined (NSMD) copper BGA landing pads for optimum board design. NSMD pads are pads that are not covered by any solder mask, as opposed to Solder Mask Defined (SMD) pads in which a small amount of solder mask covers the pad landing. [Figure 1-2](#) illustrates the difference between NSMD and SMD pads.

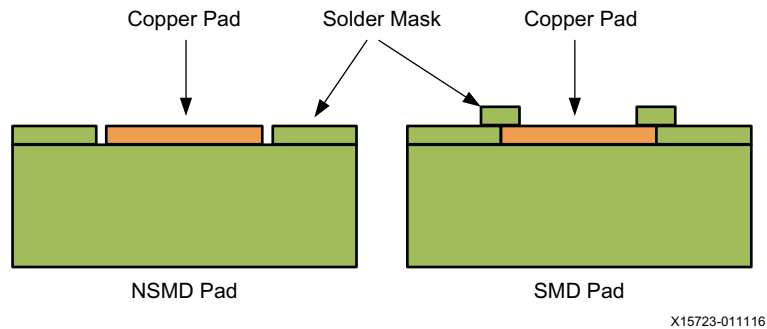


Figure 1-2: NSMD and SMD Pads

Layer Count Estimation and Optimization

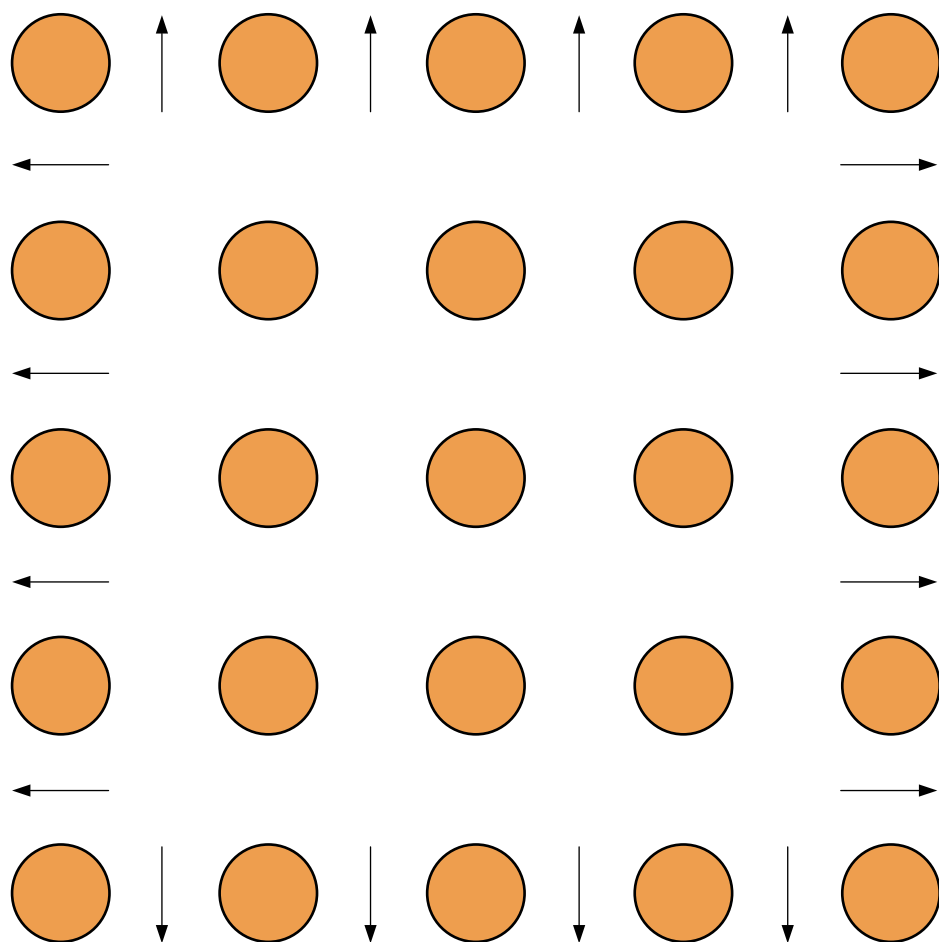
Layer Count Estimation

A quick way to estimate the number of routing layers required to fully break out signal pins from the FPGA would be to use [Equation 2-1](#):

$$\text{Layers} = \frac{\text{Signals}}{\text{Routing Channels} \times \text{Routes Per Channel}} \quad \text{Equation 2-1}$$

For Xilinx FPGAs, the amount of signals is approximately 60% of the number of BGA balls. The other 40% are power and ground signals that are most often routed directly down to planes by vias. This is assuming full I/O utilization. If fewer I/Os are used, then the number of signals to route goes down accordingly.

Routing channels are the number of available routing paths out of the BGA area (the number of BGA pins on one side minus one, times four sides). [Figure 2-1](#) shows a 5x5 grid with sixteen total routing channels (four routing channels per side times four sides).



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Figure 2-1: Definition of Routing Channel (16 Total Routing Channels Shown)

Routes per channel is either one or two, depending on whether one or two signals are routed between BGA pads. The approximate number of layers required to fully route out a Xilinx FPGA are shown in Table 2-1.

Table 2-1: Approximate Signal Layers per # of Package Pins

BGA Pins	Ball Pitch (mm)	Signal Layer Counts All Available IOs Routed Routes Per Channel	
		Two	One
196	0.5	N/A	2
225	0.8	2	3
236	0.5	N/A	3
256	1.0	2	3
324	0.8	2	3
400	0.8	2	3
484	0.8	3	4
484	1.0	2	4
625	0.8	3	4
676	1.0	3	5
784	0.8	4	5
784	1.0	3	5
900	1.0	3	5
1156	1.0	3	6
1517	1.0	4	7
1760	1.0	4	8
1924	1.0	4	8
2104	1.0	4	8
2377	1.0	5	9
2577	1.0	5	9
2892	1.0	5	10

Layer Count Optimization

UltraScale architecture, 7 series, and 6 series packages have full matrices of solder balls. The number of layers required for effective routing of these packages is dictated by a variety of factors, including:

- BGA Size (amount of pins)
- Pad size, pad pitch, and trace width
- Fixed pinouts

- Fabrication technologies

BGA Size

The amount of pins in a BGA indicates the amount of signals to route. Because of physical space constraints, the amount of signals required to route is proportional to the amount of signal layers required.

Pad Size, Pad Pitch, and Trace Width

The pad size and pitch determines the available space between adjacent balls for signal escape. Based on the chosen trace width, one or two signals can be routed between adjacent pads. If one signal escapes between adjacent pads, then one signal row can be routed on a single metal layer. The exception to this is the outermost row, which allows two routes per layer.

To facilitate routing in the ball grid area, *necking down* the trace width in the critical space between the BGA pads/vias (the breakout area) is allowable. This then allows for two signal rows to be routed on a single metal layer (or three if routing the outermost row).

The traces can then be widened after they escape the breakout area. Changes in width over very short distances can cause small impedance changes. Validate these issues with the board vendor and signal integrity engineers responsible for the design.

Fixed Pinouts

Xilinx FPGA pinouts are designed with maximum flexibility in mind. However, certain FPGA signals, such as JTAG, transceiver inputs and outputs, and Interlaken signals (among others) have fixed locations, which means routing of these signals is limited compared to other signals that can be swapped as needed. Fixed locations lead to layout trade-offs that can have an impact on the number of required signal layers.

Fabrication Technologies

Several advanced fabrication technologies can be used to reduce the amount of layers required to route a design, although each of these technologies increase fabrications costs of the board:

Blind Vias (+20% to +40% fabrication cost) – As opposed to a through-hole via, a blind via does not travel from the top layer to the bottom layer. A blind via travels either from the top or bottom layer to an inner signal layer, freeing up room above or below for other routing.

Buried Vias (+25% to +60% fabrication cost) – A buried via is located entirely inside the printed circuit board and does not touch the top or bottom layers.

Micro Vias (+30% fabrication cost) – A micro via is either a blind or buried via, only much smaller. Micro Vias are most often used in small, high density applications such as cell phones.

Back-drilled Vias (+10% fabrication cost) – A back-drilled via is a through-hole via that has a portion of its length *drilled out* such that it is no longer conductive. This improves signal integrity as it removes an unneeded stub from the route.

Via-In-Pad (+30% fabrication cost) – A via-in-pad is a via drilled directly beneath a pad. This removes the need for a separate metal trace to be drawn to drop down a via. This can result in improved signal integrity because of lower inductance, but the trade-off is a much higher board fabrication cost.

Extra Layers (+20% fabrication cost (per every two layers)) – It might be such that the cost to add two (or more) extra signal layers is lower than the cost to add an advanced technology, so adding layers is not always to be considered a negative alternative.

Maximum Board Thickness

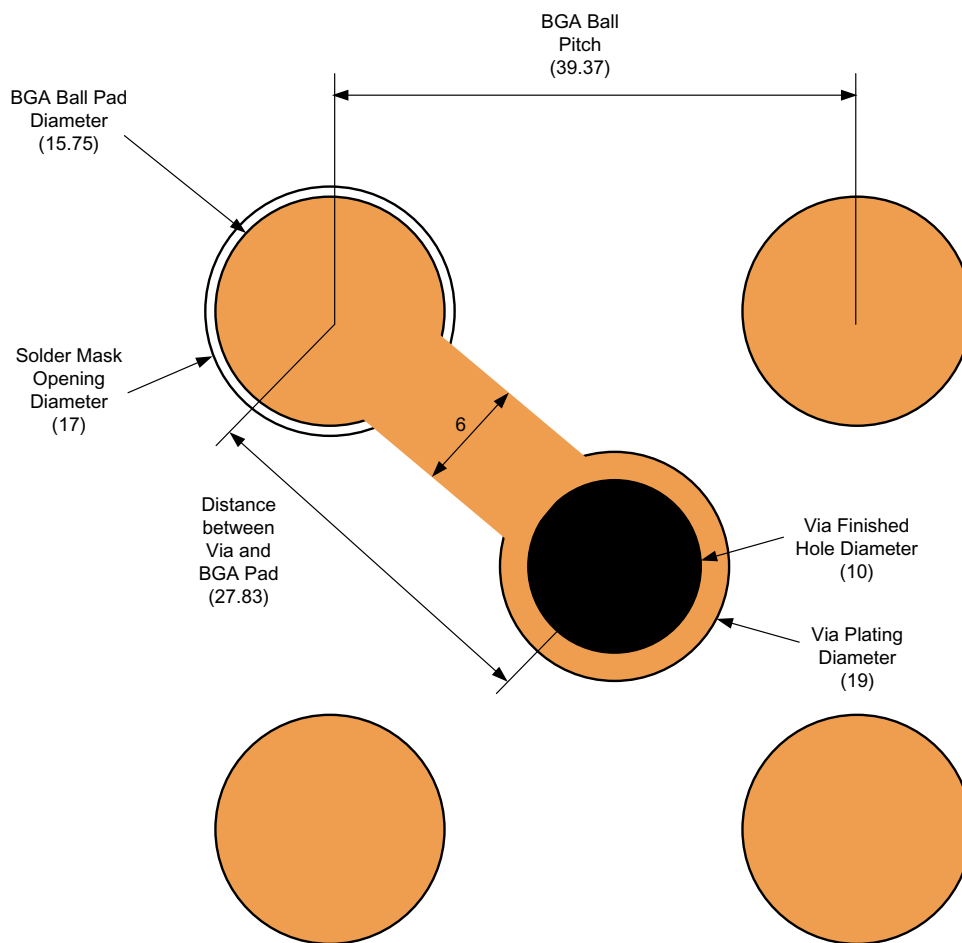
The maximum board thickness is a function of the minimum drill diameter and aspect ratio, both of which are provided by the PCB manufacturer. A typical aspect ratio of 10:1 indicates that the board can be no thicker than ten times the drill diameter. A drill diameter of 13 mils, for example, would lead to a maximum board thickness of 130 mils. With the exception of the CP package, Xilinx recommends finished drill diameters to be 10 mils, which translates to an actual drill diameter of about 13 mils (plating typically reduces the diameter by about 3 mils). A 13 mil drill would lead to a maximum board thickness of 130 mils, assuming a 10:1 aspect ratio. For the CP package, the finished drill diameter of 6 mils approximates a drill diameter of 9 mils, or a maximum board thickness of 90 mils.

If a higher board thickness than the drill diameter and aspect ratio can support is required, the use of buried or blind vias can be used, but at a higher manufacturing cost.

Recommended Layout Dimensions within BGA Area for 1.0 mm Pitch Devices

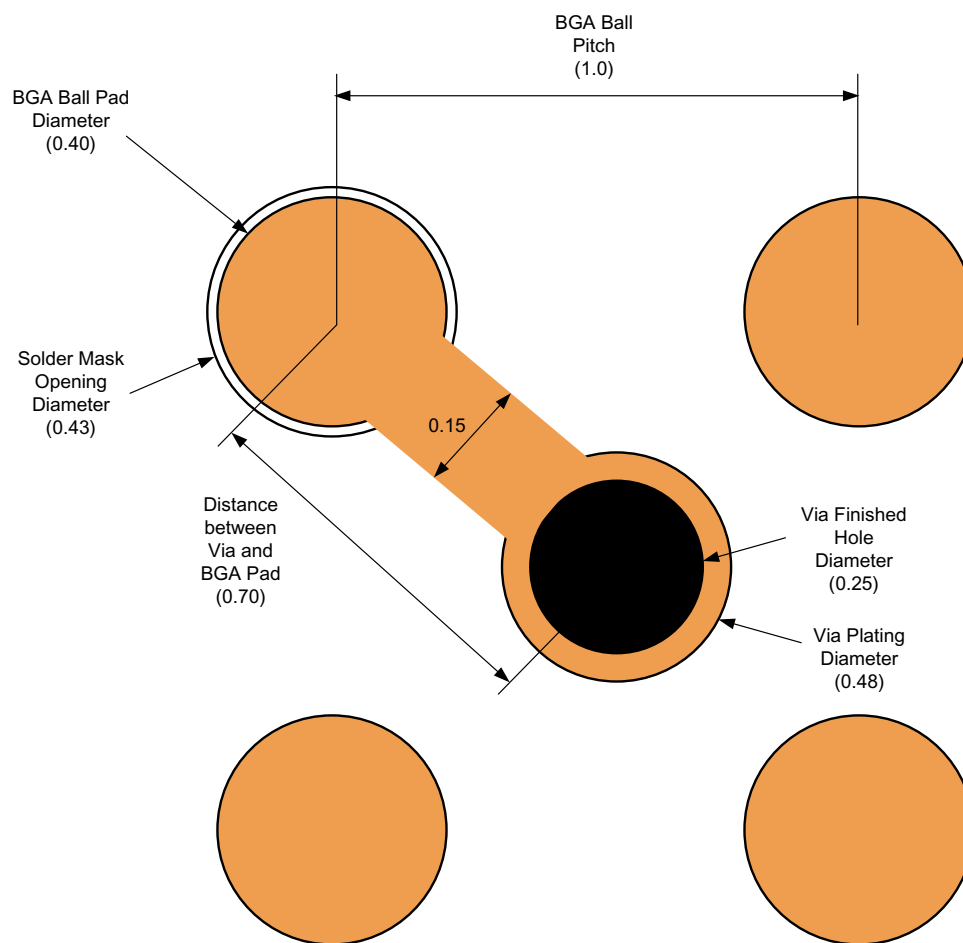
BGA Ball Pad and Via Dimensions

The amount of space available for routing under the FPGA is dependent on the area between the balls in the BGA area (for top and bottom layers), as well as the area between vias (for inner layers). The typical dimensions of FPGA ball pads and vias for 1.0 mm pitch devices are described in [Figure 3-1](#), through [Figure 3-4](#).



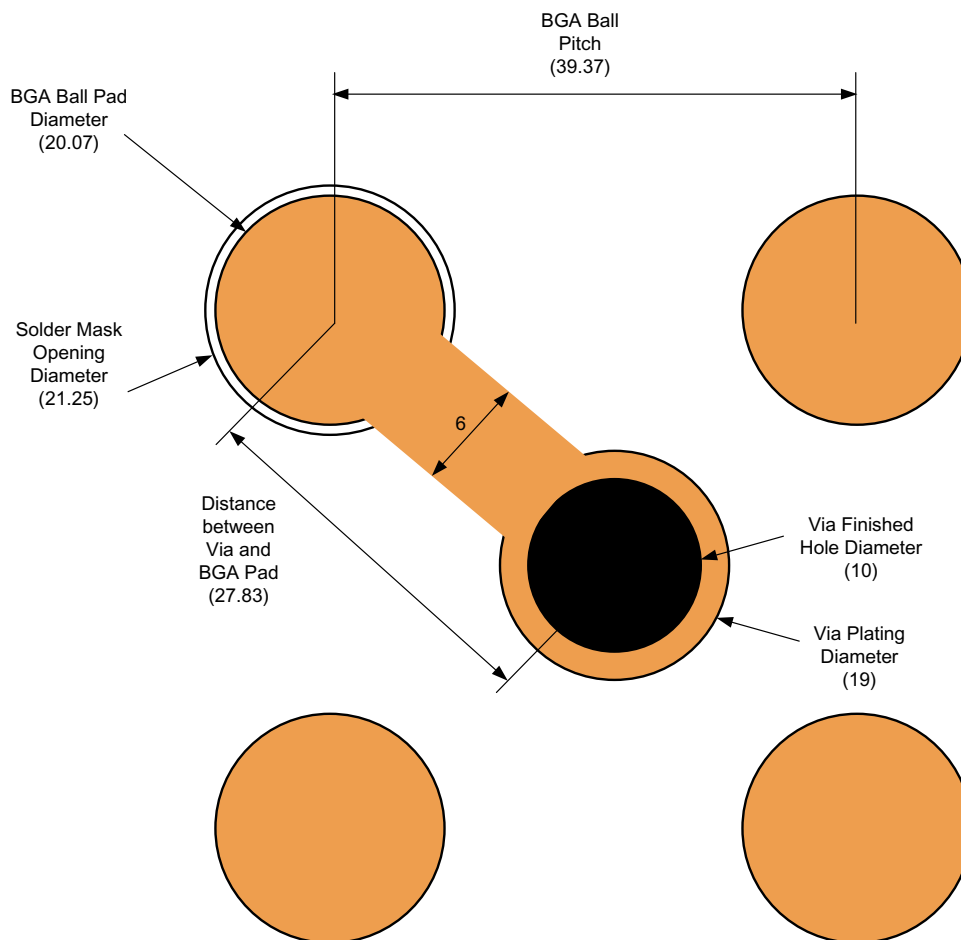
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Figure 3-1: Ball and Via Dimensions for 1.0mm Pitch FB and FT Devices (mils)



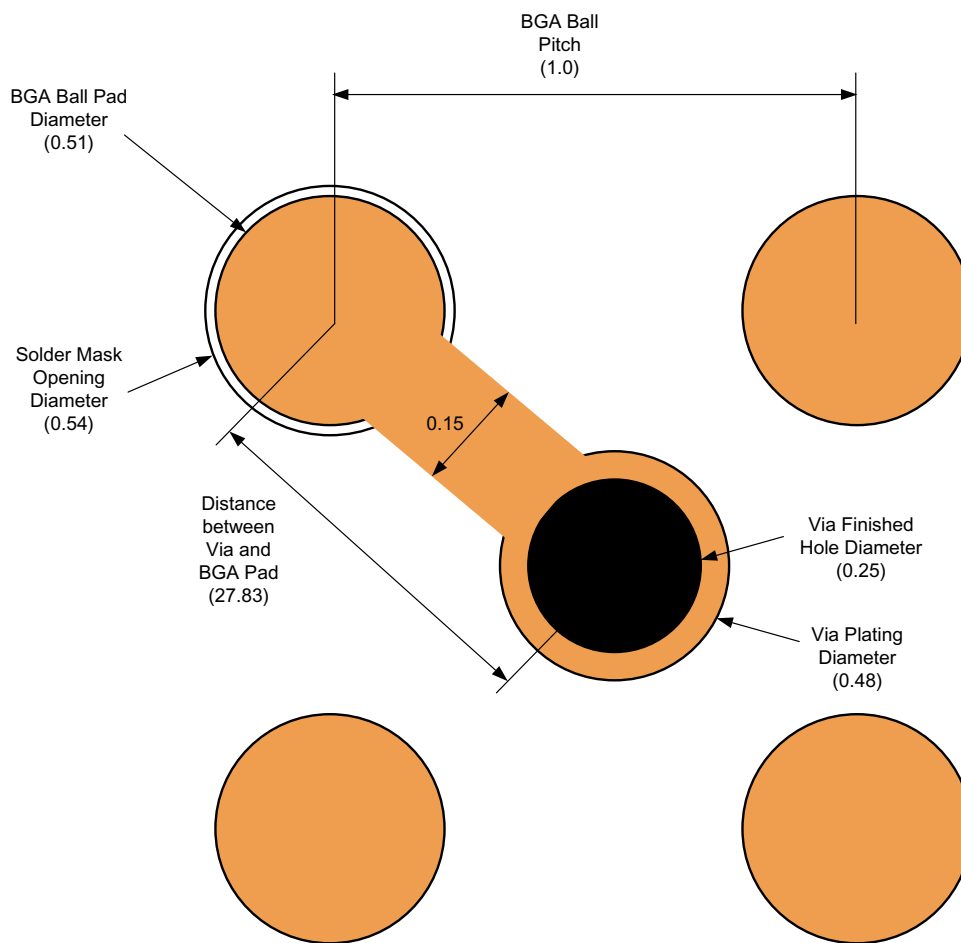
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Figure 3-2: Ball and Via Dimensions for 1.0mm Pitch FB and FT Devices (mm)



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Figure 3-3: Ball and Via Dimensions for 1.0mm Pitch FF, FG, FH, FL, RB, and RF Devices (mils)



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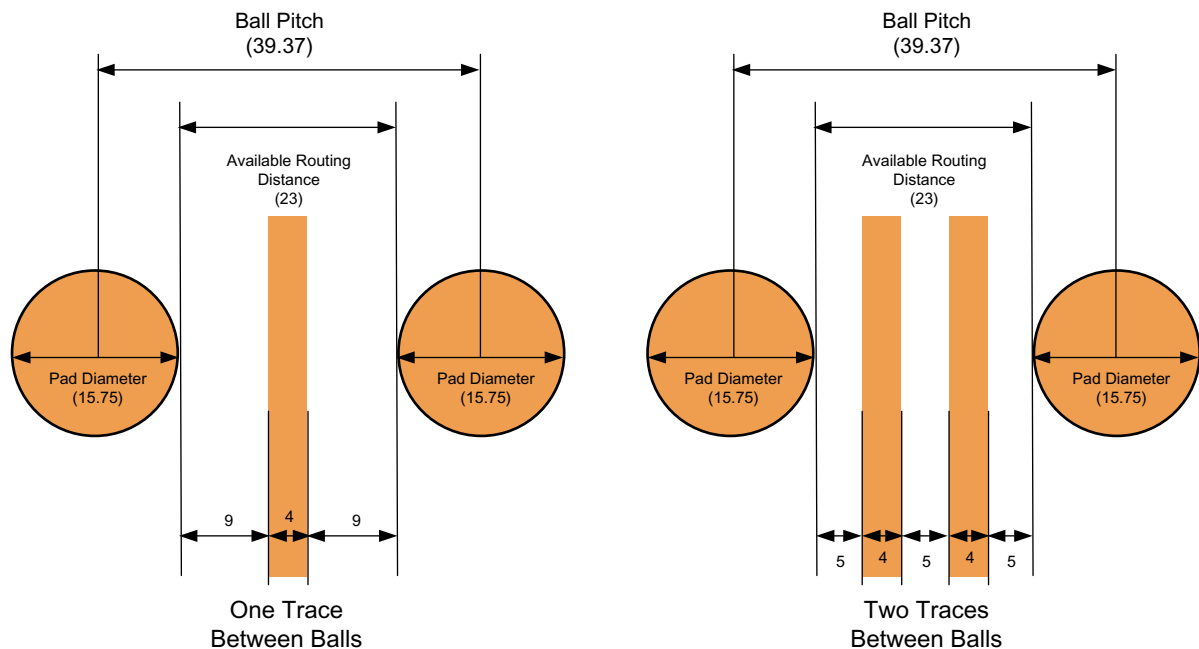
Figure 3-4: Ball and Via Dimensions for 1.0mm Pitch FF, FG, FH, FL, RB, and RF Devices (mm)

Trace Widths Dimensions inside the BGA Area

The ball pitch and BGA pad/via diameters determine how much space is available to route traces between pads or vias. Standard PCB processes can allow for as low as 3.5 mil trace widths with 3.5 mil spacing. Advanced processes can allow for as low as 2 mil trace widths with 2 mil spacing.

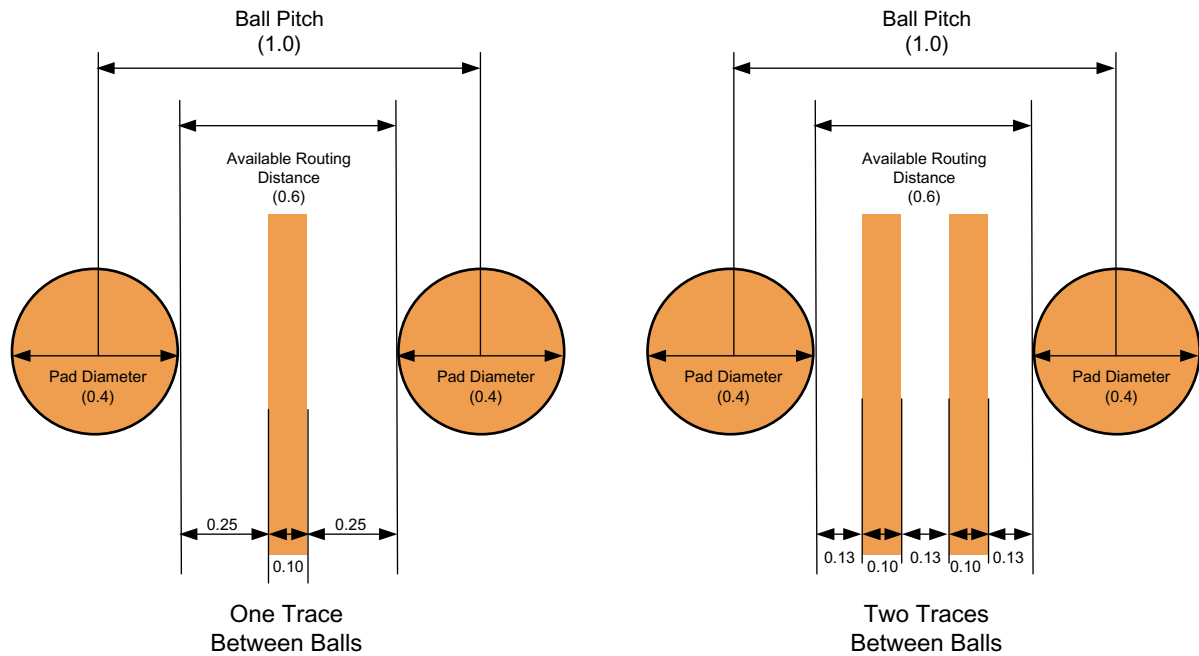
Trace Routing Between BGA Balls

One or two traces can be routed between BGA balls with varying spacing between traces, as shown in [Figure 3-5](#), through [Figure 3-8](#).



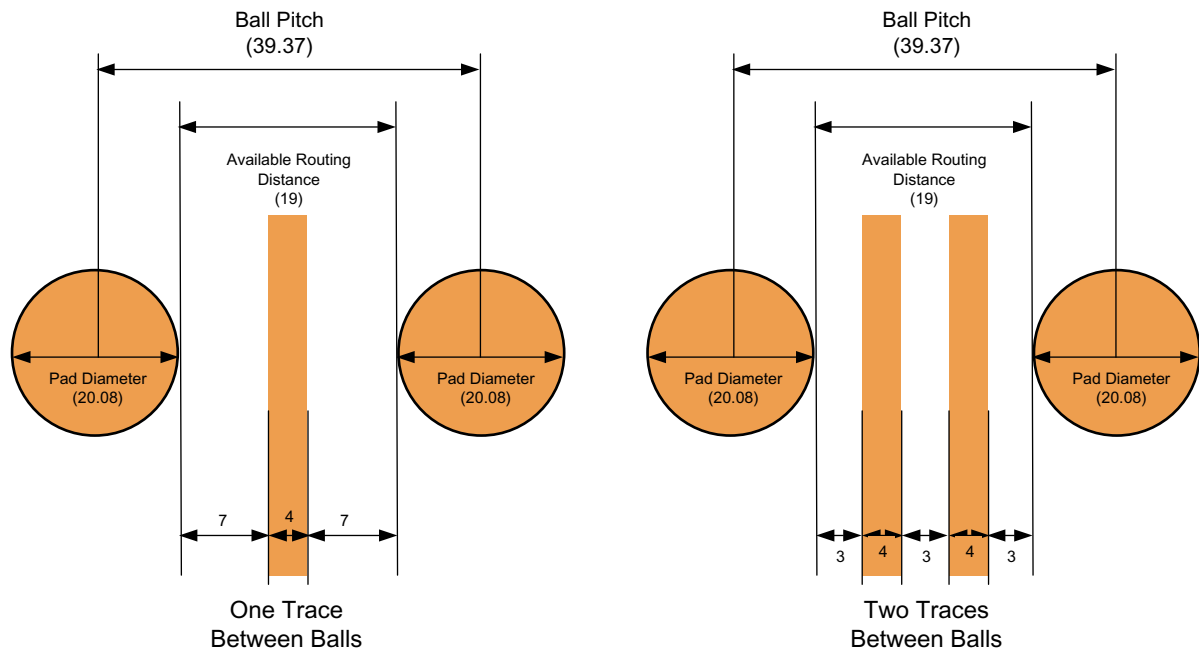
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Figure 3-5: Trace Routing Between BGA Balls for 1.0mm Pitch FB and FT Devices (mils)



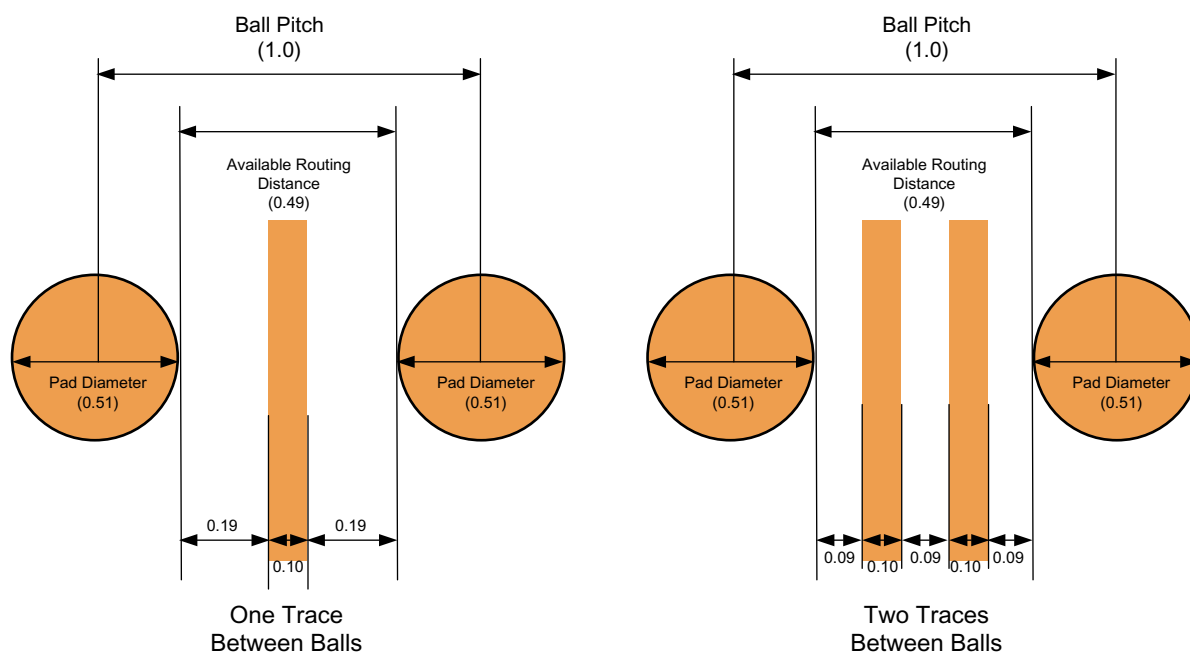
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Figure 3-6: Trace Routing Between BGA Balls for 1.0mm Pitch FB and FT Devices (mm)



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Figure 3-7: Trace Routing Between BGA Balls for 1.0mm Pitch FF, FG, FH, FL, RB, and RF Devices (mils)

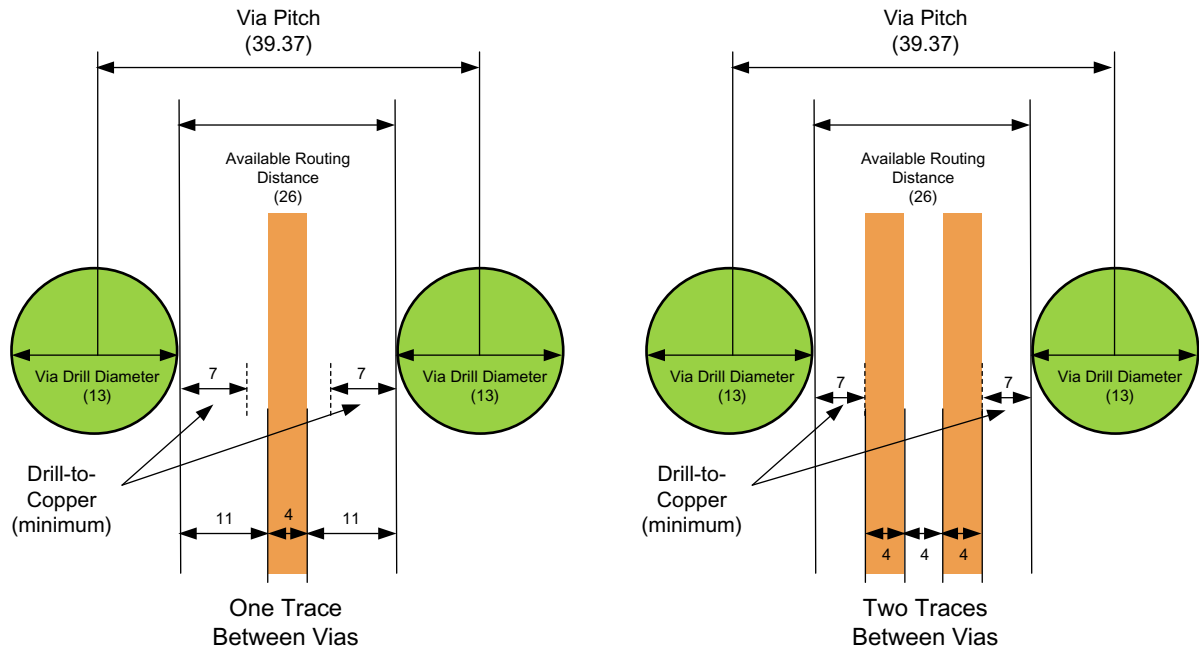


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Figure 3-8: Trace Routing Between BGA Balls for 1.0mm Pitch FF, FG, FH, FL, RB, and RF Devices (mils)

Trace Routing Between Vias

One or two traces can be routed between vias with varying spacing between traces, as shown in Figure 3-9 and Figure 3-10.



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Figure 3-9: Trace Routing Between Vias for 1.0mm Pitch Devices (mils)

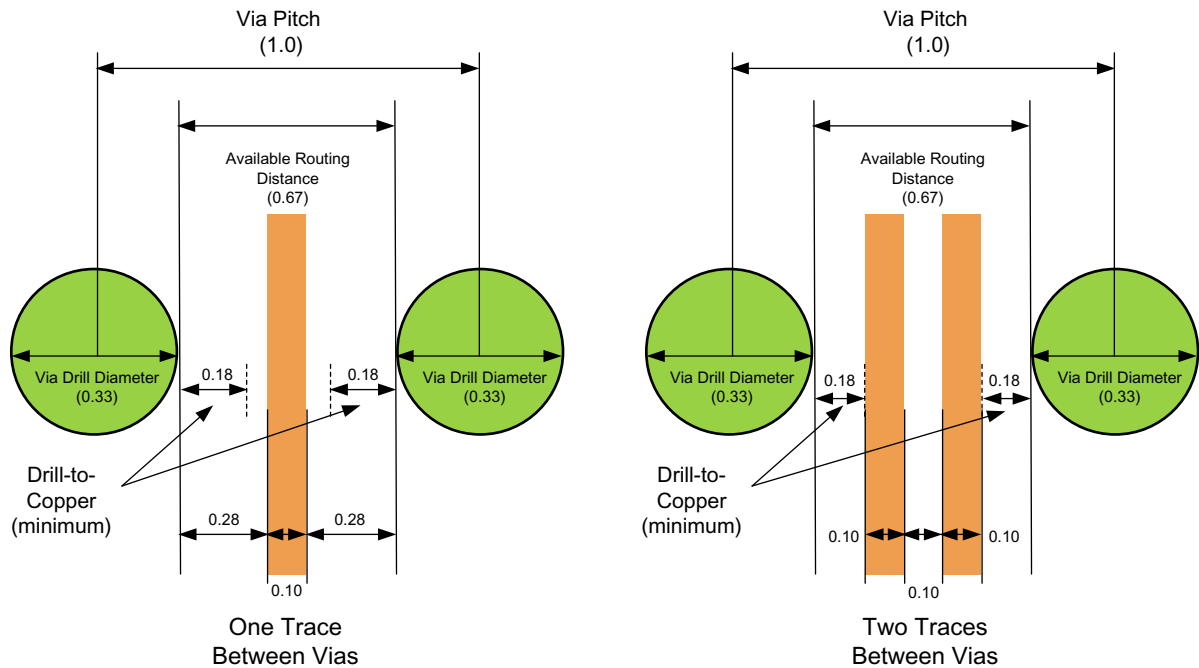


Figure 3-10: Trace Routing Between Vias for 1.0mm Pitch Devices (mils)

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Sample Breakouts using Standard and Advanced Processes

Figure 3-11 through Figure 3-15 show a representative 1.0 mm FFG900 breakout using the top PCB layer and four inner signal layers by means of a standard layout process which includes one signal route between BGA balls and vias.

Figure 3-16 through Figure 3-18 show a representative 1.0 mm FFG900 breakout using the top PCB signal layer and two inner signal layers by means of a more advanced process which includes two signal routes between BGA balls and vias.

Most power balls are located in the center region of the ball grid array, so signal routing takes place primarily on the outer edges.

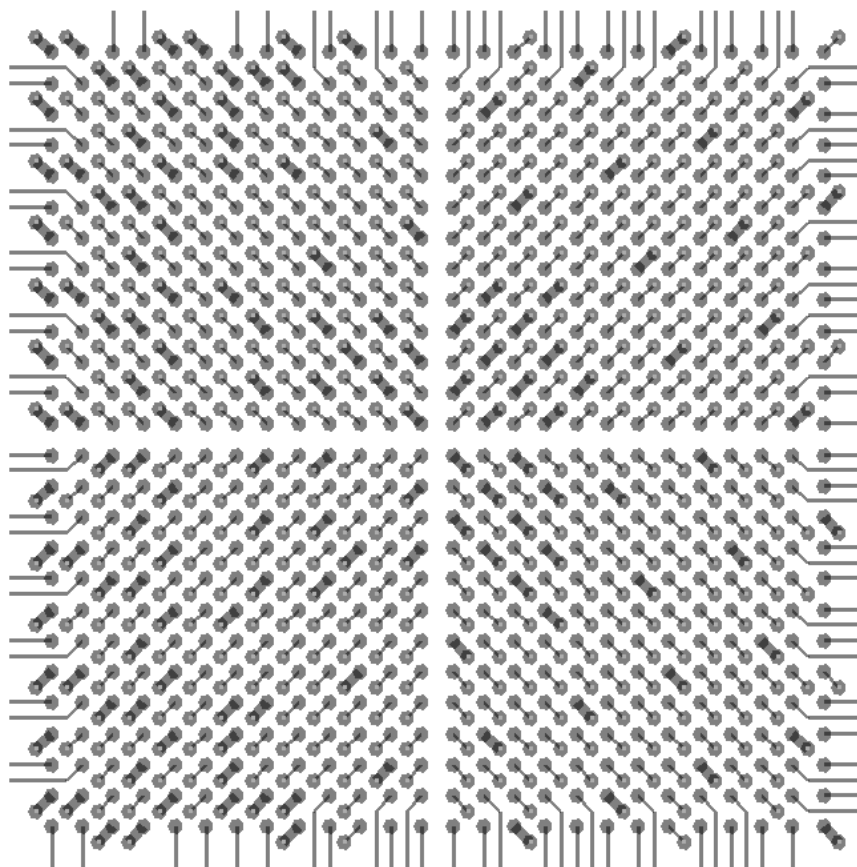


Figure 3-11: 1.0 mm Pitch FFG900 Breakout, Top Signal Layer 1, Standard PCB Process

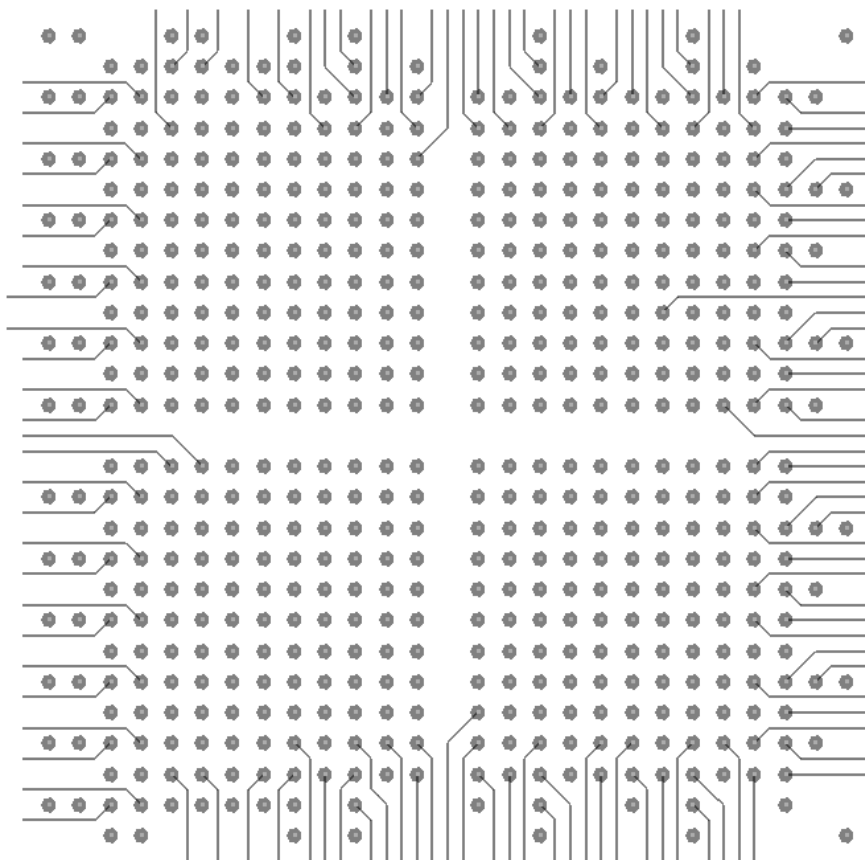


Figure 3-12: 1.0 mm Pitch FFG900 Breakout, Inner Signal Layer 2, Standard PCB Process

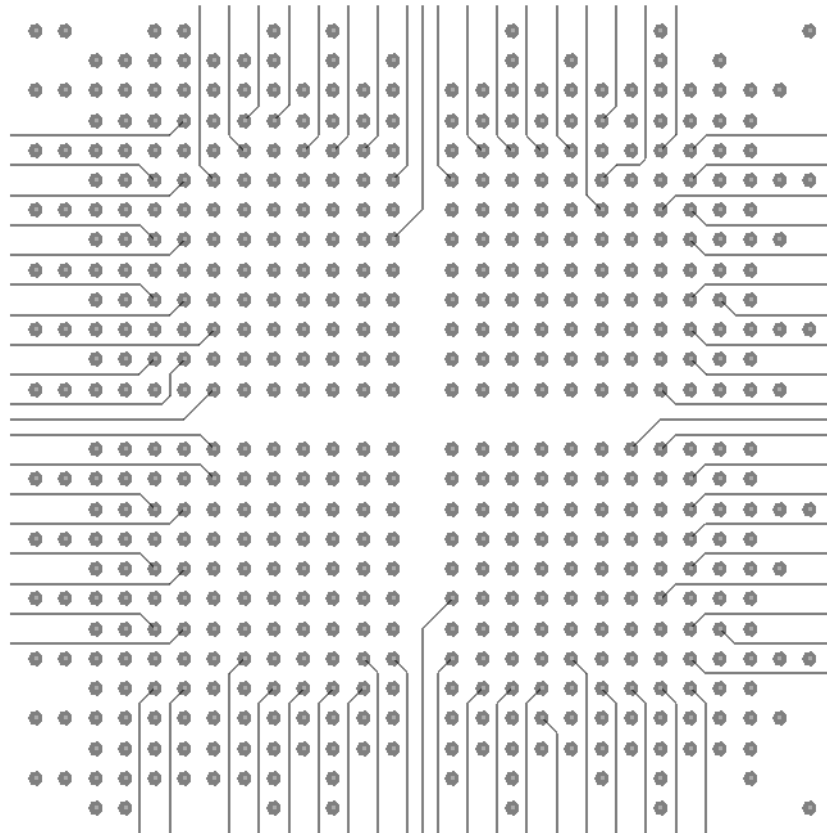


Figure 3-13: 1.0 mm Pitch FFG900 Breakout, Inner Signal Layer 3, Standard PCB Process

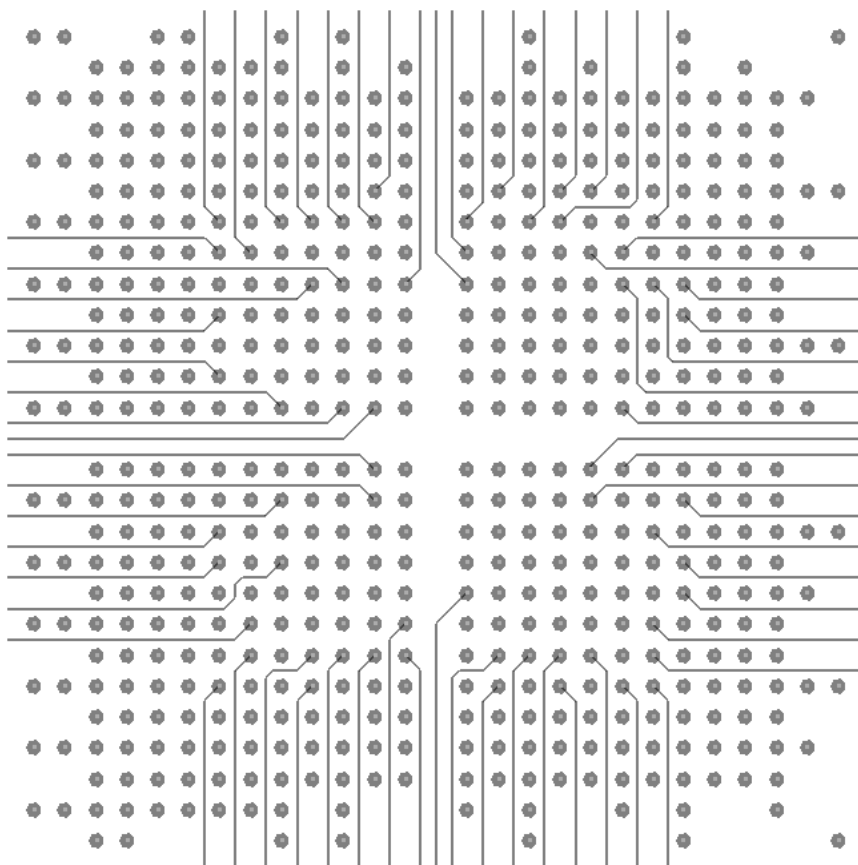


Figure 3-14: 1.0mm Pitch FFG900 Breakout, Inner Signal Layer 4, Standard PCB Process

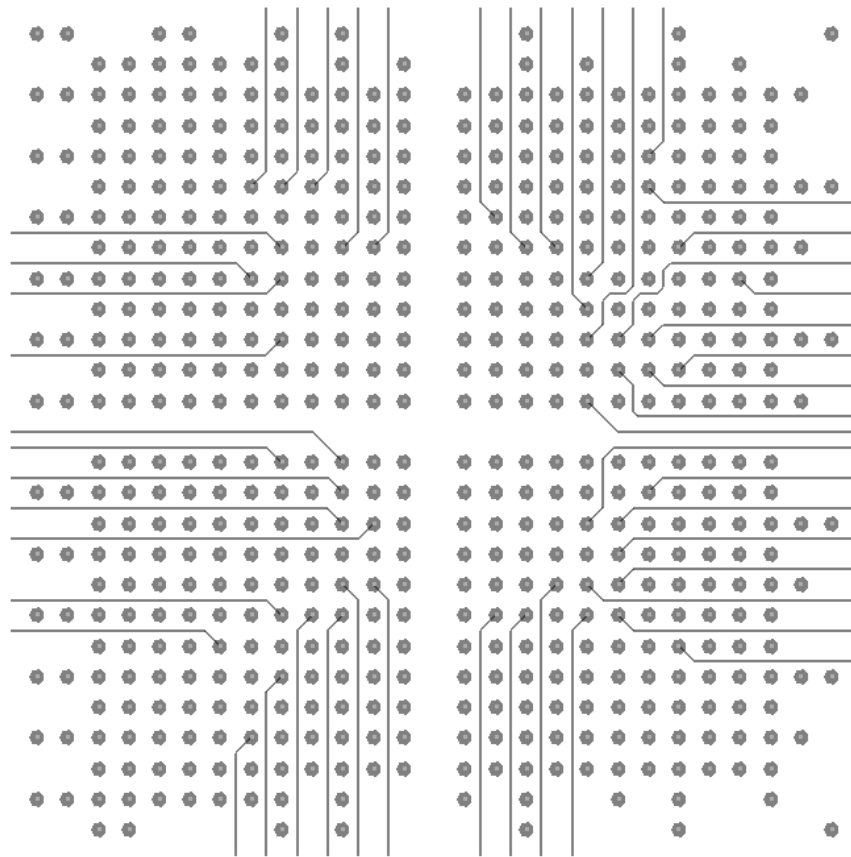


Figure 3-15: 1.0mm Pitch FFG900 Breakout, Inner Signal Layer 5, Standard PCB Process

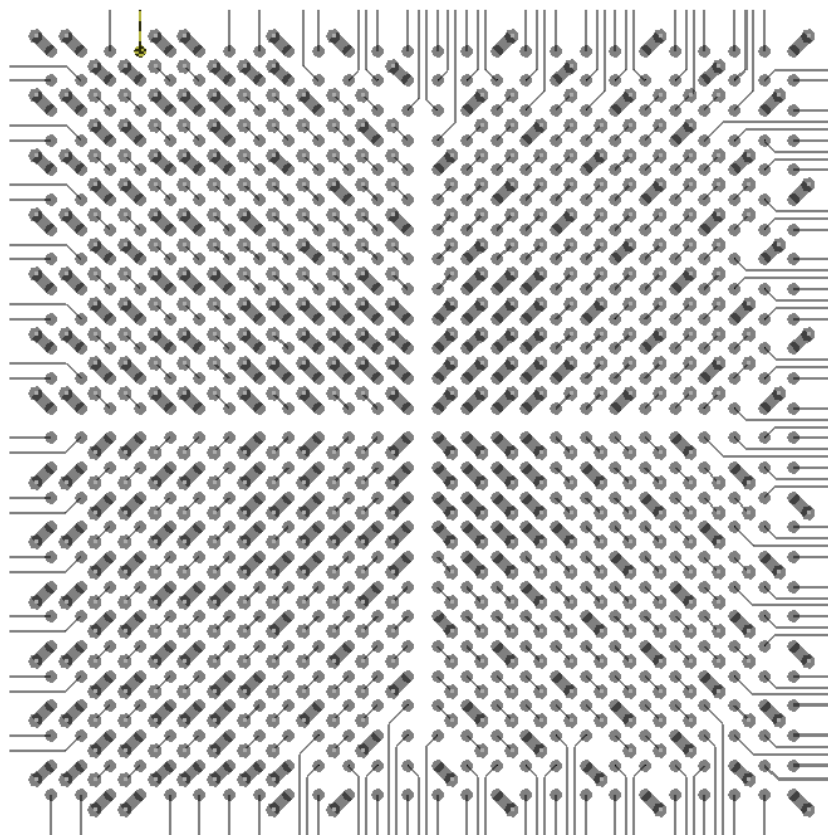


Figure 3-16: 1.0mm Pitch FFG900 Breakout, Top Signal Layer 1, Advanced PCB Process

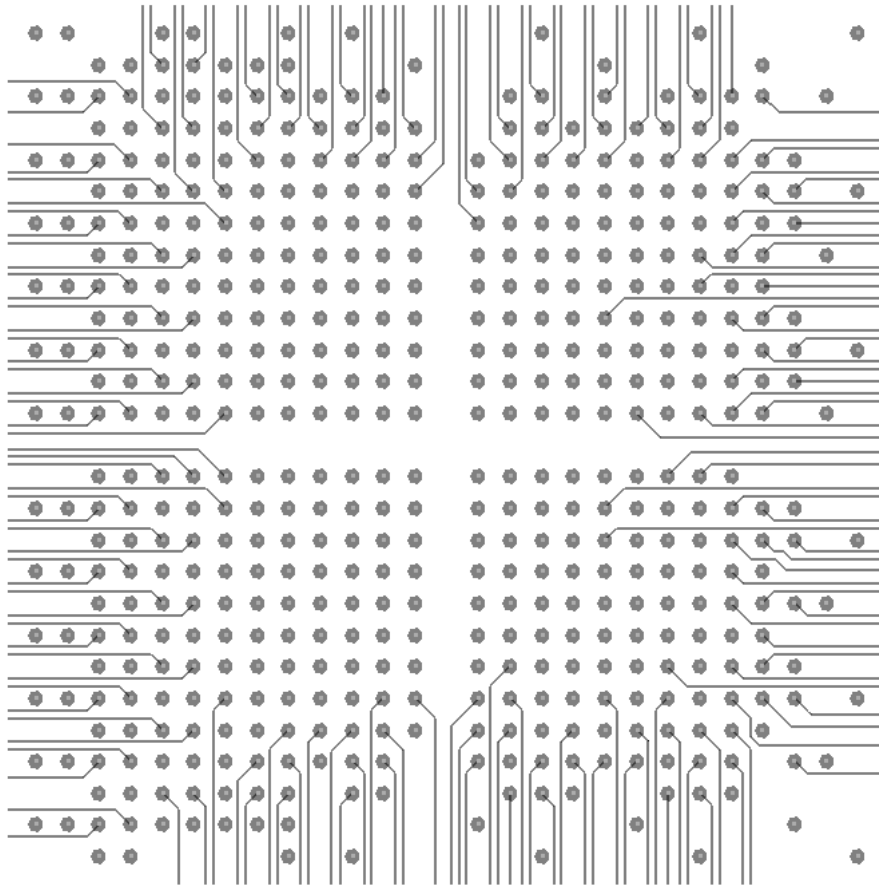


Figure 3-17: 1.0mm Pitch FFG900 Breakout, Inner Signal Layer 2, Advanced PCB Process

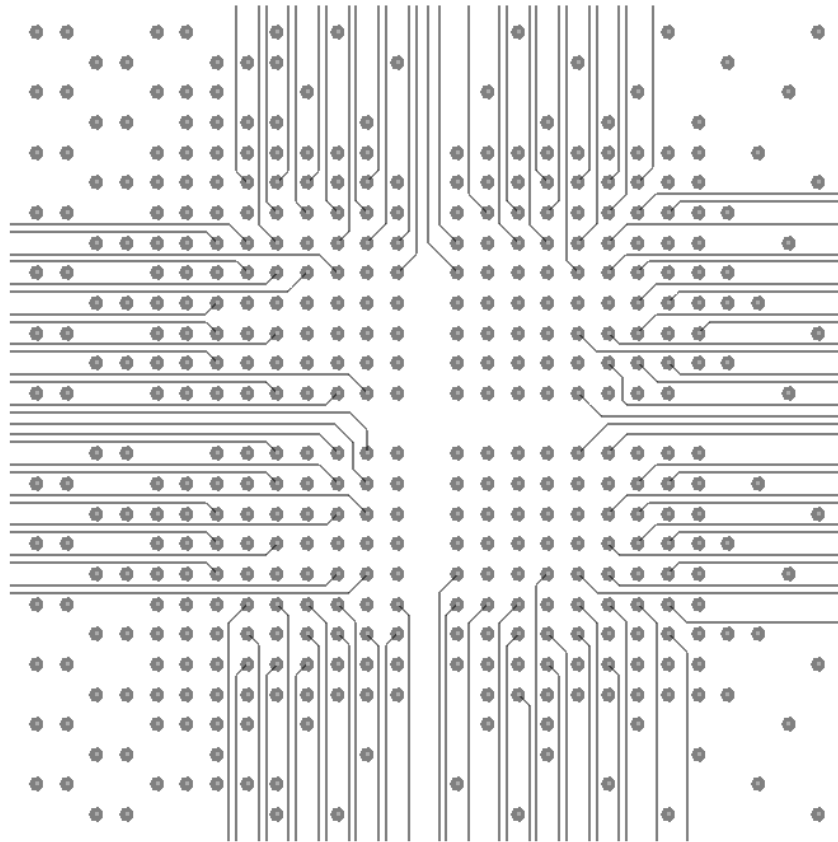
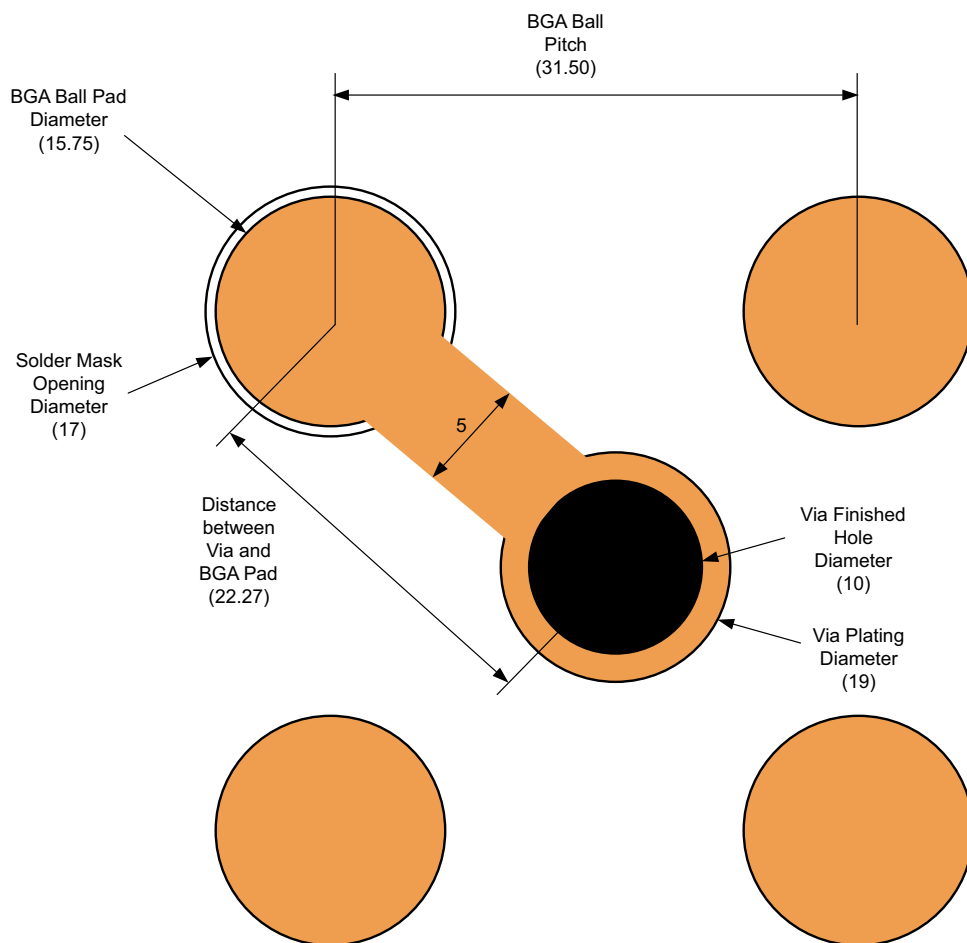


Figure 3-18: 1.0mm Pitch FFG900 Breakout, Inner Signal Layer 3, Advanced PCB Process

Recommended Layout Dimensions within BGA Area for 0.8 mm Pitch Devices

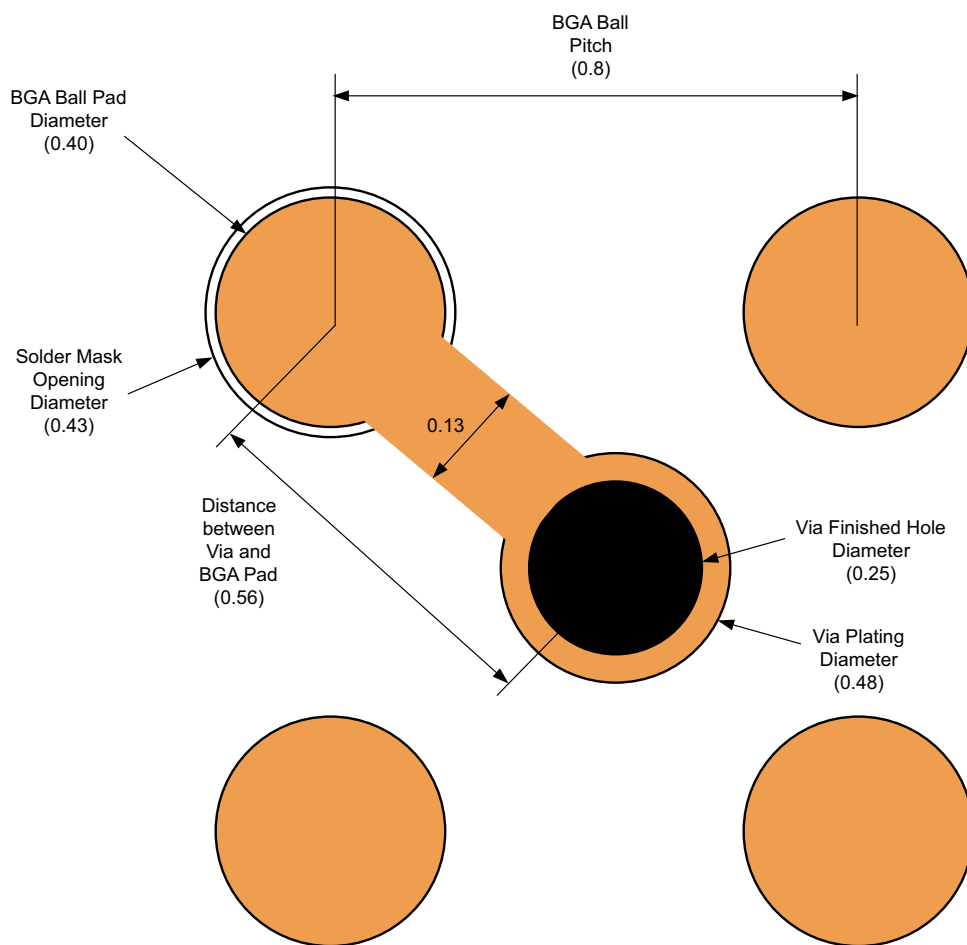
BGA Ball Pad and Via Dimensions

The amount of space available for routing under the FPGA is dependent on the area between the balls in the BGA area (for top and bottom layers), as well as the area between vias (for inner layers). The typical dimensions of FPGA ball pads and vias for 0.8 mm pitch devices are indicated in [Figure 4-1](#) and [Figure 4-2](#).



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Figure 4-1: Ball and Via Dimensions for 0.8 mm Pitch CS, RS, SB, and SF Devices (mils)



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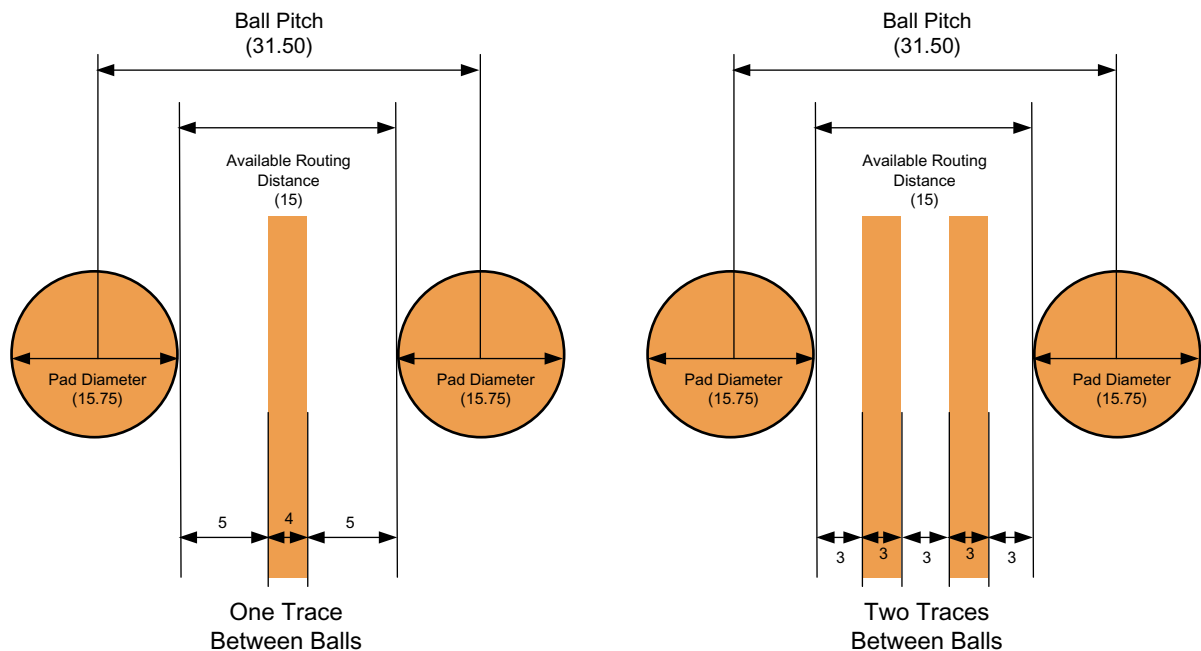
Figure 4-2: Ball and Via Dimensions for 0.8 mm Pitch CS, RS, SB, and SF Devices (mm)

Trace Widths Dimensions inside BGA Area

The ball pitch and BGA pad/via diameters determine how much space is available to route traces between pads or vias. Standard PCB processes can allow for as low as 3.5 mil trace widths with 3.5 mil spacing. Advanced processes can allow for as low as 2 mil trace widths with 2 mil spacing.

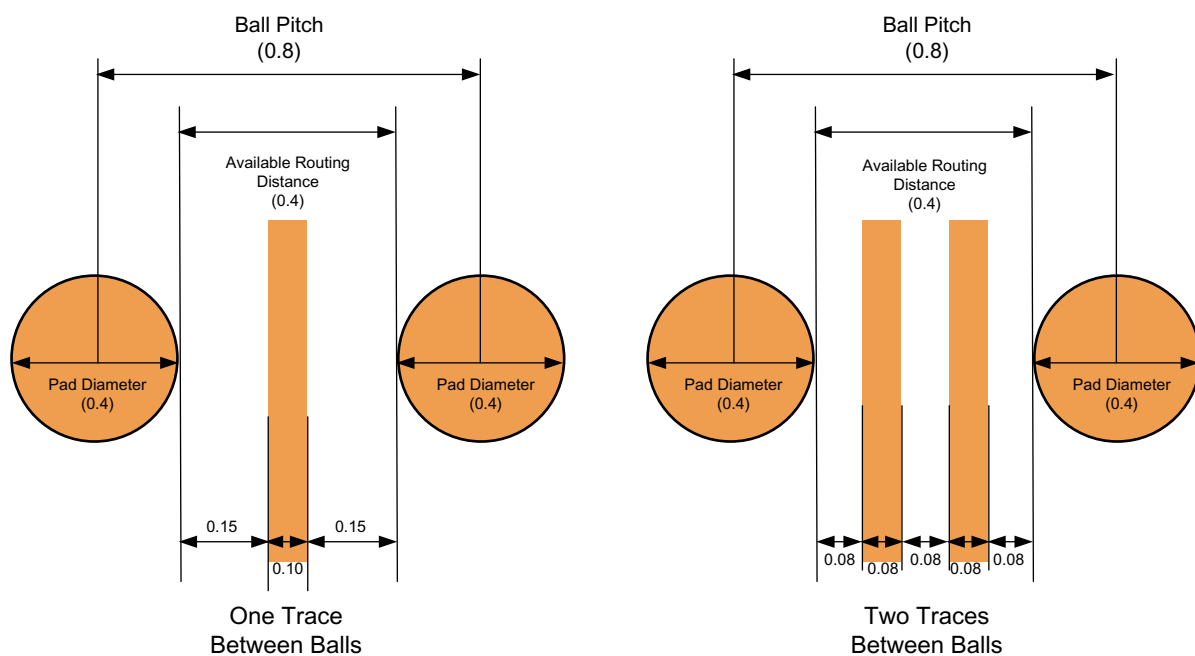
Trace Routing Between BGA Balls

One or two traces can be routed between BGA balls with varying spacing between traces, as shown in Figure 4-3 and Figure 4-4.



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Figure 4-3: Trace Routing Between BGA Balls for 0.8 mm Pitch CS, RB, SB, and SF Devices (mils)

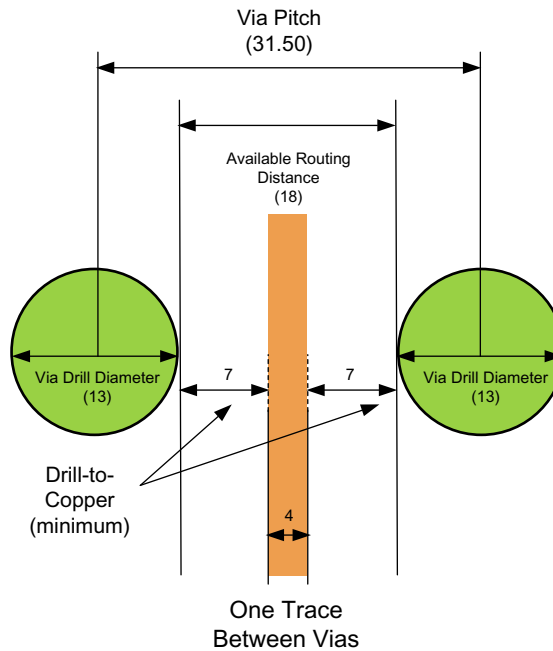


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Figure 4-4: Trace Routing Between BGA Balls for 0.8 mm Pitch CS, RB, SB, and SF Devices (mm)

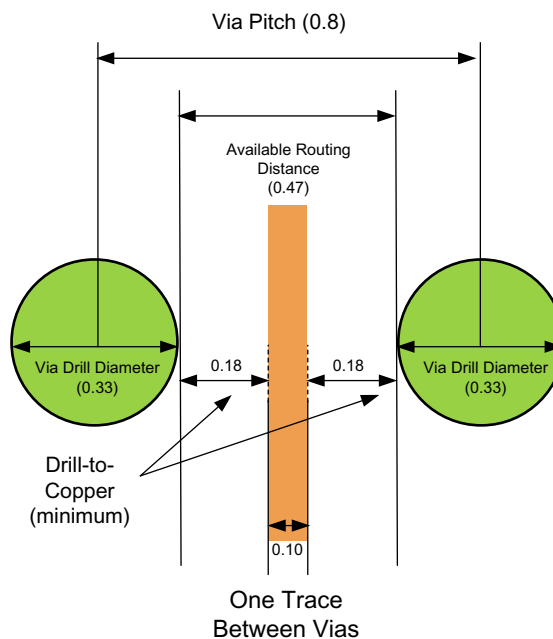
Trace Routing Between Vias

For 0.8 mm pitch devices, only one trace can be routed between vias due to drill-to-copper specifications, as shown in Figure 4-5 and Figure 4-6.



X15739-011116

Figure 4-5: Trace Routing Between Vias for 0.8 mm Pitch Devices (mils)



X15740-011116

Figure 4-6: Trace Routing Between Vias for 0.8 mm Pitch Devices (mm)

Sample Breakouts using Standard and Advanced PCB Processes

Figure 4-7 through Figure 4-10 show a representative 0.8 mm CSG484 breakout using the top PCB layer and three inner signal layers by means of a standard layout process which includes one signal route between BGA balls and vias.

Figure 4-11 through Figure 4-13 show a representative 0.8 mm CSG484 breakout using the top PCB signal layer and two inner signal layers by means of a more advanced process which includes two signal routes between BGA balls and one signal route between vias. Design rules do not allow for two routes between vias for 0.8 mm devices.

Many power balls are located in the center region of the ball grid array, so signal routing takes place primarily on the outer edges.

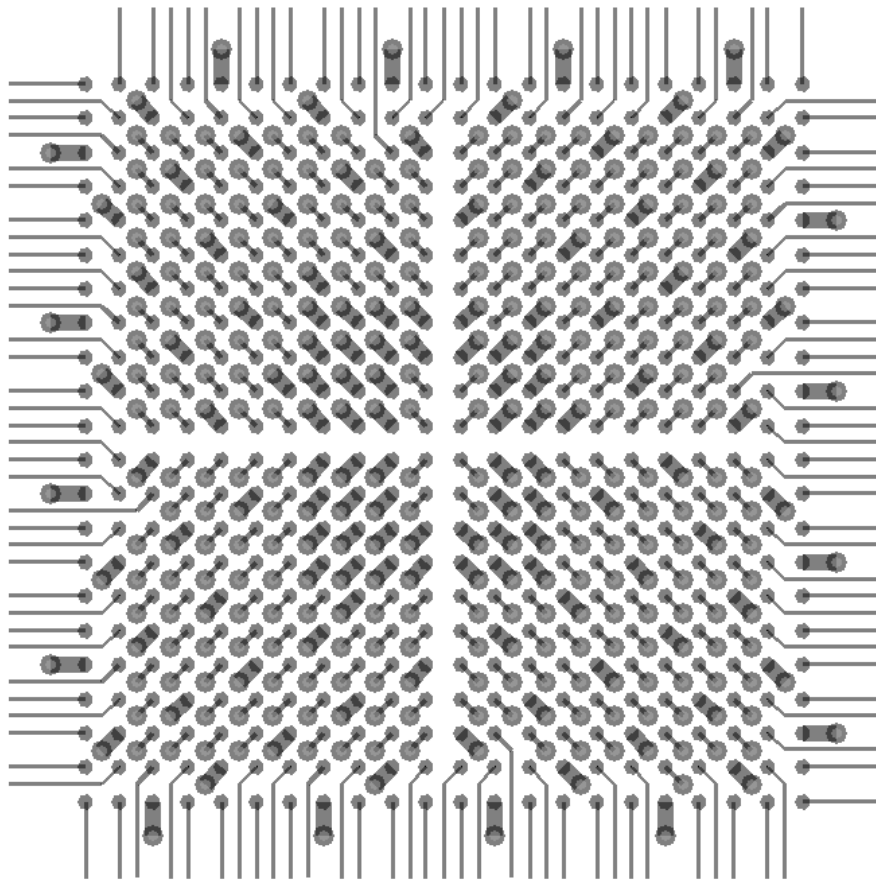


Figure 4-7: 0.8 mm Pitch CSG484 Breakout, Top Signal Layer 1, Standard PCB Process

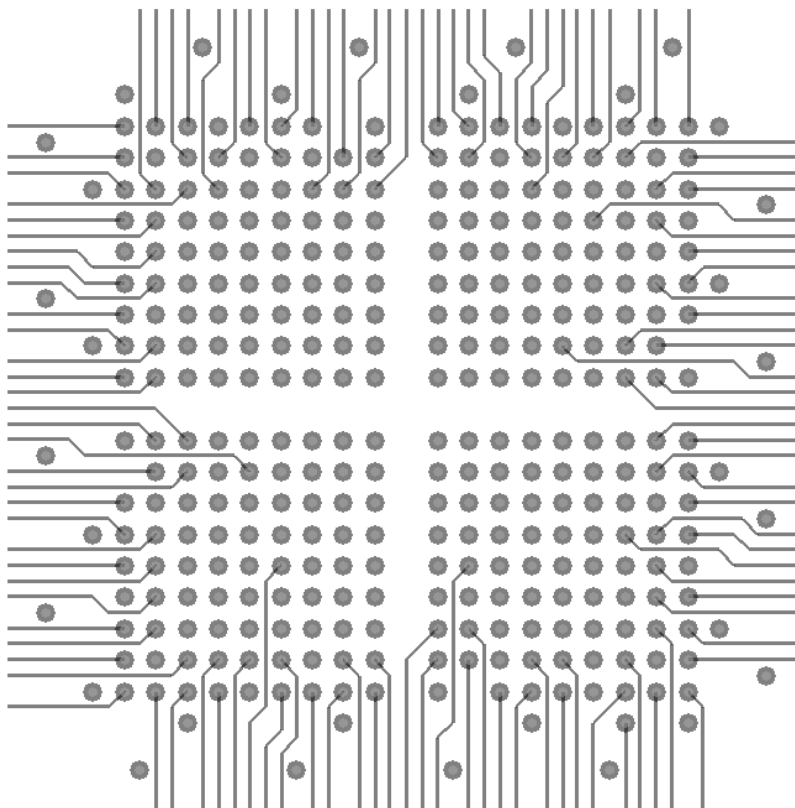


Figure 4-8: 0.8 mm Pitch CSG484 Breakout, Inner Signal Layer 2, Standard PCB Process

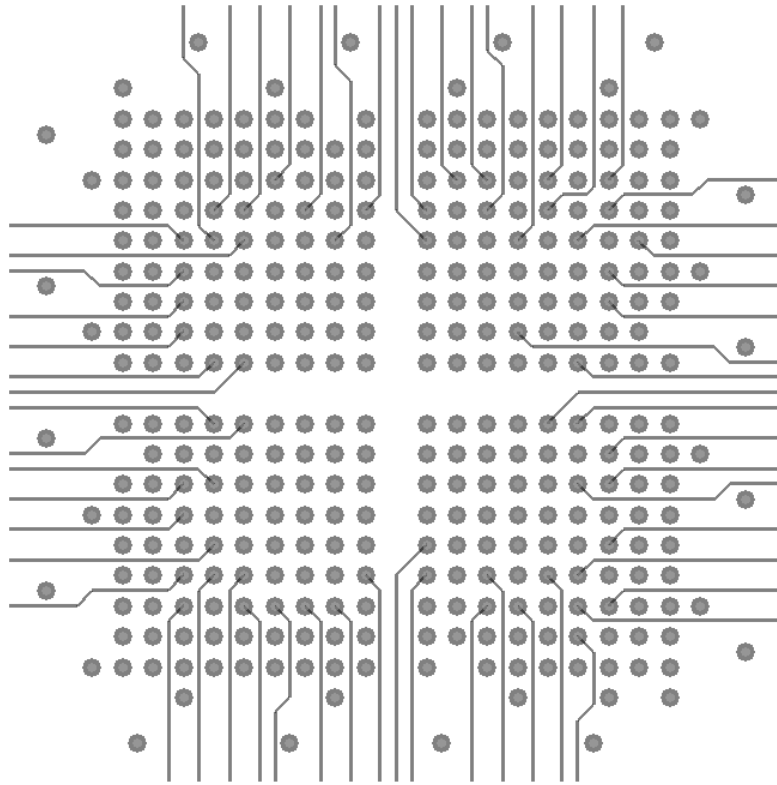


Figure 4-9: 0.8 mm Pitch CSG484 Breakout, Inner Signal Layer 3, Standard PCB Process

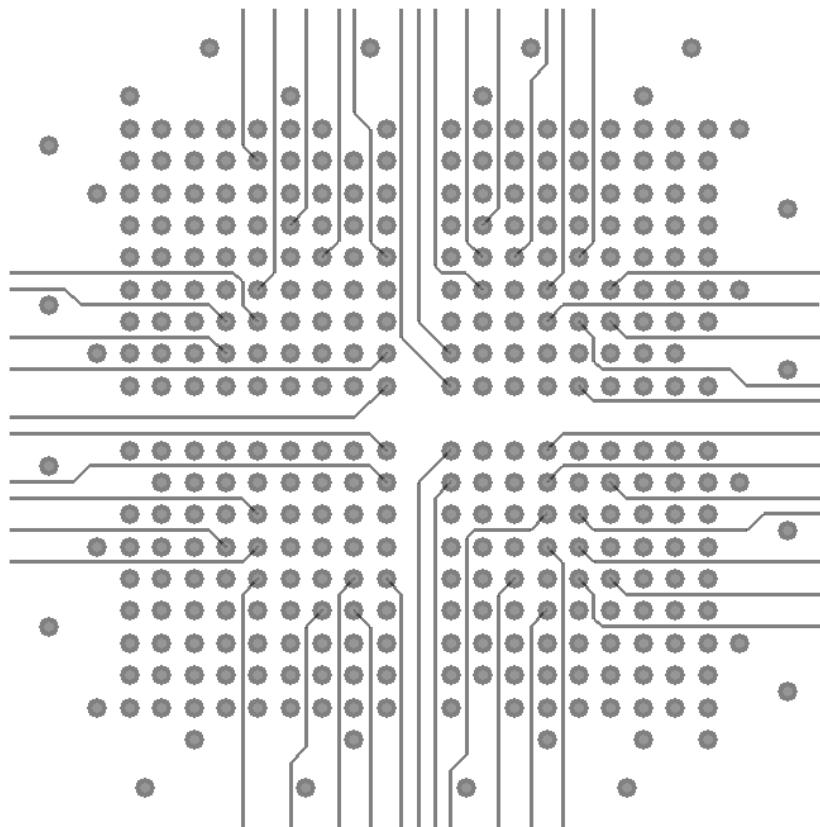


Figure 4-10: 0.8 mm Pitch CSG484 Breakout, Inner Signal Layer 4, Standard PCB Process

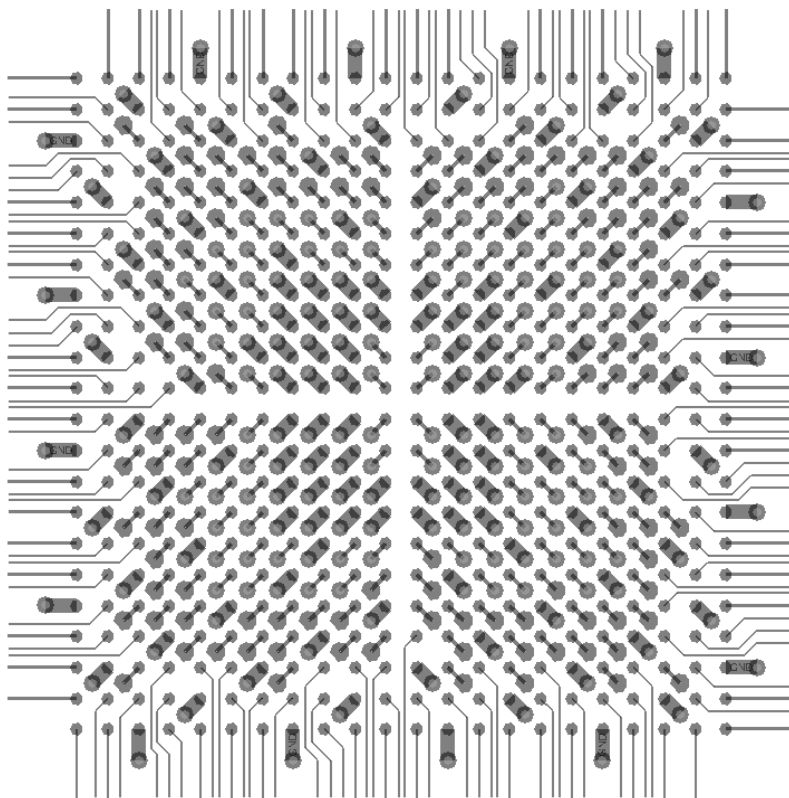


Figure 4-11: 0.8 mm Pitch CSG484 Breakout, Top Signal Layer 1, Advanced PCB Process

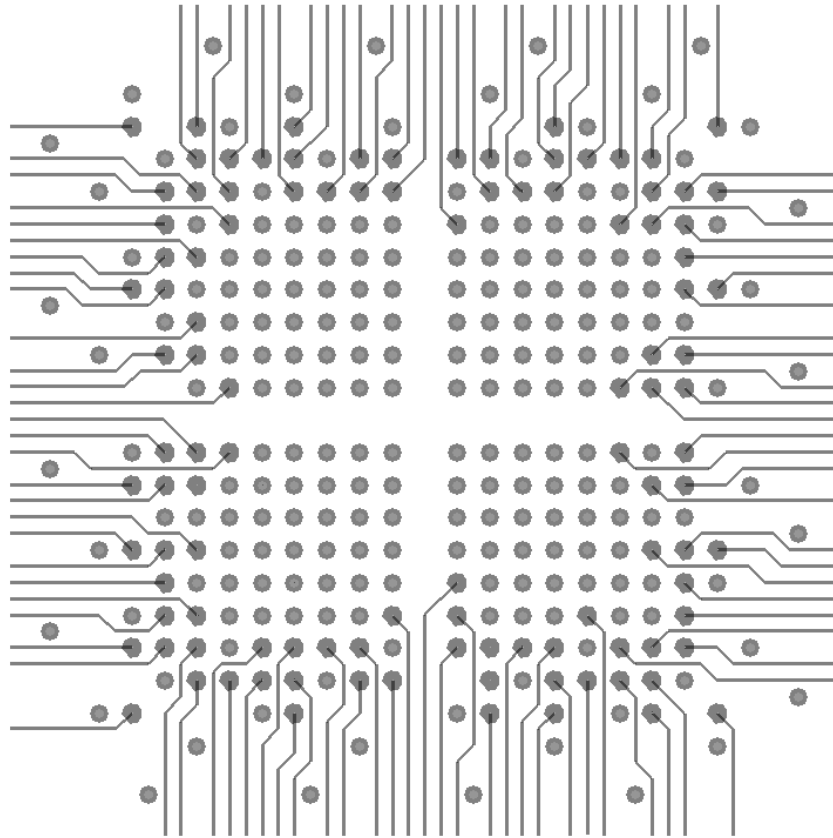


Figure 4-12: 0.8 mm Pitch CSG484 Breakout, Inner Signal Layer 2, Advanced PCB Process

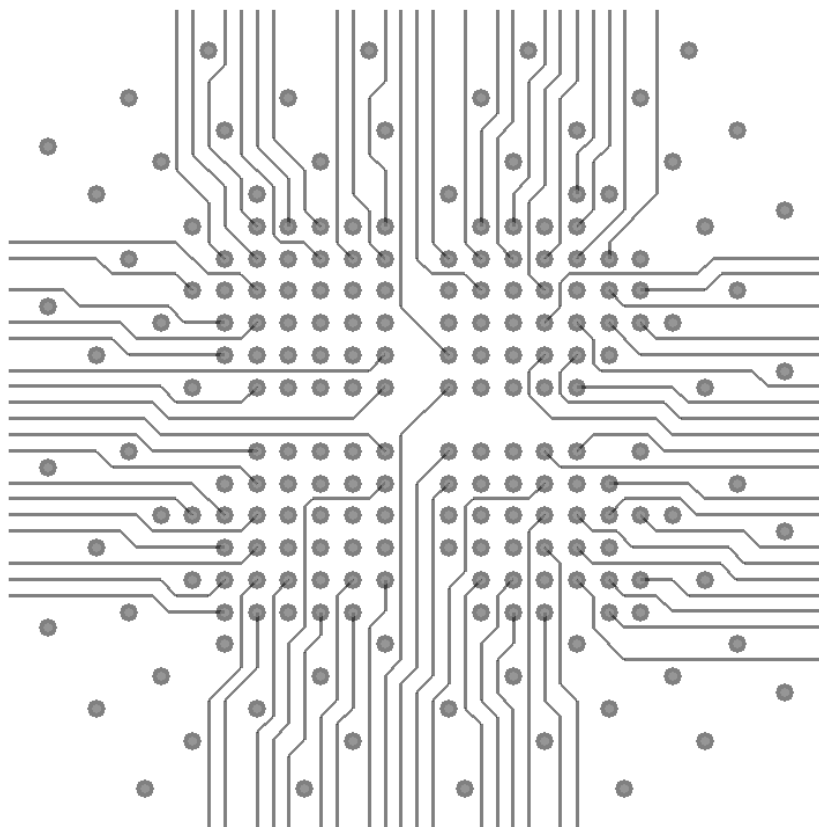
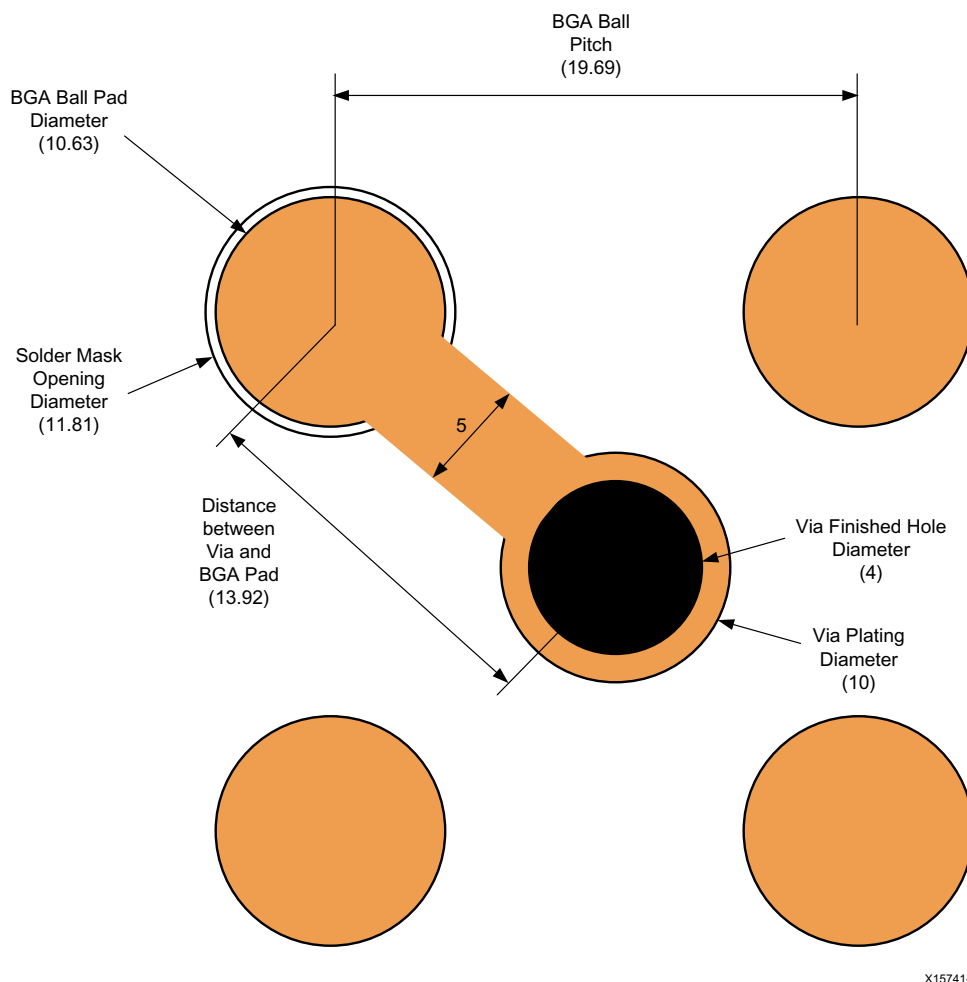


Figure 4-13: 0.8mm Pitch CSG484 Breakout, Inner Signal Layer 3, Advanced PCB Process

Recommended Layout Dimensions within BGA Area for 0.5 mm Pitch Devices

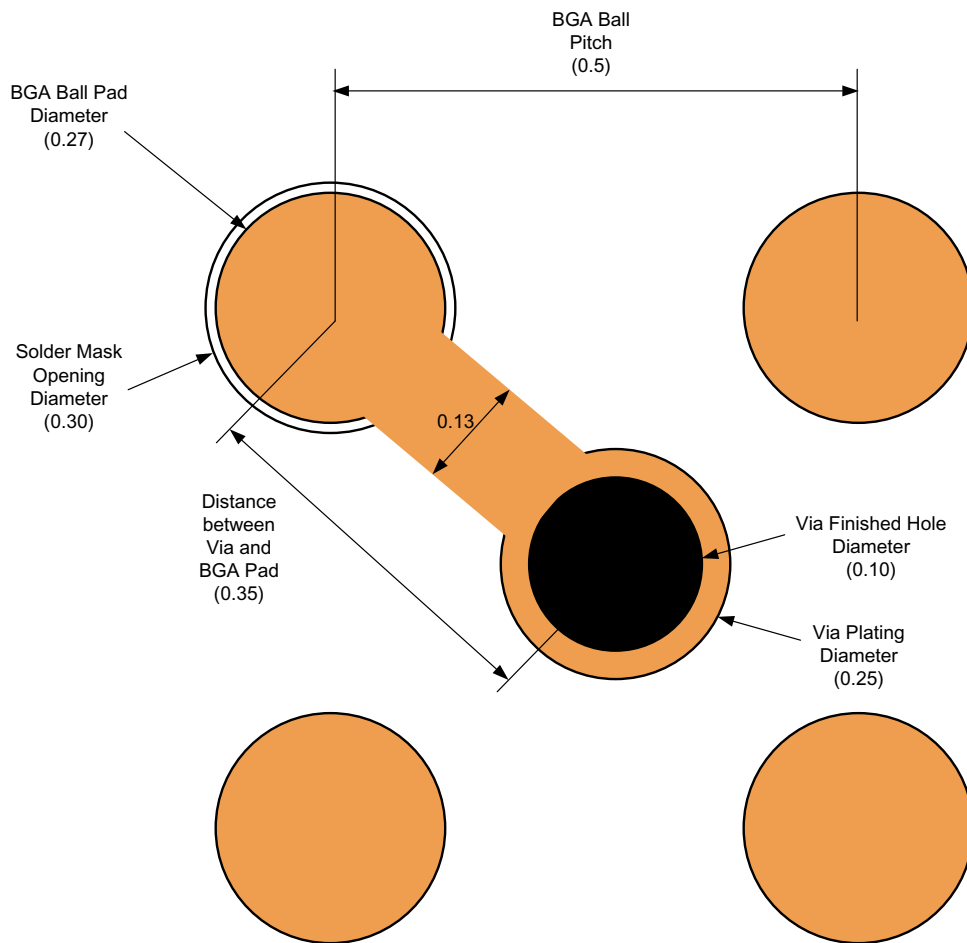
BGA Ball Pad and Via Dimensions

The amount of space available for routing under the FPGA is dependent on the area between the balls in the BGA area (for top and bottom layers), as well as the area between vias (for inner layers). The typical dimensions of FPGA ball pads and vias for 0.5 mm pitch devices are indicated in [Figure 5-1](#) and [Figure 5-2](#).



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Figure 5-1: Ball and Via Dimensions for 0.5 mm Pitch CP Devices (mils)



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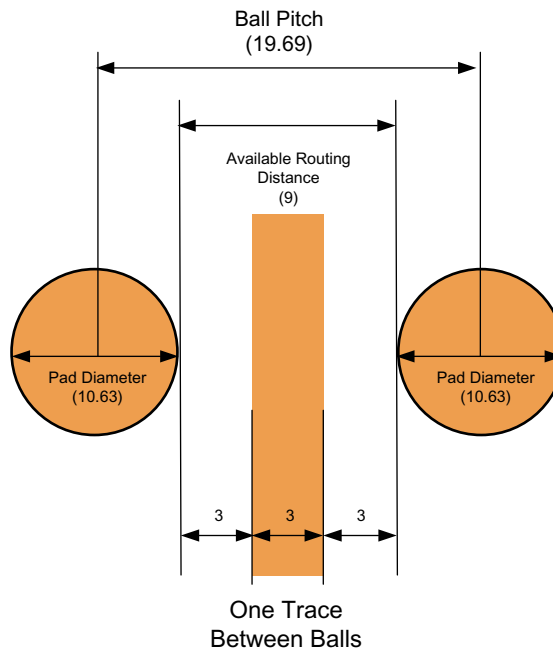
Figure 5-2: Ball and Via Dimensions for 0.5 mm Pitch CP Devices (mm)

Trace Widths Dimensions inside BGA Area

The ball pitch and BGA pad/via diameters determine how much space is available to route traces between pads or vias. Standard PCB processes can allow for as low as 3.5 mil trace widths with 3.5 mil spacing. Advanced processes can allow for as low as 2 mil trace widths with 2 mil spacing.

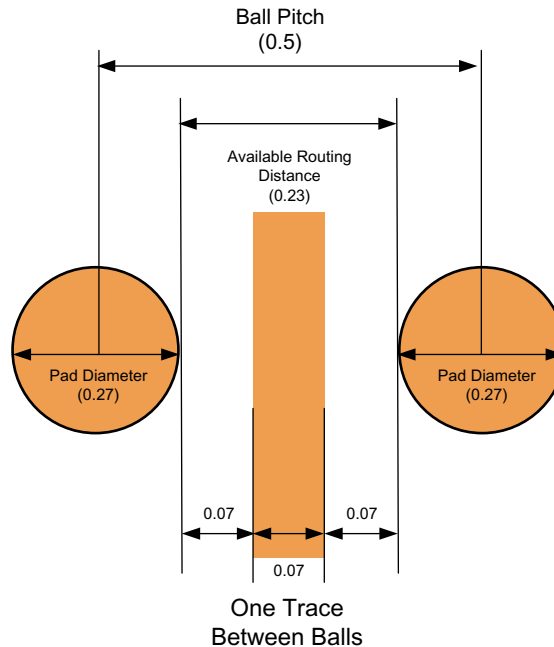
Trace Routing Between BGA Balls

Due to the very fine pitch of 0.5 mm devices, only one signal can be routed in between BGA balls, as shown in Figure 5-3 and Figure 5-4.



X15743-011116

Figure 5-3: Trace Routing Between BGA Balls for 0.5 mm Pitch CP Devices (mil)



X15744-011116

Figure 5-4: Trace Routing Between BGA Balls for 0.5 mm Pitch CP Devices (mm)

Trace Routing Between Vias

Due to the very fine pitch of 0.5 mm devices, routing traces between vias is not practical or even possible using even advanced fabrication processes. Micro-vias under the BGA pads are recommended to be used to reach a lower routing layer, at which point the signal will be out of the BGA field and standard trace routing can be utilized.

Sample Breakout Using Advanced Process

Figure 5-5 and Figure 5-6 show a representative 0.5 mm CPG236 breakout using the top PCB layer and one inner signal layer by means of an advanced layout process which includes one signal route between BGA balls and vias. Design rules do not allow for two routes between pads or vias.

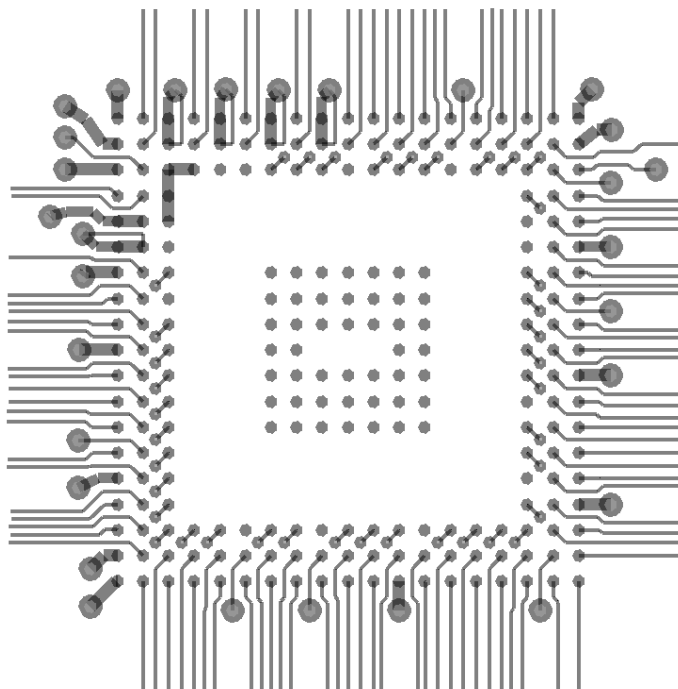


Figure 5-5: 0.5 mm Pitch CPG236 Breakout, Top Signal Layer 1, Advanced PCB Process

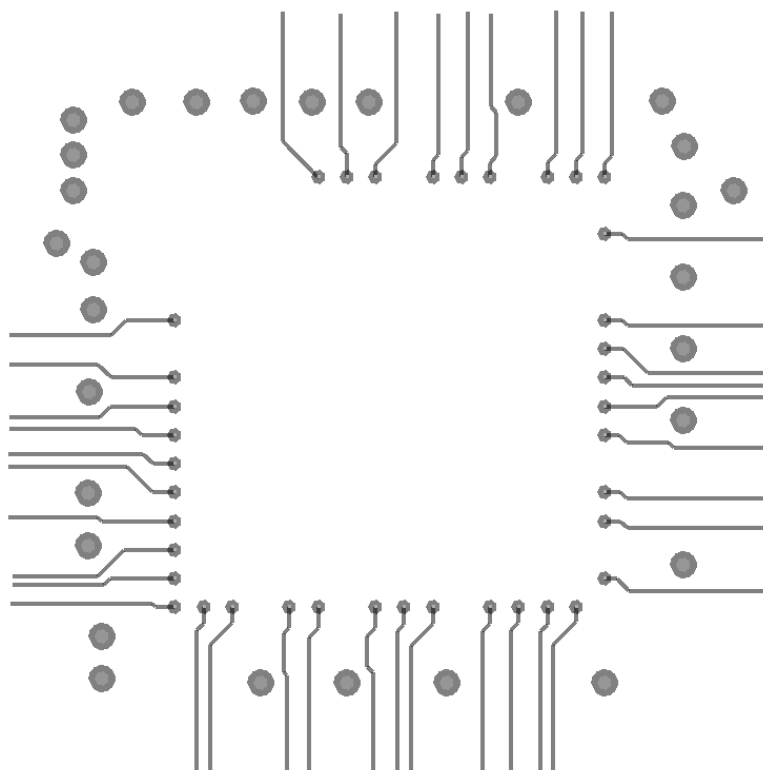
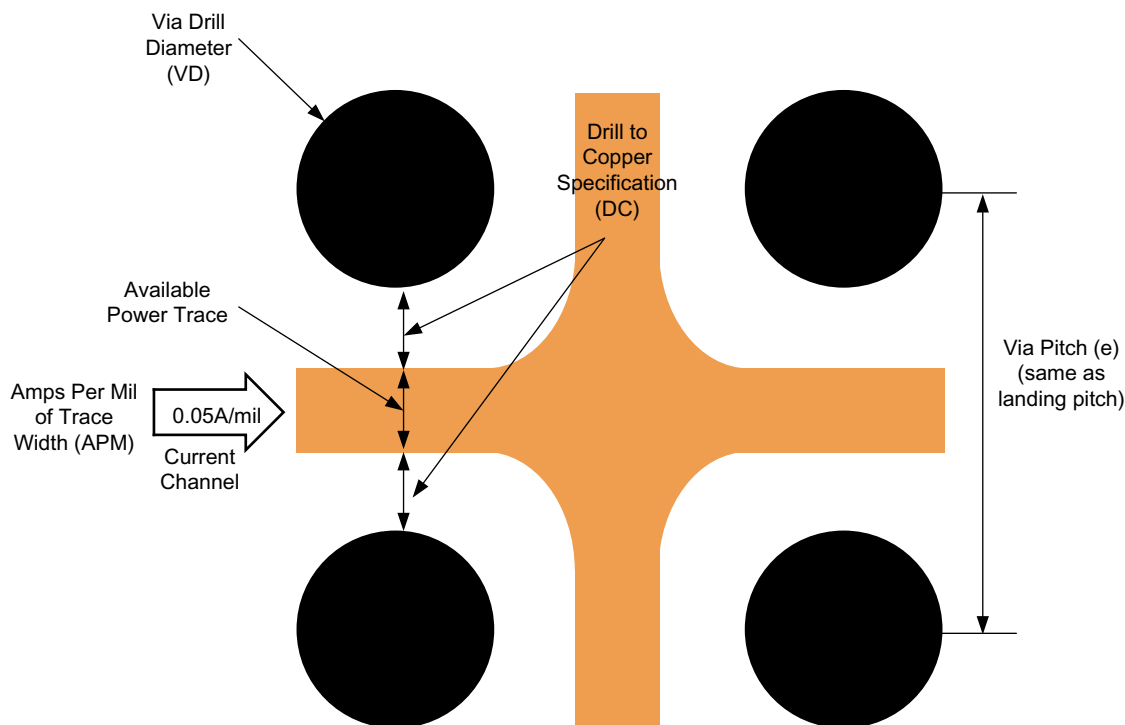


Figure 5-6: 0.5 mm Pitch CPG236 Breakout, Inner Signal Layer 2, Advanced PCB Process

Power Delivery to the FPGA

Power needs must be assessed early in the design phase to assure that there are enough layers and area to provide sufficient power to the BGA balls that require power. Because most of the BGA power pins are located in the center of the BGA area, the path the current travels traverses a myriad of vias in the BGA area. The space between vias can conservatively carry about 0.05A per mil of trace width (for 0.5 oz copper). The trace width between vias is defined by the pitch of the vias (usually the same as the pitch of the BGA), the via drill diameter, and drill-to-copper specification as defined by the fabrication house.

Figure 6-1 shows how to calculate the amount of current that can pass through each via channel. Ensure that the power planes are wide enough and encompassing enough to supply the needed amperage to the BGA power balls. Equation 6-1 can be used to calculate the current per channel. Table 6-1 and Table 6-2 show current per channel values for 0.8 mm and 1.0 mm pitch devices. Because of the very fine pitch of 0.5 mm devices, it is not possible to route in-between standard vias. Micro-vias under the BGA pads are recommended for 0.5 mm devices in order to reach the power planes.



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Figure 6-1: Power Delivery Within BGA Area (0.5 oz Copper)

Current Per Channel

Equation 6-1

$$= (\text{ViaPitch} - \text{ViaDrillDiameter} - 2 \times \text{DrillToCopperSpecification}) \times \text{AmpsPerUnitTraceWidth}$$

Table 6-1: Current Per Channel Calculation for 0.8 and 1.0 mm Devices (mils)

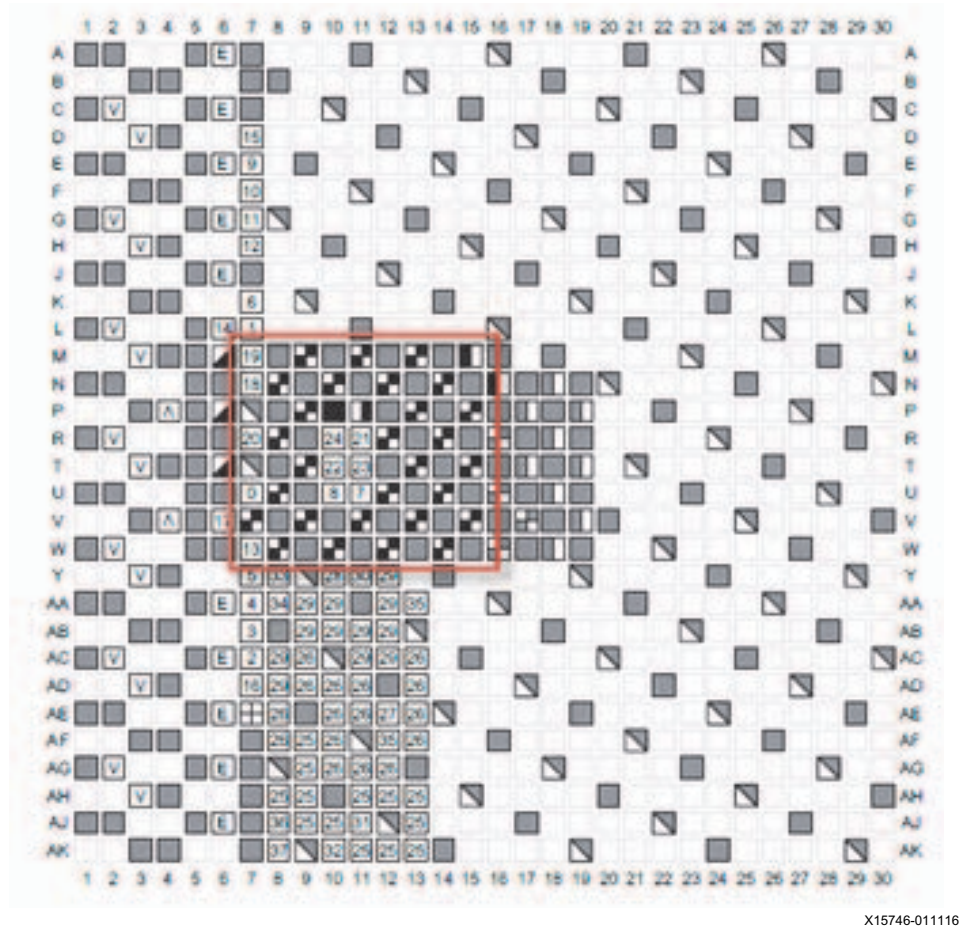
	0.8 mm Pitch	1.0 mm Pitch
Via Pitch (e)	31.50	39.37
Via Drill Diameter (VD)	13	13
Drill to Copper Specification (DC)	7	7
Amps per Unit Trace Width (ATW), 0.5 oz Cu	0.05	0.05
Amps per Unit Trace Width (ATW), 1.0 oz Cu	0.075	0.075
Current per Channel, 0.5 oz Cu	0.23A	0.61A
Current per Channel, 1.0 oz Cu	0.34A	0.93A

Table 6-2: Current Per Channel Calculation for 0.8 and 1.0mm Devices (mm)

	0.8 mm Pitch	1.0 mm Pitch
Via Pitch (e)	0.8	1.0
Via Drill Diameter (VD)	0.33	0.33
Drill to Copper Specification (DC)	0.18	0.18
Amps per Unit Trace Width (ATW), 0.5 oz Cu	1.97	1.97
Amps per Unit Trace Width (ATW), 1.0 oz Cu	2.95	2.95
Current per Channel, 0.5 oz Cu	0.23A	0.61A
Current per Channel, 1.0 oz Cu	0.34A	0.93A

Power Delivery Example: V_{CCINT} and XCKU040-FBVA900

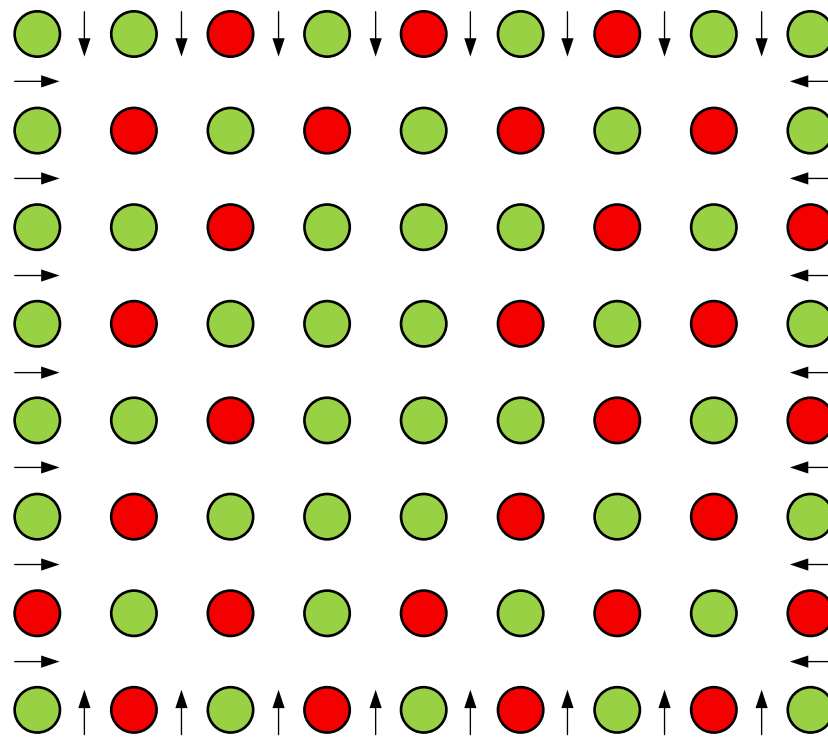
The XCKU040-FBVA900 device utilizes a 900-pin BGA package with 1.0 mm pitch between solder balls. The V_{CCINT} power pins are located in the center area of the BGA, as shown in Figure 6-2.



■ Indicates V_{CCINT} Power Pins

Figure 6-2: V_{CCINT} Ball Area in XCKU040-FBVA900 Device

All of the V_{CCINT} power must be delivered through an approximate grid of approximately 9x8 vias, as shown in Figure 6-2 (V_{CCINT} vias are shown in red).



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Figure 6-3: V_{CCINT} Via Array for XCKU040-FBVA900 Device (V_{CCINT} vias are shown in red)

There are thirty via channels that surround the 9x8 array in Figure 6-3, and all of the power for V_{CCINT} must be delivered through these openings. According Equation 6-1, the FB package can deliver 0.6A between each via channel for 0.5oz copper. Thirty via channels @0.6A per channel equates to a capability of 18A. If more current is needed than this, then either another power layer can be added for V_{CCINT} , or thicker copper can be used, supplying up to 27A for 1.0 oz copper in this example.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

Solution Centers

See the [Xilinx Solution Centers](#) for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

1. *UltraScale Architecture PCB Design User Guide* ([UG583](#))
 2. *Zynq-7000 All Programmable SoC PCB Design User Guide* ([UG933](#))
 3. *7 Series FPGAs PCB Design User Guide* ([UG483](#))
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