1 Introduction

The OSD3358 package is a 20 x 20 BGA that is a super-set of the Texas Instruments (TI) AM3358 ZCZ 18 x 18 BGA package. Most of the signals on the OSD3358 are assigned to the same pins as the AM3358. This document lists the differences between the signal locations of the two devices.

2 Revision History

Revision Number	Revision Date	Changes	Author
1	5/2/2016	Initial Revision	KT

3 Signal Differences

The OSD3358 internal power distribution network affects the use of the pins that are in the same locations as input power pins on the AM3358. The internal PMIC supplies output power to those pins with current limitations shown in the datasheet. Since the memory interface is internal to the OSD3358, none of the DDR signals are present externally. The oscillator inputs and outputs on the AM3358 have been moved to the additional rows and columns of the OSD3358. Table 1 lists the signal differences.

Table 1. Signal Differences

Pin	AM3358 Signal	AM3358 Application	OSD3358 Signal	OSD3358 Application
N16	VDDA1P8V_USB0	Power In	SYS_VDD_1P8V	Power Out
R16	VDDA1P8V_USB1	Power In	SYS_VDD_1P8V	Power Out
N15	VDDA3P3V_USB0	Power In	VDDSHV_3P3V	Monitoring
R15	VDDA3P3V_USB1	Power In	VDDSHV_3P3V	Monitoring
D8	VDDA_ADC	Power In	SYS_ADC_1P8V	Power Out
E6, E14, F9, K13, N6, P9, P14	VDDS	Power In	SYS_RTC_1P8V	Power Out
P7, P8	VDDSHV1	Power In	VDDSHV_3P3V	Monitoring
P10, P11	VDDSHV2	Power In	VDDSHV_3P3V	Monitoring
P12, P13	VDDSHV3	Power In	VDDSHV_3P3V	Monitoring
H14, J14	VDDSHV4	Power In	VDDSHV_3P3V	Monitoring
K14, L14	VDDSHV5	Power In	VDDSHV_3P3V	Monitoring
E10, E11, E12, E13, F14, G14, N5, P5, P6	VDDSHV6	Power In	VDDSHV_3P3V	Monitoring

OSD3358 Pin Assignment and Application Differences from Texas Instruments AM3358

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E5, F5, G5, H5, J5, K5, L5	VDDS_DDR	Power In	VDDS_DDR	Monitoring
R11	VDDS_OSC	Power In	VDDS_PLL	Monitoring
R10	VDDS_PLL_CORE_LCD	Power In	VDDS_PLL	Monitoring
E7	VDDS_PLL_DDR	Power In	VDDS_PLL	Monitoring
H15	VDDS_PLL_MPU	Power In	VDDS_PLL	Monitoring
D7	VDDS_RTC	Power In	SYS_RTC_1P8V	Power Out
E9	VDDS_SRAM_CORE_BG	Power In	SYS_VDD_1P8V	Power Out
D10	VDDS_SRAM_MPU_BB	Power In	SYS_VDD_1P8V	Power Out
F6, F7, G6, G7, G10, H11, J12, K6, K8, K12, L6, L7, L8, L9, M11, M13, N8, N9, N12, N13	VDD_CORE	Power In	VDD_CORE	Monitoring
F10, F11, F12, F13, G13, H13, J13	VDD_MPU	Power In	VDD_MPU	Monitoring
A9	VREFN	Voltage Reference	VSSA_ADC	Analog Ground
M14, N14	VSSA_USB	USB Ground	VSS	Digital Ground
V11	VSS_OSC	Oscillator Ground	No Connect	No Connect
A5	VSS_RTC	Digital Ground	SYS_ADC_1P8V	Power Out
V10	XTALIN	Oscillator Input	No Connect	No Connect
U11	XTALOUT	Oscillator Output	No Connect	No Connect
B1 – B3, C1 – C4, D1 – D5, E1 – E4, F1 – F4, G1 – G4, H 1 – H4, J1 – J4, K1 – K4, L1 – L4, M1 – M4, N1 – N4, P1 – P4	DDR Interface	I/O	No Connect	No Connect

F20	Not Available	None	OSC1_OUT	Oscillator Output
G20	Not Available	None	OSC1_GND	Oscillator Ground
H20	Not Available	None	OSC1_IN	Oscillator Input
K20	Not Available	None	OSC0_OUT	Oscillator Output
L20	Not Available	None	OSC0_GND	Oscillator Ground
M20	Not Available	None	OSC0_IN	Oscillator Input

Important Notice