Released Data Sheet

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SanDisk® Industrial iNAND™ Embedded Flash Drive

e.MMC 4.51 with HS200 Interface

REVISION HISTORY

Doc. No	Revision	Date	Description	Reference
80-36-03750	1.0	May-19-2015	Preliminary release	
80-36-03750	1.1	Jun-17-2015	Updated 64GB package size to 12x16mm and added relevant package drawings and pin assignments	
80-36-03750	1.2	Jul-20-2015	Updated Package drawings and table of dimensions in Physical specifications section	

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1. INTRODUCTION

1.1. General Description

SanDisk Industrial iNAND Embedded Flash Drive (EFD) with extended temperature support is an ideal embedded storage solution for industrial applications requiring colder operating temperature functionality than typical embedded solutions.

The iNAND EFD is a hybrid device combining an embedded thin flash controller and standard MLC (2 bit per cell) NAND flash memory, with an industry standard e.MMC HS200 4.51[1] interface.

Empowered with e.MMC4.51 features, as well as legacy e.MMC4.41 features such as Boot and RPMB partitions, HPI, and HW Reset, iNAND EFD is the optimal device for reliable code and data storage.

iNAND EFD's optimized algorithm for flash memory management ensures high data reliability and maximizes flash memory life expectancy. With the dedicated controller and hardware ECC engine, iNAND EFD will reduce CPU overhead in managing raw NAND and show higher system performance.

All iNAND EFDs are built and tested with SanDisk's high quality and reliability procedures and supported by a dedicated global team.

1.2. Plug-and-Play Integration

iNAND EFD fully emulates a hard disk to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. iNAND EFD includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

By supporting the e.MMC interface, iNAND EFD eliminates the need for complicated software integration and enables a practically plug-and-play integration in the system. The replacement of one iNAND EFD with another of a newer generation requires virtually no changes to the host. This makes iNAND EFD the perfect solution for platforms and reference designs, as it allows for the utilization of more advanced NAND flash memory technology with minimal integration or qualification efforts.

Figure 1 shows a block diagram of the iNAND EFD with MMC Interface.

[1] Refer to JEDEC Standards No. JESD84-B451

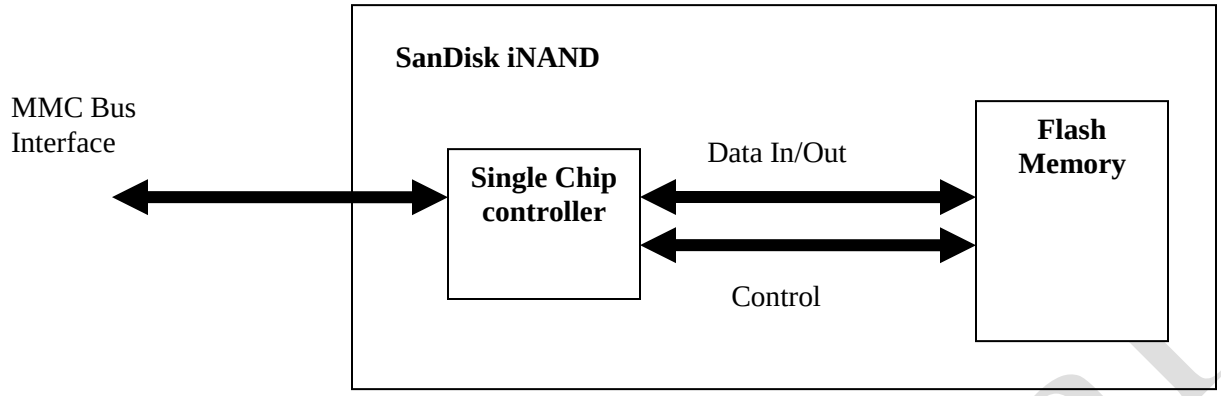

Figure 1 - SanDisk iNAND Embedded Flash Drive with MMC I/F Block Diagram

1.3. Feature Overview

Extended Temperature iNAND EFD, with e.MMC interface, features include the following:

- Memory controller and NAND flash memory
- Mechanical design complies with JEDED MO-276C Specification
- Offered in two TFBGA packages compliant with e.MMC 4.51[2]
  - 11.5mm x 13mm x 1.0mm (4GB - 32GB)
  - 11.5mm x 13mm x 1.2mm (64GB for wide operating temp device)
  - 12mm x 16mm x 1.4mm (64B for extended operating temp device)
- Offered in two versions for different operating temperatures:
  - Industrial wide operating temperature (Tcase) range: –25C° to +85C°
  - Industrial extended operating temperature (Tcase) range: –40C° to +85C°
- Dual power system
- Core voltage (VCC) 2.7-3.6 V
- I/O (VCCQ) voltage, either: 1.7-1.95 V or 2.7-3.6 V
- Up to 64GB of data storage.
- Supports three data bus widths: 1bit (default), 4bit, 8bit.
- Complies with e.MMC Specification Ver. 4.51 HS200[3]
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed), 0-200 MHz (HS200)

[2] Refer to JEDEC Standards No. JESD84-B451
[3] Refer to JEDEC Standards No. JESD84-B451

- Up to 200 MB/sec bus transfer rate, using 8 parallel data lines at 200 MHz, HS200 Mode
- Correction of memory field errors
- Supports eMMC cache

1.4. Functional Description

SanDisk iNAND EFD contains a high-level, intelligent subsystem as shown in Figure 1. This intelligent (microprocessor) subsystem provides many capabilities not found in other types of storage devices. These capabilities include:

- Host independence from details of erasing and programming flash memory
- Sophisticated system for managing defects
- Sophisticated system for error recovery including a powerful ECC
- Power management for low power operation

1.5. Technology Independence

SanDisk iNAND EFD uses 512 bytes as a sector size. To write or read a sector (or multiple sectors), the host software simply issues a read or write command to the device. The command contains the address and number of sectors to write or read. The host software then waits for the command to complete.

There is no host software involvement in the details of flash operations such as erase, program or read. This is extremely important since flash memory based devices are becoming increasingly complex with current advanced NAND MLC processes. Because iNAND EFD uses an intelligent on-board controller, host system software will not need to be updated as new flash memory evolves. In other words, systems that support iNAND EFD technology today will be able to access future SanDisk EFDs built with new flash memory technology without having to update or change the host software.

1.6. Defect and Error Management

The SanDisk iNAND EFD contains a sophisticated defect and error management system. If necessary, iNAND EFD will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume any user data space. In the extremely rare case that a read error does occur, iNAND EFD has innovative algorithms to recover the data.

1.7. MMC bus and Power Lines

SanDisk iNAND EFD with MMC interface supports the e.MMC protocol. For more details regarding these buses refer to JEDEC standards No. JESD84-B451.

The iNAND EFD bus has the following communication and power lines:

- CMD: Command is a bidirectional signal. The host and iNAND EFD operate in two modes, open drain and push-pull.

- DAT0-7: Data lines are bidirectional signals. Host and iNAND EFD operate in push-pull mode.
- CLK: Clock input.
- RST_n: Hardware Reset Input
- VCCQ: VCCQ is the power supply line for host interface.
- VCC: VCC is the power supply line for internal flash memory.
- VDDi: VDDi is iNAND EFD's internal power node, not the power supply. Connect 0.1uF capacitor from VDDi to ground.
- VSS, VSSQ: ground lines.

1.7.1. Bus operating conditions

Table 1 - Bus operating conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	VCCQ+0.5	V
Input Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA
Output Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA

Table 2 – Power supply voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ (Low)	1.7	1.95	V
	VCCQ (High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ	-0.5	0.5	V

Note: HS200 mode only supports the 1.7 – 1.95 V VCCQ option

2. E.MMC4.51 SELECTED FEATURES OVERVIEW

2.1. HS200 I/F

Support HS200 signaling to achieve bus speed of 200 MB/s via a 200MHz single data rate clock frequency. HS200 mode supports 4 or 8 bit bus width and the 1.7 – 1.95 VCCQ option. Due to the speed, the host may need to have an adjustable sampling point to reliably receive the incoming data. For additional information please refer to JESD84-B451 standard.

2.2. Cache

The eMMC cache is dedicated volatile memory at the size of 128KB. It will help to reduce read and write latency over sequential transactions to the iNAND EFD. For additional information please refer to JESD84-B451 standard.

2.3. Discard

iNAND EFD supports discard command as defined in e.MMC4.51 spec[4]. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the media. It is highly recommended for use to guarantee optimal performance of iNAND EFD and reduce the amount of housekeeping operation.

2.4. Power Off Notifications

iNAND EFD supports power off notifications as defined in e.MMC4.51 spec[5]. The usage of power off notifications allows the device to prepare itself to power off, and improve user experience during power-on. Note that the device may be set into sleep mode while Power Off Notification is enabled.

- **Latency** – overall user experience is improved. Device returns quicker from each write operation
- **Burst performance** is improved – performing housekeeping during idle allows us to better prepare for the next burst operations. (Cleaning up the SLC cache for future usage)
- **Graceful shutdown** – power off notification itself allows the device to shutdown properly and save important data for fast boot time on the next power cycle

2.5. Packed Commands

To enable optimal system performance, iNAND EFD supports packed commands as defined in e.MMC4.51 spec[6]. It allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus. Thus, it allows reducing overall bus overhead.

[4] For additional information refer to JEDEC Standard No. JESD84-B451

[5] For additional information refer to JEDEC Standard No. JESD84-B451

[6] For additional information refer to JEDEC Standard No. JESD84-B451

Faster sequential write performance on platform level using packed CMD

- Convert packed sequential commands to a single internal write. (ie. 8x128K packed writes become a single 1MB write)
- Hides host TAT, pipelines writes

2.6. Boot partitions Size

iNAND EFD supports e.MMC 4.51 boot operation modes. The 4-8GB iNAND EFD has two boot area partitions with a default size of 2MB each, and 16-64GB iNAND EFD has two boot area partitions with a default size of 4MB each. Boot area resize is supported, but the boot areas cannot be increased beyond their default size.

2.7. Automatic Sleep Mode

A unique feature of iNAND EFD is automatic entrance and exit from sleep mode. Upon completion of an operation, the device enters sleep mode to conserve power if no further commands are received. Typically the entrance to sleep mode occurs after 10ms, max value entering sleep mode is 850ms due to housekeeping operation. The host does not have to take any action for this to occur, however, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most systems, embedded devices are in sleep mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in sleep mode, any command issued to it will cause it to exit sleep and respond immediately.

2.8. Sleep (CMD5)

An iNAND EFD may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The Vcc power supply may be switched off in Sleep state to enable even further system power consumption saving.

For additional information please refer JESD84-B451 section number 6.6.28.

2.9. Enhanced Reliable Write

iNAND EFD supports enhanced reliable write as defined in e.MMC 4.51 spec[7].

Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

[7] For additional information refer to JEDEC Standards No. JESD84-B451

2.10. Secure Erase

For backward compatibility reasons, in addition to the standard erase command the iNAND EFD supports the optional Secure Erase command[8].
The Secure Erase command differs from the basic Erase command in that it requires the iNAND EFD to execute the erase operation on the memory array when the command is issued and requires the iNAND EFD and host to wait until the operation is complete before moving to the next iNAND EFD operation.

The secure erase command requires the iNAND EFD to perform a secure purge operation on the erase groups, and copy items identified for erase, in those erase groups.
A purge operation is defined as overwriting addressable locations with a single character and then performing an erase.

This new command meets high security application requirements (e.g. those used by military and government customers) that once data has been erased, it can no longer be retrieved from the device.

2.11. Secure Trim

For backward compatibility reasons, iNAND EFD supports Secure Trim command. The Secure Trim[9] command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups. The size of a write block in the iNAND device is 512B.

2.12. Trim

The Trim function is similar to the Erase command but applies the erase operation to write blocks instead of erase groups. The size of a write block in the iNAND EFD is 512B.

For additional information on the Trim function, refer to JEDEC standards No. JESD84-B451.

2.13. Partition management

The iNAND EFD offers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore memory block area scan be classified as follows[10]:

- Factory configuration supplies two boot partitions (refer to section 2.6) and one RPMB partitioning of 4MB in size. The sizes of these partitions are set as default by the factory.
- Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group (16MB). Size can be programmed once in device life-cycle (one-time programmable).

[8] For additional information refer to JEDEC Standards No. JESD84-B451

[9] For additional information refer to JEDEC Standards No. JESD84-B451

[10] For additional information refer to JEDEC Standards No. JESD84-B451

2.14. Device Health

Device Health is SanDisk proprietary feature and is similar to SMART feature of modern hard disks, it provides only vital NAND EFD flash program/erase cycles information in percentage of useful flash life span.

Host can query Device Health information utilizing standard MMC command, CMD_8, to get extended CSD structure. Device health feature will provide % of the wear of the device in 10% fragments.

The following 2 Extended CSD fields will hold the average percentage of usage for an iNAND device. Each one holds a value for of the specified memory types:

- MLC User Area
- SLC Internal memory such as Binary Cache

Name	Field	Size (Byte)	Cell Type	Hex Offset (Byte)	Dec. Offset (Byte)
MLC Device health status	MLC_DEVICE_HEALTH_STATUS	1	R	0x5E	94
SLC Device health status	SLC_DEVICE_HEALTH_STATUS	1	R	0x57	87

2.15. Enhanced Write Protection

To allow the host to protect data against erase or write, the iNAND EFD supports two levels of write protect command[11]:

- The entire iNAND EFD (including the Boot Area Partitions, General Purpose Area Partition, and User Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD.
- Specific segments of the iNAND EFD may be permanently, power-on or temporarily write protected. Segment size can be programmed via the EXT_CSD register.

For additional information please refer JESD84-B451 standard.

2.16. High Priority Interrupt (HPI)

Many operating-systems use demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.

[11] For additional information refer to JEDEC Standards No. JESD84-B451

The high priority interrupt (HPI) as defined in JESD84-B451 enables low read latency operation by suspending a lower priority operation before it is actually completed. This mechanism can reduce read latency, in typical condition to below 10msec.

For additional information on the HPI function, refer to JESD84-B451 standard section 6.6.23.

2.17. H/W Reset

Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that were power-on write protected before the reset was asserted. For more information, refer to JESD84-B451 standard.

2.18. DDR I/F

Supports DDR signaling to double bus performance. For additional information please refer to JESD84-B451 standard.

3. PRODUCT SPECIFICATIONS

3.1. Typical Power Requirements

Table 3 - iNAND Embedded Flash Drive Max Sleep Power Requirements (Ta=25°C@3.3V)

	4GB	8GB	16GB	32GB	64GB	Measurement
Auto Sleep mode	350	350	350	400	500	uA
Sleep (CMD5 – VCCQ, VCC off)	300	300	300	300	300	uA

Table 4 - iNAND Embedded Flash Drive Max Active Power Requirements Peak VCC / VCCQ (Ta=25°C@3.3V/1.8V)

	4GB	8GB	16GB	32GB	64GB	Measurement
Peak VCC	200	100	200	200	200	mA
Peak VCCQ	150	150	150	150	150	mA
Total	300	300	300	300	300	mA

Table 5 - iNAND Embedded Flash Drive MaxActive Power Requirements RMS VCC / VCCQ (Ta=25°C@3.3V/1.8V)

		4GB	8GB	16GB	32GB	64GB	Measurement
Read	RMS VCC	100	100	100	100	100	mA
	RMS VCCQ	150	100	150	150	150	mA
	Total	200	200	200	200	200	mA
Write	RMS VCC	100	50	100	100	100	mA
	RMS VCCQ	100	50	100	150	150	mA
	Total	200	100	200	200	200	mA

Note 1: RMS Current measurements are average over 100 mSecs.

Note 2: Sleep current is measured at room temperature

Note 3: In sleep state, triggered by CMD5, Flash Vcc power supply is switched off

Note 4: Peak current is measured over 3 uSecs.

Note 5: Measured under HS200 mode with a bus width of 8 bit

3.2. Operating Conditions

3.2.1. Operating and Storage Temperature Specifications

Table 6 - Operating and Storage Temperatures

Temperature	Operating (-I SKUs)	-25° C to 85° C
	Operating (-XI SKUs)	-40° C to 85° C
	Non-Operating: After soldered onto PC Board	-40° C to 85° C

3.2.2. Moisture Sensitivity

The moisture sensitivity level for iNAND EFD is MSL = 3.

3.3. System Performance

All performance values for iNAND EFD Tables 7 and 8 were measured under the following conditions:

- Voltage range:

  Core voltage (VCC): 2.7-3.6 V

  Host voltage (VCCQ), either: 1.7-1.95 V or 2.7-3.6 V

- Operating temperature

  (Tcase) -40° C to 85° C for extended operating temp device

  (Tcase) -25° C to 85° C for wide operating temp device

Table 7 - Sequential System Performance

Density	Sustained Write Up to	Sustained Read Up to
4GB	17MB/s	90 MB/s
8GB	17MB/s	90 MB/s
16GB	30 MB/s	115 MB/s
32GB	37 MB/s	120 MB/s
64GB	37 MB/s	120 MB/s

Table 8-– Random System Performance

SKU	Sustained Write Up to	Sustained Read Up to
4GB	500 IOPS	4500 IOPS
8GB	850 IOPS	4500 IOPS
16GB	1200 IOPS	4500 IOPS
32GB	1200 IOPS	4500 IOPS
64GB	1200 IOPS	4500 IOPS

Note 1: Sustained Sequential Read/Write performance is measured under HS200 mode with a bus width of 8 bit at 200 MHz, chunk size of 512KB, and data transfer of 1GB.

Note 2: Random performance is measured with a chunk size of 4KB and address range of 100MB.

Note 3: All performance is measured using SanDisk proprietary test environment, without file system overhead and host turn-around time (HTAT). Performance may vary based on capacity applications and usage. 1MB = 1,000,000 bytes.

Table 9 - System Timing Performance

Timing	Value
Block Read Access Time (MAX)	100 ms
Block Write Access Time (MAX)	250 ms
CMD1 to Ready after Power-up (MAX)	1000 ms

Note: Timing performance numbers valid with PON on or off

3.4. Data Retention and Read Endurance

Based on the application usage model and the frequency of reads and writes, the customer may need to implement a read-refresh process between the host and eMMC to help protect overly read portions of the memory in case the below reliability specifications are exceeded. Please contact your local SanDisk field application engineering representative for more details.

Table 10 – Critical Reliability Characteristics

Reliability Characteristic	Description	Value
Data Retention	Data Retention for cycled up to 10% of max Write Endurance specification 300 P/E cycles devices	10 years of Data Retention @55°C
	Data Retention for cycled up to maximum Write Endurance devices	1 year of Data Retention @55°C
Read Endurance	Read Endurance for cycled up to 10% of max Write Endurance specification 300 P/E cycles devices	100K Read cycles
	Read Endurance for cycled up to maximum Write Endurance devices	10K Read cycles

4. PHYSICAL SPECIFICATIONS

The SanDisk iNAND Embedded Flash Drive is a 153 or 169-pin, thin fine-pitched ball grid array (BGA). See Figure 2, Figure 3, and Table 11 for physical specifications and dimensions of 153 pin and Figure 4, Figure 5, and Table 12 for physical specifications and dimensions of 169 pin.

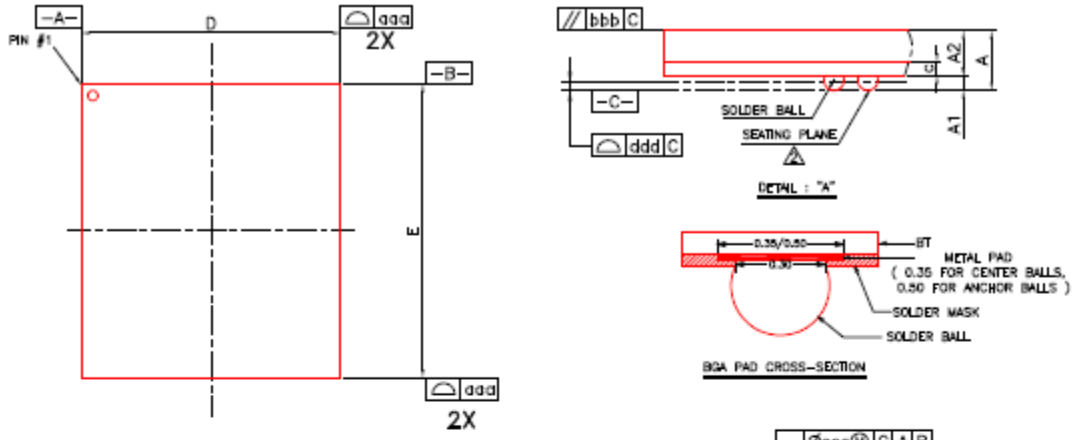

Figure 2 – 11.5x13 153 Ball Package Outline Drawing Top and Side View

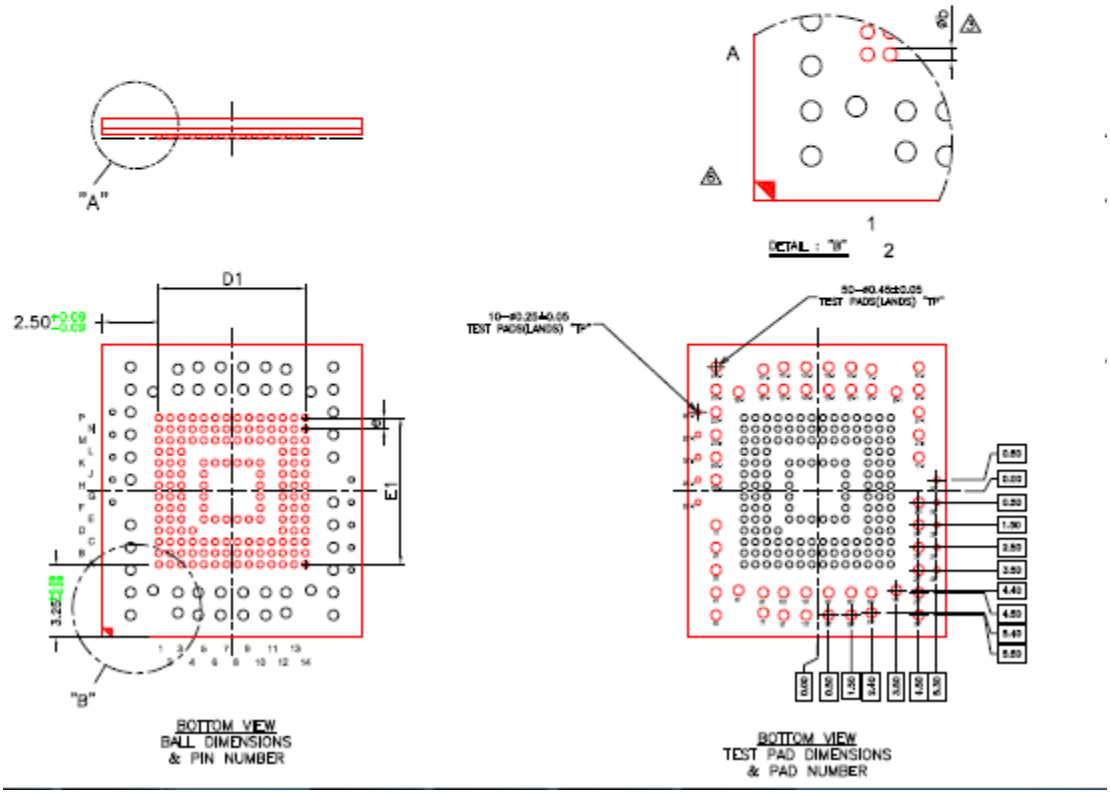

Figure 3- 11.5x13 153 Ball Package Outline Drawing Bottom View

Table 11 - iNAND Embedded Flash Drive 153 Ball Package Specification

153 ball		Dimension in millimeters			Dimension in inches		
Package Size	**Symbol**	**Minimum**	**Nominal**	**Maximum**	**Minimum**	**Nominal**	**Maximum**
11.5X13X1.0	A	---	---	1.0	---	---	0.039
11.5X13X1.0	A1	0.17	0.22	0.27	0.007	0.009	0.011
11.5X13X1.0	A2	0.61	0.66	0.71	0.024	0.026	0.028
11.5X13X1.2	A	---	---	1.2	---	---	0.039
11.5X13X1.2	A1	0.17	0.22	0.27	0.007	0.009	0.011
11.5X13X1.2	A2	0.785	0.835	0.885	0.031	0.033	0.035
All	C	0.17	0.21	0.25	0.007	0.008	0.010
All	D	11.43	11.50	11.57	0.450	0.453	0.456
11.5X13X1.0 (4GB products)	E	12.93	13	13.07	0.509	0.512	0.515
11.5X13X1.0 (8GB,16GB,32GB products)	E	12.96	13.02	13.08	0.510	0.513	0.515
11.5X13X1.2	E	12.96	13.02	13.08	0.510	0.513	0.515
All	D1	---	6.5	---	---	0.256	---
All	E1	---	6.5	---	---	0.256	---
All	e	---	0.5	---	---	0.020	---
All	b	0.25	0.3	0.35	0.010	0.012	0.014
All	aaa	0.10			0.004		
All	bbb	0.10			0.004		
All	ddd	0.08			0.003		
All	eee	0.15			0.006		
All	fff	0.05			0.002		
All	MD/WE	14/14			14/14		

Figure 4 – 12x16 169 Ball Package Outline Drawing Top and Side View

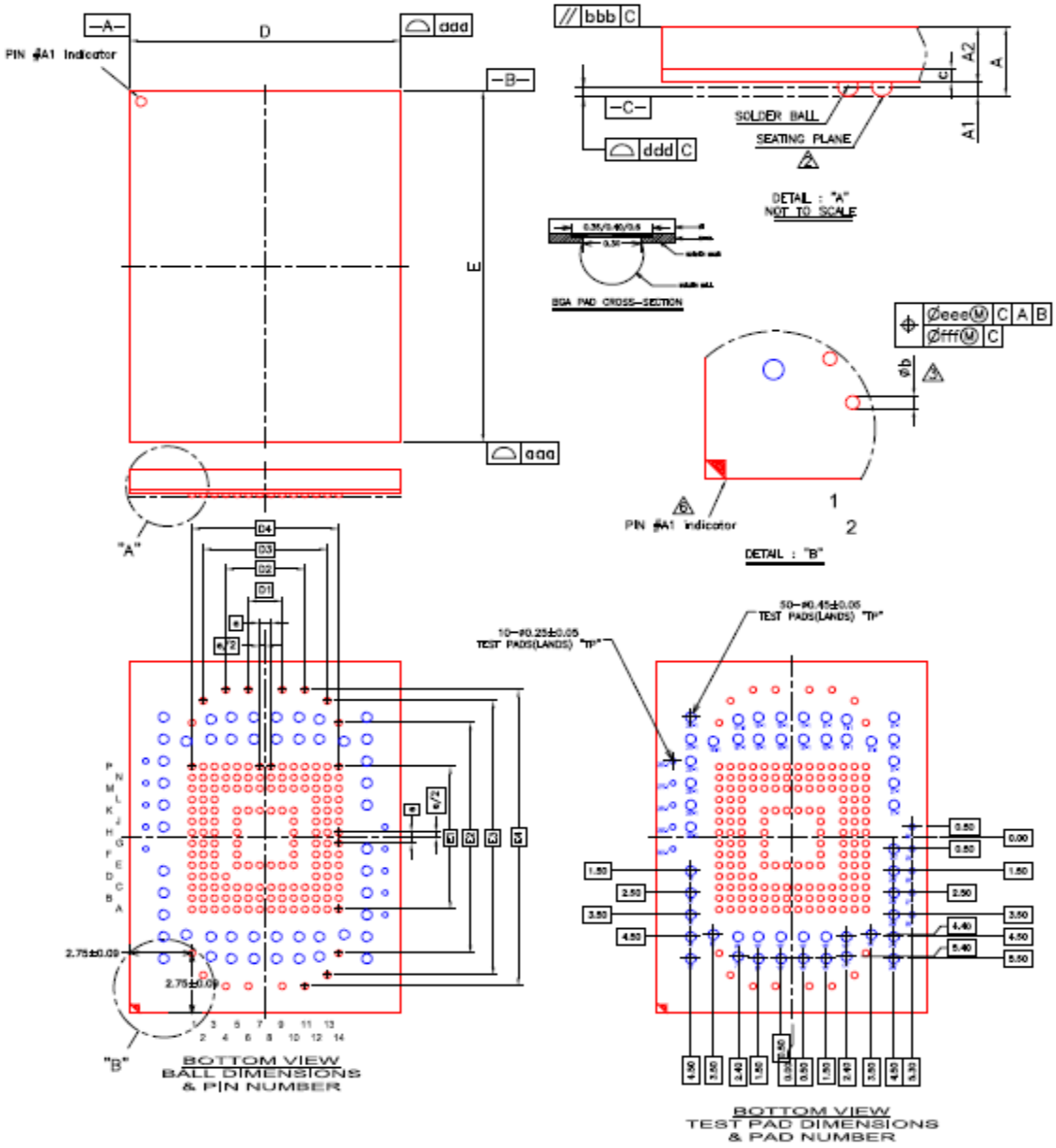

Figure 5 – 12x16 169 Ball Package Outline Drawing Bottom View

Table 12 – iNAND Embedded Flash Drive 169 Ball Package Specification

169 Ball		Dimension in millimeters			Dimension in inches		
Package Size	**Symbol**	**Minimum**	**Nominal**	**Maximum**	**Minimum**	**Nominal**	**Maximum**
12x16x1.4	A	---	---	1.40	---	---	0.055
12x16x1.4	A1	0.17	0.22	0.27	0.007	0.009	0.011
12x16x1.4	A2	1.01	1.05	1.09	0.040	0.041	0.043
12x16x1.4	c	0.14	0.17	0.20	0.006	0.007	0.008
12x16x1.4	D	11.93	12.00	12.07	0.470	0.472	0.475
12x16x1.4	E	15.93	16.00	16.07	0.627	0.630	0.633
12x16x1.4	D1	---	1.50	---	---	0.059	---
12x16x1.4	D2	---	3.50	---	---	0.138	---
12x16x1.4	D3	---	5.50	---	---	0.217	---
12x16x1.4	D4	---	6.50	---	---	0.256	---
12x16x1.4	E1	---	6.50	---	---	0.256	---
12x16x1.4	E2	---	10.50	---	---	0.413	---
12x16x1.4	E3	---	12.50	---	---	0.492	---
12x16x1.4	E4	---	13.50	---	---	0.531	---
12x16x1.4	e	---	0.50	---	---	0.020	---
12x16x1.4	b	0.25	0.30	0.35	0.010	0.012	0.014
12x16x1.4	aaa	0.10			0.004		
12x16x1.4	bbb	0.10			0.004		
12x16x1.4	ddd	0.08			0.003		
12x16x1.4	eee	0.15			0.006		
12x16x1.4	fff	0.05			0.002		
12x16x1.4	MD/ME	14/14			14/14		

5. INTERFACE DESCRIPTION

5.1. MMC I/F Ball Array

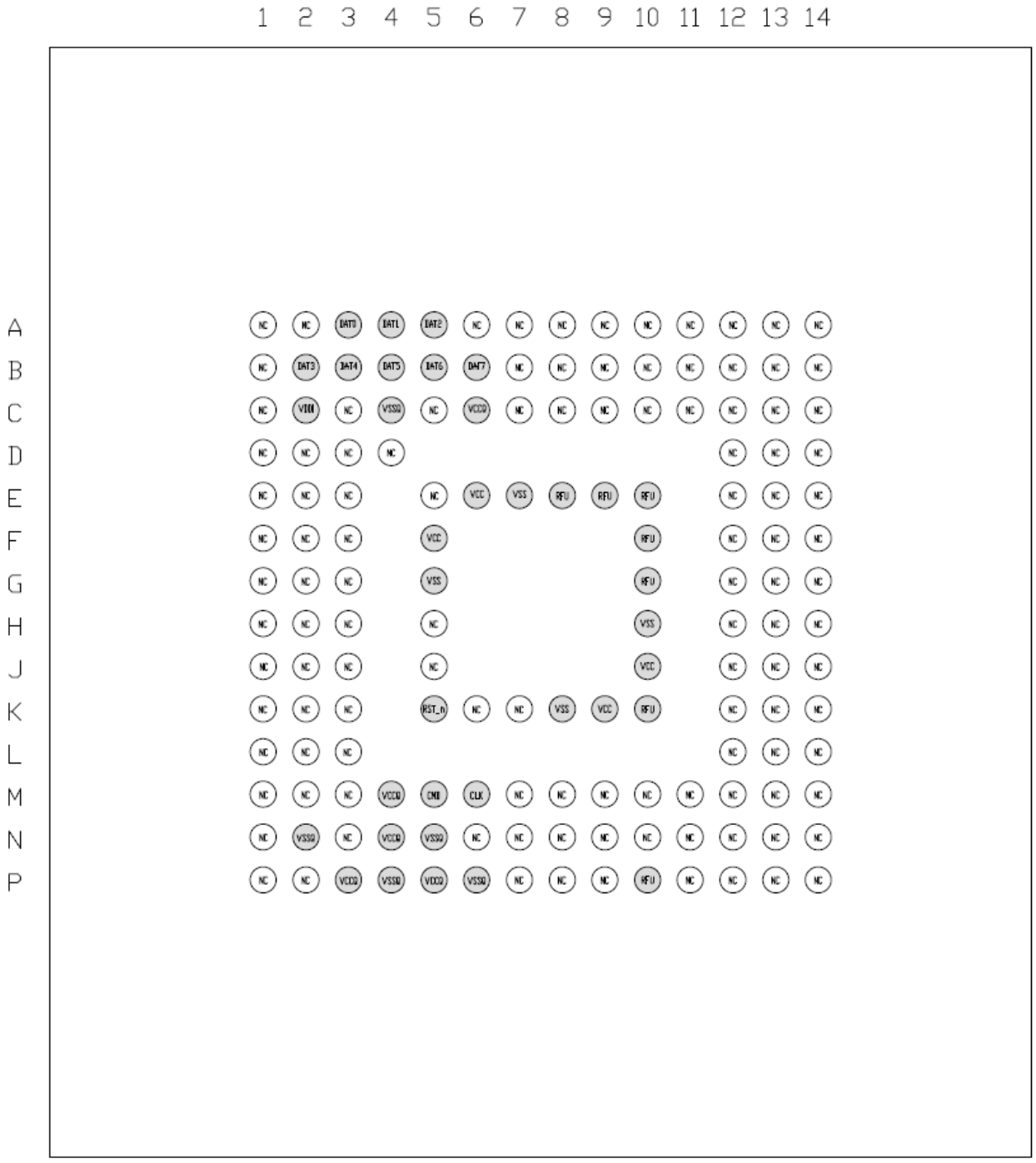

Figure 6 - 153 Ball Array (Top View)

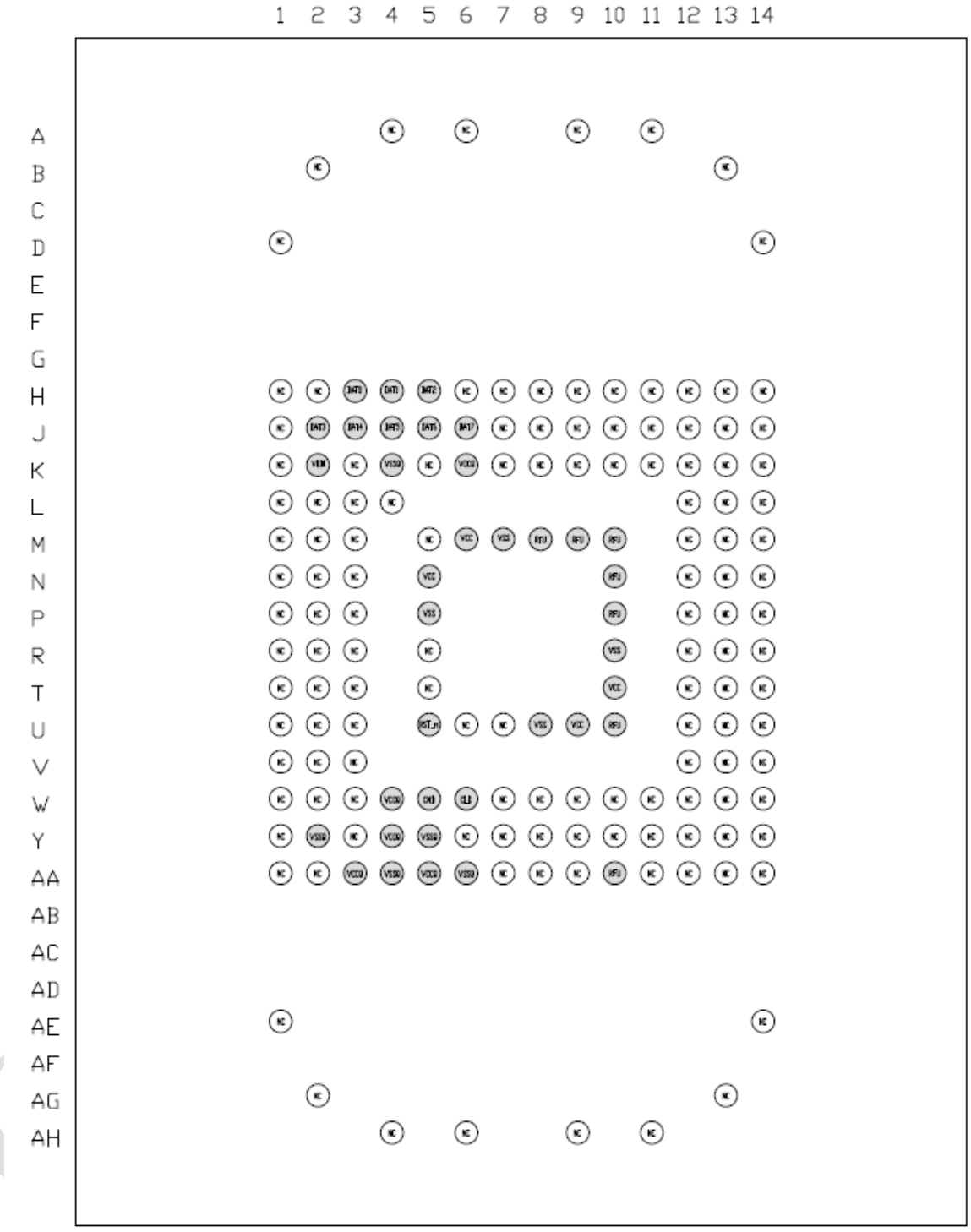

Figure 7 - 169 Ball Array (Top View)

5.2. Pins and Signal Description

Table 13 contains the SanDisk iNAND Embedded Flash Drive 153 ball package functional pin assignment.

Table 13 - Functional Pin Assignment, 153 balls

Ball No.	Ball Signal	Type	Description
A3	DAT0	I/O	Data I/O: Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
K5	RST_n		Hardware Reset
E6	VCC	Supply	Flash I/O and memory power supply
F5	VCC		
J10	VCC		
K9	VCC		
C6	VCCQ	Supply	Memory controller core and MMC I/F I/O power supply
M4	VCCQ		
N4	VCCQ		
P3	VCCQ		
P5	VCCQ		
E7	VSS	Supply	Flash I/O and memory ground connection
G5	VSS		
H10	VSS		
K8	VSS		
C4	VSSQ		Memory controller core and MMC I/F ground connection
N2	VSSQ		
N5	VSSQ		
P4	VSSQ		
P6	VSSQ		
C2	VDDi		Internal power node. Connect 0.1uF capacitor from VDDi to ground

Note: Pins E8, E9, E10, F10, G10, K10, P10 are reserved for future use [RFU]

Note: All other pins are not connected [NC] and can be connected to GND or left floating

Table 14 contains the SanDisk iNAND Embedded Flash Drive 169 ball package functional pin assignment.

Table 14 - Functional Pin Assignment, 169 balls

Ball No.	Ball Signal	Type	Description
H3	DAT0	I/O	Data I/O: Bidirectional channel used for data transfer
H4	DAT1		
H5	DAT2		
J2	DAT3		
J3	DAT4		
J4	DAT5		
J5	DAT6		
J6	DAT7		
W5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
W6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
U5	RST_n		Hardware Reset
M6	VCC	Supply	Flash I/O and memory power supply
N5	VCC		
T10	VCC		
U9	VCC		
K6	VCCQ	Supply	Memory controller core and MMC I/F I/O power supply
W4	VCCQ		
Y4	VCCQ		
AA3	VCCQ		
AA5	VCCQ		
M7	VSS	Supply	Flash I/O and memory ground connection
P5	VSS		
R10	VSS		
U8	VSS		
K4	VSSQ		Memory controller core and MMC I/F ground connection
Y2	VSSQ		
Y5	VSSQ		
AA4	VSSQ		
AA6	VSSQ		
K2	VDDi		Internal power node. Connect 0.1uF capacitor from VDDi to ground

Note: Pins M8, M9, M10, N10, P10, U10, AA10 are reserved for future use [RFU]

Note: All other pins are not connected [NC] and can be connected to GND or left floating

5.3. iNAND Embedded Flash Drive Registers

5.3.1. OCR Register

Value: 0xC0FF8080

Note: Bit 30 is set because the device is High Capacity; bit 31 will be set only when the device is ready

Parameter	OCR slice	Description	Value	**Width**
Access Mode	[30:29]	Access mode	10b	2
	[23:15]	VDD: 2.7 - 3.6 range	111111111b	9
	[14:8]	VDD: 2.0 - 2.6 range	0000000b	7
	[7]	VDD: 1.7 - 1.95 range	1b	1

5.3.2. CID Register

Parameter	**CID slice**	**Description**	**Value**	**Width**
MID	[127:120]	Manufacturer ID	45h	8
CBX	[113:112]	Device BGA	01b	2
OID	[111:104]	OEM/Application ID	00h	8
PNM	[103:56]	Product name	4GB: 53454D313447h ("SEM04G") 8GB: 53454D303847h ("SEM08G") 16GB: 53454D313647h ("SEM16G") 32GB: 53454D333247h ("SEM32G") 64GB: 53454D363447h (“SEM64G”)	48
PRV	[55:48]	Product revision	Counter to indicate FW revision	8
PSN	[47:16]	Product serial number	Random by Production	32
MDT	[15:8]	Manufacturing date	month, year	8
CRC	[7:1]	CRC7 checksum	0000000b	7

Refer to the new definition of the MDT field as defined in eMMC Spec Ver 4.51

5.3.3. DSR Register

Parameter	**DSR slice**	**Description**	**Value**	**Width**
RSRVD	[15:8]	Reserved	04h	8
RSRVD	[7:0]	Reserved	04h	8

DSR is not implemented; in case of read, value of 0x0404 will be returned.

5.3.4. CSD Register

Parameter	CSD Slice	Description	Value	Width
CSD_STRUCTURE	[127:126]	CSD structure	11b	2
SPEC_VERS	[125:122]	System specification version	0100b	4
TAAC	[119:112]	Data read access-time 1	0Fh	8
NSAC	[111:104]	Data read access-time 2 in CLK cycles (NSAC*100)	00h	8
TRAN_SPEED	[103:96]	Max. bus clock frequency	32h	8
CCC	[95:84]	Device command classes	0F5h	12
READ_BL_LEN	[83:80]	Max. read data block length	9h	4
READ_BL_PARTIAL	[79:79]	Partial blocks for read allowed	0b	1
WRITE_BLK_MISALIGN	[78:78]	Write block misalignment	0b	1
READ_BLK_MISALIGN	[77:77]	Read block misalignment	0b	1
DSR_IMP	[76:76]	DSR implemented	0b	1
C_SIZE	[73:62]	Device size	FFFh	12
VDD_R_CURR_MIN	[61:59]	Max. read current @ VDD min	111b	3
VDD_R_CURR_MAX	[58:56]	Max. read current @ VDD max	111b	3
VDD_W_CURR_MIN	[55:53]	Max. write current @ VDD min	111b	3
VDD_W_CURR_MAX	[52:50]	Max. write current @ VDD max	111b	3
C_SIZE_MULT	[49:47]	Device size multiplier	111b	3
ERASE_GRP_SIZE	[46:42]	Erase group size	11111b	5
ERASE_GRP_MULT	[41:37]	Erase group size multiplier	11111b	5
WP_GRP_SIZE	[36:32]	Write protect group size	11111b	5
WP_GRP_ENABLE	[31:31]	Write protect group enable	1b	1
DEFAULT_ECC	[30:29]	Manufacturer default	00b	2
R2W_FACTOR	[28:26]	Write speed factor	10b	3
WRITE_BL_LEN	[25:22]	Max. write data block length	9h	4
WRITE_BL_PARTIAL	[21:21]	Partial blocks for write allowed	0b	1
CONTENT_PROT_APP	[16:16]	Content protection application	0b	1
FILE_FORMAT_GRP	[15:15]	File format group	0b	1
COPY	[14:14]	Copy flag (OTP)	1b	1
PERM_WRITE_PROTECT	[13:13]	Permanent write protection	0b	1
TMP_WRITE_PROTECT	[12:12]	Temporary write protection	0b	1
FILE_FORMAT	[11:10]	File format	00b	2
ECC	[9:8]	ECC code	00b	2
CRC	[7:1]	Calculated CRC	0000000b	7

5.3.5. EXT_CSD Register

Parameter	ECSD slice [bytes]	Description	Value
S_CMD_SET	[504]	Supported Command Sets	1h
HPI_FEATURES	[503]	HPI Features	1h
BKOPS_SUPPORT	[502]	Background operations support	1h
MAX_PACKED_READS	[501]	Max packed read commands	3Fh
MAX_PACKED_WRITES	[500]	Max packed write commands	3Fh
DATA_TAG_SUPPORT	[499]	Data Tag Support	1h
TAG_UNIT_SIZE	[498]	Tag Unit Size	3h
TAG_RES_SIZE	[497]	Tag Resources Size	3h
CONTEXT_CAPABILITIES	[496]	Context management capabilities	5h
LARGE_UNIT_SIZE_M1	[495]	Large Unit size	0h
EXT_SUPPORT	[494]	Extended partitions attribute support	0h
CACHE_SIZE	[252:249]	Cache size	0400h
GENERIC_CMD6_TIME	[248]	Generic CMD6 timeout	19h
POWER_OFF_LONG_TIME	[247]	Power off notification(long) timeout	64h
BKOPS_STATUS	[246]	Background operations status	Default = 0h Updated in Run time
CORRECTLY_PRG_SECTORS_NUM	[245:242]	Number of correctly programmed sectors	Default = 0h Updated in Run time
INI_TIMEOUT_AP	[241]	1st Initialization time after partitioning	Ah
PWR_CL_DDR_52_360	[239]	Power class for 52MHz, DDR at 3.6V	4GB = 0h 8GB 1D = 0h 8GB 2D = 22h 16GB = 22h 32-64GB = 44h
PWR_CL_DDR_52_195	[238]	Power class for 52MHz, DDR at 1.95V	0h
PWR_CL_200_360	[237]	Power class for 200MHz at 3.6V	0h
PWR_CL_200_195	[236]	Power class for 200MHz, at 1.95V	0h
MIN_PERF_DDR_W_8_52	[235]	Minimum Write Performance for 8bit at 52MHz in DDR mode	0h
MIN_PERF_DDR_R_8_52	[234]	Minimum Read Performance for 8bit at 52MHz in DDR mode	0h
TRIM _MULT	[232]	TRIM Multiplier	Eh
SEC_FEATURE_SUPPORT	[231]	Secure Feature support	55h
SEC_ERASE_MULT	[230]	Secure Erase Multiplier	44h
SEC_TRIM_MULT	[229]	Secure TRIM Multiplier	44h
BOOT_INFO	[228]	Boot Information	7h
BOOT_SIZE_MULT	[226]	Boot partition size	4-8GB = 10h 16-64GB = 20h
ACCESS_SIZE	[225]	Access size	8h
HC_ERASE_GROUP_SIZE	[224]	High Capacity Erase unit size	Table 16
ERASE_TIMEOUT_MULT	[223]	High capacity erase time out	Eh

Parameter	ECSD slice [bytes]	Description	Value
REL_WR_SEC_C	[222]	Reliable write sector count	1h
HC_WP_GRP_SIZE	[221]	High capacity write protect group size	Table 16
S_C_VCC	[220]	Sleep current [VCC]	8h
S_C_VCCQ	[219]	Sleep current [VCCQ]	7h
S_A_TIMEOUT	[217]	Sleep/Awake time out	13h
SEC_COUNT	[215:212]	Sector count	Table 15
MIN_PERF_W_8_52	[210]	Minimum Write Performance for 8bit @52MHz	Ah
MIN_PERF_R_8_52	[209]	Minimum Read Performance for 8bit @52MHz	Ah
MIN_PERF_W_8_26_4_52	[208]	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_R_8_26_4_52	[207]	Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_W_4_26	[206]	Minimum Write Performance for 4bit @26MHz	Ah
MIN_PERF_R_4_26	[205]	Minimum Read Performance for 4bit @26MHz	Ah
PWR_CL_26_360	[203]	Power Class for 26MHz @ 3.6V	4GB = 0h 8GB 1D = 0h 8GB 2D = 22h 16GB = 22h 32-64GB = 44h
PWR_CL_52_360	[202]	Power Class for 52MHz @ 3.6V	4GB = 0h 8GB 1D = 0h 8GB 2D = 22h 16GB = 22h 32-64GB = 44h
PWR_CL_26_195	[201]	Power Class for 26MHz @ 1.95V	0h
PWR_CL_52_195	[200]	Power Class for 52MHz @ 1.95V	0h
PARTITION_SWITCH_TIME	[199]	Partition switching timing	3h
OUT_OF_INTERRUPT_TIME	[198]	Out-of-interrupt busy timing	19h
DRIVER_STRENGTH	[197]	I/O Driver Strength	1h
DEVICE_TYPE	[196]	Device Type	17h
CSD_STRUCTURE	[194]	CSD Structure Version	2h
EXT_CSD_REV	[192]	Extended CSD Revision	6h
CMD_SET	[191]	Command Set	Default = 0h Updated in Run time
CMD_SET_REV	[189]	Command Set Revision	0h
POWER_CLASS	[187]	Power Class	4GB = 0h

Parameter	ECSD slice [bytes]	Description	Value
			8GB 1D = 0h 8GB 2D = 2h 16GB = 2h 32-64GB = 4h
HS_TIMING	[185]	High Speed Interface Timing	Default = 0h Updated in Run time
BUS_WIDTH	[183]	Bus Width Mode	Default = 0h Updated in Run time
ERASE_MEM_CONT	[181]	Content of explicit erased memory range	0h
PARTITION_CONFIG	[179]	Partition Configuration	Default = 0h Updated in Run time
BOOT_CONFIG_PROT	[178]	Boot config protection	Default = 0h Updated in Run time
BOOT_BUS_CONDITIONS	[177]	Boot bus width1	Default = 0h Updated in Run time
ERASE_GROUP_DEF	[175]	High-density erase group definition	Default = 0h Updated in Run time
BOOT_WP_STATUS	[174]	Boot write protection status registers	Default = 0h Updated in Run time
BOOT_WP	[173]	Boot area write protect register	0h
USER_WP	[171]	User area write protect register	0h
FW_CONFIG	[169]	FW Configuration	0h
RPMB_SIZE_MULT	[168]	RPMB Size	4-8GB = 10h 16-64GB = 20h
WR_REL_SET	[167]	Write reliability setting register	1Fh
WR_REL_PARAM	[166]	Write reliability parameter register	5h
SANITIZE_START	[165]	Start Sanitize operation	Default = 0h Updated in Run time
BKOPS_START	[164]	Manually start background operations	Default = 0h Updated in Run time
BKOPS_EN	[163]	Enable background operations handshake	0h
RST_n_FUNCTION	[162]	H/W reset function	Default = 0h Updated by the host
HPI_MGMT	[161]	HPI management	Default = 0h Updated by the host
PARTITIONING SUPPORT	[160]	Partitioning support	5h
MAX_ENH_SIZE_MULT	[159:157]	Max Enhanced Area Size	4GB = 76h

Parameter	ECSD slice [bytes]	Description	Value
			8GB = E9h 16GB = 1D5h 32GB = 3A3h 64GB = 747h
PARTITIONS_ATTRIBUTE	[156]	Partitions Attribute	Default = 0h Updated by the host
PARTITION_SETTING_ COMPLETED	[155]	Partitioning Setting	Default = 0h Updated by the host
GP_SIZE_MULT	[154:143]	General Purpose Partition Size	0h
ENH_SIZE_MULT	[142:140]	Enhanced User Data Area Size	0h
ENH_START_ADDR	[139:136]	Enhanced User Data Start Address	0h
SEC_BAD_BLK_MGMNT	[134]	Bad Block Management mode	0h
TCASE_SUPPORT	[132]	Package Case Temperature is controlled	0h
PERIODIC_WAKEUP	[131]	Periodic Wake-up	0h
PROGRAM_CID_CSD_DDR_SUPP ORT	[130]	Program CID/CSD in DDR mode support	1h
VENDOR_SPECIFIC_FIELD	[127:64]	Vendor Specific Fields	Reserved
NATIVE_SECTOR_SIZE	[63]	Native sector size	0h
USE_NATIVE_SECTOR	[62]	Sector size emulation	0h
DATA_SECTOR_SIZE	[61]	Sector size	0h
INI_TIMEOUT_EMU	[60]	1st initialization after disabling sector size emulation	0h
CLASS_6_CTRL	[59]	Class 6 commands control	0h
DYNCAP_NEEDED	[58]	Number of addressed group to be Released	0h
EXCEPTION_EVENTS_CTRL	[57:56]	Exception events control	0h
EXCEPTION_EVENTS_STATUS	[55:54]	Exception events status	0h
EXT_PARTITIONS_ATTRIBUTE	[53:52]	Extended Partitions Attribute	0h
CONTEXT_CONF	[51:37]	Context configuration	Default = 0h Updated in Run time
PACKED_COMMAND_STATUS	[36]	Packed command status	Default = 0h Updated in Run time
PACKED_FAILURE_INDEX	[35]	Packed command failure index	Default = 0h Updated in Run time
POWER_OFF_NOTIFICATION	[34]	Power Off Notification	Default = 0h Updated in Run time
CACHE_CTRL	[33]	Control to turn the Cache ON/OFF	0h
FLUSH_CACHE	[32]	Flushing of the cache	0h

The following table shows the capacity available for user data for the various device capacities:

Table 15 – Capacity for User Data

Density	LBA [Hex]	LBA [Dec]	Capacity [Bytes]
4GB	0x760000	7,733,248	3,959,422,976
8GB	0xE90000	15,269,888	7,818,182,656
16GB	0x1D5A000	30,777,344	15,758,000,128
32GB	0x3A3E000	61,071,360	31,268,536,320
64GB	0x747C000	122,142,720	62,537,072,640

Table 16 - Write protect group size

Density	HC_ERASE_GROUP_SIZE	HC_WP_GRP_SIZE	Erase Unit Size [MB]	Write Protect Group Size [MB]
4GB	1h	20h	512KB	16MB
8GB	1h	20h	512KB	16MB
16GB	1h	20h	512KB	16MB
32GB	1h	20h	512KB	16MB
64GB	1h	20h	512KB	16MB

6. POWER DELIVERY AND CAPACITOR SPECIFICATIONS

6.1. SanDisk iNAND Embedded Flash Drive Power Domains

SanDisk iNAND EFD has three power domains assigned to VCCQ, VCC and VDDi, as shown in Table 17.

Table 17 - Power Domains

Pin	Power Domain	Comments
VCCQ	Host Interface	Supported voltage ranges:
		High Voltage Region: 3.3V (nominal)
		Low Voltage Region: 1.8V (nominal)
VCC	Memory	Supported voltage range:
		High Voltage Region: 3.3V (nominal)
VDDi	Internal	VDDi is the internal regulator connection to an external decoupling capacitor.

6.2. Capacitor Connection Guidelines

6.2.1. VDDi Connections

The VDDi (C2) ball must only be connected to an external capacitor that is connected to VSS. This signal may not be left floating. The capacitor's specifications and its placement instructions are detailed below.

The capacitor is part of an internal voltage regulator that provides power to the controller.

Caution: Failure to follow the guidelines below, or connecting the VDDi ball to any external signal or power supply, may cause the device to malfunction.

The trace requirements for the VDDi (C2/K2) ball to the capacitor are as follows:

- Resistance: <2 ohm
- Inductance: <5 nH

The capacitor requirements are as follows:

- Capacitance: >=0.1 uF
- Voltage Rating: >=6.3 V
- Dielectric: X7R or X5R

6.2.2. VCC and VCCQ Connections

- All VCC balls should be connected to a 3.3V supply
- All VCCQ balls should be connected either to a 3.3V or 1.8V supply

SanDisk recommends providing separate bypass capacitors for each power domain as shown in Figure 8.

Note: Signal routing in the diagram is for illustration purposes only and the final routing depends on your PCB layout. Also, for clarity, the diagram does not show the VSS connection. All balls marked VSS should be connected to a ground (GND) plane.

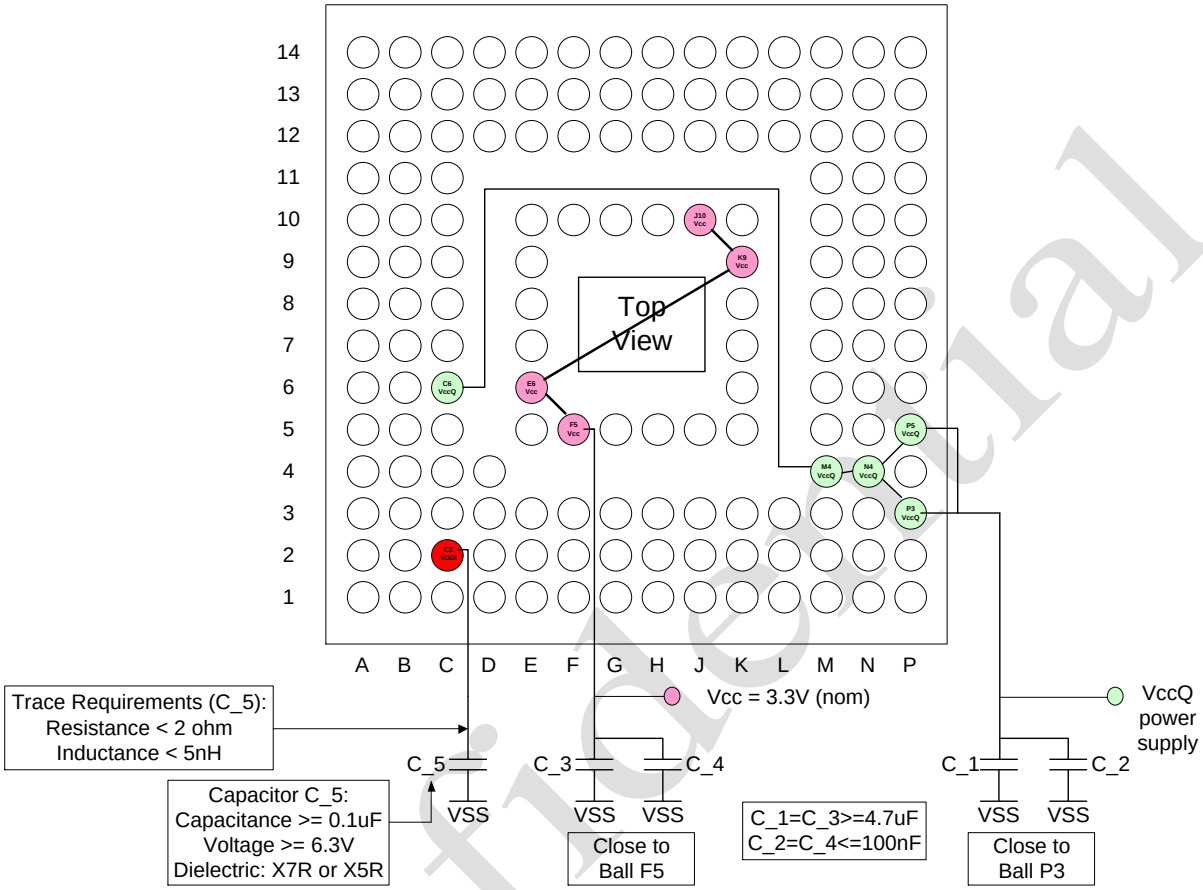

Figure 8 - Recommended Power Domain Connections

7. MARKING

First row: Simplified SanDisk Logo

Second row: Sales item P/N

Third row: Country of origin i.e. 'TAIWAN' or 'CHINA'

XI - Extended Temperature Industrial iNAND

Fourth row: Y - Last digit of year

WW - Work week

D - A day within the week.

MTLLXXX - Internal use

2D barcode: Stores the 10 digit unique ID information as reflected in the fourth row.

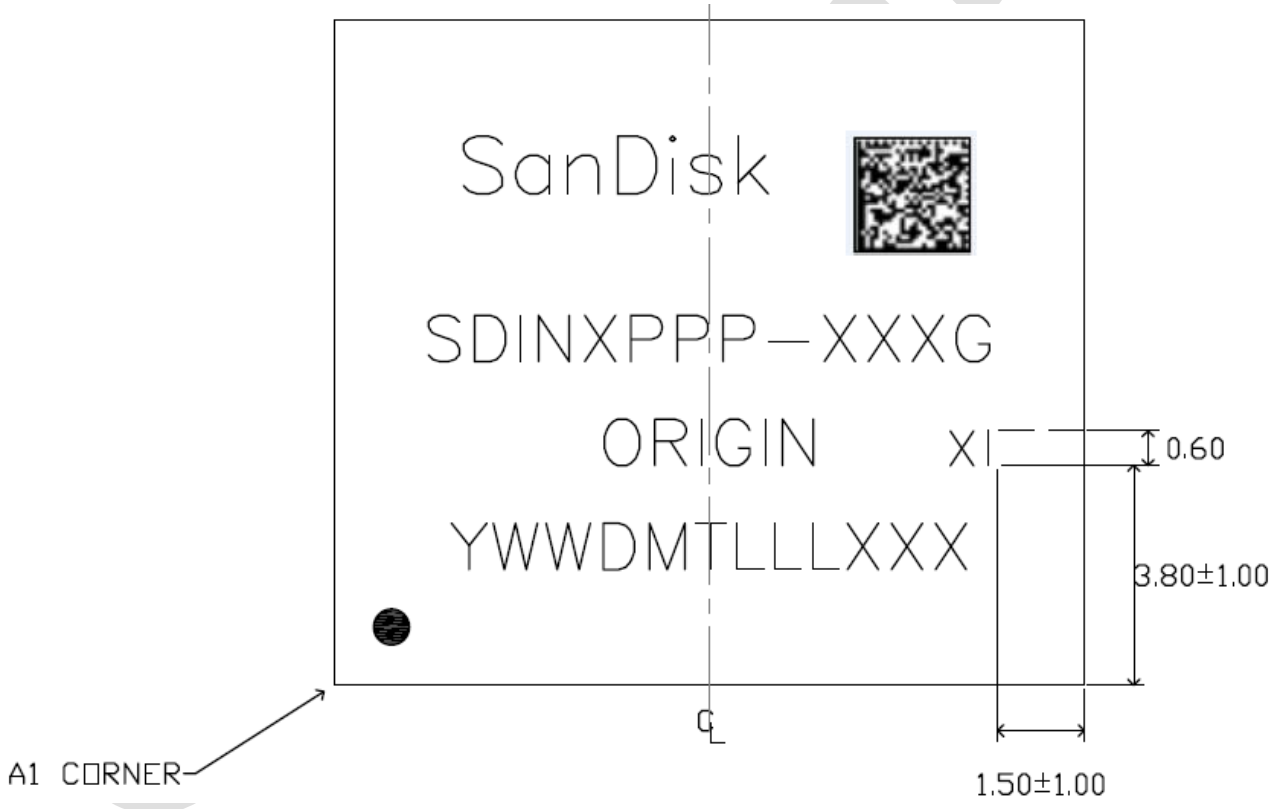

Figure 9 - Product marking

Note: XI only marked on extended temperature parts with –XI SKU suffix

8. ORDERING INFORMATION

Table 16 - Ordering Information (Industrial Wide Temperature Range)

Capacity	Technology	Part Number	Package
4GB	1Xnm MLC	SDIN8DE2-4G-I	11.5mmx13mmx1.0mm
8GB	1Xnm MLC	SDIN8DE1-8G-I	11.5mmx13mmx1.0mm
16GB	1Xnm MLC	SDIN8DE2-16G-I	11.5mmx13mmx1.0mm
32GB	1Xnm MLC	SDIN8DE4-32G-I	11.5mmx13mmx1.0mm
64GB	1Xnm MLC	SDIN8DE4-64G-I	11.5mmx13mmx1.2mm

Table 17 - Ordering Information (Industrial Extended Temperature Range)

Capacity	Technology	Part Number	Package
4GB	1Xnm MLC	SDIN8DE2-4G-XI	11.5mmx13mmx1.0mm
8GB	1Xnm MLC	SDIN8DE1-8G-XI	11.5mmx13mmx1.0mm
16GB	1Xnm MLC	SDIN8DE2-16G-XI	11.5mmx13mmx1.0mm
32GB	1Xnm MLC	SDIN8DE4-32G-XI	11.5mmx13mmx1.0mm
64GB	1Xnm MLC	SDIN8CE4-64G-XI	12mmx16mmx1.4mm

Note 1: Additional –T suffix on SKUs indicates parts are shipped in tape & reel packing.

Note 2: Optional customer code may be added at the end of the part number. For example, SDIN8DE1-8G-999XI.

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