AX88179 USB3.0 to Gigabit Demo Board Schematic

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AX88179 UA2/UA3
EEPROM
25MHz Crystal
USB/RJ-45 Connectors
Power Circuit
RT8075

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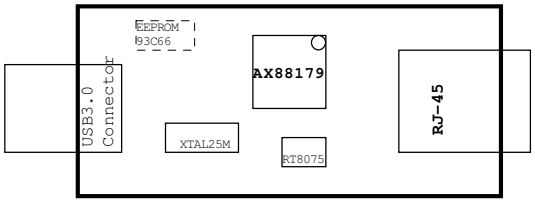
Revision History



5V to 3.3V&1.2V
Dual channel out
voltage

Note:
1.Please refer to AX88179 USB 3.0 to Gigabit Ethernet Application Design Note for more AX88179 PCB layout design notes.

2.Please deliver us your AX88179 schematic and PCB layout file for further review.

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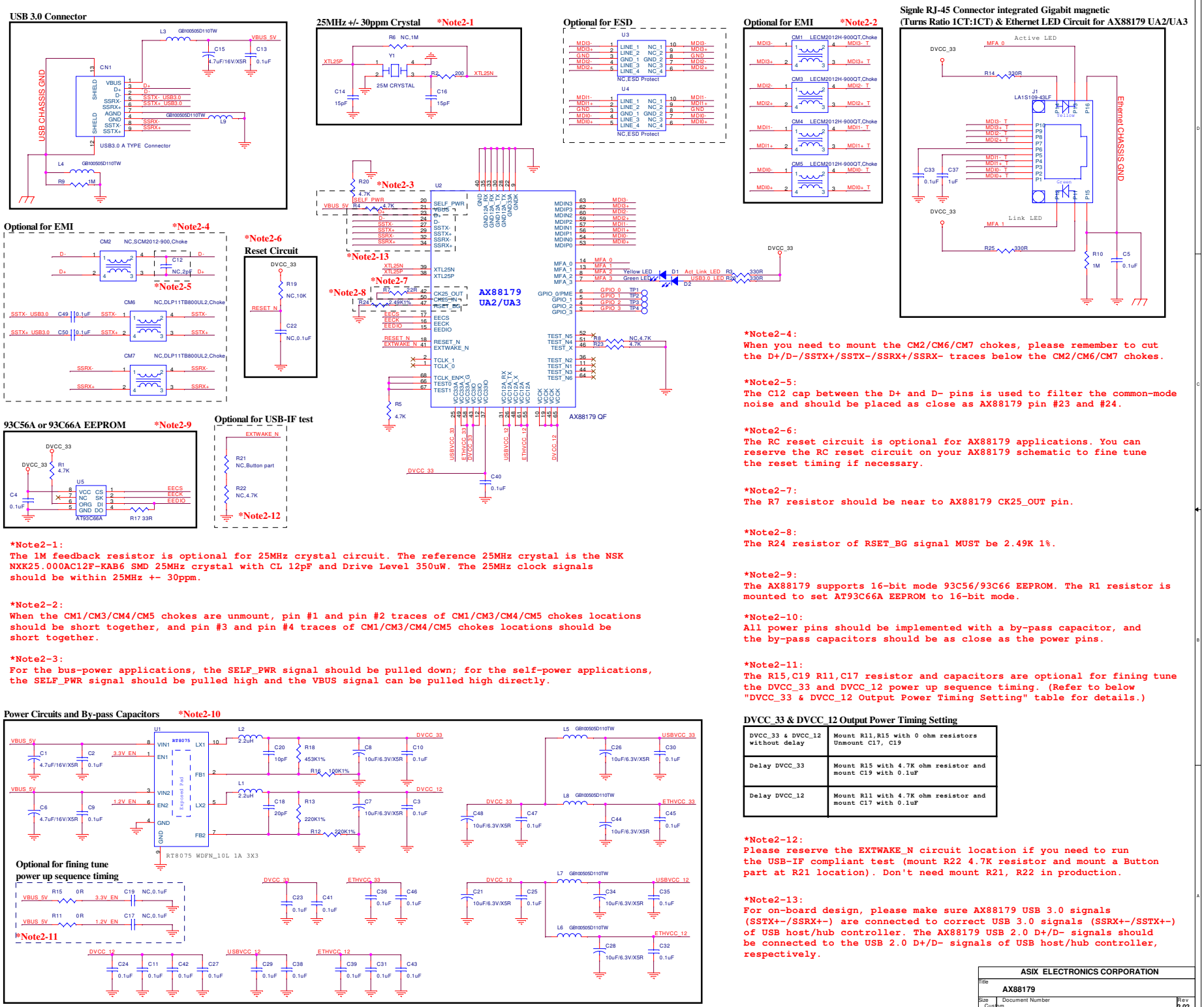

*Note2-1:
The 1M feedback resistor is optional for 25MHz crystal circuit. The reference 25MHz crystal is the NSK NXK25.000AC12F-KAB6 SMD 25MHz crystal with CL 12pF and Drive Level 350uW. The 25MHz clock signals should be within 25MHz +- 30ppm.

*Note2-2:
When the CM1/CM3/CM4/CM5 chokes are unmount, pin #1 and pin #2 traces of CM1/CM3/CM4/CM5 chokes locations should be short together, and pin #3 and pin #4 traces of CM1/CM3/CM4/CM5 chokes locations should be short together.

*Note2-3:
For the bus-power applications, the SELF_PWR signal should be pulled down; for the self-power applications, the SELF_PWR signal should be pulled high and the VBUS signal can be pulled high directly.

*Note2-4:
When you need to mount the CM2/CM6/CM7 chokes, please remember to cut the D+/D-/SSTX+/SSTX-/SSRX+/SSRX- traces below the CM2/CM6/CM7 chokes.

*Note2-5:
The C12 cap between the D+ and D- pins is used to filter the common-mode noise and should be placed as close as AX88179 pin #23 and #24.

*Note2-6:
The RC reset circuit is optional for AX88179 applications. You can reserve the RC reset circuit on your AX88179 schematic to fine tune the reset timing if necessary.

*Note2-7:
The R7 resistor should be near to AX88179 CK25_OUT pin.

*Note2-8:
The R24 resistor of RSET_BG signal MUST be 2.49K 1%.

*Note2-9:
The AX88179 supports 16-bit mode 93C56/93C66 EEPROM. The R1 resistor is mounted to set AT93C66A EEPROM to 16-bit mode.

*Note2-10:
All power pins should be implemented with a by-pass capacitor, and the by-pass capacitors should be as close as the power pins.

*Note2-11:
The R15,C19 R11,C17 resistor and capacitors are optional for fining tune the DVCC_33 and DVCC_12 power up sequence timing. (Refer to below "DVCC_33 & DVCC_12 Output Power Timing Setting" table for details.)

DVCC_33 & DVCC_12 Output Power Timing Setting

DVCC_33 & DVCC_12 without delay	Mount R11,R15 with 0 ohm resistors Unmount C17, C19
Delay DVCC_33	Mount R15 with 4.7K ohm resistor and mount C19 with 0.1uF
Delay DVCC_12	Mount R11 with 4.7K ohm resistor and mount C17 with 0.1uF

*Note2-12:
Please reserve the EXTWAKE_N circuit location if you need to run the USB-IF compliant test (mount R22 4.7K resistor and mount a Button part at R21 location). Don't need mount R21, R22 in production.

*Note2-13:
For on-board design, please make sure AX88179 USB 3.0 signals (SSTX+/-/SSRX+-) are connected to correct USB 3.0 signals (SSRX+-/SSTX+-) of USB host/hub controller. The AX88179 USB 2.0 D+/D- signals should be connected to the USB 2.0 D+/D- signals of USB host/hub controller, respectively.

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Revision History

Revision	Date	Comment
V1.00	2012/03/27	Initial release.
V1.10	2012/05/30	1.Modified for AX88179 UA2. (Mount R3,R19,R20,R22,R31,R34; Unmount R1,R2,R4,R18,R21,R30)
V1.11	2012/07/12	1.Added AX88179 UA3 string. 2.Updated the name of J1 to "LA1S109-43".
V2.00	2013/01/10	1.Updated for new AX88179 PCB v2.0 demo board. (Reset the reference numbers of all components) 2.Updated the Ethernet magnetic circuit. 3.Updated 25MHz crystal circuit. 4.Modified some descriptions in Note2-1. 5.Changed TEST_N4 R8 resistor to NC. 6.Added Note2-12.
V2.01	2013/05/29	1.Modified some descriptions in Note 2-3.
V2.02	2013/09/23	1.Corrected pin definition typo of CN1 and CM1~CM7.

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