AX88178A USB2.0 to Gigabit Reference Schematic

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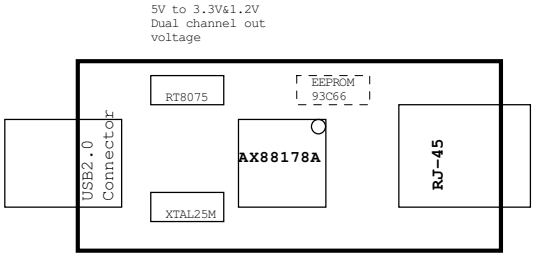

Note:
1.Please refer to AX88178A USB 2.0 to Gigabit Ethernet Application Design Note for more AX88178A PCB layout design notes.

2.Please deliver us your AX88178A schematic and PCB layout file for further review.

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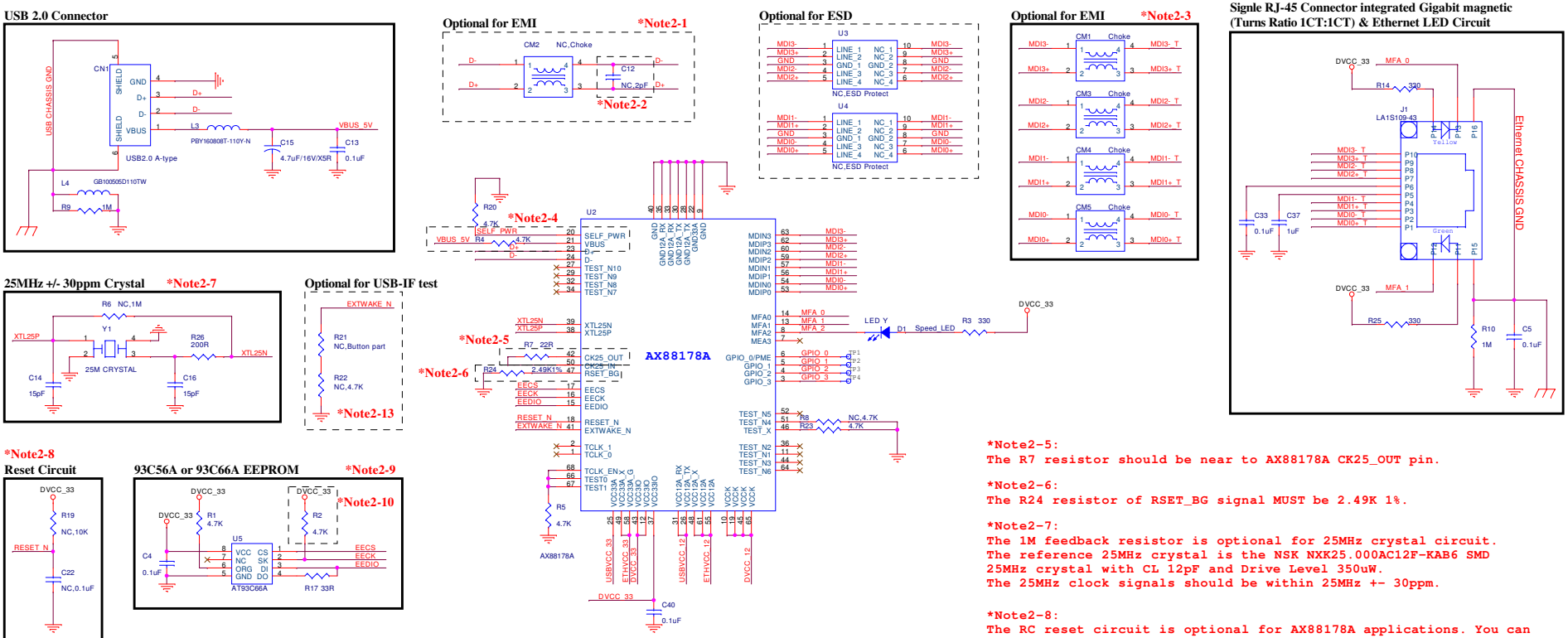

*Note2-1:
When you need to mount the CM2 choke, please remember to cut the D+/D- traces below the CM2 choke.

*Note2-2:
The C12 cap between the D+ and D- pins is used to filter the common-mode noise and should be placed as close as AX88178A pin #23 and #24.

*Note2-3:
When the CM1/CM3/CM4/CM5 chokes are unmount, pin #1 and pin #2 traces of CM1/CM3/CM4/CM5 chokes locations should be short together,and pin #3 and pin #4 traces of CM1/CM3/CM4/CM5 chokes locations should be short together.

*Note2-4:
For the bus-power applications, the SELF_PWR signal should be pulled down; for the self-power applications, the SELF_PWR signal should be pulled high and the VBUS signal can be pulled high directly.

*Note2-5:
The R7 resistor should be near to AX88178A CK25_OUT pin.

*Note2-6:
The R24 resistor of RSET_BG signal MUST be 2.49K 1%.

*Note2-7:
The 1M feedback resistor is optional for 25MHz crystal circuit.
The reference 25MHz crystal is the NSK NXK25.000AC12F-KAB6 SMD 25MHz crystal with CL 12pF and Drive Level 350uW.
The 25MHz clock signals should be within 25MHz +- 30ppm.

*Note2-8:
The RC reset circuit is optional for AX88178A applications. You can reserve the RC reset circuit on your AX88178A schematic to fine tune the reset timing if necessary.

*Note2-9:
The AX88178A supports 16-bit mode 93C56/93C66 EEPROM. The R1 resistor is mounted to set the AT93C66A EEPROM to 16-bit mode.

*Note2-10:
The AX88178A EECK signal MUST be pulled up through 4.7K resistor (R2) for normal operation.

*Note2-11:
All power pins should be implemented with a by-pass capacitor, and the by-pass capacitors should be as close as the power pins.

*Note2-12:
The R11,C17 R15,C19 resistors and capacitors are optional for fining tune the DVCC_33 and DVCC_12 power up sequence timing. (Refer to below "DVCC_33 & DVCC_12 Output Power Timing Setting" table for details.)

DVCC_33 & DVCC_12 Output Power Timing Setting

DVCC_33 & DVCC_12 without delay	Mount R11,R15 with 0 ohm resistors Unmount C17, C19
Delay DVCC_33	Mount R15 with 4.7K ohm resistor and mount C19 with 0.1uF
Delay DVCC_12	Mount R11 with 4.7K ohm resistor and mount C17 with 0.1uF

*Note2-13:
Please reserve the EXTWAKE_N circuit location if you need to run the USB-IF compliant test (mount R22 4.7K resistor and mount a Button part at R21 location). Don't need mount R21, R22 in production.

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Revision History

Revision	Date	Comment
V0.10	2012/07/06	Preliminary release.
V1.00	2012/07/23	1.Corrected the name of J1 to "LA1S109-43".
V1.10	2013/01/08	1.Modified 25MHz crystal reference circuit. 2.Modified some descriptions in Note2-7. 3.Changed TEST_N4 R8 resistor to NC. 4.Added Note2-13.
V1.11	2013/02/05	1.Modified some descriptions in Note2-2, Note2-4, Note2-13.
V1.12	2013/05/29	1.Correct U2 Pin #26 and #31 pin names typos. 2.Modified some descriptions in Note 2-4.

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