1. 1. What is the priority resolver in 8259A?

The priority resolver in 8259A determines which interrupt request has the highest priority when multiple interrupts occur simultaneously. It ensures that the highest priority device gets serviced first.

2. 2. What are the steps involved in Interrupt Driven I/O data transfer?

The CPU enables the device interrupt, performs other tasks, receives an interrupt request, executes the ISR, transfers data, and returns to the main program.

3. 3. What is the difference between maskable and non-maskable interrupts?

Maskable interrupts can be disabled by software using the interrupt flag, while non-maskable interrupts (NMI) cannot be disabled and have the highest priority.

4. 4. What is an interrupt?

An interrupt is a signal sent to the CPU to temporarily stop the current program and execute a special service routine to handle an event.

5. 5. What is the function of the DMA Request (DREQ) and DMA Acknowledge (DACK) signals?

DREQ is sent by a peripheral to request data transfer via DMA, and DACK is sent by the DMA controller to acknowledge the request and start the transfer.

6. 6. What is the function of the 8237A DMA controller?

The 8237A DMA controller transfers data directly between I/O devices and memory without involving the CPU, improving data transfer speed and efficiency.

7. 7. What are the steps involved in programmed I/O data transfer?

The CPU checks device status, sends a command to the device, transfers data, and repeats the process until the operation is complete.

8. 8. What are the steps involved in Interrupt Driven I/O data transfer?

The device sends an interrupt request, the CPU acknowledges it, executes the ISR, performs the data transfer, and resumes the main program.

9. 9. Draw the block diagram of an interrupt-driven I/O system and explain its operation.

The system includes CPU, interrupt controller, and I/O devices. The device generates an interrupt, CPU acknowledges, executes ISR, and resumes the program. (Diagram to be drawn).

10. 10. What is the purpose of the INT and INTA signals?

INT is the interrupt request signal sent to the CPU by peripherals, while INTA is the interrupt acknowledge signal sent by the CPU to confirm receipt.

11. 11. State the purpose of priority resolver in 82C59A.

It assigns priorities among multiple interrupt requests and selects the highest priority interrupt for servicing by the CPU.

12. 12. Differentiate between Programmed I/O and Interrupt driven I/O.

In programmed I/O, the CPU continuously checks device status. In interrupt-driven I/O, the device interrupts the CPU only when ready, reducing CPU idle time.

13. 13. What is the role of the CPU in programmed I/O?

The CPU actively monitors the device status, sends commands, and transfers data between the device and memory without any hardware automation.

14. 14. What are the advantages of using DMA controller over programmed I/O or interrupt driven I/O?

DMA allows direct data transfer between memory and devices without CPU involvement, reducing overhead and increasing data transfer speed.

15. 15. Analyze how Intel 8237A DMA controller reduces CPU overhead.

The 8237A handles data transfers independently, freeing the CPU to perform other operations instead of managing I/O transfers.

16. 16. Explain control word register in the Intel 8255A.

The control word register configures the operation modes of ports A, B, and C in the 8255A for input/output or handshake modes.

17. 17. Illustrate with a block diagram how Direct Memory Access (DMA) improves system throughput.

DMA improves throughput by transferring data directly between I/O and memory, bypassing the CPU. (Diagram to be drawn).

18. 18. Analyze how the 8255A Programmable Peripheral Interface (PPI) can be used to interface with a keyboard and display with diagram.

8255A ports can be configured to receive input from a keyboard and send output to a display. It provides flexible data communication. (Diagram to be drawn).

19. 19. Explain how an I/O module acts as an interface between the CPU and external devices with diagram.

The I/O module manages data exchange, control, and status signals between CPU and peripherals, ensuring synchronization. (Diagram to be drawn).

20. 20. Explain architecture diagram of 8255A.

The 8255A architecture includes three 8-bit ports (A, B, C), a control unit, and a data bus buffer for programmable I/O operations. (Diagram to be drawn).