CHI-HUNG (JOE) WANG

Cedar Park, TX 78613 | 408-786-7596 | princechopin@gmail.com | linkedin.com/in/chi-hung-wang-98334328

Software Architect

A proven problem solver, game changer, innovator and leader in software industry. Strong desire and quickness to learn. A teammate with a can-do attitude, high energy, detail-oriented. Stellar communication skills. Ability and flexibility to work and communicate effectively in a multi-national, multi-time-zone corporate environment. Accomplished five leading software products for two major consolidated IC design automation companies; part of the reasons led into the top three acquisitions in design automation history. Core competencies include:

Data Structures | Computer Algorithms | Object-Oriented Designs| Project Management | Numerical Analysis | Design Automation Software| Computational Software | Business Intelligence | Data Visualization | Cloud Computing Software Designs | Big Data | Graph/AI/ML Algorithms | Problem Solving

TECHNICAL SKILLS

- Front-end |back-end | full-stack: Java | JavaScript | CSS | React | Spring Rest | Spring Boot | Redux | Redux-saga | node | HTML | Json | XML | Git/GitHub | IntelliJ | Gradle | Electron | Selenium | Jasmine | Enzyme | Junit | Docker | Jsoup | CI/CD | Agile under Scrum
- C/C++ | YACC | Python(NumPy, Tensorflow, PyTorch) | Ruby | Matlab | CUDA | Tcl | Skill | csh | bash | perl | awk | boost | Cmake | Perforce | Coverity | Purify | valgrind | asan | ccolab/rbt/code review
- Windows | Mac OS | Linux | Ubuntu
- Internet/network : Client | Server | IPC | TCP/IP | Micro services | REST api | HTTP | HTTPS| gRPC
- Distributed System/Parallel/HPC: Master-slave | LSF | multi-threading | fork | concurrent | SIMD | CUDA | asynchronous | embedded system
- Automation Algorithms: Constrained pre-conditioned large sparse matrix non-linear solver | Computation Geometry | Graph | Poisson equation| Simulated Annealing | static timing | AST/BDD | Place | Route | Floorplan | DRC/LVS | Synthesis | ML solvers, logistic regressions, CNN, RNN, GAN, LLM
- Cloud: SQL/non-SQL | AWS | Kubernetes | Splunk | Cloud Connectors | OAuth
- Data Visualization: Tableau Desktop | Prep builder | Tableau Cloud
- Layout Editor/GUI: QT | QML | OpenGL | OpenCV | TK | MVC | MVVM | widget applications | plugins | undo/redo | push/shove
- IC design files: LEF | DEF | EDIF | SDF | SPEF | CDL | Spice | YAML | Verilog | pdk/ipdk
- EDA logic/physical databases: Cadence CDBA, OpenAccess, Magma Titan, Talus Bedrock, Synopsys Milkyway, Innovus DB, Siemens Parasolid, ACIS modeling, GDSII
- EDA SOC tools/flows: Cadence Genus, Innovus, Quantus, Voltus, Sigrity, Modus, Tempus, Conformal, Virtuoso ADE VXL | Synopsys design compiler, prime time, ICC2, Custom Compiler, Star RC, Mentor Calibre, Scan Chain, JTAG, BSRG, BIST, ATPG

EXPERIENCE

Cadence Design Systems, Inc., Austin, TX **September 2022 – June 2024**

Software Architect

Worked on the latest Innovus SOC distributed optimization product, which uses multi-threading / multi-machine / master-slave architectures to build a flow that leverages all features in Innovus to optimize SOC designs to satisfy timing / power / area / density / congestion constraints.

- Facilitated debug / analyze / identify issues in complex flows including floor planning, partition, placement, routing, extraction, static timing analysis, cts, buffer insertion, flip-flop merging, density, power analysis, inter-process communication, primarily in TCL / C++ / csh / lsf on Linux grids.
- Learned and fixed key bugs / flow-related issues / performance bottlenecks / inconsistent timing / random crashes / hang-ups that few others can identify. Improved several key components' performances by more than 30%, reduced the disk space usage by 90%.

Salesforce, inc., (Tableau) Austin, TX **September 2019 – September 2022**
Lead Software Engineer,
Worked on Tableau data prep, security-and-sharing, cloud connector authentication products, applied modern front-end / full-stack technologies in big data / visualization flow using Java / React-JavaScript / TypeScript / Redux / Rest on Electron / IntelliJ platforms.

- Reduced assigned defects / stories by 100%, created new key features that cover the entire flow and significantly simplified usage model, welcomed by the customers right away. Quickly mastered modern software development skills in client / server / cloud environment.
- Implemented practical features like auto-updater which can automatically guide users to install the most up-to-date releases in multi-language platforms in a SAAS / cloud environment in a timely manner.
- Masterful for various software testing / regressions / unit test methodologies like canary tests, Selenium, JUnit, Jsoup; heavily involved in AWS kubernetes / docker and other Cloud platforms.

Synopsys Design, Inc., Austin, TX **April 2007 – July 2019**
R&D engineer, Senior Staff, Architect (Magma Design, acquired by Synopsys)

- Accomplished the Placement Assistant product in Custom Compiler by integrating tools / features / flows from 4 leading companies using state-of-art coding / algorithmic and data flow skills; coded in C++ / Python / YAML / S-expression / TCL / QT to resolve modern placement problems for 7 to 10 nm technologies. Went through 10+ release cycles.
- Continued to enhance the AVP product that I authored in Magma, evolved it into the core engine for Placement Assistant. Made it adapt to the Helix / Custom Compiler hierarchical design flow. Used threading technology | distributed computing | genetic algorithms to speed the placer by a magnitude of 10X and output multiple optimized solutions in parallel.
- Led teams in India, China and Taiwan to fix bugs and implement sub-features.
- Started from scratch to accomplish a new custom placement platform for Magma Design. Overcame major deficiencies by competitors.
- Invented new ***force-driven/hierarchical sequence pair*** packing algorithms, using mathematical constrained formulas, machine learning techniques, Poisson equations and simulated annealing to simultaneously optimize connectivity and resolve timing/DRC/incremental placement issues with topological constraints for leaf-level devices, rectilinear modules, CMOS PNStacks, standard cells, memory, I/O pins with complex custom/geometrical rules.
- Invented interactive Constraint-aware editing protocol / core to tightly work with layout editor through QT / TCL / GUI commands / callbacks, reduce overall coding work by more than 80%.

ADDITIONAL RELEVANT EXPERIENCE

Cadence Design Systems, Inc., San Jose, CA **August 1995 – April 2007**
Architect | Senior Software Engineer, (Cooper and Chyan Technology, acquired by Cadence)
The sole author for Virtuoso VXL/VCP product, beat 5 internal/external teams and become the Custom Placer for Virtuoso. Mentored teams in China/India to implement sub-features and fixing bugs.

Synopsys, Inc., Mountain View, CA **August 1992 – April 1995**
Senior R&D Engineer,
Initiated the first Synopsys physical floorplanning/placement tool using fast numerical placer, integrated it with Design Compiler/Prime Time.

- Authored the first fixed-die detailed routing tool for ArcSys(acquired by Synopsys through Avant!), achieved an area-based dynamic/incremental DRC checking system in ArcGate from scratch, which ran 100x faster than the traditional DRC/LVS checking.
- Invented dynamic rip-and-reroute, window-based algorithms to handle routing forests, track connectivity information and improve routing patterns/fix antenna effects in the most efficient ways.

LSI Logic Corp., Milpitas, CA **August 1990 – April 1992**
R&D Engineer,

- Obtained a patent for a Metal Utilization package to solve lonely wire problems in DFM.
- Developed various utilities for IC layout designers, like boundary scan ring placement, placement legalizer in C++; rectilinear hierarchical functional shape editing for top-level floorplans in C++/QT.

EDUCATION

Master of Science, MS, Computer Engineering, Syracuse University, New York,
Member of Tau-Beta-Pi, honor society for international students.
Master Projects:

Using perfect shuffle to parallelize FFT on a simulated scalable SIMD machine in C/Unix;
Automatic PLA synthesis/folding/routing system in C/Unix/Mentor GDT;
Automated laryngeal recognition system using neural network in C/Unix;
Lisp machine architecture designs/simulations in C/Unix/Mentor GDT.

Bachelor of Science, BS, Computer Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan,
Projects/Interns:

Embedded system controlled large scaled Chinese LED display board; Military personnel/Golf player database management system in COBOL/JCL/Dbase II; Assembler/loader/simulator for Pseudo stack machine; Commercial invoice/inventory control system in Dbase II.

PATENTS/Certificates

Patent Number: 5818729 **Date Issued:** October 6, 1998
Title of Patent: Method and system for placing cells using quadratic placement and a spanning tree model
Patent Number: 5654897 **Date Issued:** August 5, 1997
Title of Patent: Method and structure for improving patterning design for processing

Salesforce Amazon AWS EKS certificate, July 2022
Cadence SOC design flow certificate, Dec 2022
Cadence AI in EDA certificate, Sep 2023
Coursera ML certificates: Neural Networks and Deep Learning, May 2024; Improving Deep Neural Networks: Hyperparameter Tuning, Regularization and Optimization, May 2024; Structuring Machine Learning Projects, May 2024; Convolutional Neural Networks, June 2024; Sequence Models, June 2024