

CHI-HUNG (JOE) WANG

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Software Architect

Proven problem solver, game changer, innovator and leader in software industry and with a strong desire and quickness to learn. Dedicated teammate with can-do attitude, high energy, detail-oriented. Ability and flexibility to work and communicate effectively in a multi-national, multi-time-zone corporate environment. Accomplished five leading software products for two major consolidated IC design automation companies, efforts that resulted in top three acquisitions in design automation history.

Core Competencies:

Data Structures | Computer Algorithms | Object-Oriented Designs | Project Management | Numerical Analysis | Design Automation Software | Computational Software | Business Intelligence | Data Visualization | Cloud Computing Software Designs | Big Data | Graph/AI/ML Algorithms

TECHNICAL SKILLS

- Front-end | back-end | full-stack: Java | JavaScript | TypeScript | node.js | CSS | React | Spring Rest | Spring Boot | Redux | Redux-saga | C# .NET | HTML | Json | XML | Git/GitHub | IntelliJ | vscode | Gradle | Electron | Selenium | Jasmine | Enzyme | Junit | Docker | Jsoup | CI/CD | Agile under Scrum
- C/C++ | YACC | Python(NumPy, Tensorflow, PyTorch) | Ruby | Matlab | CUDA | Tcl | Skill | csh | bash | perl | awk | boost | Cmake | Perforce | Coverity | Purify | valgrind | asan | ccolab/rbt/code review
- Windows | Mac OS | Linux | Ubuntu
- Internet/network : Client | Server | IPC | TCP/IP | Micro services | REST api | HTTP | HTTPS | gRPC
- Distributed System/Parallel/HPC: Master-slave | LSF | multi-threading | fork | concurrent | SIMD | CUDA | asynchronous | embedded system
- Automation Algorithms: Constrained pre-conditioned large sparse matrix non-linear solver | Computation Geometry | Graph | Poisson equation | Simulated Annealing | static timing | AST/BDD | Place | Route | Floorplan | DRC/LVS | Synthesis | ML solvers, logistic regressions, CNN, RNN, GAN, LLM
- Cloud: SQL/non-SQL | AWS | Kubernetes | Splunk | Cloud Connectors | OAuth
- Data Visualization: Tableau Desktop | Prep builder | Tableau Cloud
- Layout Editor/GUI: QT | QML | OpenGL | OpenCV | TK | MVC | MVVM | widget applications | plugins | undo/redo | push/shove
- IC design files: LEF | DEF | EDIF | SDF | SPEF | CDL | Spice | YAML | Verilog | pdk/ipdk
- EDA logic/physical databases: Cadence CDBA, OpenAccess, Magma Titan, Talus Bedrock, Synopsys Milkyway, Innovus DB, Siemens Parasolid, ACIS modeling, GDSII
- EDA SOC tools/flows: Cadence Genus, Innovus, Quantus, Voltus, Sigrity, Modus, Tempus, Conformal, Virtuoso ADE VXL | Synopsys design compiler, prime time, ICC2, Custom Compiler, Star RC, Mentor Calibre, Scan Chain, JTAG, BSRG, BIST, ATPG

CAREER EXPERIENCE

Cadence Design Systems, Inc., Austin, TX

September 2022 – July 2024

Software Architect

Worked on latest Innovus SOC distributed optimization product, using multi-threading / multi-machine / master-slave architectures to build flow that leverages all features in Innovus to optimize SOC designs to satisfy timing / power / area / density / congestion constraints.

- Facilitated debug / analyze / identify issues in complex flows including floor planning, partition, placement, routing, extraction, static timing analysis, CTS, buffer insertion, flip-flop merging, density, power analysis, inter-process communication, primarily in TCL / C++ / CSH / LSF on Linux grids.
- Learned and fixed key bugs / flow-related issues / performance bottlenecks / inconsistent timing / random crashes / hang-ups rarely identified.
- Improved several key components' performances by more than 30%, reduced disk space usage by 90%.

Salesforce, Inc., (Tableau) Austin, TX**September 2019 – September 2022****Lead Software Engineer,**

Worked on Tableau data prep, security-and-sharing, cloud connector authentication products, applied modern front-end / full-stack technologies in big data / visualization flow using Java / React-JavaScript / TypeScript / Redux / Rest on Electron / IntelliJ platforms.

- Reduced assigned defects / stories by 100%, created new key features that cover entire flow and significantly simplified usage model, welcomed by customers right away.
- Implemented practical features like auto-updater which can automatically guide users to install most up-to-date releases in multi-language platforms in a SAAS / cloud environment.
- Gained wealth of knowledge in various software testing, regressions, and unit test methodologies like canary tests, Selenium, JUnit, Jsoup; heavily involved in AWS Kubernetes / docker and other Cloud platforms.

Synopsys Design, Inc., Austin, TX**April 2007 – July 2019****R&D engineer, Senior Staff, Architect (Magma Design, acquired by Synopsys)**

- Accomplished placement assistant product in custom compiler by integrating tools / features / flows from four leading companies using state-of-art coding / algorithmic and data flow skills; coded in C++ / Python / YAML / S-expression / TCL / QT to resolve modern placement problems for 7 to 10 nm technologies. Went through 10+ release cycles.
- Continued to enhance the AVP product that I authored in Magma, evolved it into the core engine for placement assistant. Made it adapt to the Helix / Custom Compiler hierarchical design flow. Used threading technology | distributed computing | genetic algorithms to speed the placer by magnitude of 10X and output multiple optimized solutions in parallel.
- Led teams in India, China and Taiwan to fix bugs and implement sub-features.
- Started from scratch to accomplish new custom placement platform for Magma Design. Overcame major deficiencies by competitors.
- Invented new force-driven/hierarchical sequence pair packing algorithms, using mathematical constrained formulas, machine learning techniques, Poisson equations and simulated annealing to simultaneously optimize connectivity and resolve timing/DRC/incremental placement issues with topological constraints for leaf-level devices, rectilinear modules, CMOS PNStacks, standard cells, memory, I/O pins with complex custom/geometrical rules.
- Invented interactive Constraint-aware editing protocol / core to tightly work with layout editor through QT / TCL / GUI commands / callbacks, reduce overall coding work by more than 80%.

ADDITIONAL RELEVANT EXPERIENCE

Architect | Senior Software Engineer | Cooper and Chyan Technology, acquired by Cadence | Cadence Design Systems, Inc. | San Jose, CA (1995 – 2007)

Senior R&D Engineer | Synopsys, Inc. | Mountain View, CA (1992 – 1995)

EDUCATION

Master of Science in Computer Engineering | Syracuse University | New York

Bachelor of Science in Computer Engineering | National Chiao-Tung University | Hsin-Chu, Taiwan

INDUSTRY CREDENTIALS

[Sequence Models](#), June 2024

[Convolutional Neural Networks](#), June 2024

[Machine Learning](#), June 2024

[Neural Networks and Deep Learning](#), May 2024

[Improving Deep Neural Networks: Hyperparameter Tuning, Regularization and Optimization](#), May 2024

[Structuring Machine Learning Projects](#), May 2024

Cadence AI in EDA certificate, Sep 2023

Cadence SOC design flow certificate, Dec 2022

Salesforce Amazon AWS EKS certificate, July 2022

<https://github.com/princechopin>

PATENTS

Patent Number: 5818729 **Date Issued:** October 6, 1998

Title of Patent: Method and system for placing cells using quadratic placement and a spanning tree model

Patent Number: 5654897 **Date Issued:** August 5, 1997

Title of Patent: Method and structure for improving patterning design for processing