OS

ID : 23DCE043 CE 361 CIE-1

(1) Program counter (PC)

(2)

	RISC	CISC
→	~~complex~~ simple	~~simple~~ complex
→	single-cycle	multicycle
→	Longer	smaller
⇒		

⇒ CISC ~~saves~~ memory
RISC favors speed

(3) If we increase word size then instruction length will also increase

(4) If we have fewer pipeline stages in instruction execution then it will reduce clock speed.

(5) Stack Pointer
Base Pointer

(6) Incorrect answer will be produced.

(7) Indirect Addressing leads to more flexible code but higher overhead.

(8) Cost and Increased access time

(9) Indexed addressing mode

(10) Branch control instruction

(11) Arithmatic logic instruction

(12) Addition

(13) Size 16 bits
$2^4 = 16$

(14) Increase Power consumption

(15) must be fetched in multiple cycle