

# AVM 864 - RF Integrated Circuits

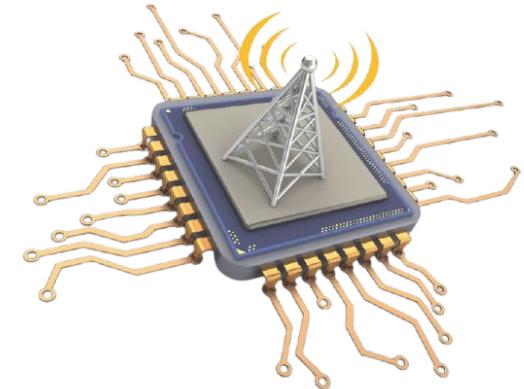
## Course Project



Design of Low-Power Noise cancelling  
LNA for LoRa IoT application

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# Introduction

# LoRa :



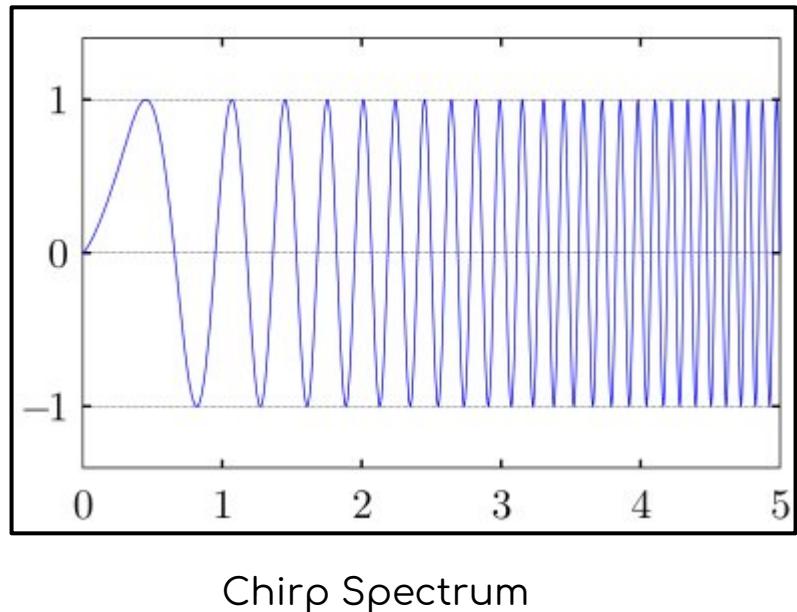
- Used for long range communication majorly between the sensor nodes of a Wireless Sensor Network
- This forces some major requirements on the receiver design architecture i.e
  - Low Power Consumption
  - High range and thus forcing higher sensitivity

Region	Frequency (MHz)
Asia	433
Europe, Russia, India, Africa (parts)	863-870
US	902-928

Region	Frequency (MHz)
Australia	915-928
Canada	779-787
China	779-787, 470-510

# LoRa :

- LoRa (short for long range) is a spread spectrum modulation technique derived from chirp spread spectrum (CSS) technology.
- The resulting bit rate will vary between 300 bps and 37.5kbps.
- Here we are using Frequency range with minimum and maximum frequency defined and in between frequency defines different Symbols.
- We are using 860MHz band for our project.



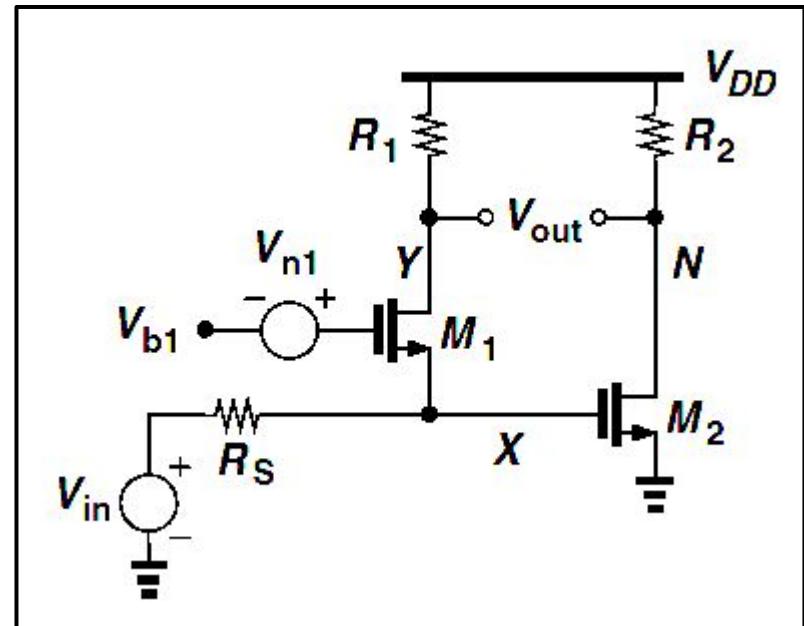
# Literature Review

# Noise cancellation :CG topology

- The CG stage realizes wideband input impedance matching and gain, while the CS stage realizes an anti-phase output signal which is responsible for noise cancelling.
- It cancels the noise of the CG transistor in order to obtain a noise figure (NF) close to or lower than 3 dB.

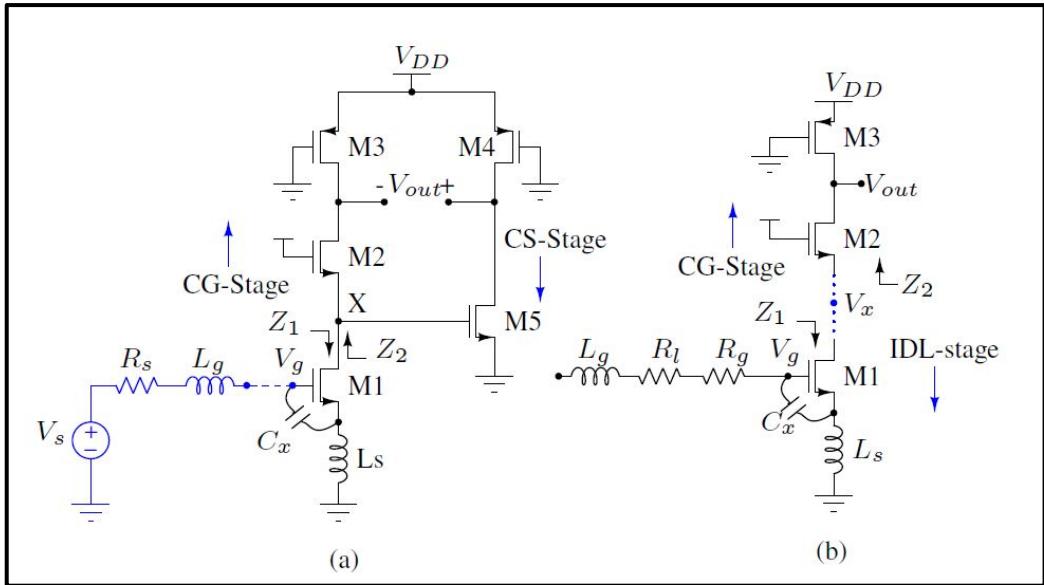
Gain matching :

$$g_{m1} \times R_1 = g_{m2} \times R_2$$



# Noise cancellation :CS topology

- Here we can see the same concept of noise cancellation in CS LNA also.
- $Z_1$  and  $Z_2$ , matched at the input resonant frequency to cancel noise contributed by the cascoding transistor,  $M_2$ .



Gain matching :

$$g_{m2} \times \left( \frac{1}{g_{m3}} \right) = g_{m5} \times \left( \frac{1}{g_{m4}} \right)$$

# CS with Inductive degeneration LNA

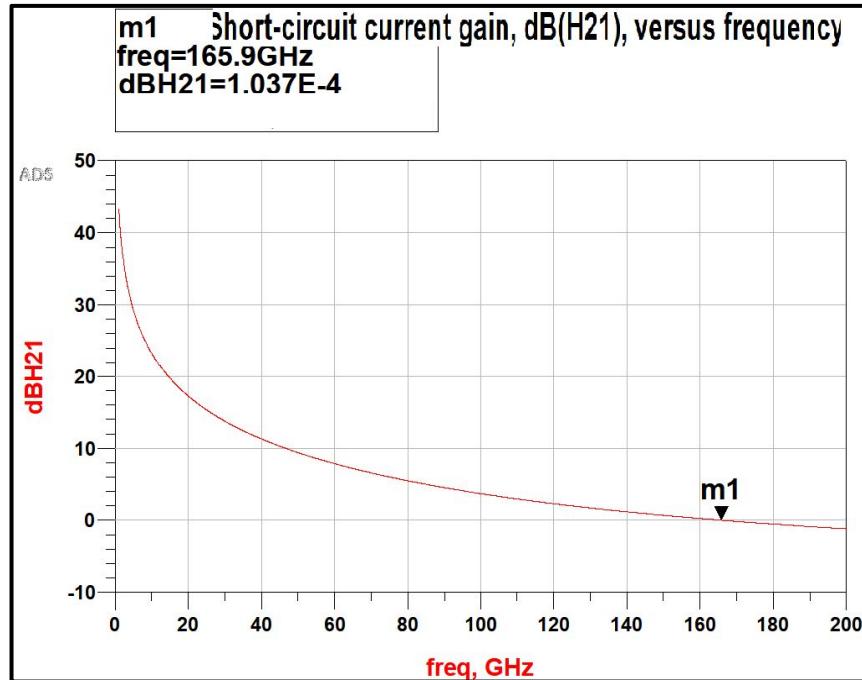
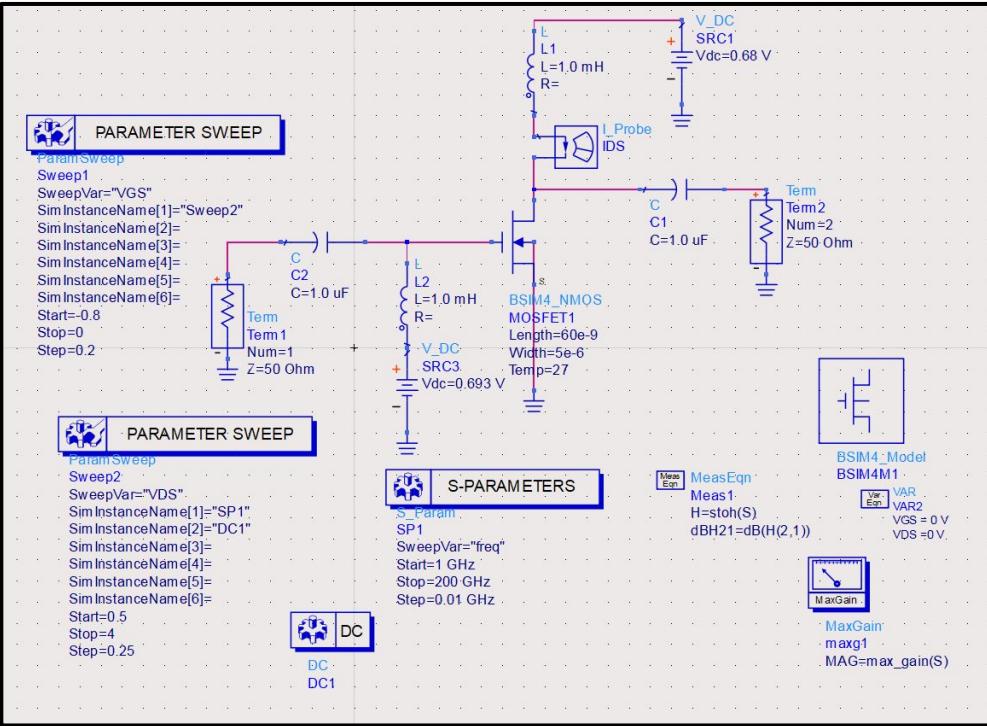
## Governing Equations:

$$\frac{1}{(L_G + L_1)(C_{GS1} + C_{pad})} = \omega_0^2$$

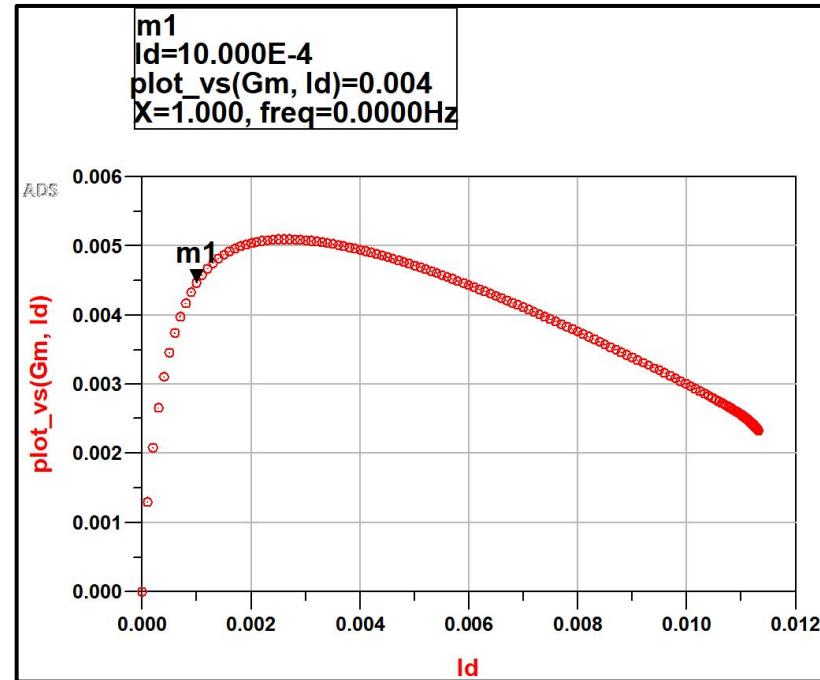
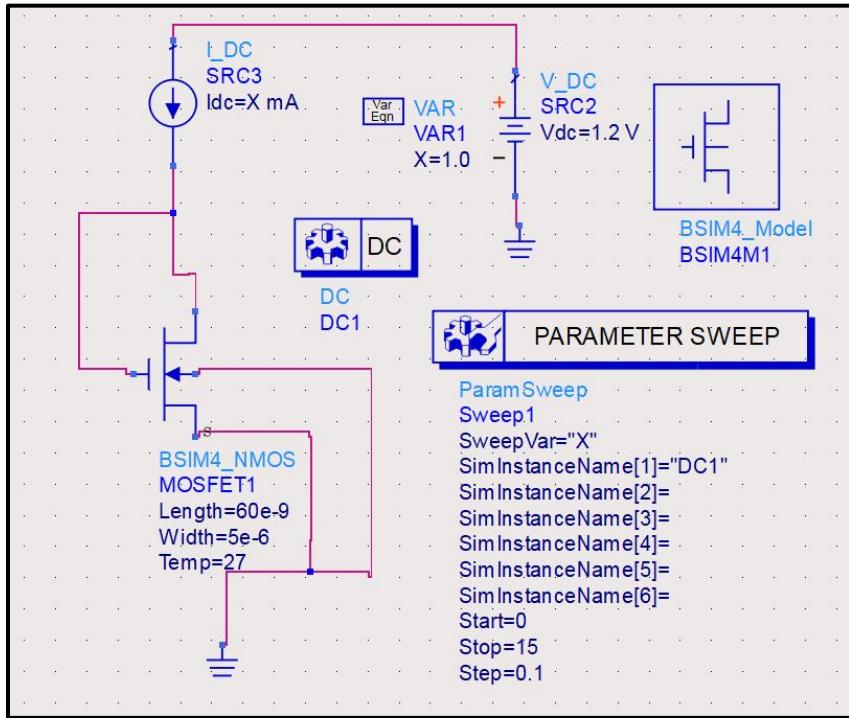
$$\left( \frac{C_{GS1}}{C_{GS1} + C_{pad}} \right)^2 L_1 \omega_T = R_S.$$

$$\omega_T \approx \frac{g_m}{C_{gs}}$$

# Transition frequency



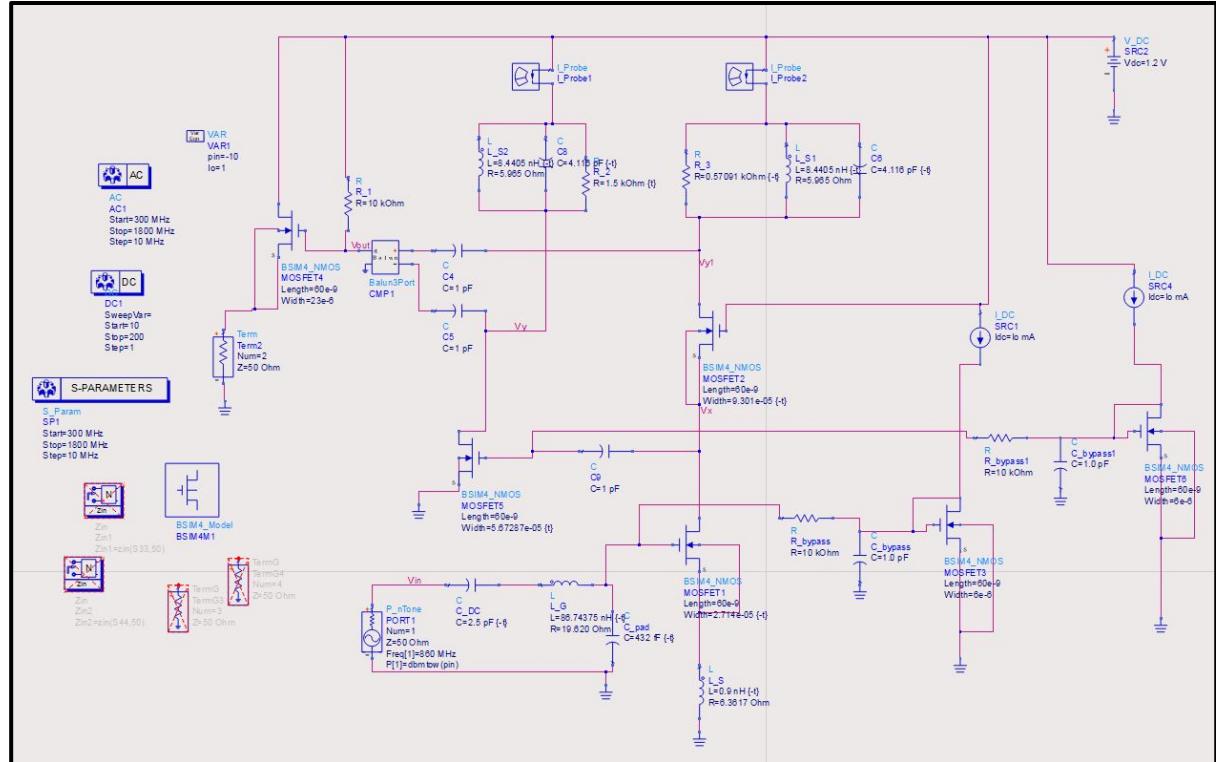
# DC operating point



# Circuit with Noise Cancellation

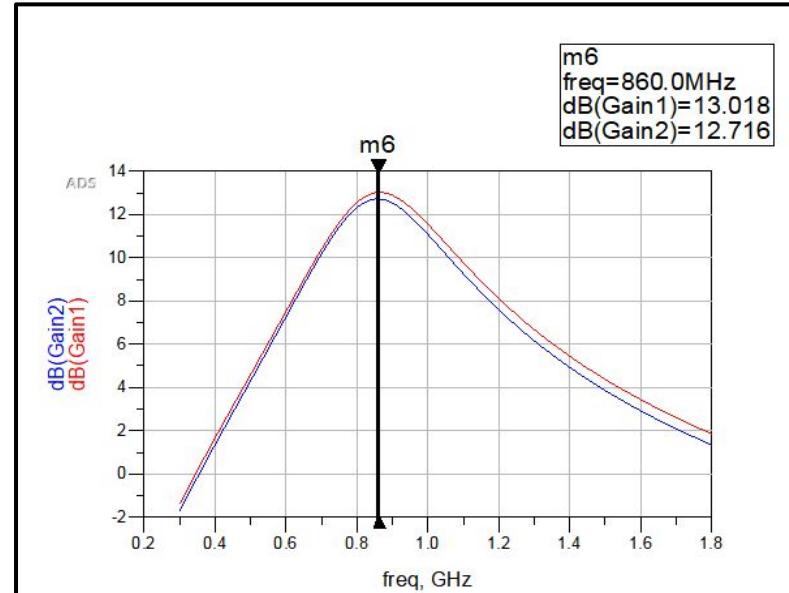
CS circuit with  
Inductive degeneration

Here we used  
impedance matching  
for proper noise  
cancellation



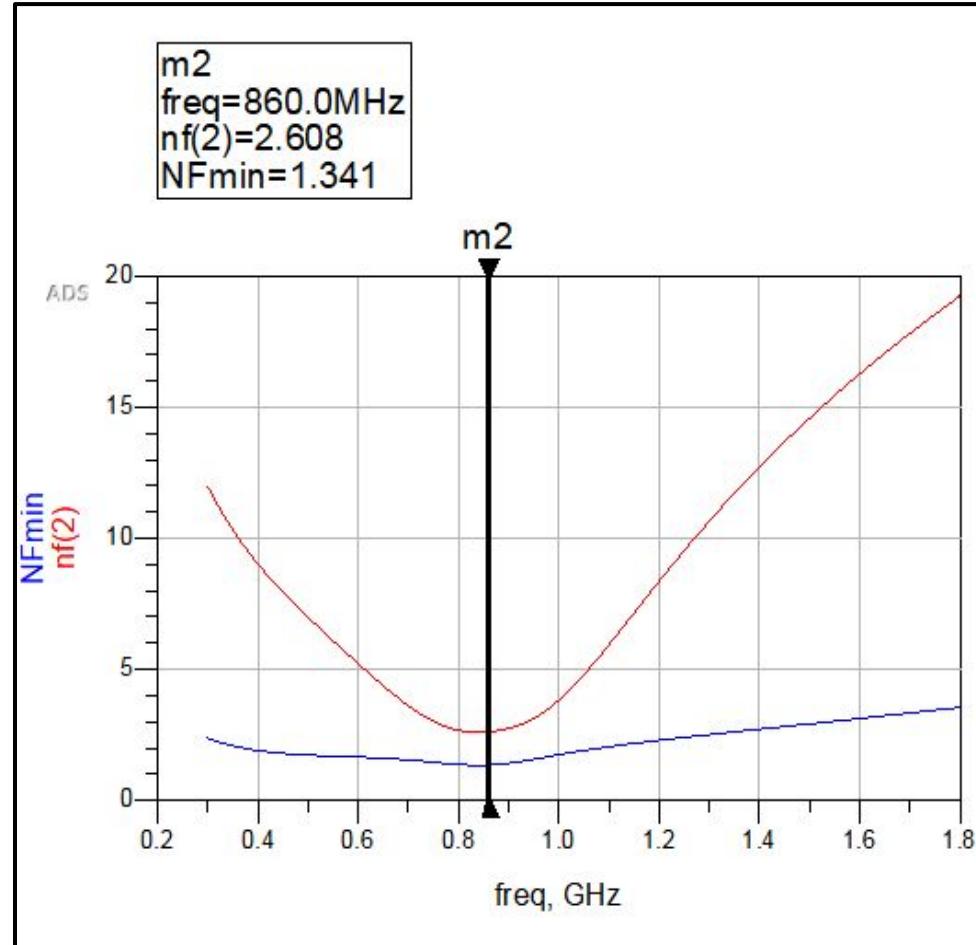
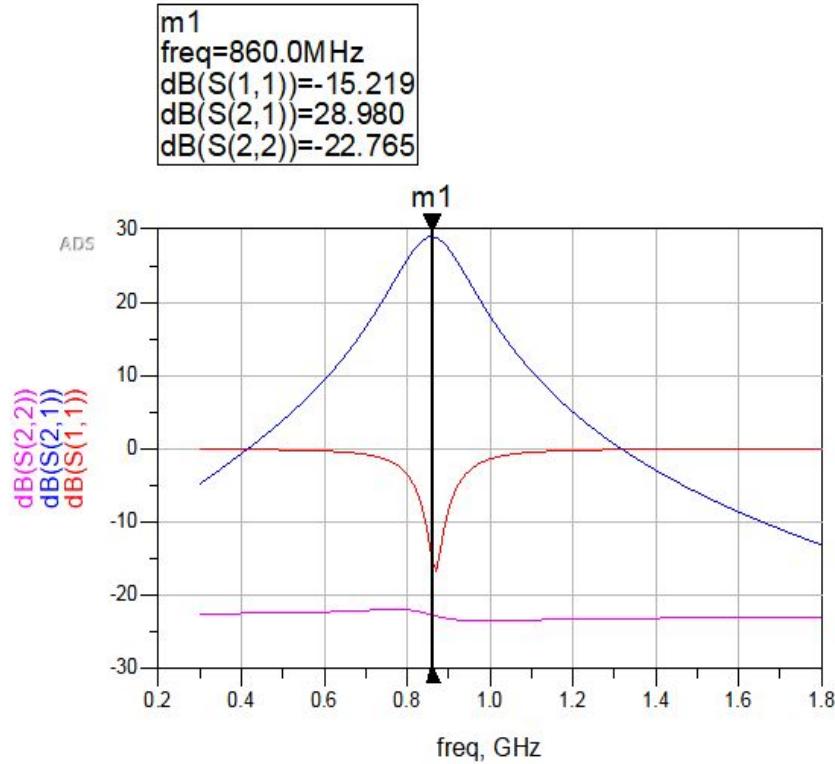
# Gain Matching for Noise Cancelling Stage

Gain matching for noise cancelling stage is done so as to cancel noise as much as possible on all frequency range.



index	Gm*1000	Id*1000	Vgs	Vth	Vds	Vdsat	....DeviceId
1	22.071	4.119	0.633	0.414	0.661	0.205	MOSFET1
2	41.018	4.119	0.491	0.433	0.464	0.136	MOSFET2
3	5.061	1.000	0.659	0.421	0.648	0.210	MOSFET3
4	22.309	7.470	0.807	0.401	0.786	0.270	MOSFET4
5	52.887	12.657	0.655	0.366	1.097	0.227	MOSFET5
6	5.061	1.000	0.659	0.421	0.648	0.210	MOSFET6

# Results



# Issues

- ★ Power Consumption -- too high
- ★  $L_g = 86.7 \text{ nH}$  -- Off chip
- ★ Noise figure = 2.608 dB -- High value for CS topology

$$\text{Eqn } P_{WB} = (DC.I\_Probe1.i + DC.I\_Probe2.i) * 1.2$$

freq	DC.I_Probe1.i	DC.I_Probe2.i	P_WB*1000
0.0000 Hz	12.66 mA	4.119 mA	20.131

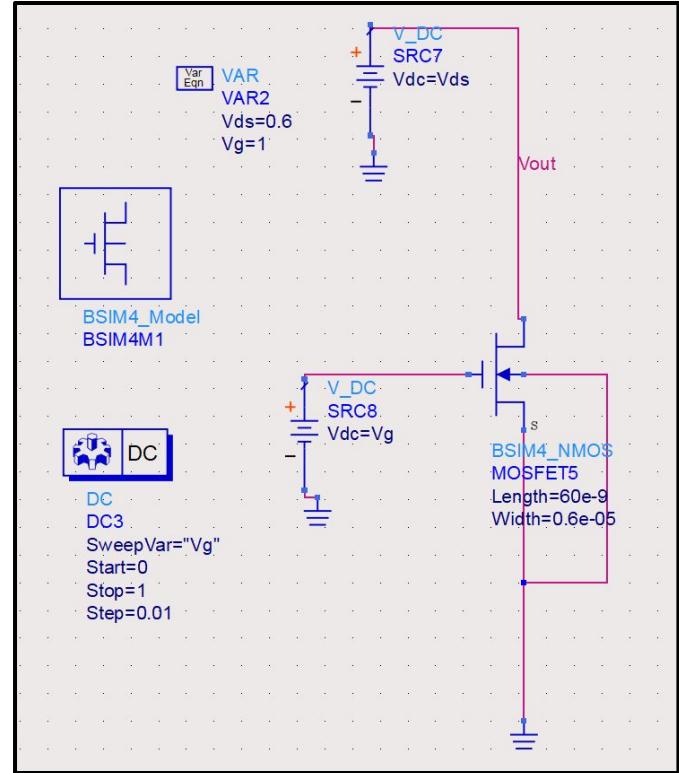


# CG LNA design (without noise cancellation)

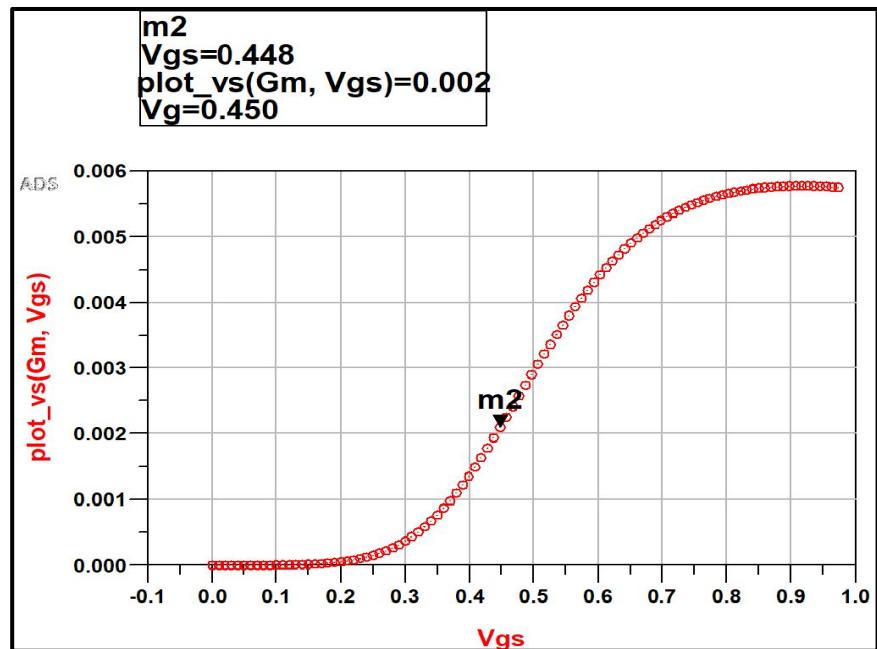
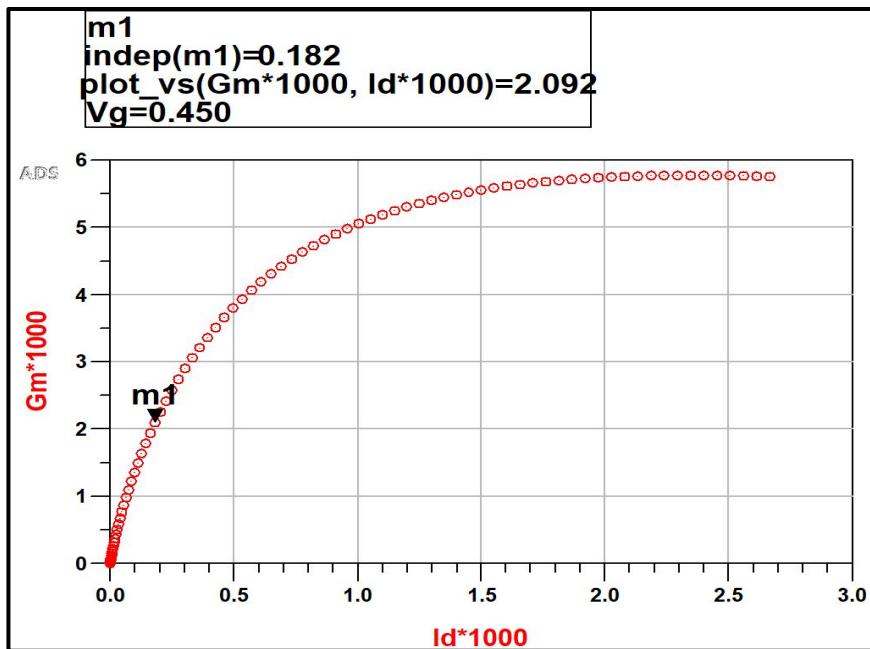
# DC operating point : circuit

- Made biasing circuit with
  - $V_{ds} = 0.6 \text{ V}$
  - $W = 6 \mu\text{m}$
- Sweeping  $V_{gs}$  and plotting  $gm$  vs  $I_d$  and  $gm$  vs  $V_{gs}$  curve to choose operating point along with table.

Gm	$I_d$	$V_{gs}$	$V_{th}$	$V_{ds}$
1.935	0.162	0.438	0.427	0.597
<b>2.092</b>	<b>0.182</b>	<b>0.448</b>	<b>0.428</b>	<b>0.596</b>
2.251	0.203	0.458	0.428	0.596



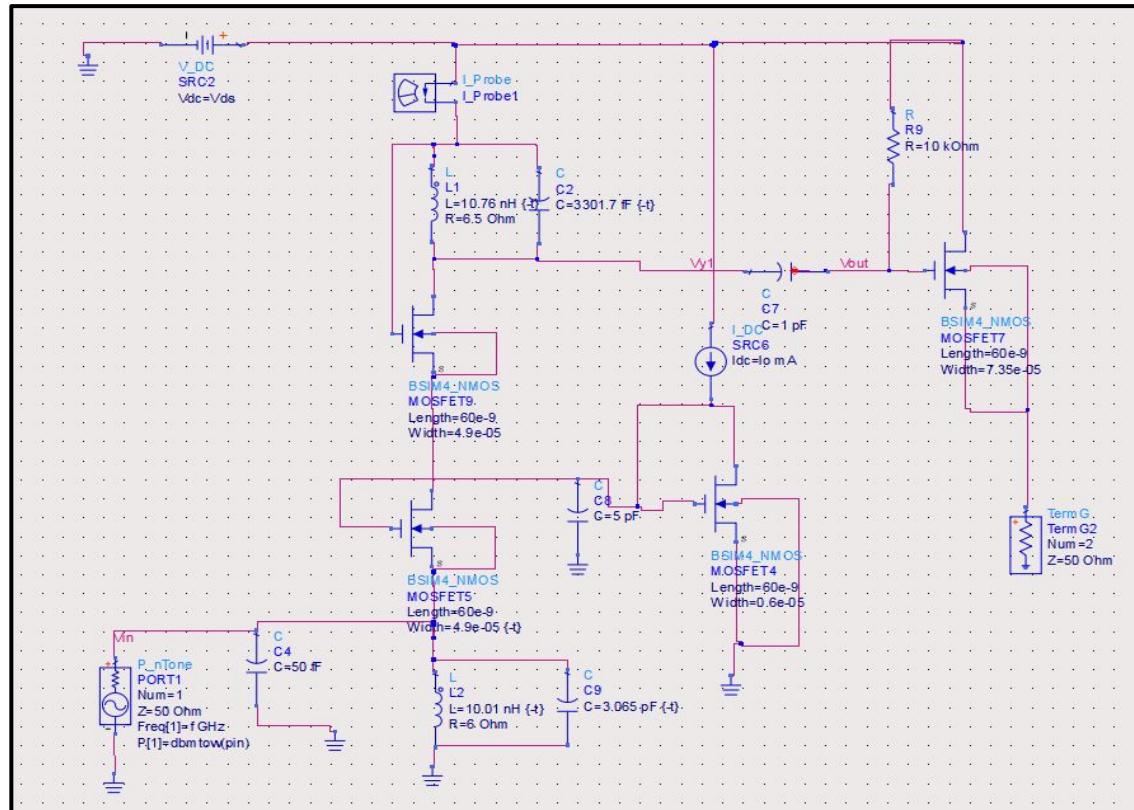
# DC Operating Point: Point Selection



Point is to be chosen at a lower side to obtain less power consumption.

# CG LNA Circuit Design

- Started with CG topology and made a model with focus on less power consumption and least amount of noise possible with a constrain of all the inductors being on chip
- First scale the width and then tune the width to get gm as 20 ms.
- Tune the inductor and capacitor to get proper matching and gain.



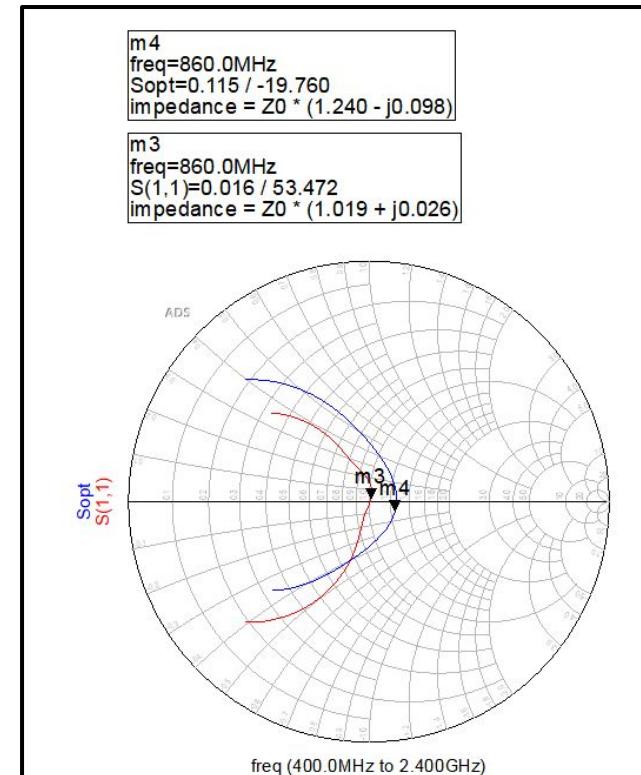
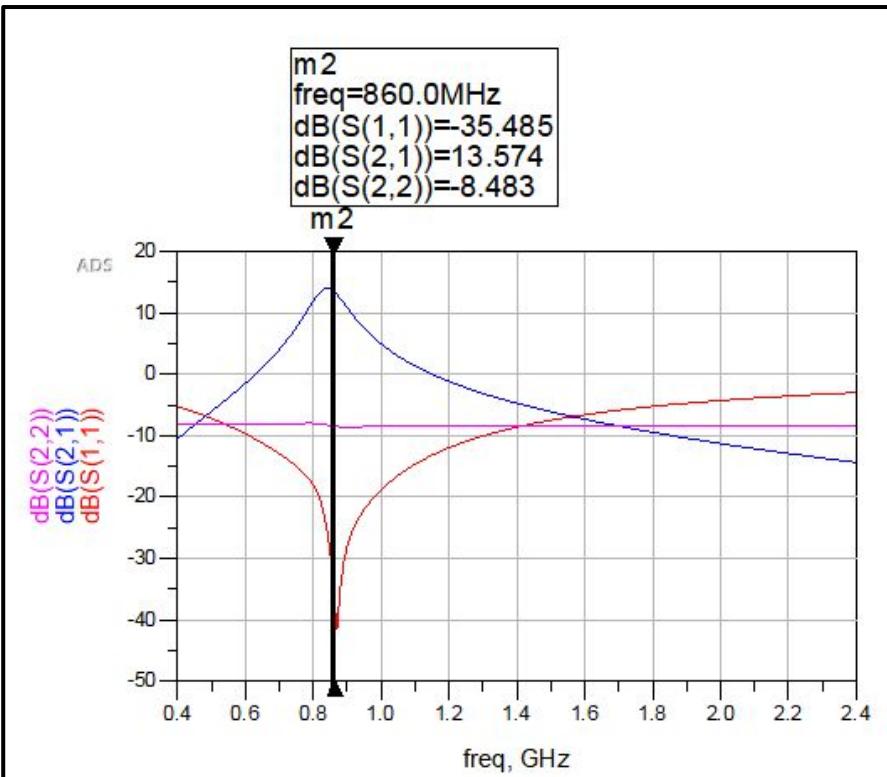
# DC Parameter and Power

index	Gm*1000	Id*1000	Vgs	Vth	...P.Deviceld	Vds	Vdsat
1	2.082	0.182	0.466	0.442	MOSFET4	0.464	0.117
2	20.870	2.011	0.454	0.410	MOSFET5	0.697	0.129
3	43.564	9.950	0.690	0.412	MOSFET7	0.677	0.226
4	20.685	2.011	0.485	0.435	MOSFET9	0.469	0.132

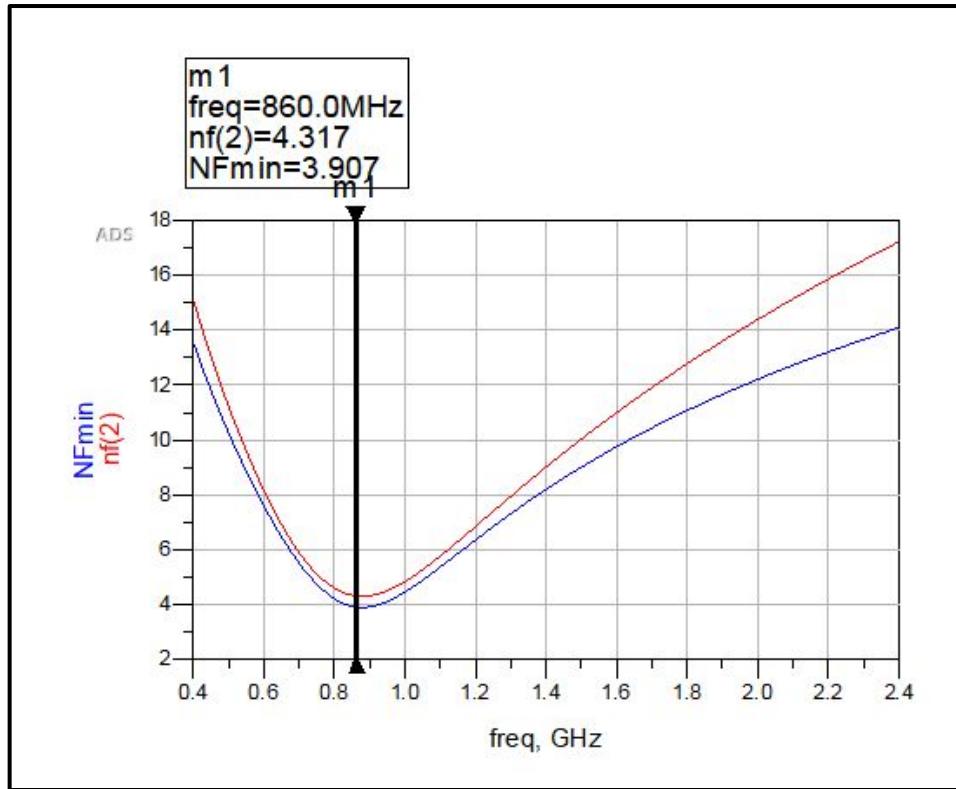
freq	I_Probe1.i	power*1000
0.0000 Hz	2.011 mA	2.413

Eqn power = I\_Probe1.i\*1.2

# S-Parameter



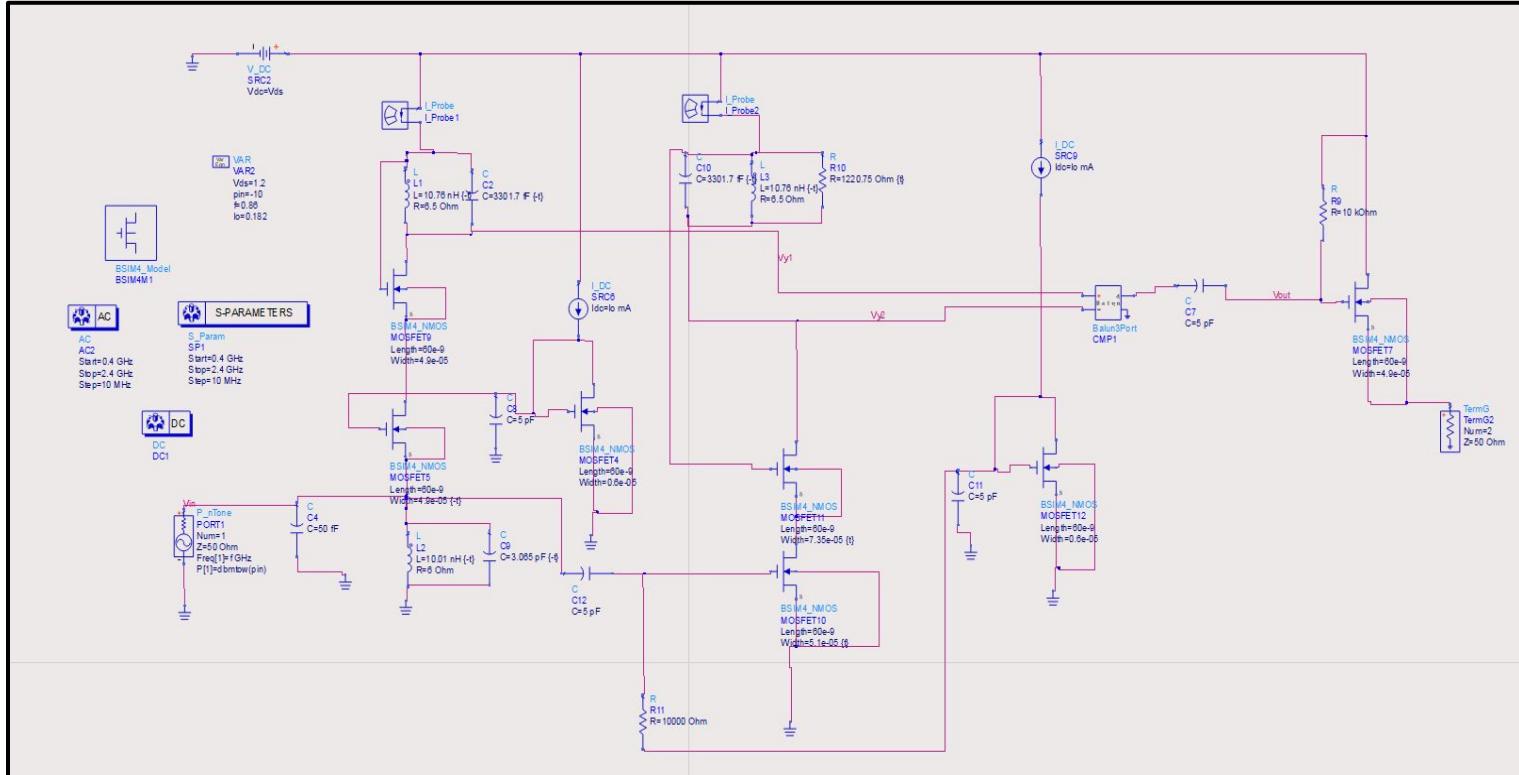
# Noise Figure



# CG LNA : Noise Cancellation

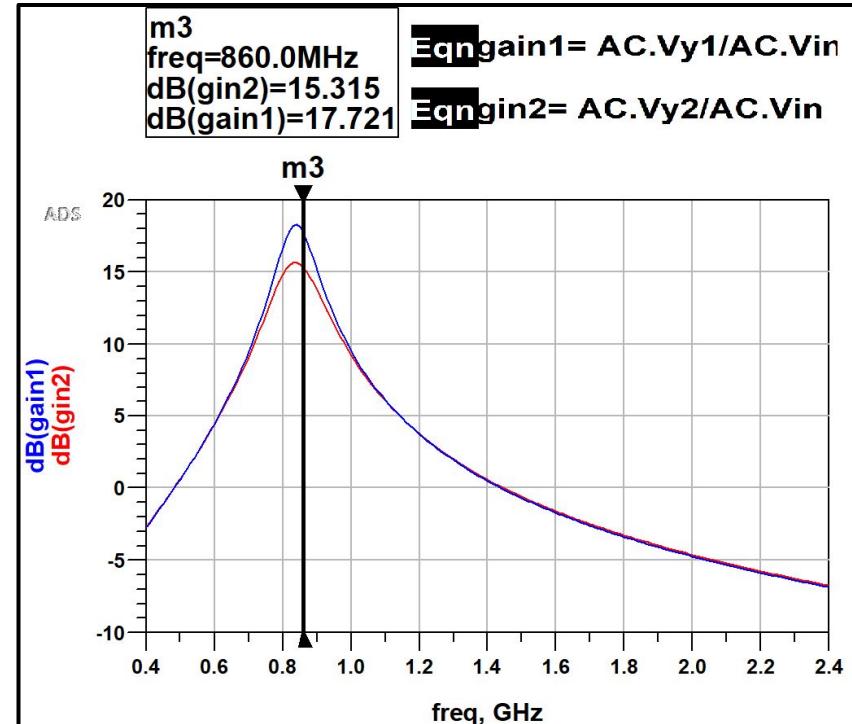
# With Noise Cancellation: Circuit diagram

Used same width and load along with an extra resistance in parallel to control gain



# With Noise Cancellation: Gain matching

- Tuned the widths and resistance to match the gain of main stage and noise cancelling stage
- Same profile because of same load with same Q



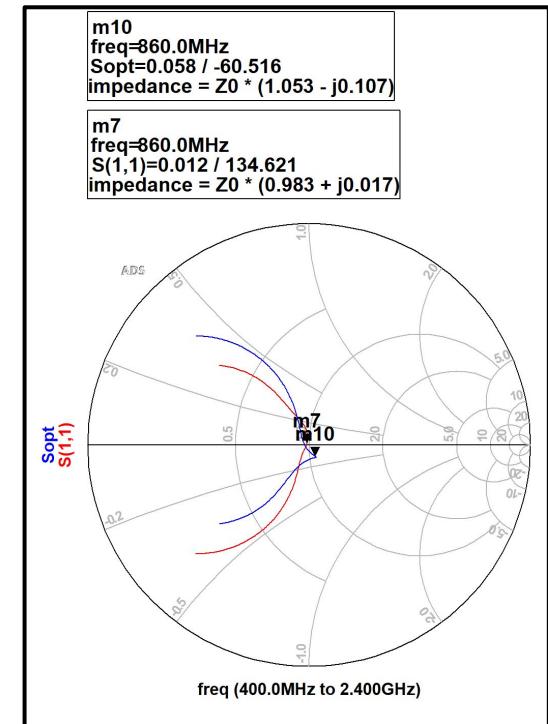
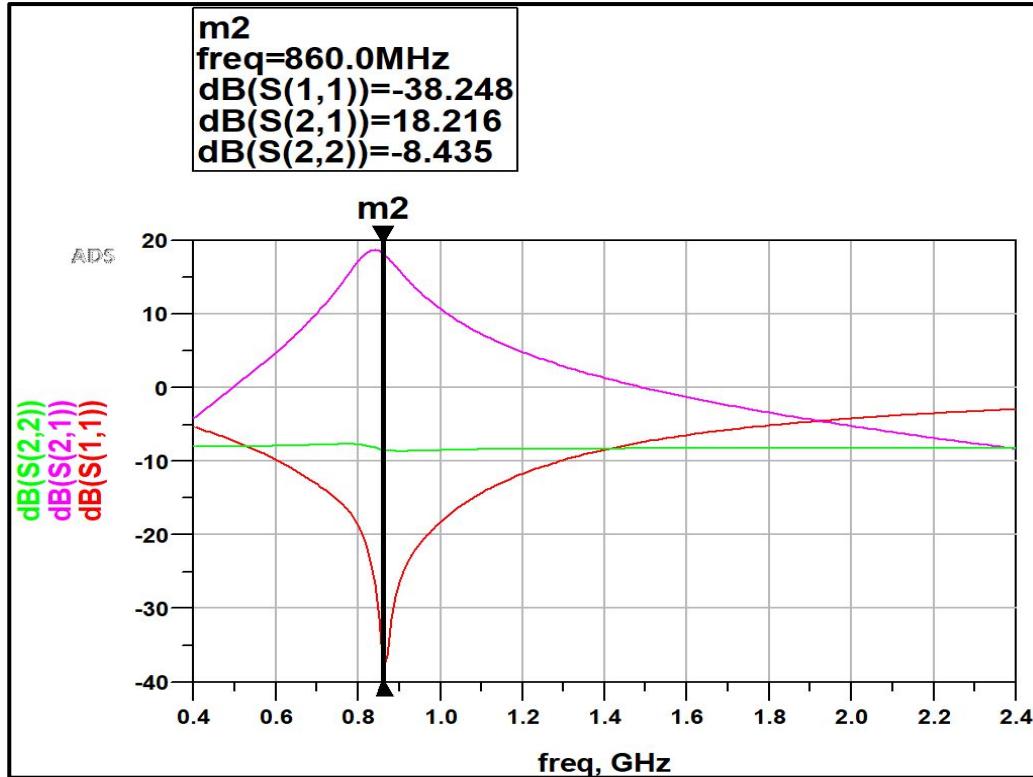
# With Noise cancellation: DC parameters and power

index	Gm*1000	Id*1000	Vgs	Vth	...P.Deviceld	Vds	Vdsat
1	23.767	2.416	0.465	0.407	MOSFET10	0.726	0.135
2	26.883	2.416	0.466	0.436	MOSFET11	0.448	0.123
3	2.082	0.182	0.466	0.442	MOSFET12	0.464	0.117
4	2.082	0.182	0.466	0.442	MOSFET4	0.464	0.117
5	20.870	2.011	0.454	0.410	MOSFET5	0.697	0.129
6	43.564	9.950	0.690	0.412	MOSFET7	0.677	0.226
7	20.685	2.011	0.485	0.435	MOSFET9	0.469	0.132

freq	DC.I_Probe1.i	DC.I_Probe2.i	Power_WB*1000
0.0000 Hz	2.011 mA	2.416 mA	5.312

Power consumption excludes buffer stage and biasing circuit.

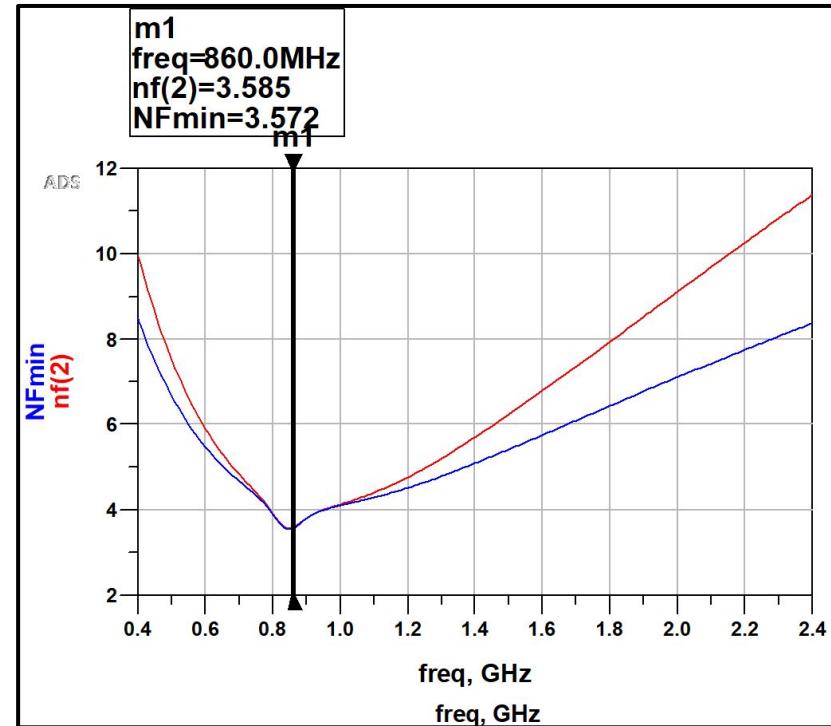
# With Noise Cancellation: S-parameter



Operating point is  
near to the  $S_{\text{opt}}$  point

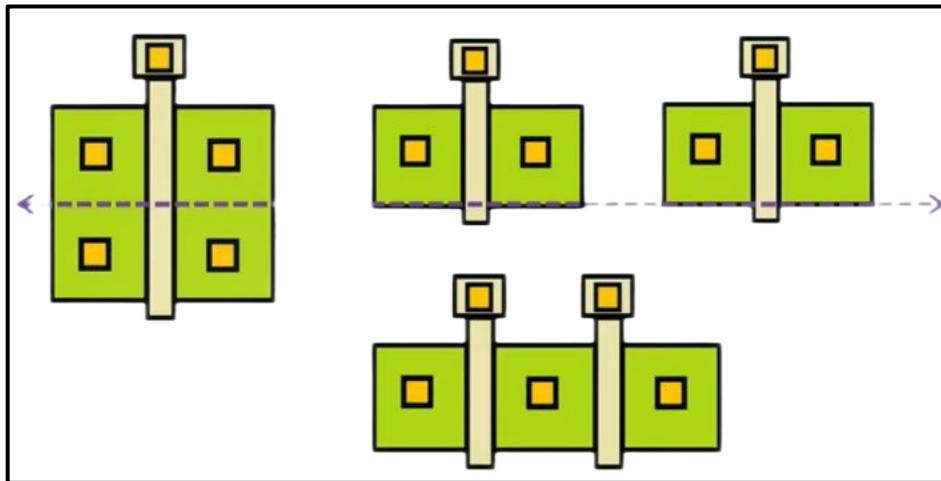
# With Noise Cancellation: Noise Figure

- We can see Noise Cancelling stage had a great impact on NF which created a dip around the desired frequency.
- As expected, NF is closer to the  $NF_{min}$



# Number of Fingers' Effect

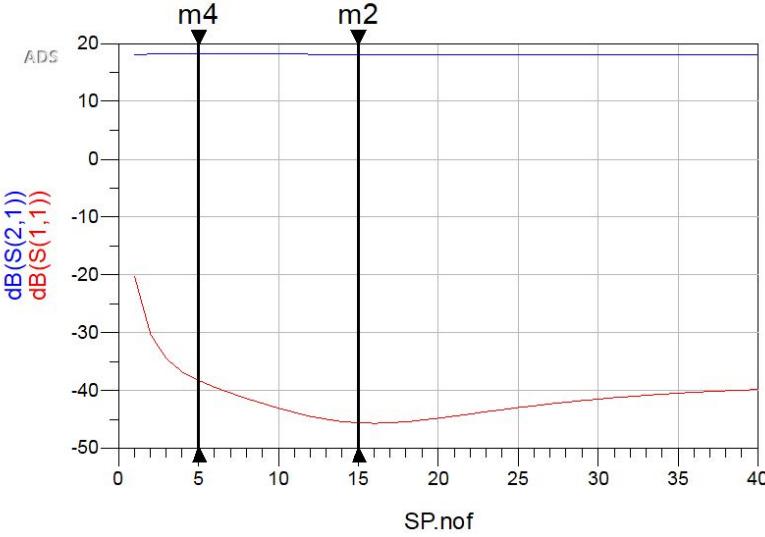
# Introduction



## Increasing NoF

- Decreases Parasitic Capacitance
- Decreases Gate resistance of MOSFET
- NF decreases
- IIP3 Increases

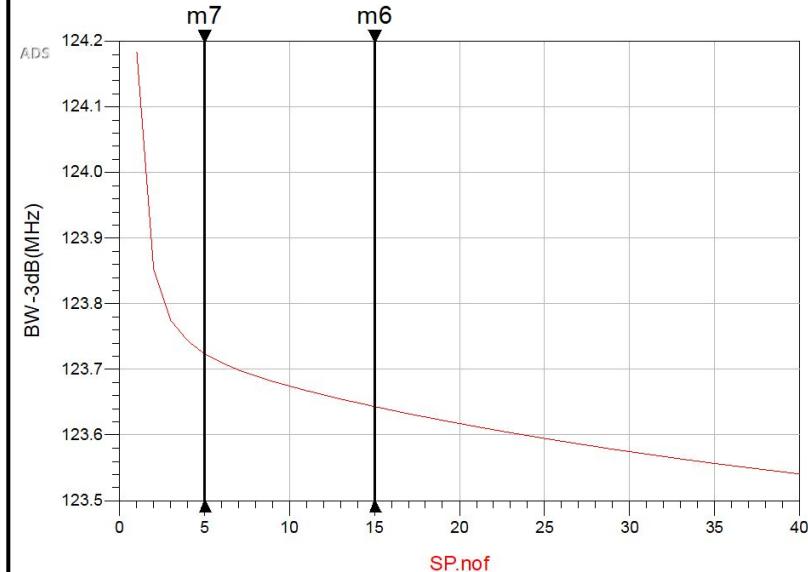
**m2**  
 indep=15.000  
 plot\_vs(dB(S(1,1)), SP.nof)=-45.557  
 plot\_vs(dB(S(2,1)), SP.nof)=18.134



**m4**  
 indep=5.000  
 plot\_vs(dB(S(1,1)), SP.nof)=-38.248  
 plot\_vs(dB(S(2,1)), SP.nof)=18.216

**m7**  
 indep=5.000  
 plot\_vs(bw3dB, SP.nof)=123.723

**m6**  
 indep=15.000  
 plot\_vs(bw3dB, SP.nof)=123.643

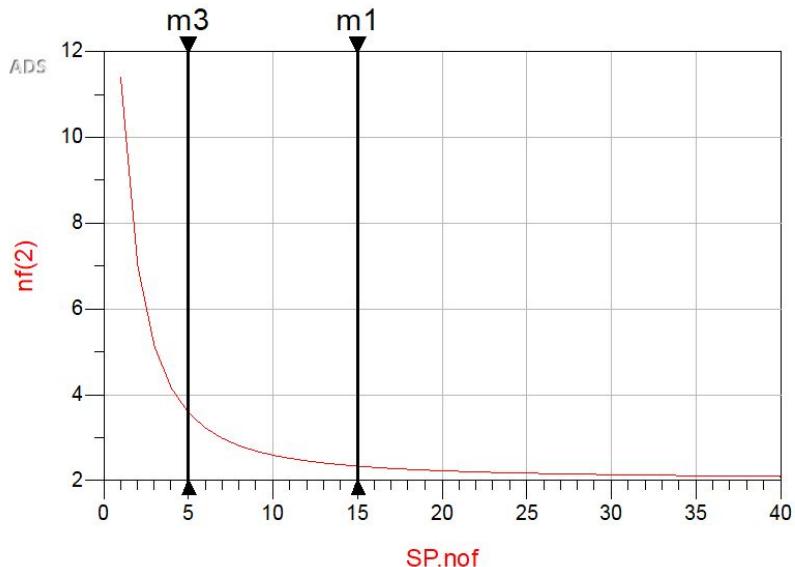


S11 changing Non-uniformly

Bandwidth decreasing exponentially (Low Drop)

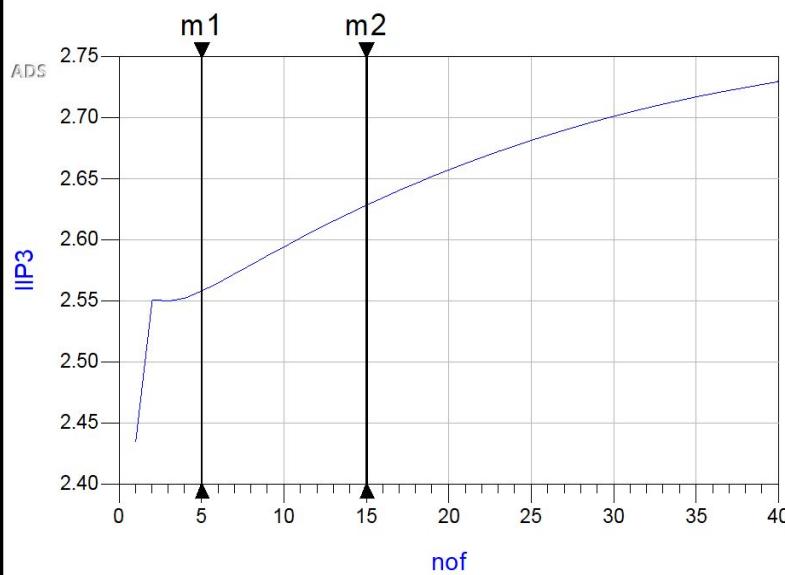
m3  
indep=5.000  
plot\_vs(nf(2), SP.nof)=3.585

m1  
indep=15.000  
plot\_vs(nf(2), SP.nof)=2.336



m1  
nof=5.000  
IIP3=2.558

m2  
nof=15.000  
IIP3=2.629



Noise-Figure decreasing exponentially

Small increment in IIP3

# Number of Fingers : Special Case

Used in the scale of half of the width

- Value of Nof in our design:
  - MOSFET5 ( $W=49 \text{ um}$ ) : 25
  - MOSFET9 ( $W=49 \text{ um}$ ) : 25
  - MOSFET10 ( $W=51 \text{ um}$ ) : 25
  - MOSFET11 ( $W=73.5 \text{ um}$ ) : 35

Used only for main transistors, not for biasing and buffer stage.

Without Noise cancelling  
design with number of fingers

# DC parameters and Power

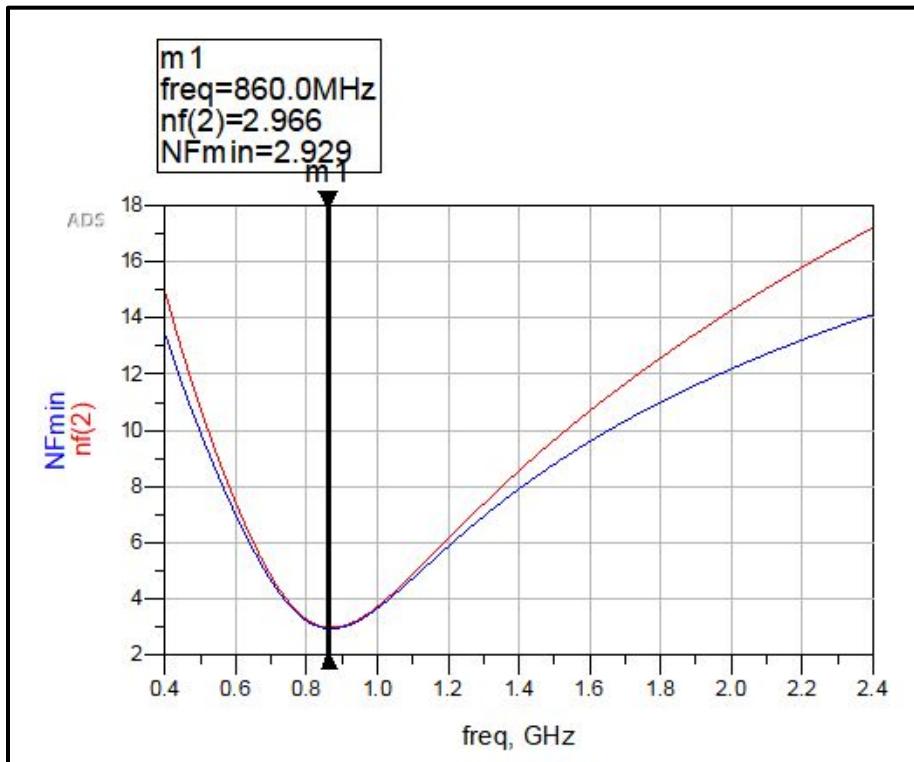
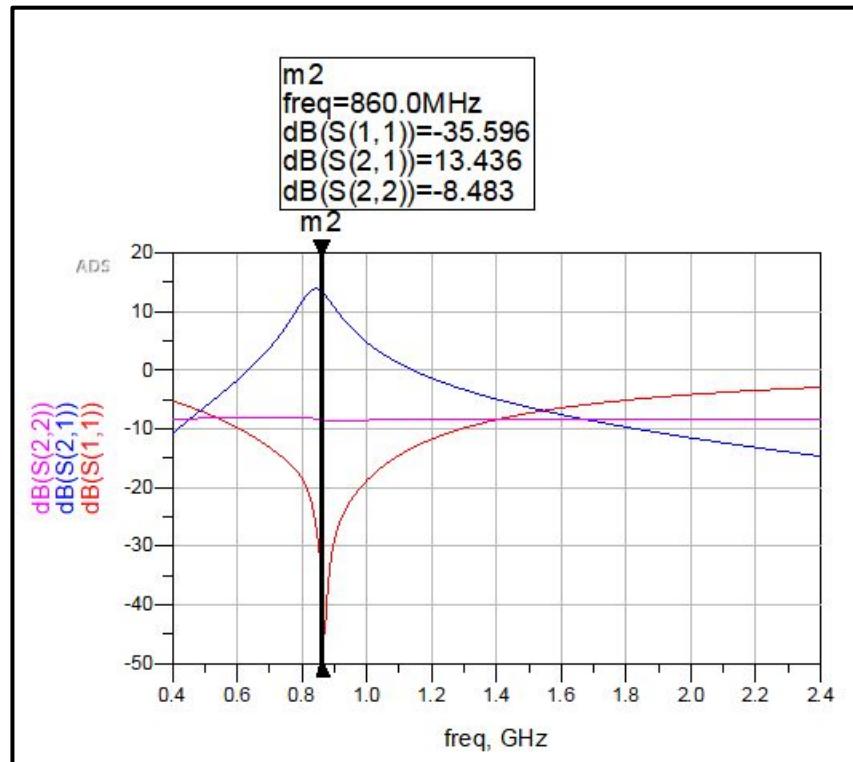
index	Gm*1000	Id*1000	Vgs	Vth	...P.DevicelD	Vds	Vdsat
1	2.082	0.182	0.466	0.442	MOSFET4	0.464	0.117
2	20.120	1.898	0.455	0.415	MOSFET5	0.697	0.125
3	43.564	9.950	0.690	0.412	MOSFET7	0.677	0.226
4	19.946	1.898	0.485	0.440	MOSFET9	0.471	0.128

$$\text{EqnPower\_WB} = (\text{DC.I_Probe1.i}) * 1.2$$

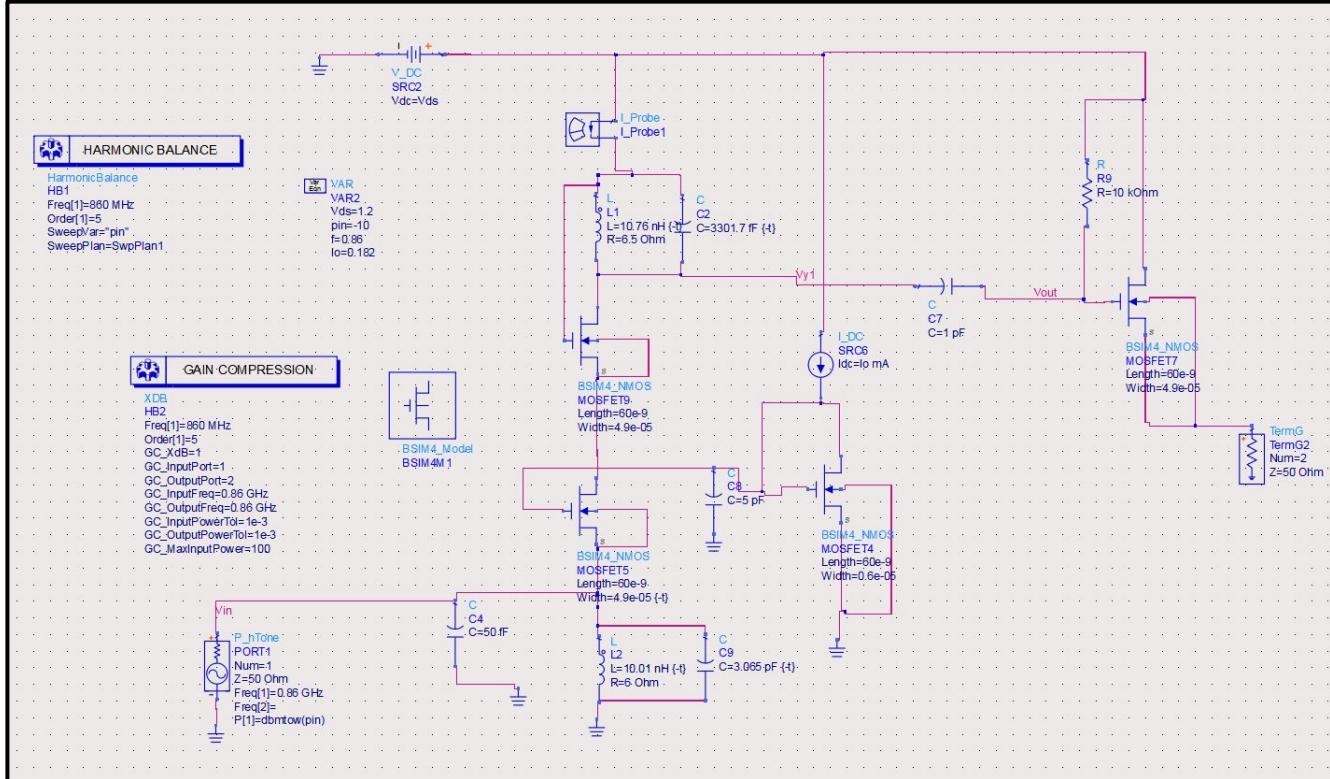
freq	DC.I_Probe1.i	Power_WB*1000
0.0000 Hz	1.898 mA	2.278

Power consumption decrease..

# S-parameter and Noise figure



# Circuit for Nonlinearity Analysis



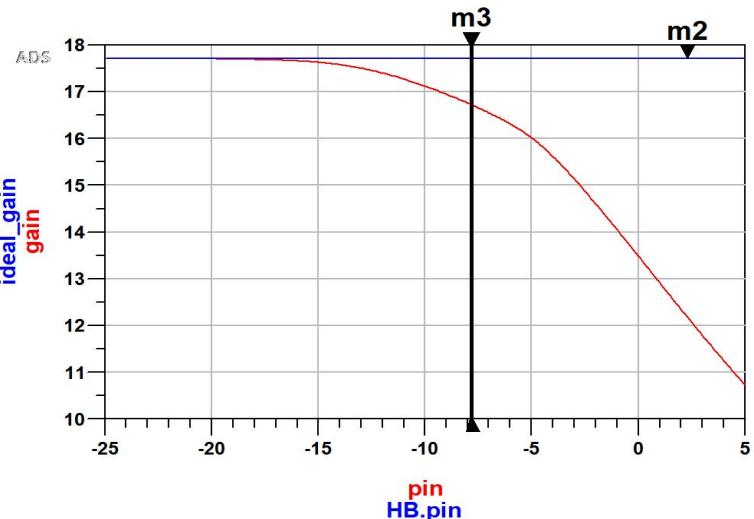
# 1-dB Compression Point

Eqn gain=dBm(HB1.HB.Vout[1])-HB.pin

Eqn ideal\_gain=gain[0]

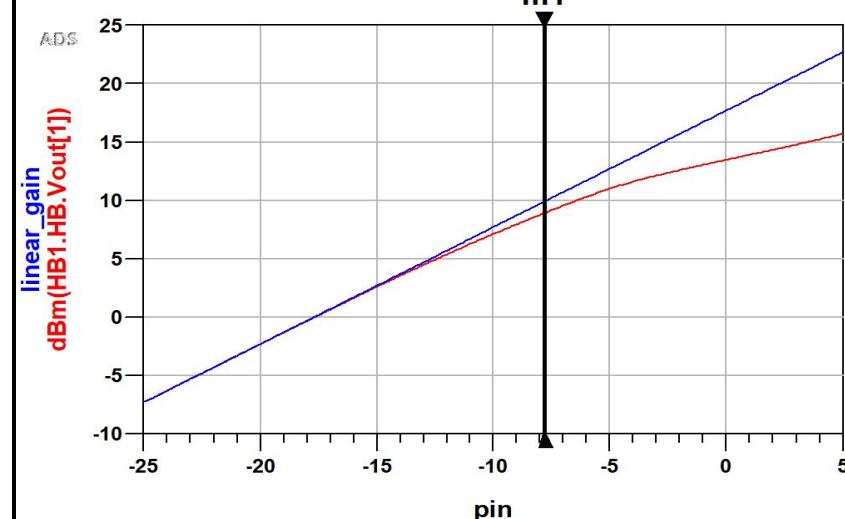
m3  
pin=7.800  
gain=16.719

m2  
indep(m2)=2.300  
plot\_vs(ideal\_gain, HB.pin)=17.714

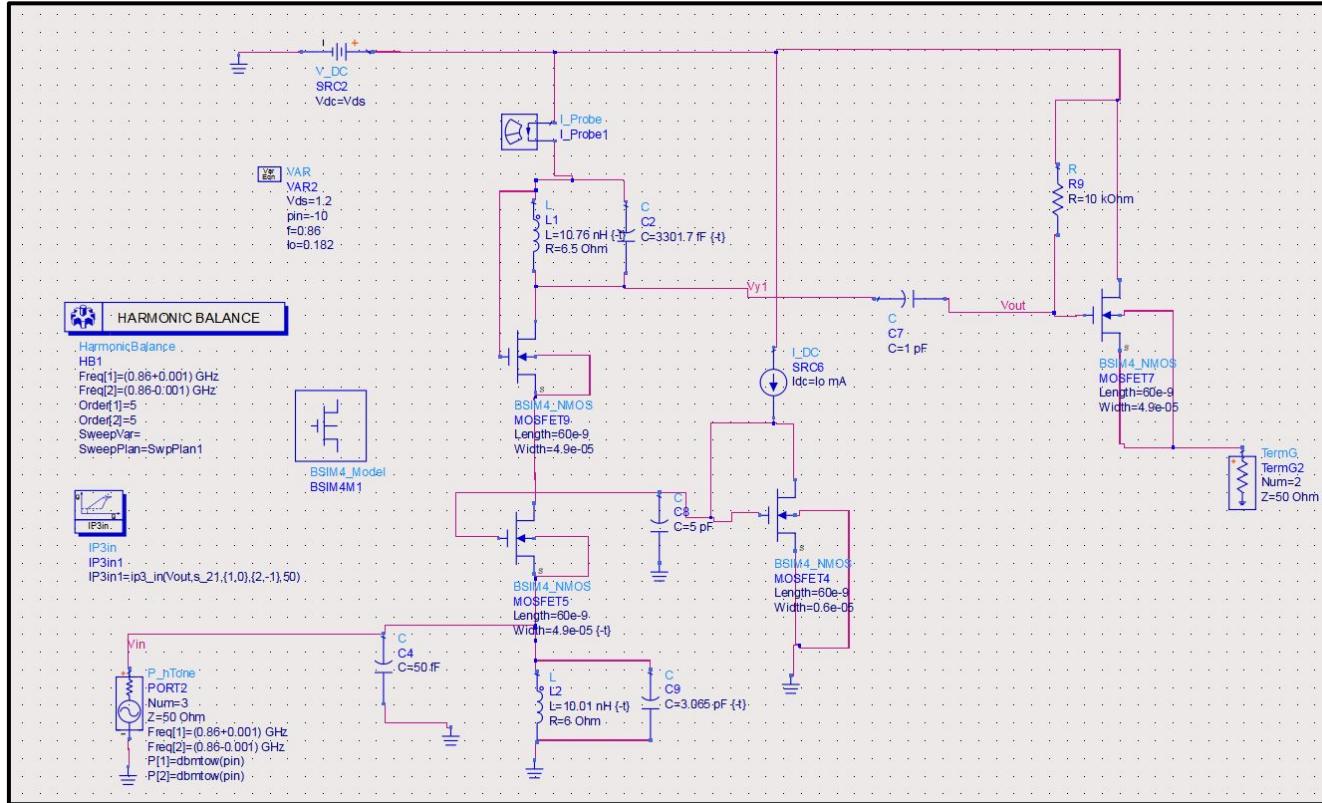


Eqn linear\_gain=gain[0]+LNA\_non\_linear..HB.pin

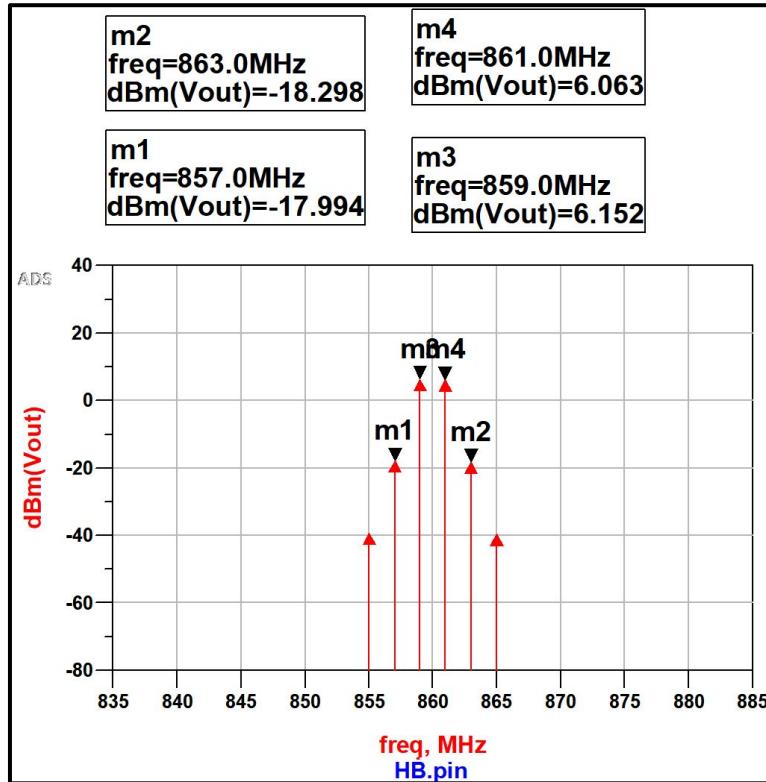
m1  
pin=-7.800  
dBm(HB1.HB.Vout[1])=8.919  
linear\_gain=10.048



# Circuit for Two-Tone Test



# IIP3 Analysis



freq, MHz			
855.0 MHz	-2	3	
857.0 MHz	-1	2	
859.0 MHz	0	1	
861.0 MHz	1	0	
863.0 MHz	2	-1	
865.0 MHz	3	-2	

$$\text{Eqn } s\_gain=17.633$$

$$\text{Eqn } \text{IIP3\_lower}=\text{ip3\_in}(\text{Vout}, s\_gain, \{1,0\}, \{2,-1\}, 50)$$

$$\text{Eqn } \text{IIP3}=\text{ip3\_in}(\text{Vout}, s\_gain, \{0,1\}, \{-1,2\}, 50)$$

freq	IIP3	IIP3_lower
<invalid>Hz	0.592	0.611

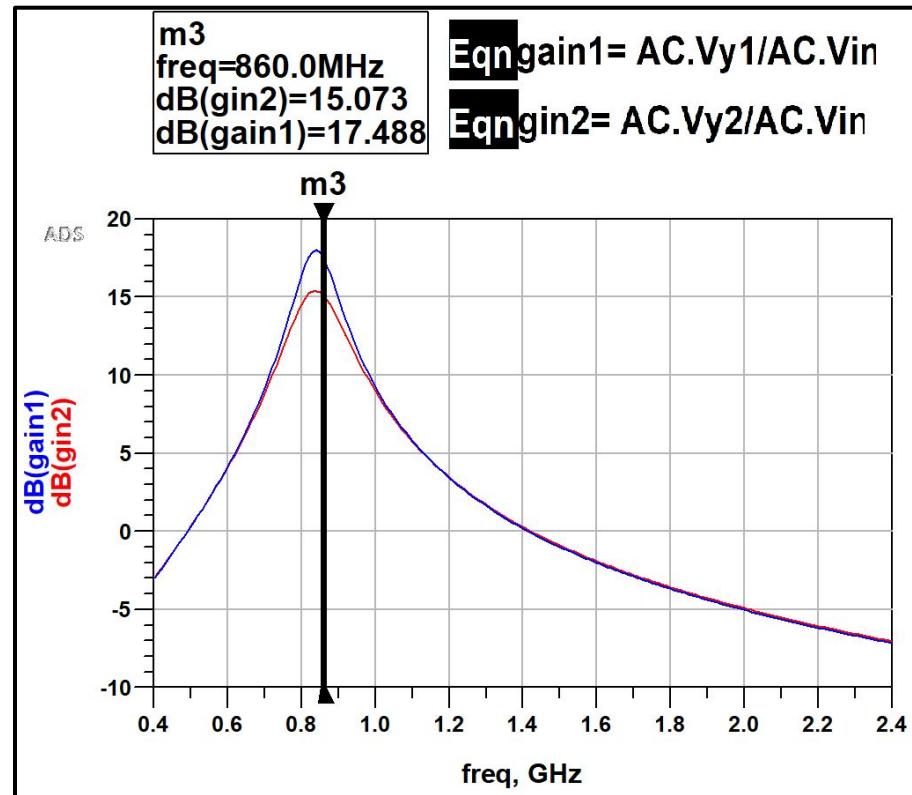
As expected,  $\text{IIP3} \sim P_{1\text{dB}} + 9.6 \text{ dB}$



# Noise cancelling design with number of fingers

# Gain Matching

- Already matched, no change.
- No effect of Number of fingers.



# DC Parameters and Power

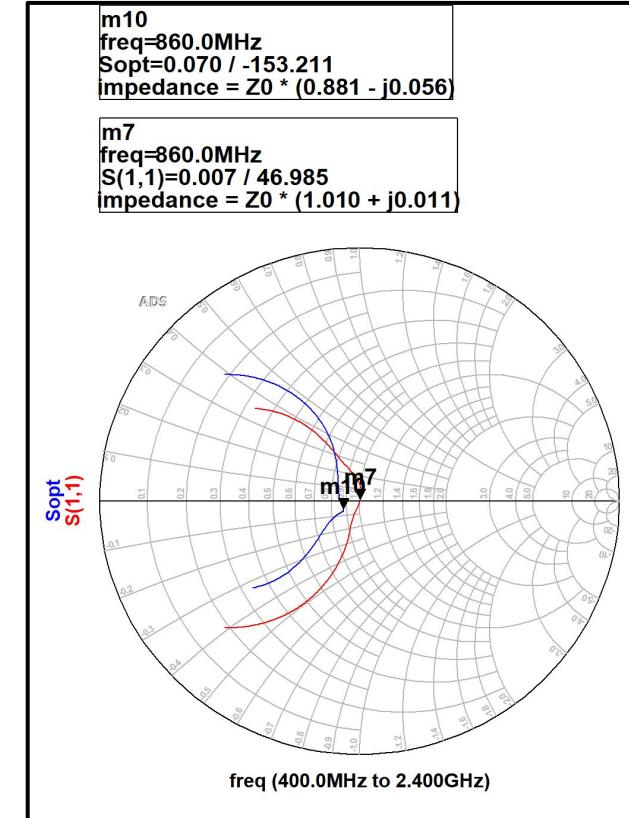
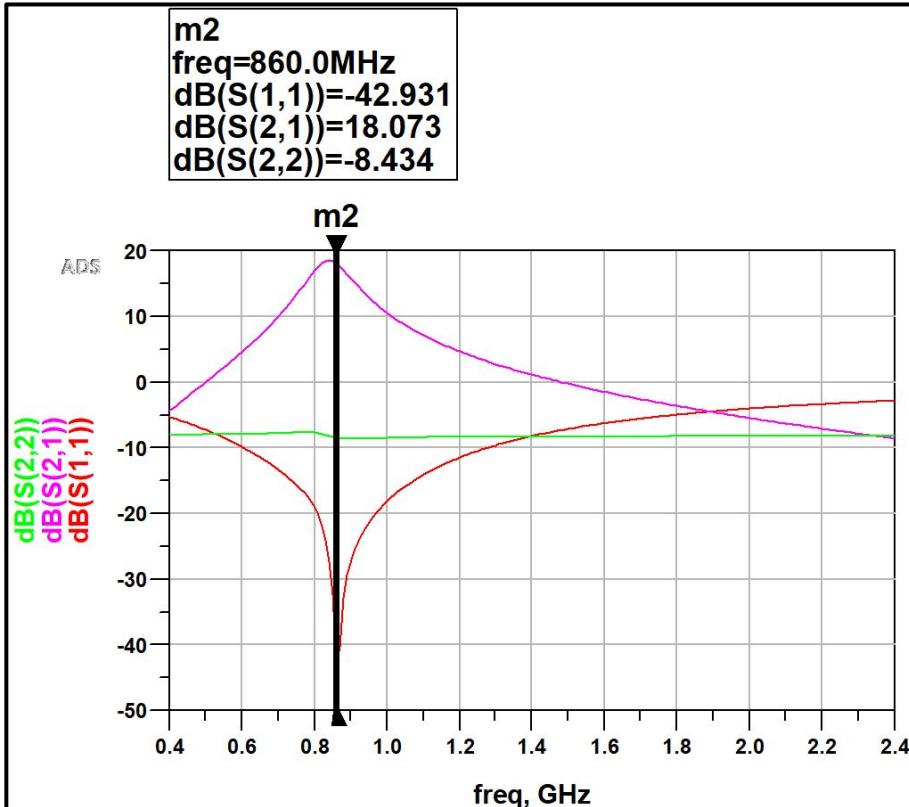
index	Gm*1000	Id*1000	Vgs	Vth	...P.DevicelD	Vds	Vdsat
1	22.901	2.273	0.465	0.412	MOSFET10	0.725	0.130
2	25.806	2.273	0.467	0.442	MOSFET11	0.451	0.119
3	2.082	0.182	0.466	0.442	MOSFET12	0.464	0.117
4	2.082	0.182	0.466	0.442	MOSFET4	0.464	0.117
5	20.120	1.898	0.455	0.415	MOSFET5	0.697	0.125
6	43.564	9.950	0.690	0.412	MOSFET7	0.677	0.226
7	19.946	1.898	0.485	0.440	MOSFET9	0.471	0.128

**Eqn** Power\_WB=(DC.I\_Probe1.i+DC.I\_Probe2.i)\*1.2

freq	DC.I_Probe1.i	DC.I_Probe2.i	Power_WB*1000
0.0000 Hz	1.898 mA	2.273 mA	5.006

Power consumption decrease..

# S-Parameter

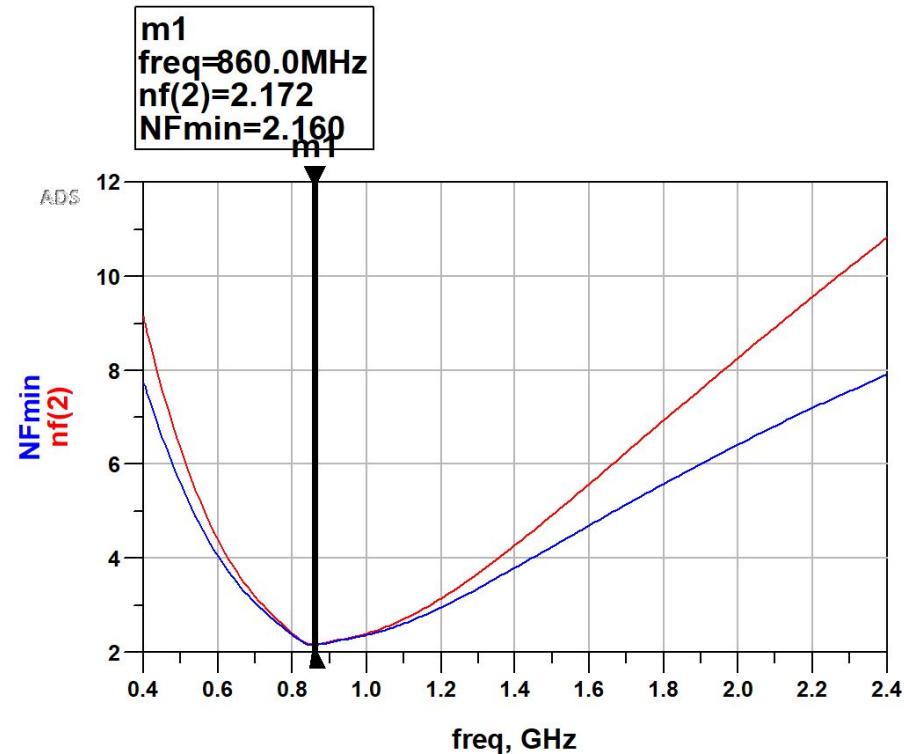


Again Operating point is  
near to the  $S_{\text{opt}}$  point

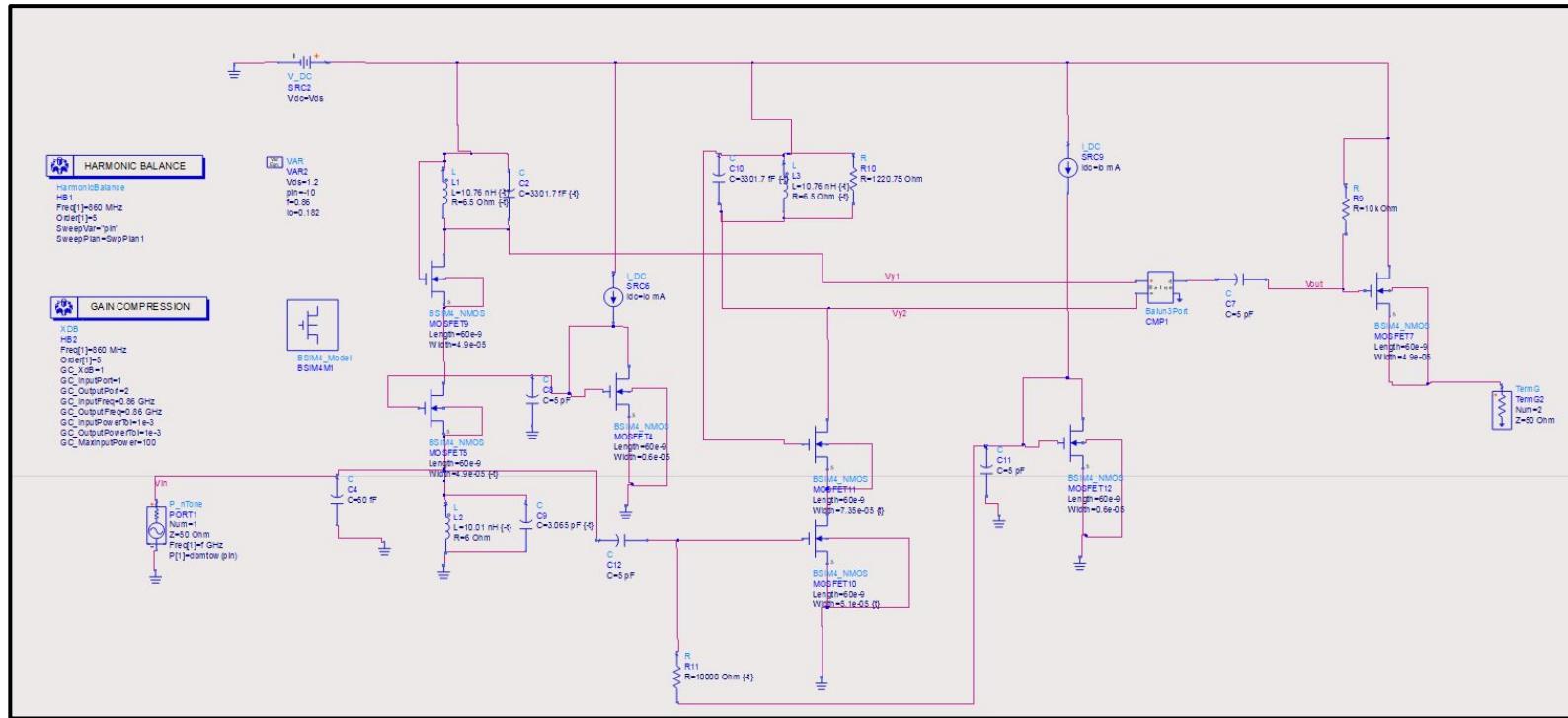
# Noise Figure

As expected, NF is closer to the NFmin

NF value decrease due to added fingers.



# Circuit for Nonlinearity Analysis



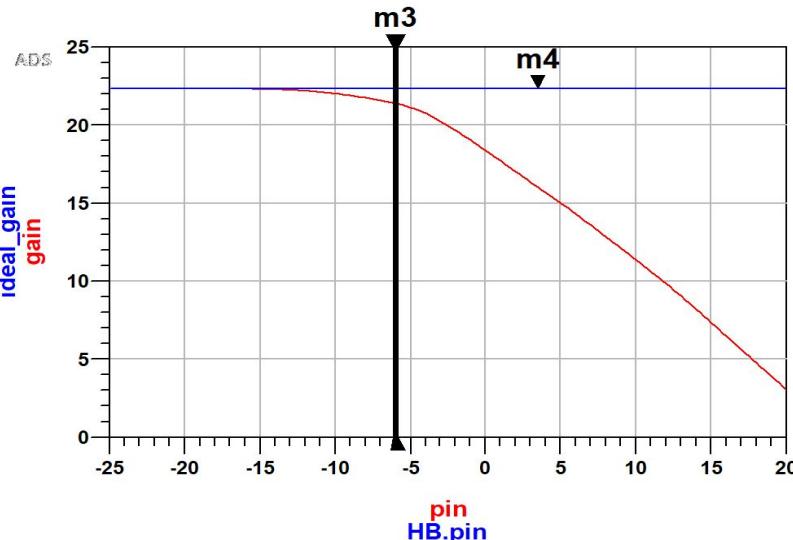
# 1-dB Compression Point

Eqn  $gain = dBm(HB1.HB.Vout[1]) - HB.pin$

Eqn  $ideal\_gain = gain[0]$

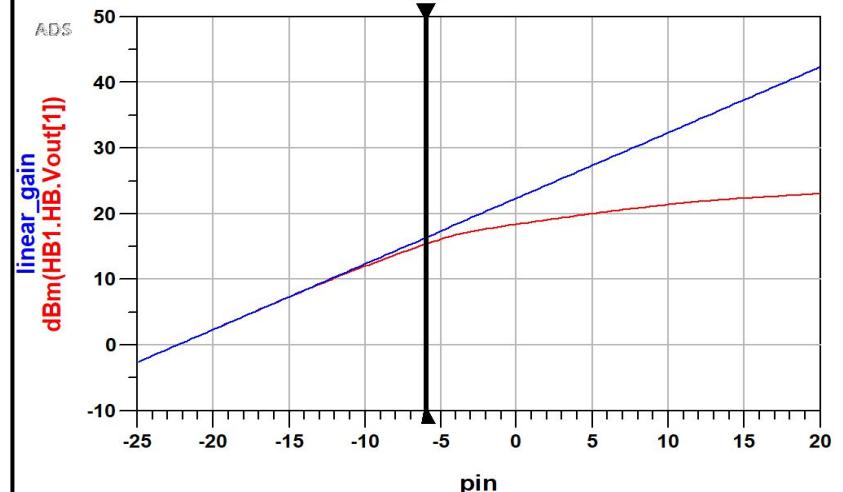
m3  
pin=-6.000  
gain=21.384

m4  
indep(m4)=3.500  
plot\_vs(ideal\_gain, HB.pin)=22.356

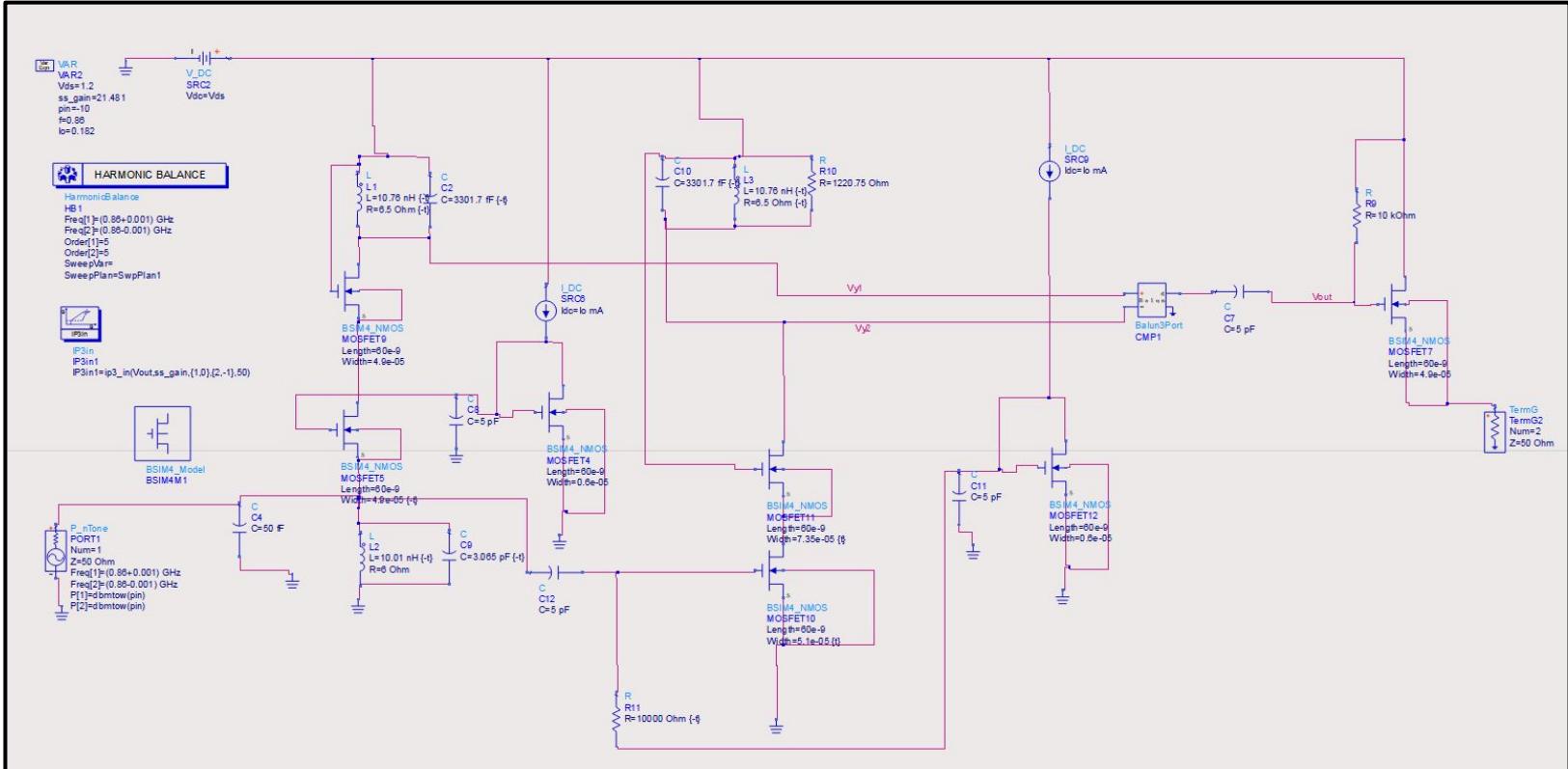


Eqn  $linear\_gain = gain[0] + LNA\_non\_linear..HB.pin$

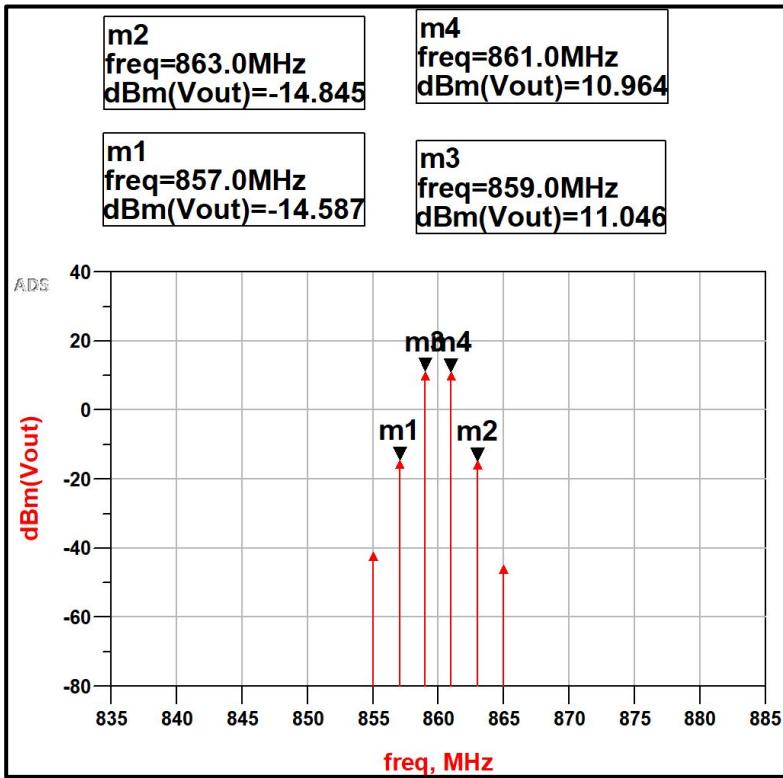
m2  
pin=-6.000  
 $dBm(HB1.HB.Vout[1])=15.384$   
 $linear\_gain=16.356$



# Circuit for Two-Tone Test



# IIP3 Analysis



freq, MHz
855.0 MHz
857.0 MHz
859.0 MHz
861.0 MHz
863.0 MHz
865.0 MHz

freq, MHz
3
2
1
0
-1
-2

$$\text{Eqn ss\_gain}=22.316$$

$$\text{Eqn IIP3\_lower}=\text{ip3\_in}(\text{Vout}, \text{ss\_gain}, \{1,0\}, \{2,-1\}, 50)$$

$$\text{Eqn IIP3}=\text{ip3\_in}(\text{Vout}, \text{ss\_gain}, \{0,1\}, \{-1,2\}, 50)$$

freq	IIP3	IIP3_lower
<invalid>Hz	1.849	1.855

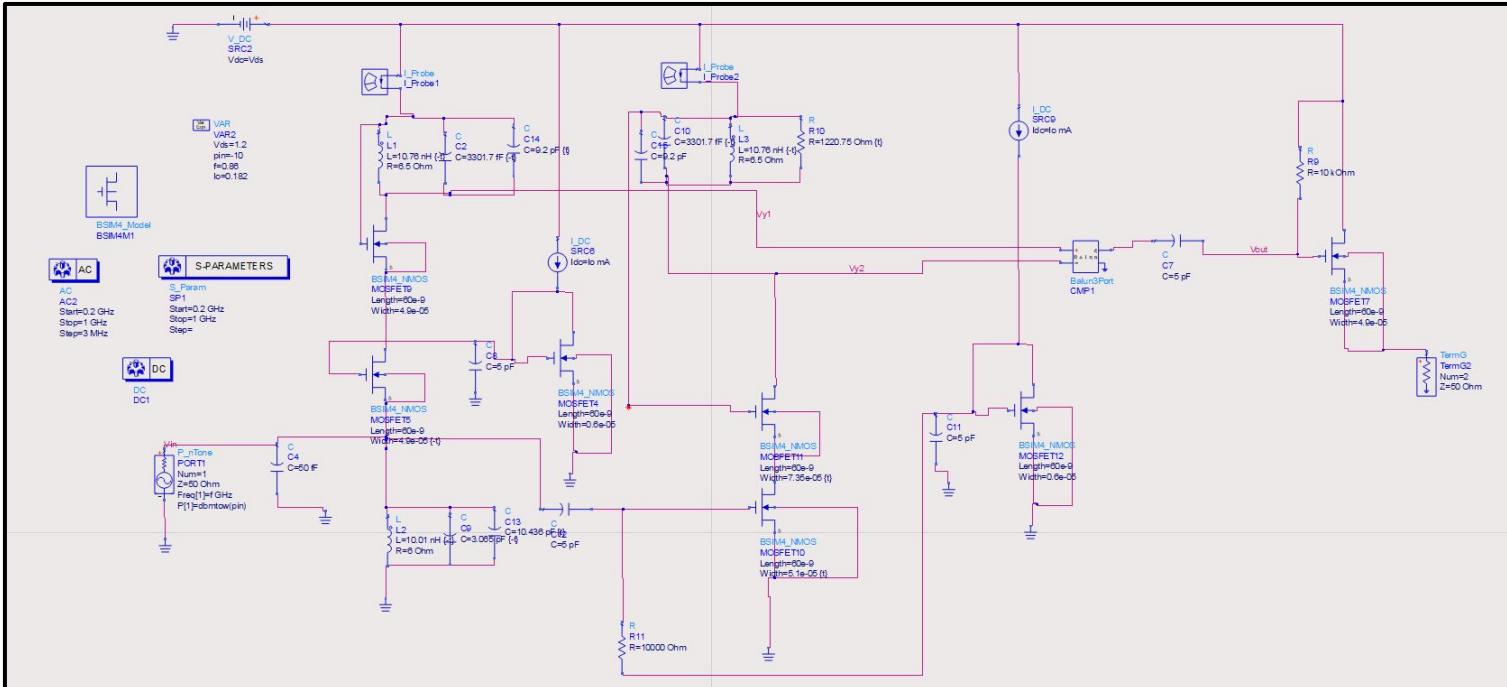
As expected,  $\text{IIP3} \sim P_{1\text{dB}} + 9.6 \text{ dB}$

# Conclusion Table

Sl.No	LNA Design	(S(1,1)) dB	(S(2,1)) dB	Noise Figure (Nf)	Power Consumption (mW)	$P_{1dB}$ (dBm)	IIP3 (dBm)
1	CG LNA(without noise cancellation)	-35.485	13.574	4.317	2.413		
2	CG LNA (without noise cancellation <b>with Nof</b> )	-35.596	13.436	2.966	2.278	-7.8	0.6
3	CG LNA(with Noise cancellation)	-38.248	18.216	3.585	5.312		
4	CG LNA(with noise cancellation <b>with Nof</b> )	-42.931	18.073	2.172	5.006	-6	1.85

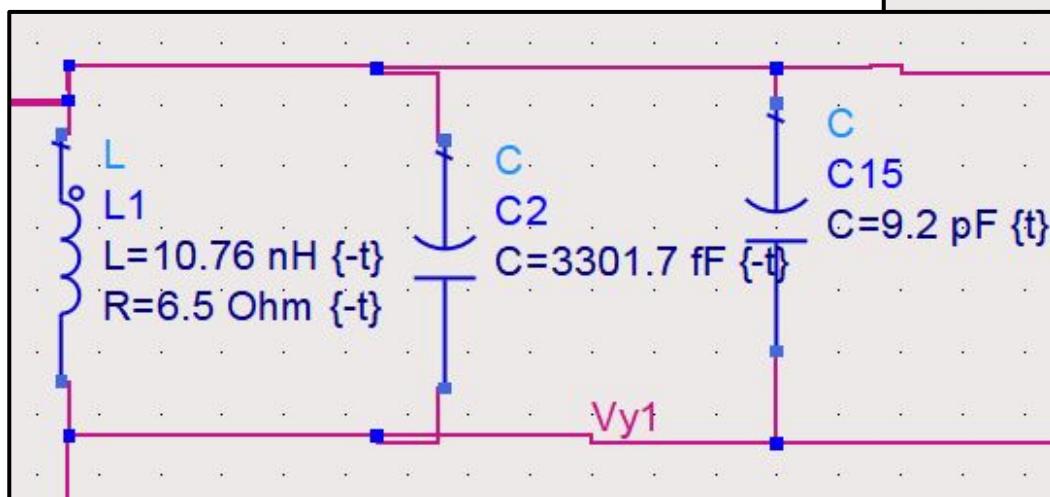
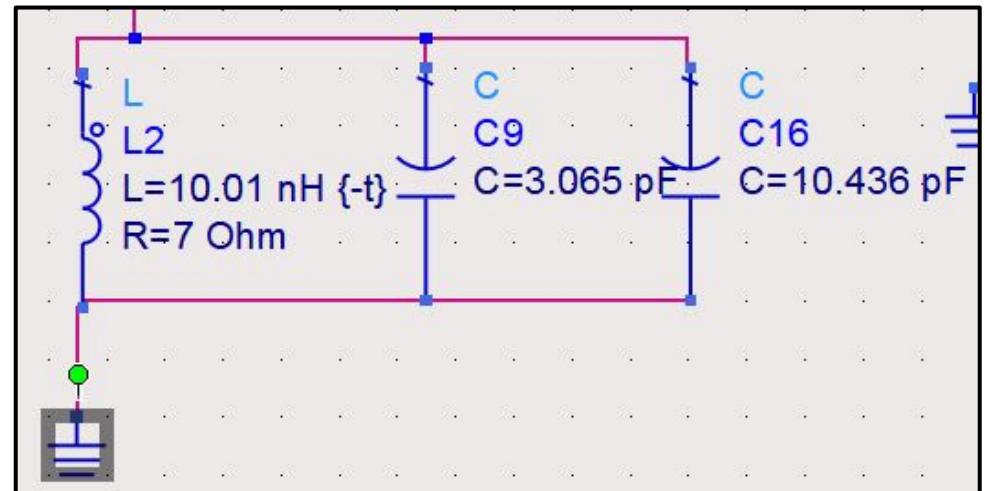
# Dual Band LNA design : Circuit

Used extra capacitor (C13,C14 and C15) with ideal switch to get another band at 433 MHz.

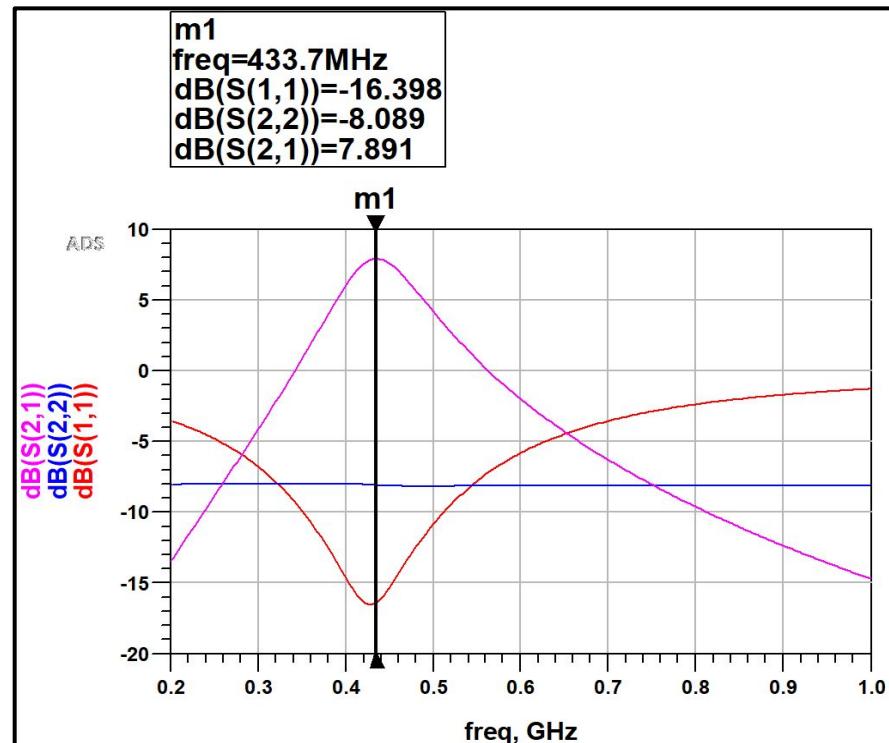
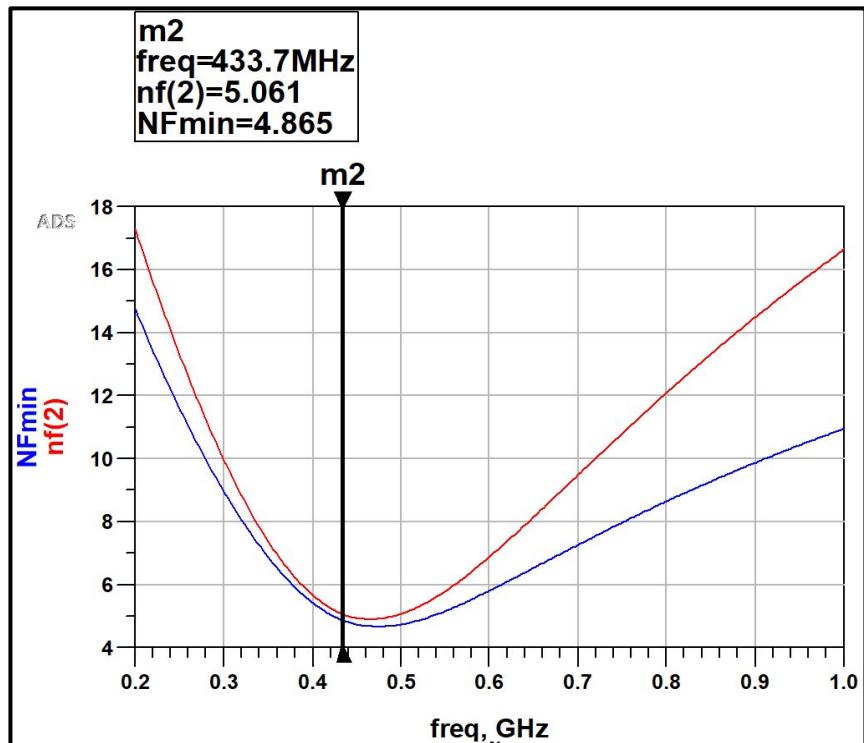


Here we added capacitor bank which can be used in conjunction with the mosfet switches to get to the desired band.

This is a preliminary work and need some optimizations.



# Dual Band LNA design : Results



# CONCLUSION

We successfully designed LNA with following specifications:

- Differential output
- All components are on-chip
- Lower noise figure with use of number of fingers
- High linearity

Demerit:

- Slightly higher power consumption

Future work of this could be to optimize dual band LNA design using MOSFET as switch.

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# Thank You

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