Analog VLSI Circuit Final Project

Presented By-

Group-4

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Contents

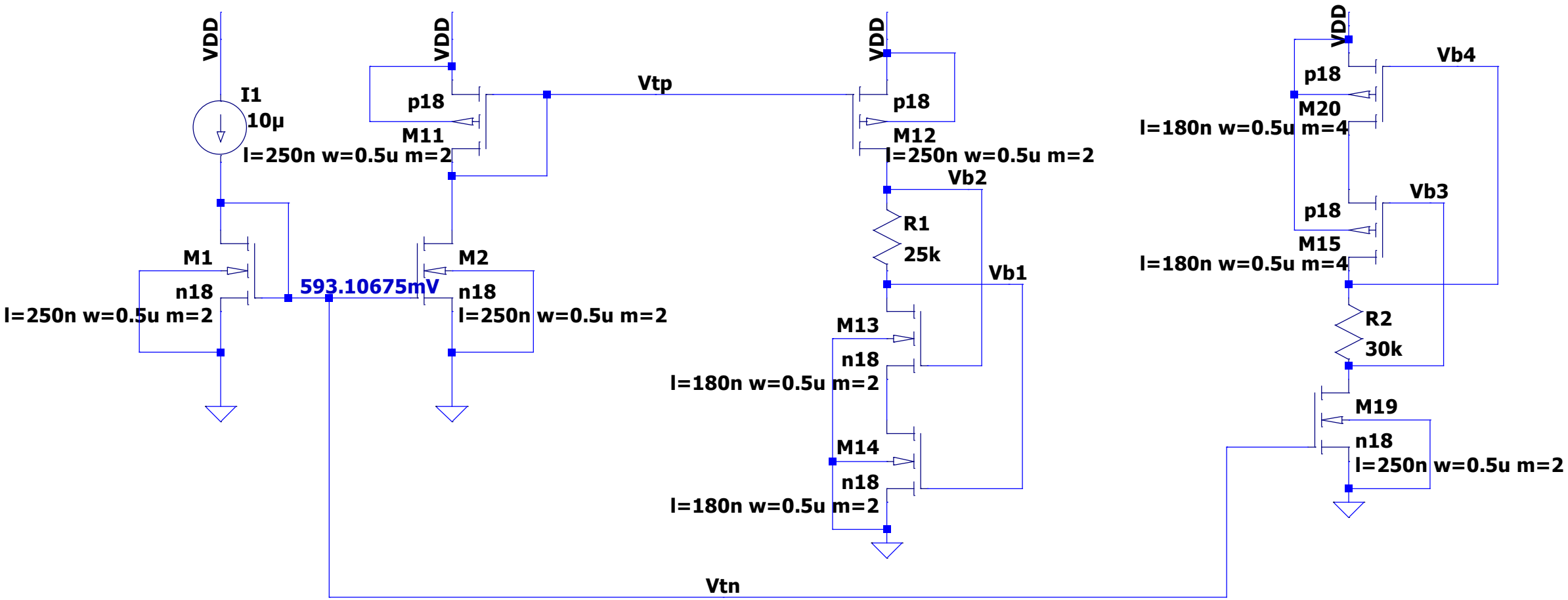
Objective

Design Requirements

- $A_v \geq 70\ dB$
- $UGF \geq 100MHz$
- Fully Differential OpAmp
- Rail-to-Rail input capability
- CMFB
- $C_L = 500fF$

Current Mirror

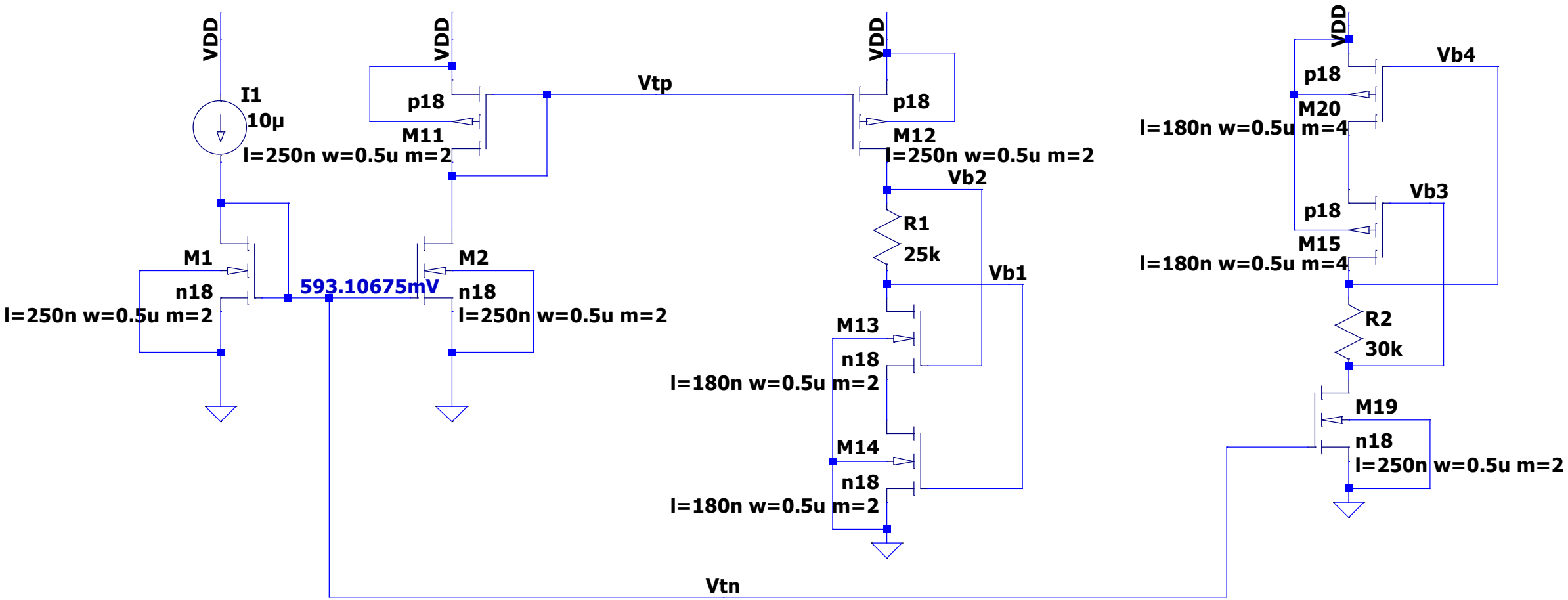
Current Mirror



Current Mirror

- V_{tp} – biases PMOS Tail Current for M0p Transistor
- V_{tn} – biases NMOS Tail Current for M0n Transistor and others
- V_{b1} – biases M3 and M4 Transistor(Lower NMOS Stack)
- V_{b2} – biases M5 and M6 Transistor(Upper NMOS Stack)
- V_{b3} – biases M7 and M8 Transistor(Lower PMOS Stack)
- V_{b4} – biases M9 and M10 Transistor(Upper PMOS Stack)

Current Mirror



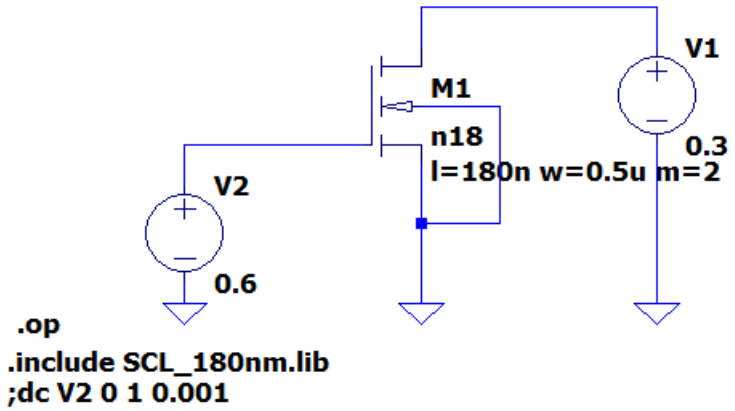
Folded Cascode Rail-to-Rail Design

Design Budgeting

- $UGF \approx \frac{g_m}{2\pi C_L} \geq 100\text{MHz}$
- $\Rightarrow g_m \geq 2\pi \times 100MHz \times C_L$
- $\Rightarrow g_m \geq 0.314mS$

- Let's choose g_m=1 mS
- Let the design $V_{in,cm}$=0.9V
- 0.6V – Vgs biasing
- 0.3V – Vdssat + margin for tail current source

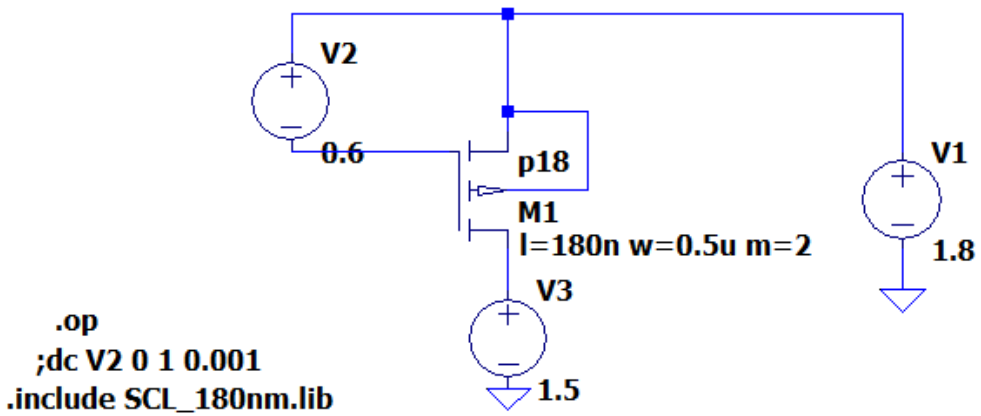
NMOS Characterization



Id:	1.13e-05
Vgs:	6.00e-01
Vds:	3.00e-01
Vbs:	0.00e+00
Vth:	4.82e-01
Vdsat:	1.30e-01
Gm:	1.34e-04

We must scale NMOS such that g_m=1mS $W_{req.d}=7.4*W_1$

PMOS Characterization



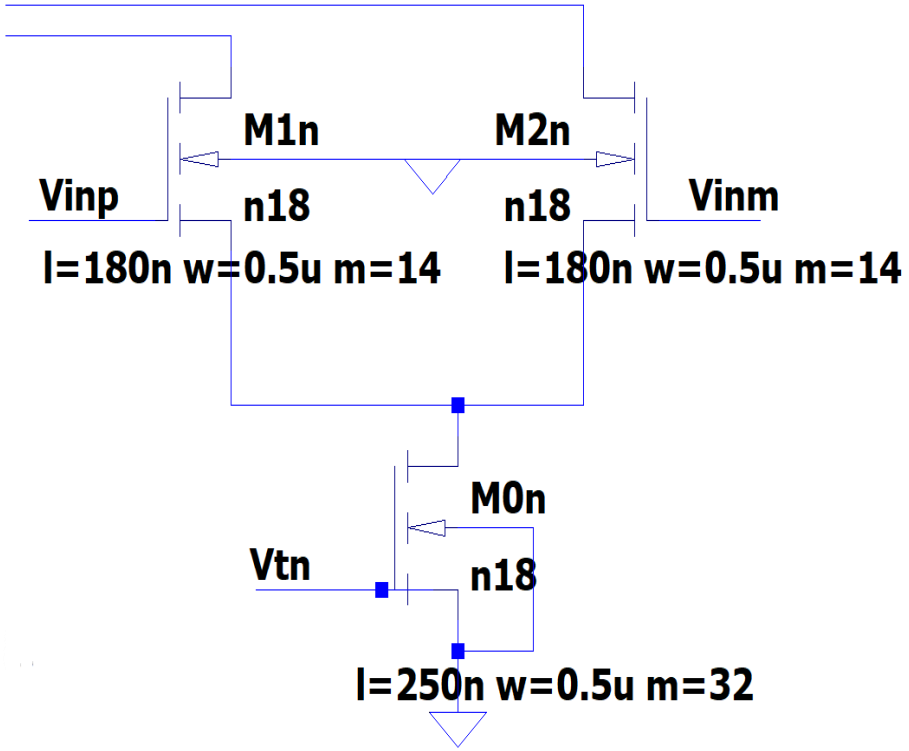
Id:	1.62e-06
Vgs:	6.00e-01
Vds:	3.00e-01
Vbs:	0.00e+00
Vth:	5.16e-01
Vdsat:	9.91e-02
Gm:	2.35e-05

We must scale PMOS such that g_m=1mS

W_{reqd}=42.5*W_1

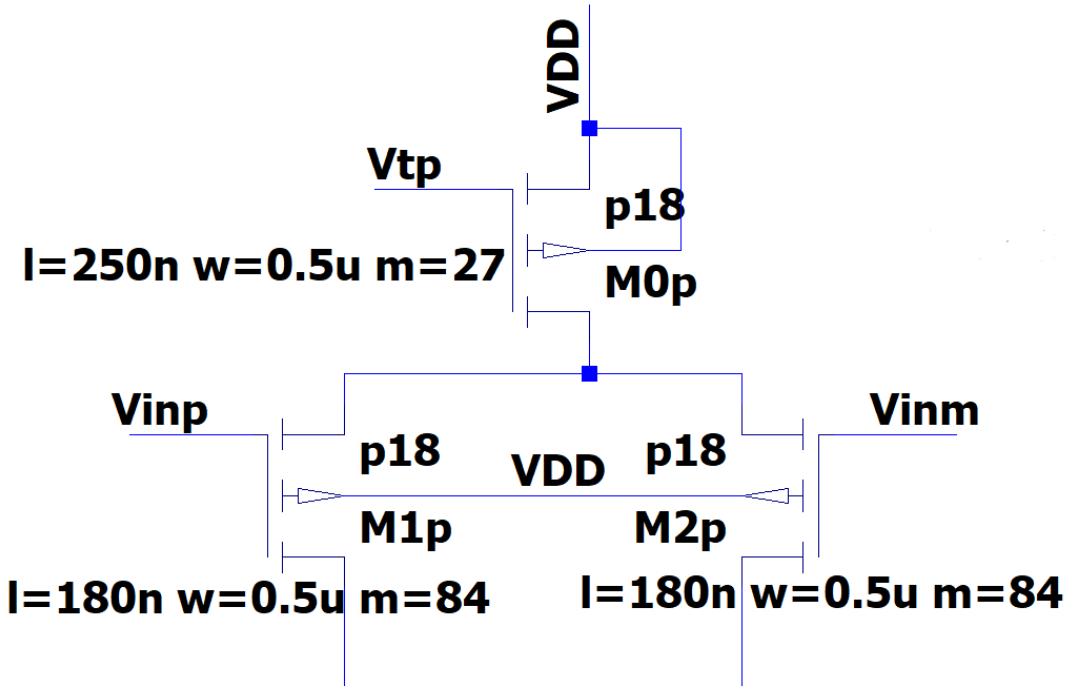
NMOS Input Pair

Name:	m1n	m2n	m0n
Model:	n18	n18	n18
Id:	7.39e-05	7.39e-05	1.48e-04
Vgs:	6.17e-01	6.17e-01	5.93e-01
Vds:	1.27e+00	1.27e+00	2.83e-01
Vbs:	-2.83e-01	-2.83e-01	0.00e+00
Vth:	5.30e-01	5.30e-01	4.63e-01
Vdsat:	1.12e-01	1.12e-01	1.42e-01
Gm:	9.75e-04	9.75e-04	1.69e-03
Gds:	1.99e-05	1.99e-05	5.83e-05

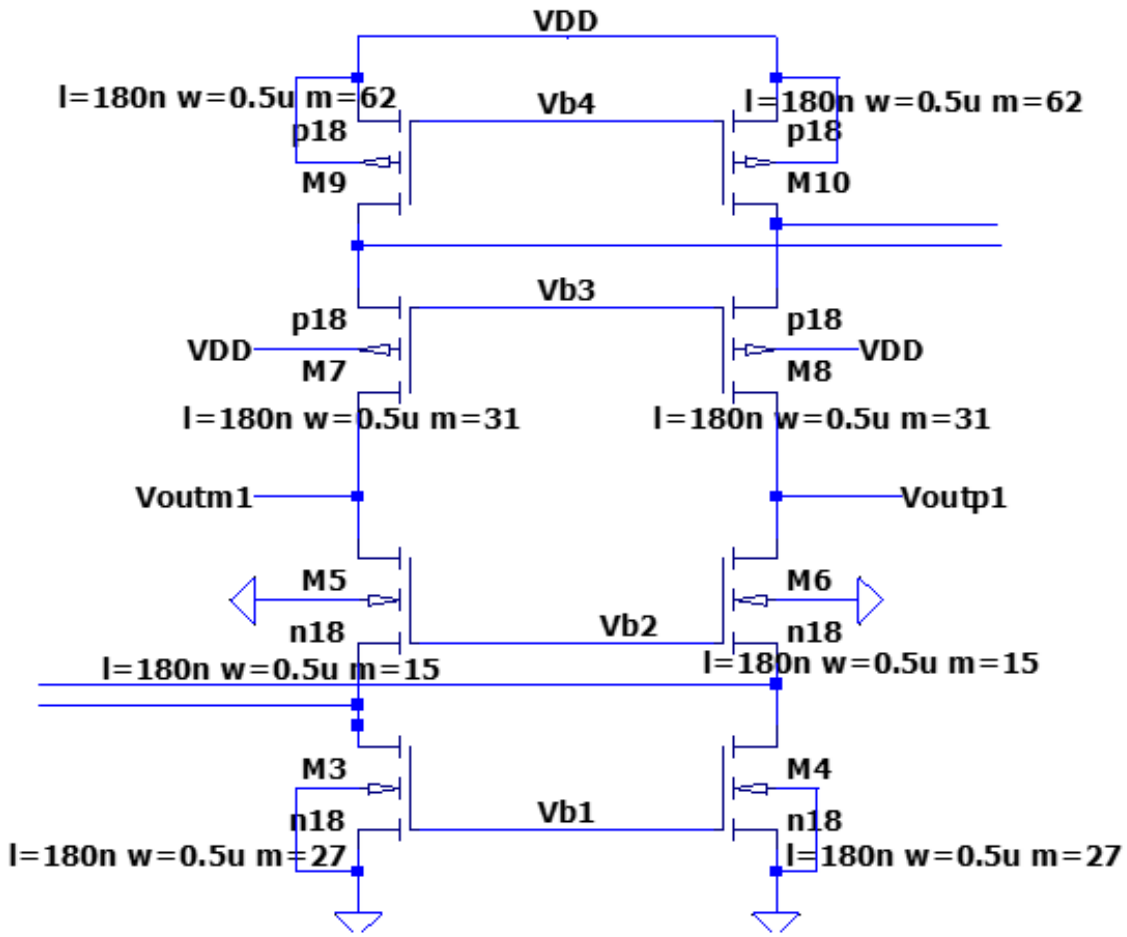


PMOS Input Pair

Name:	m1p	m2p	m0p
Model:	p18	p18	p18
Id:	-6.30e-05	-6.30e-05	-1.26e-04
Vgs:	-6.47e-01	-6.47e-01	-7.17e-01
Vds:	-1.30e+00	-1.30e+00	-2.53e-01
Vbs:	2.53e-01	2.53e-01	0.00e+00
Vth:	-5.30e-01	-5.86e-01	-4.32e-01
Vdsat:	-9.10e-02	-9.10e-02	-2.42e-01
Gm:	9.77e-04	9.77e-04	7.37e-04
Gds:	1.67e-05	1.67e-05	1.06e-04



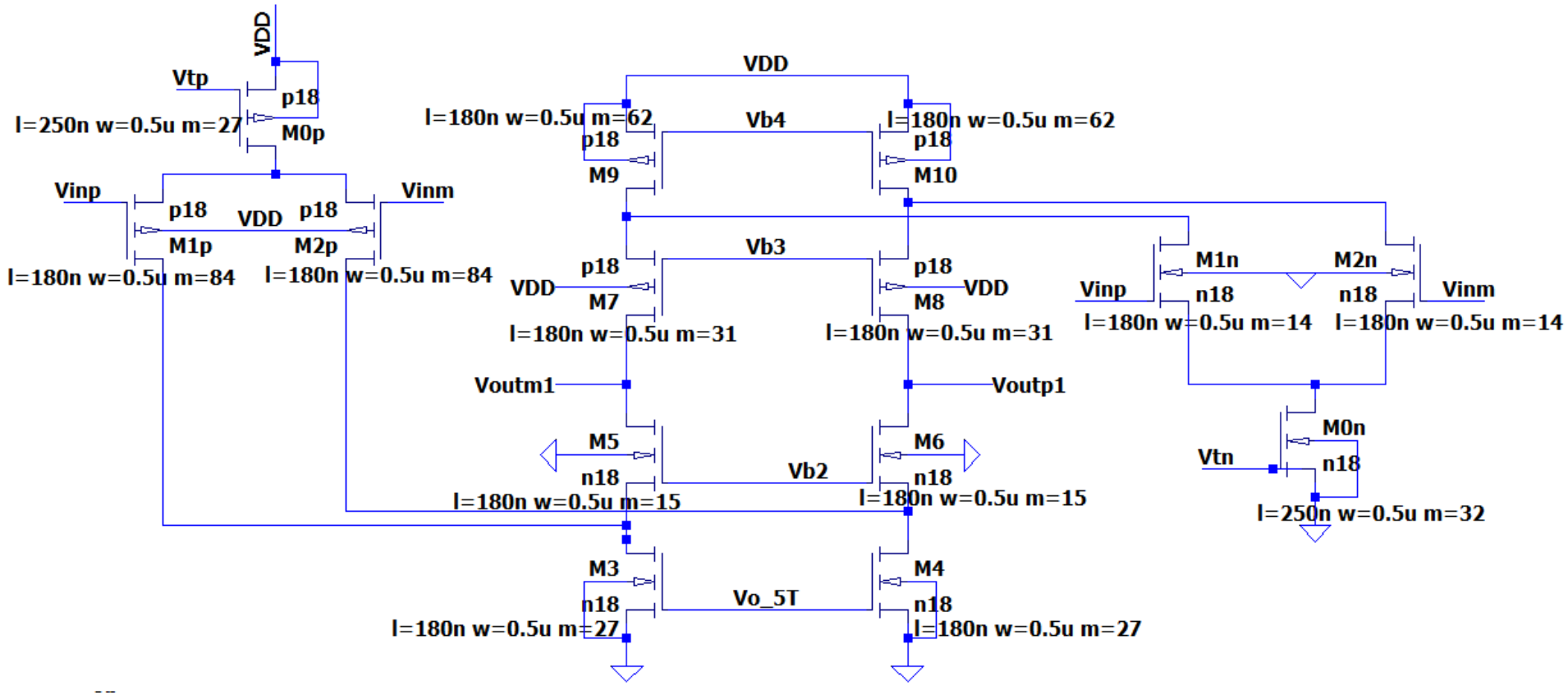
Main Transistor Stack



Main Transistor Stack

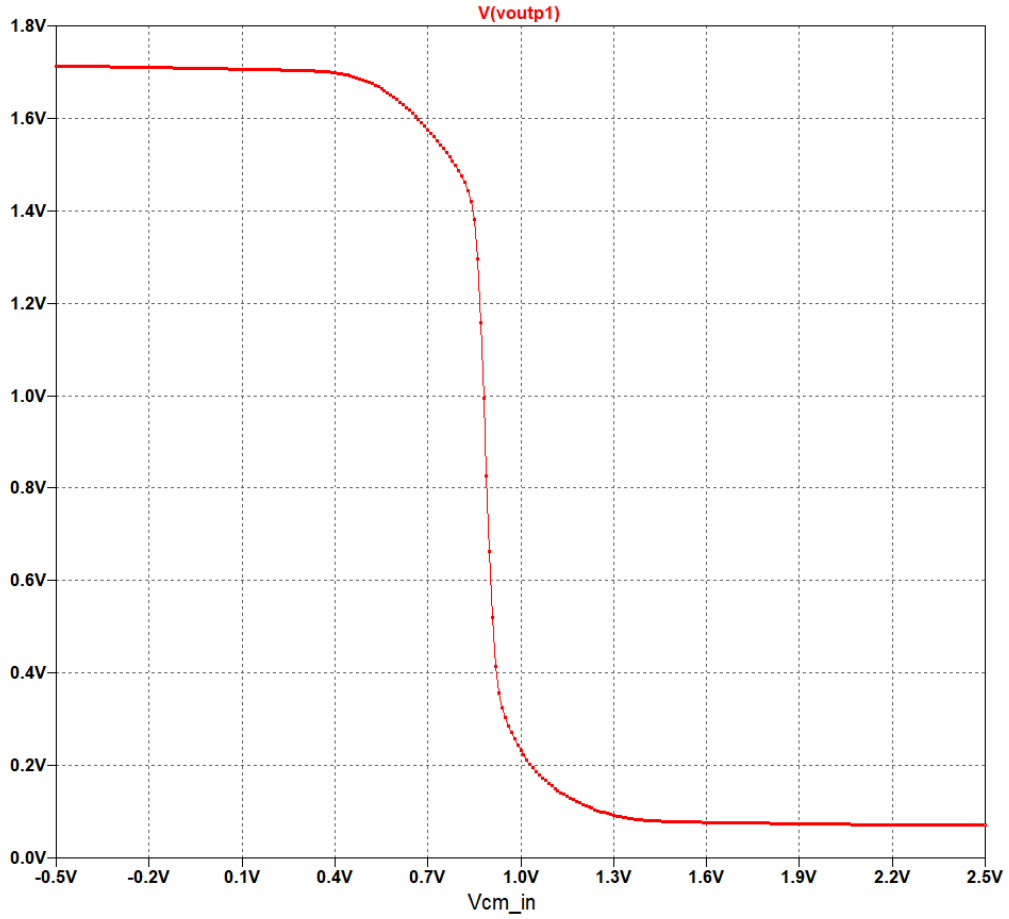
	M3	M5	M7	M9
I_D	149µA	86.1µA	86.1µA	160µA
V_{GS}	601mV	637mV	759mV	700mV
g_m	1.75mS	1.05mS	0.841mS	1.49mS
r_o	10.2kΩ	27.78kΩ	56.82kΩ	13.26kΩ

Circuit Design



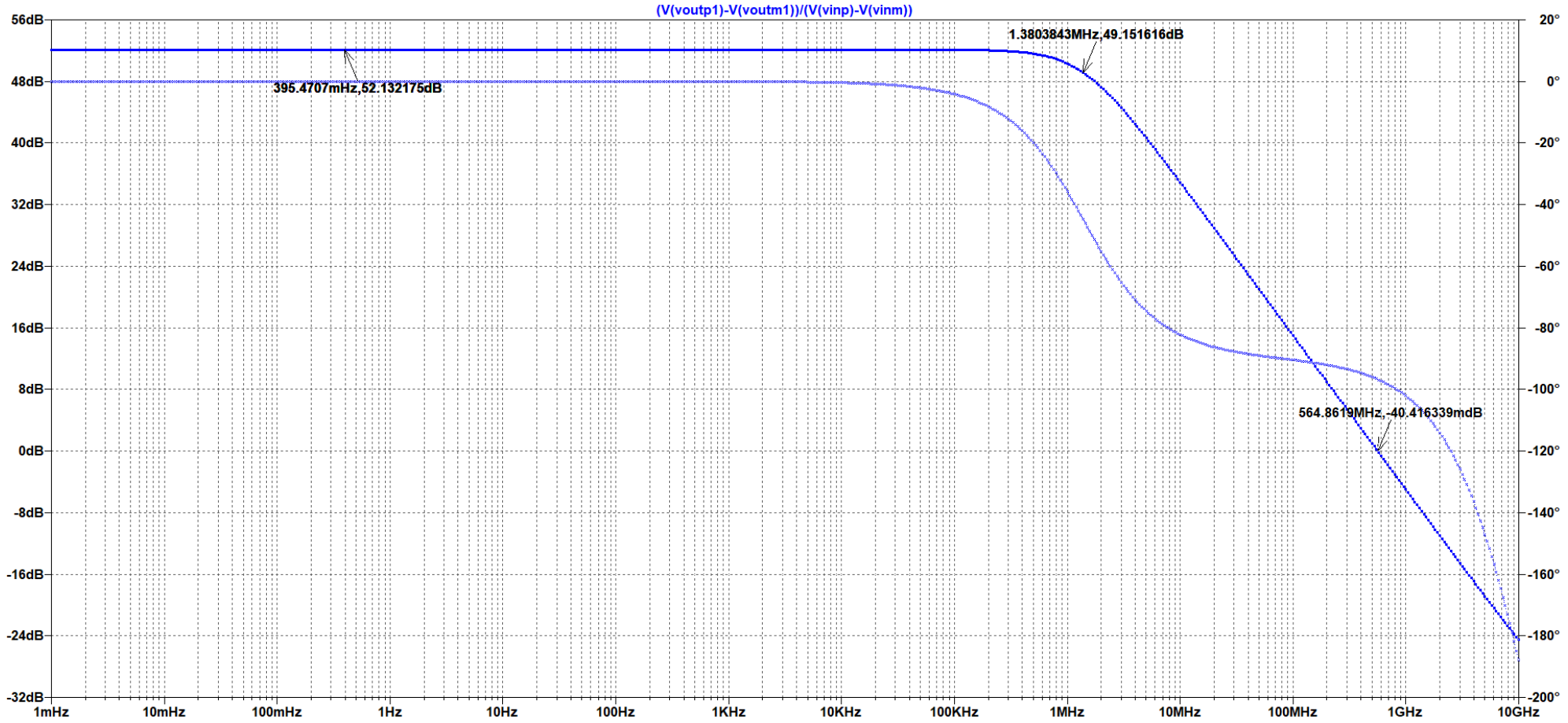
NMOS-PMOS Folded Cascode design

DC Analysis

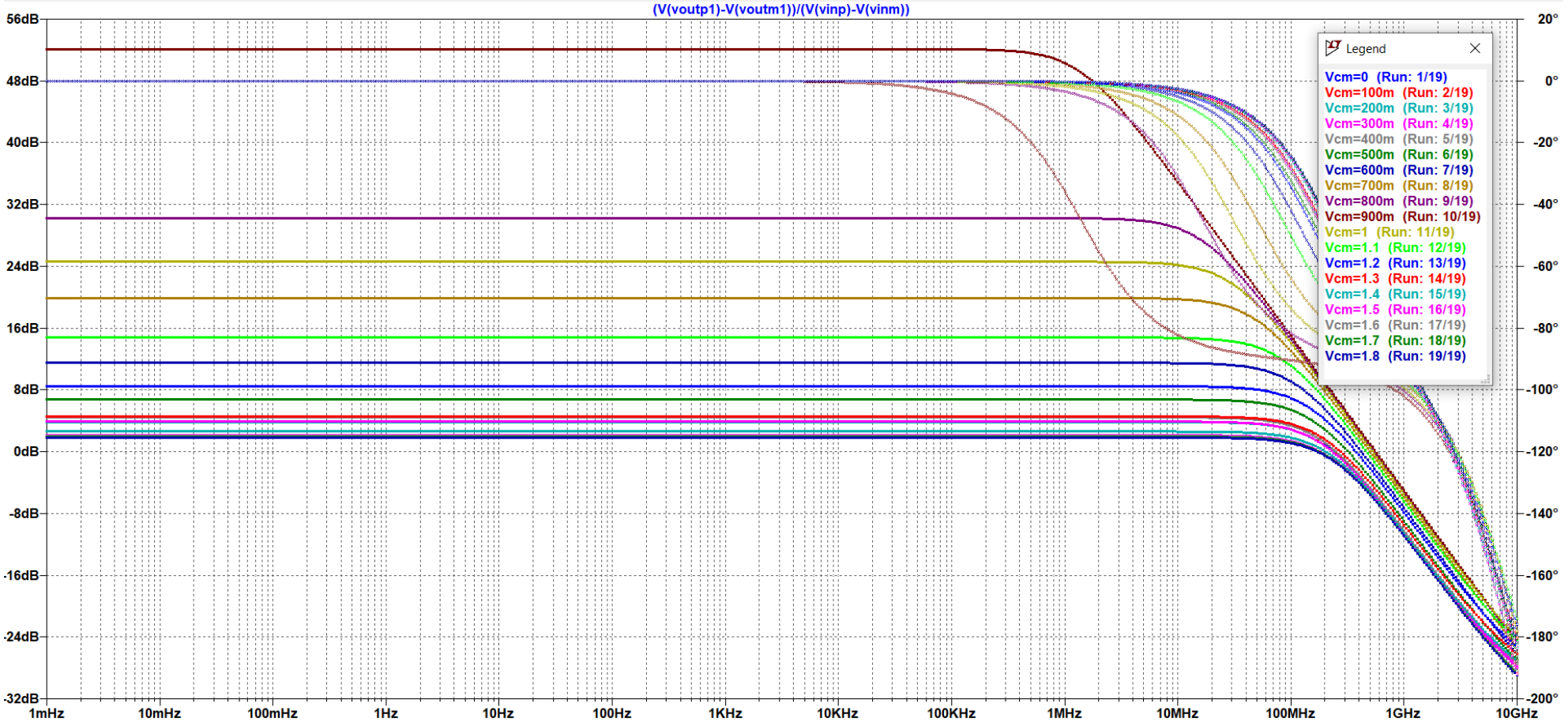


- Input CM Voltage
  - Sweep from -0.5V to 2.5V
- Output DC Voltage
  - Range: 0.7V to 1V
- Rail to Rail working capability
  - Input CM voltage
  - 0.7V to 1V

AC Analysis(V_{cm}=0.9V)



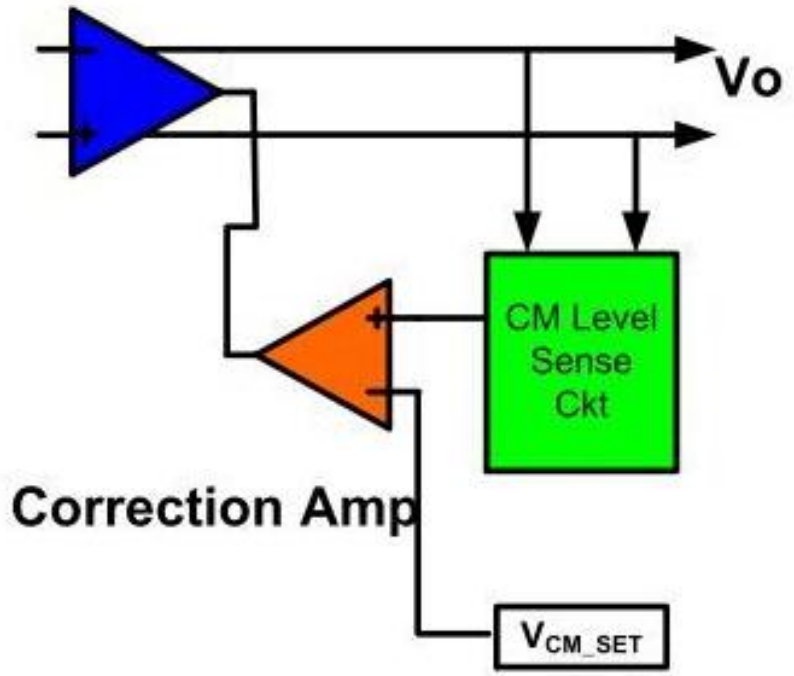
AC Analysis


(V(voutp1)-V(voutm1))/(V(vinp)-V(vinm))
56dB
48dB
40dB
32dB
24dB
16dB
8dB
0dB
-8dB
-16dB
-24dB
-32dB
20°
0°
-20°
-40°
-60°
-80°
-100°
-120°
-140°
-160°
-180°
-200°
1mHz
10mHz
100mHz
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
100MHz
1GHz
10GHz
Legend
Vcm=0 (Run: 1/19)
Vcm=100m (Run: 2/19)
Vcm=200m (Run: 3/19)
Vcm=300m (Run: 4/19)
Vcm=400m (Run: 5/19)
Vcm=500m (Run: 6/19)
Vcm=600m (Run: 7/19)
Vcm=700m (Run: 8/19)
Vcm=800m (Run: 9/19)
Vcm=900m (Run: 10/19)
Vcm=1 (Run: 11/19)
Vcm=1.1 (Run: 12/19)
Vcm=1.2 (Run: 13/19)
Vcm=1.3 (Run: 14/19)
Vcm=1.4 (Run: 15/19)
Vcm=1.5 (Run: 16/19)
Vcm=1.6 (Run: 17/19)
Vcm=1.7 (Run: 18/19)
Vcm=1.8 (Run: 19/19)

CMFB

Principle of CMFB

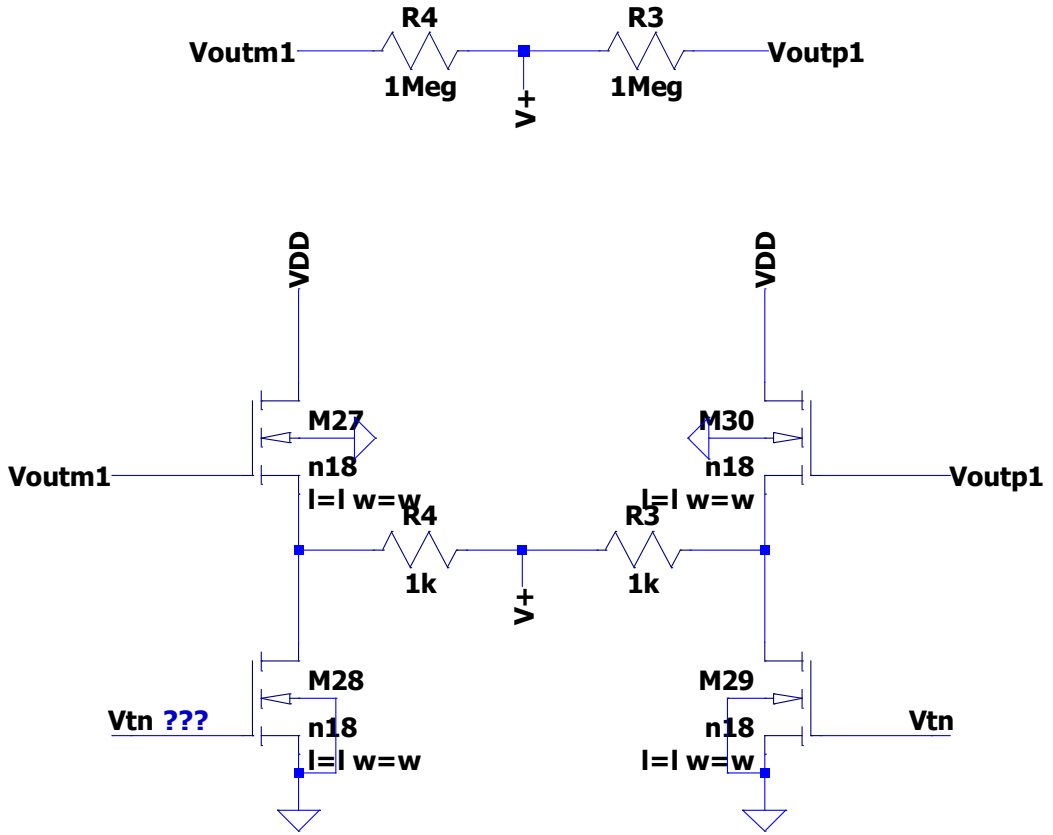
- Common Mode Feedback to correct for V_{cm} because of variation in PMOS and NMOS current pairs
- Compare the Common mode voltage to reference voltage
- Output signal of CMFB Stage can be fed back
- Providing it on gate terminal helps in controlling V_{gs} and hence, current through it.



Detection of Common mode voltage

- Sensed by simple resistor
- But direct resistor comes parallel to R_{out}
- Results in low gain
- Require high value of Resistor

- Solution is to use buffer stage
- Followed by low value resistor to detect the output V_{CM}



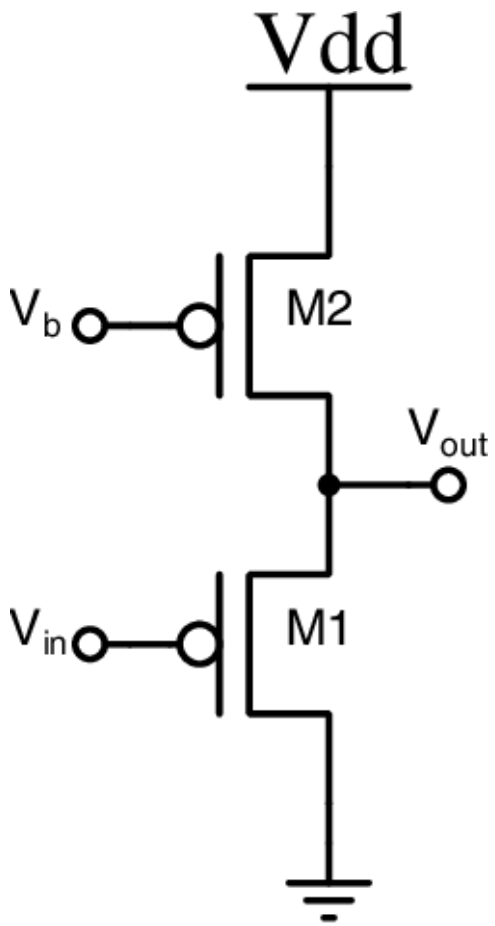
Source Follower

Benefits:

- Very high input impedance

Price:

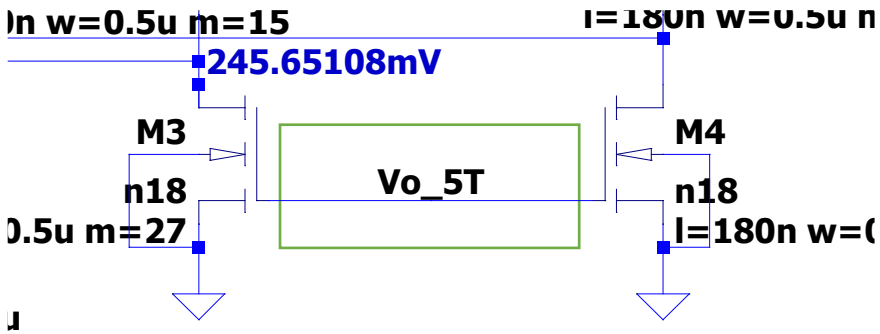
- Voltage(V_{GS}) drop across the M2 transistor
- Reference voltage = V_{CMref}- V_{GS}

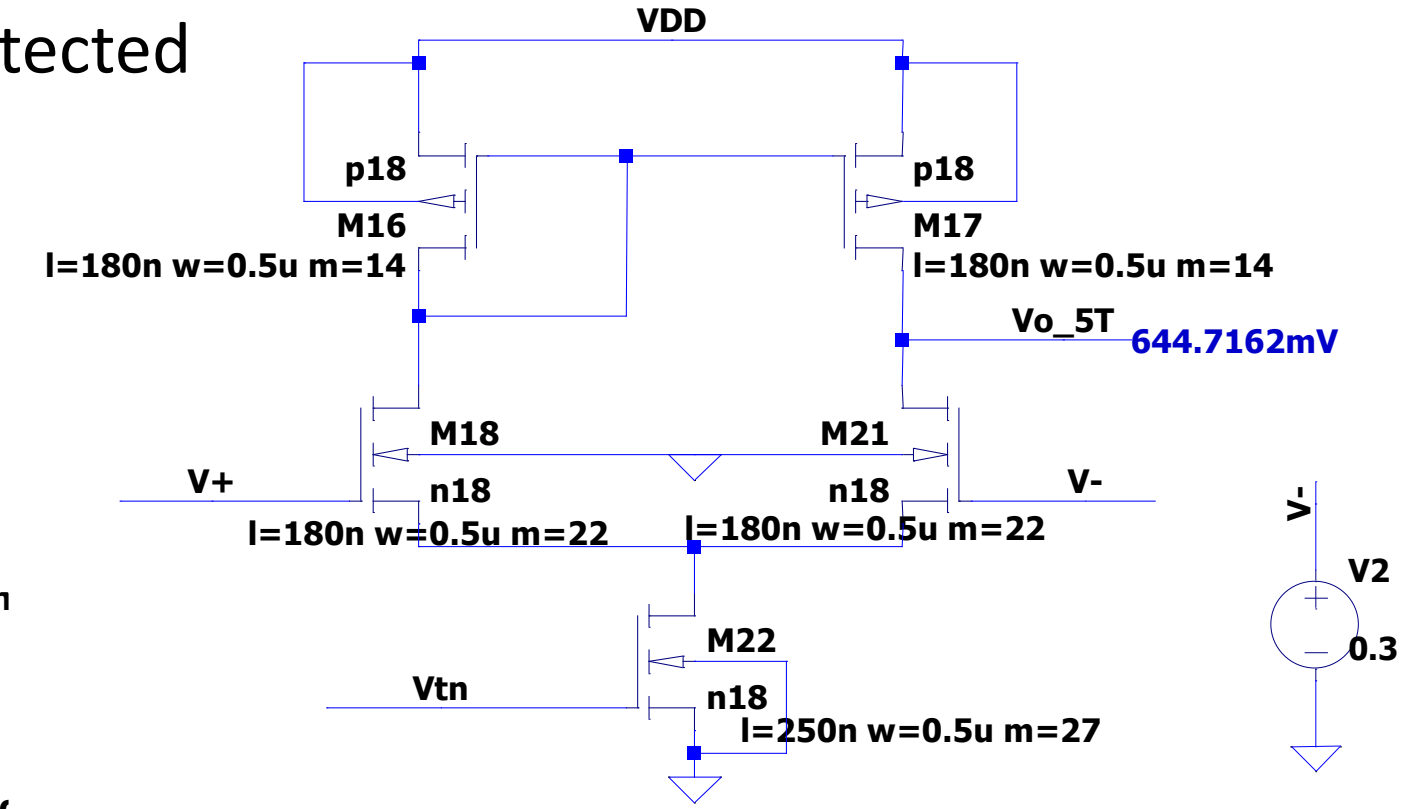


- V_{CMref} = 0.9V
- V_{GS} = 0.593V ≈ 0.6V

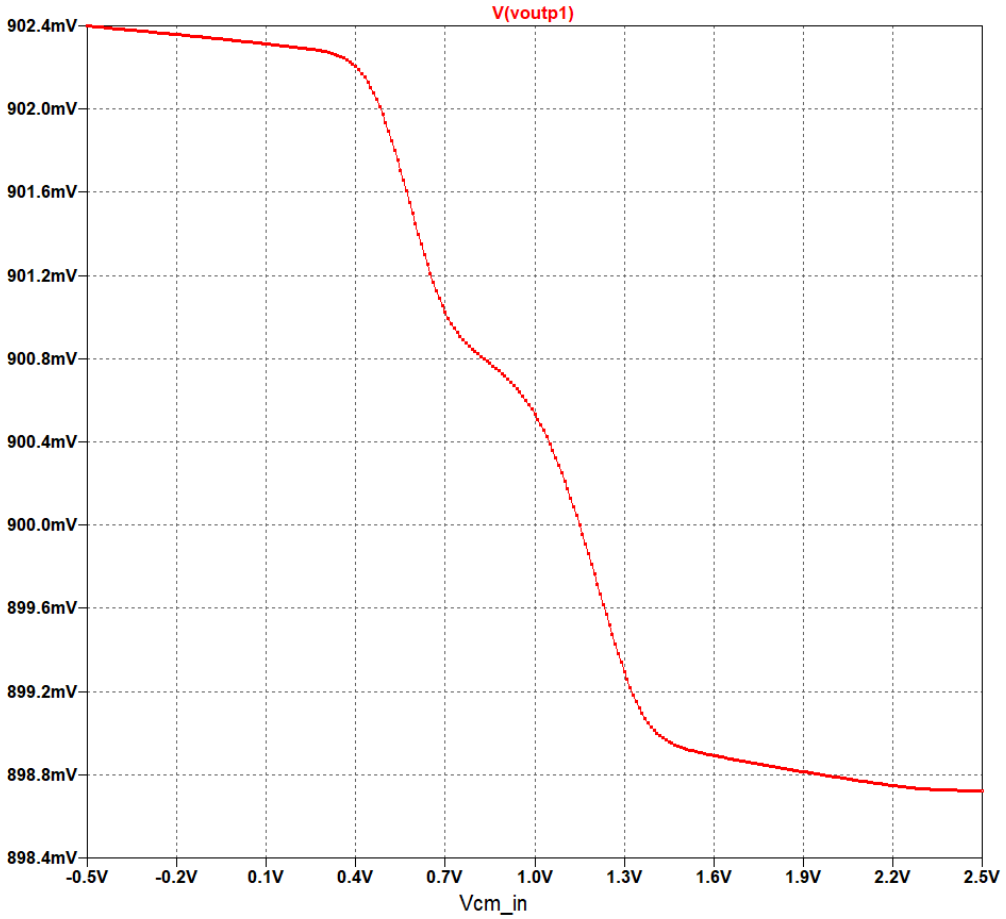
Correction for Common Mode voltage

- Common Mode voltage detected
- CMFB stage: 5T OTA
- Output: Vo_5T
- Reference voltage : (V-)
  - $(V-) = V_{CMref} - V_{GS} = 0.3$





DC Analysis

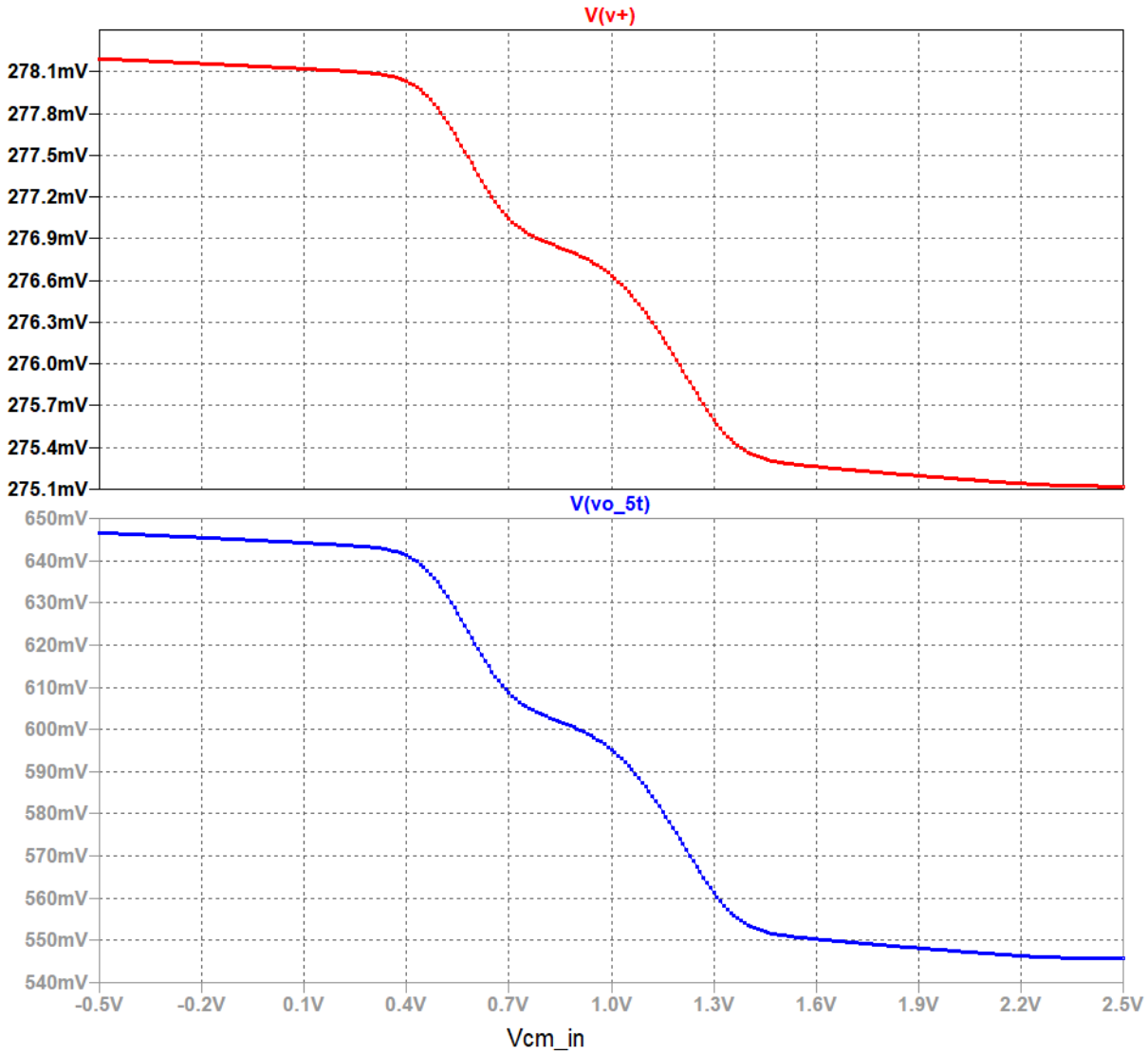


- Input CM Voltage
  - Sweep from -0.5V to 2.5V
- Output DC Voltage
  - Not much Variation.

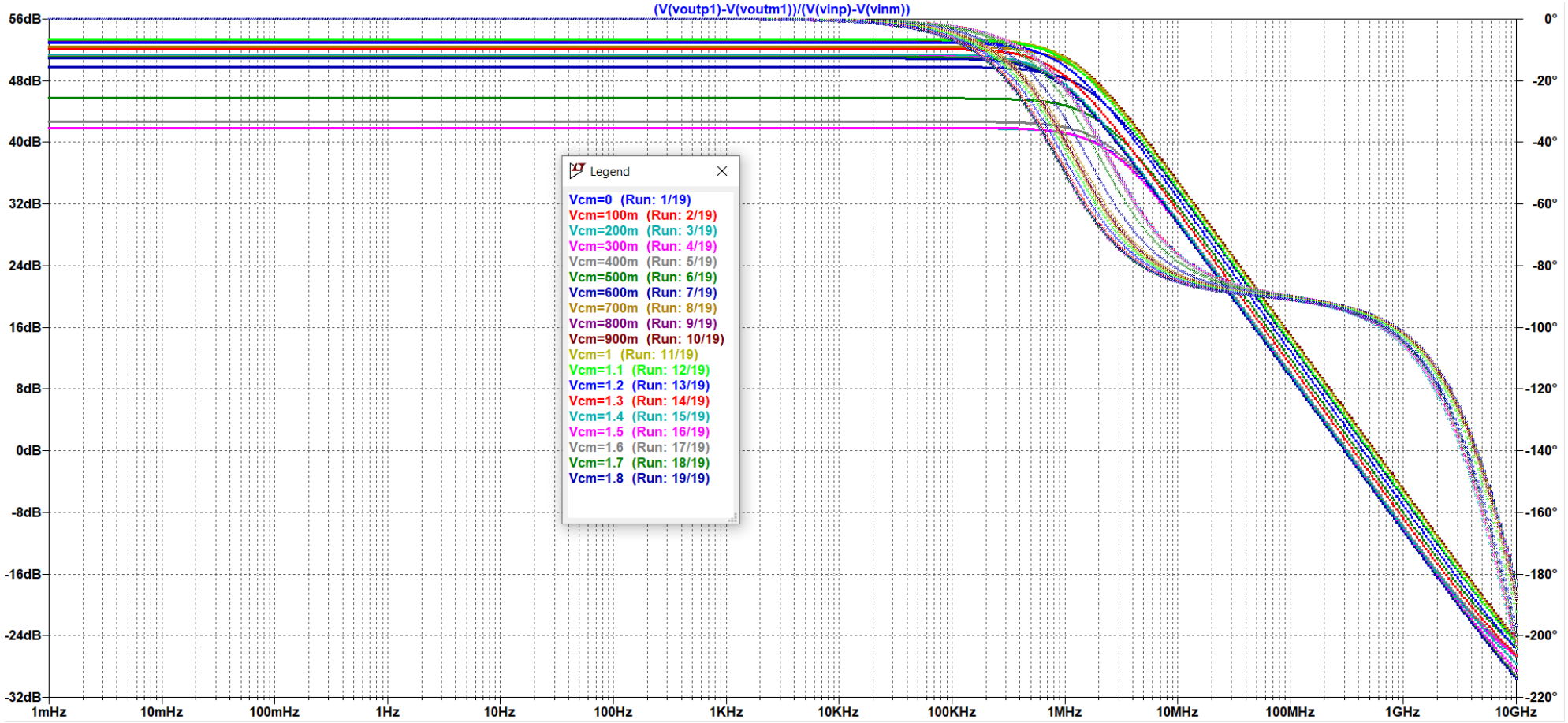
- Rail to Rail working capability
  - Input CM voltage
  - Full Range

DC Analysis

- Input CM Voltage
  - Sweep from -0.5V to 2.5V
- Output CM Voltage
  - Range: 0.4V to 1.4V
- Output of CMFB Stage
  - Range: 0.4V to 1.4V
  - Similar behavior



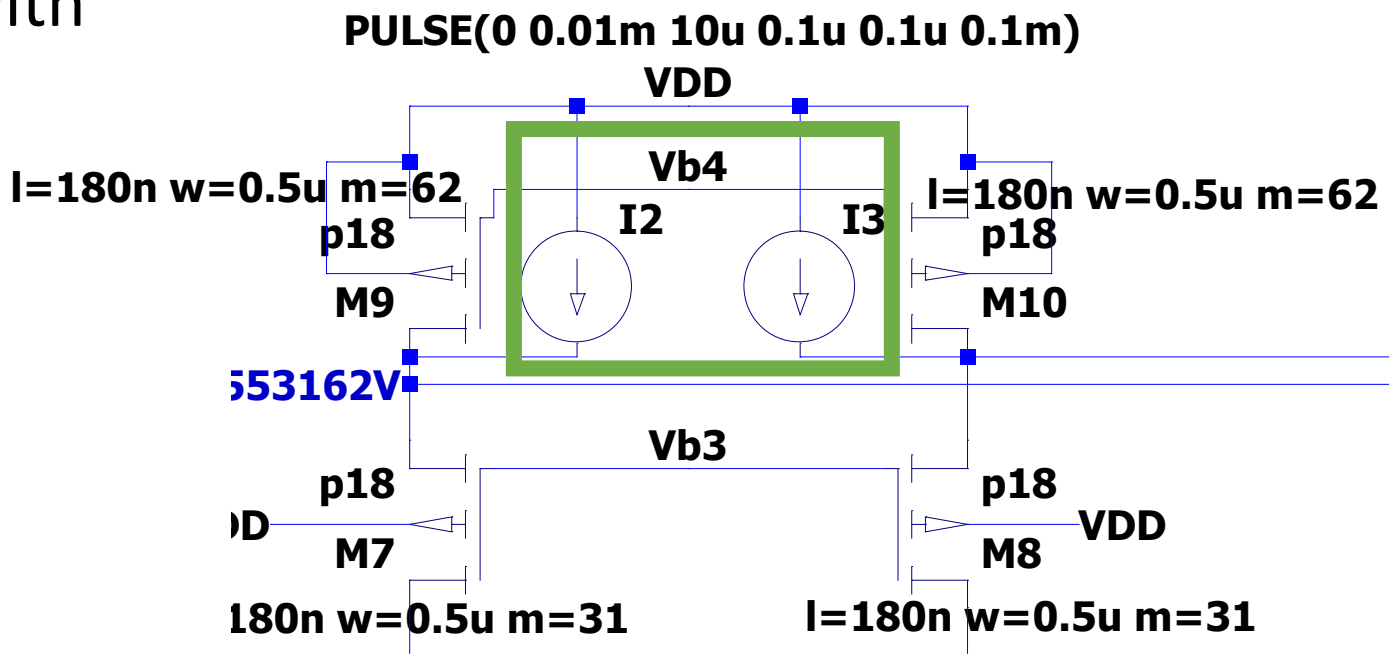
AC Analysis



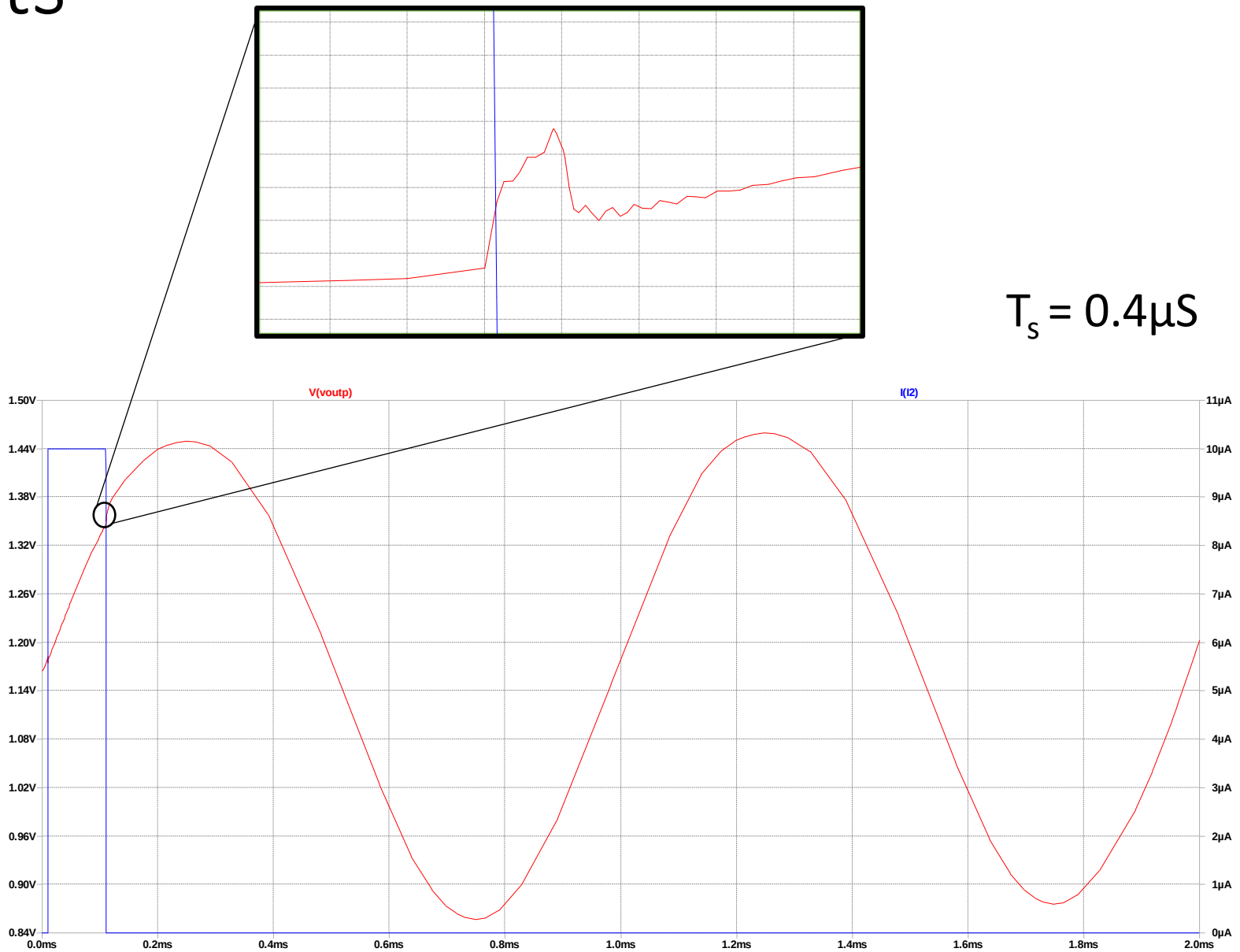
Folded cascode with CMFB

Transient Analysis

- To simulate current disturbance: extra current source used.
- Current sources in parallel with the MOSFET
- Current source: Pulse input

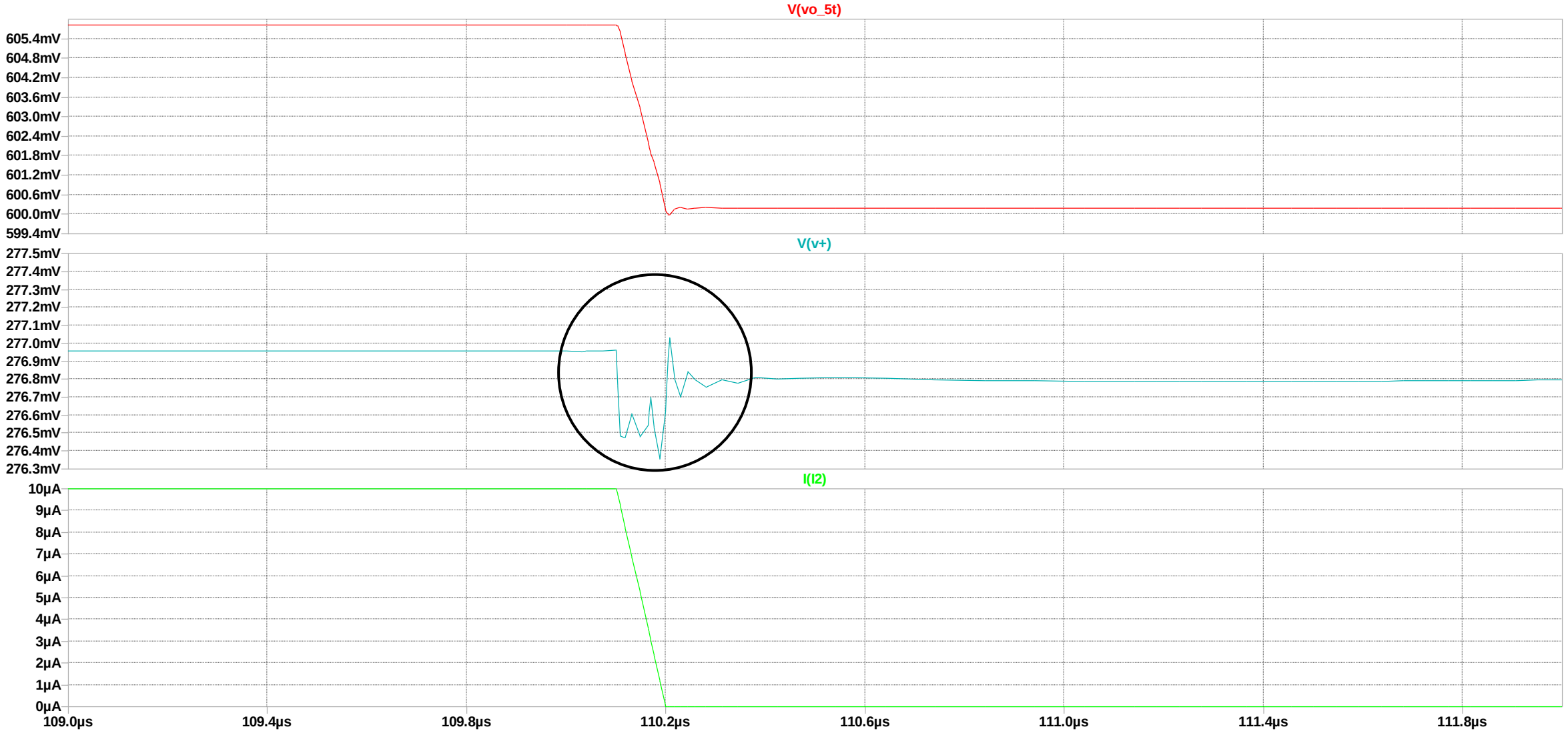


Results


$T_s = 0.4\mu S$
V(voutp)
I(I2)
1.50V
1.44V
1.38V
1.32V
1.26V
1.20V
1.14V
1.08V
1.02V
0.96V
0.90V
0.84V
11µA
10µA
9µA
8µA
7µA
6µA
5µA
4µA
3µA
2µA
1µA
0µA
0.0ms
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms
2.0ms

Transient Voltage analysis

$T_s = 0.4\mu S$

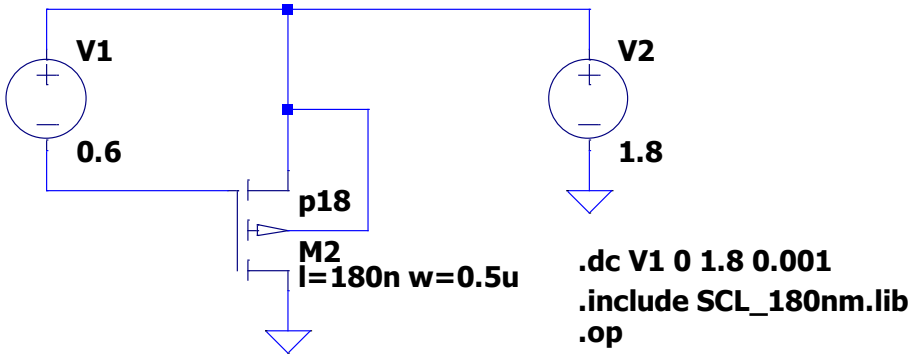


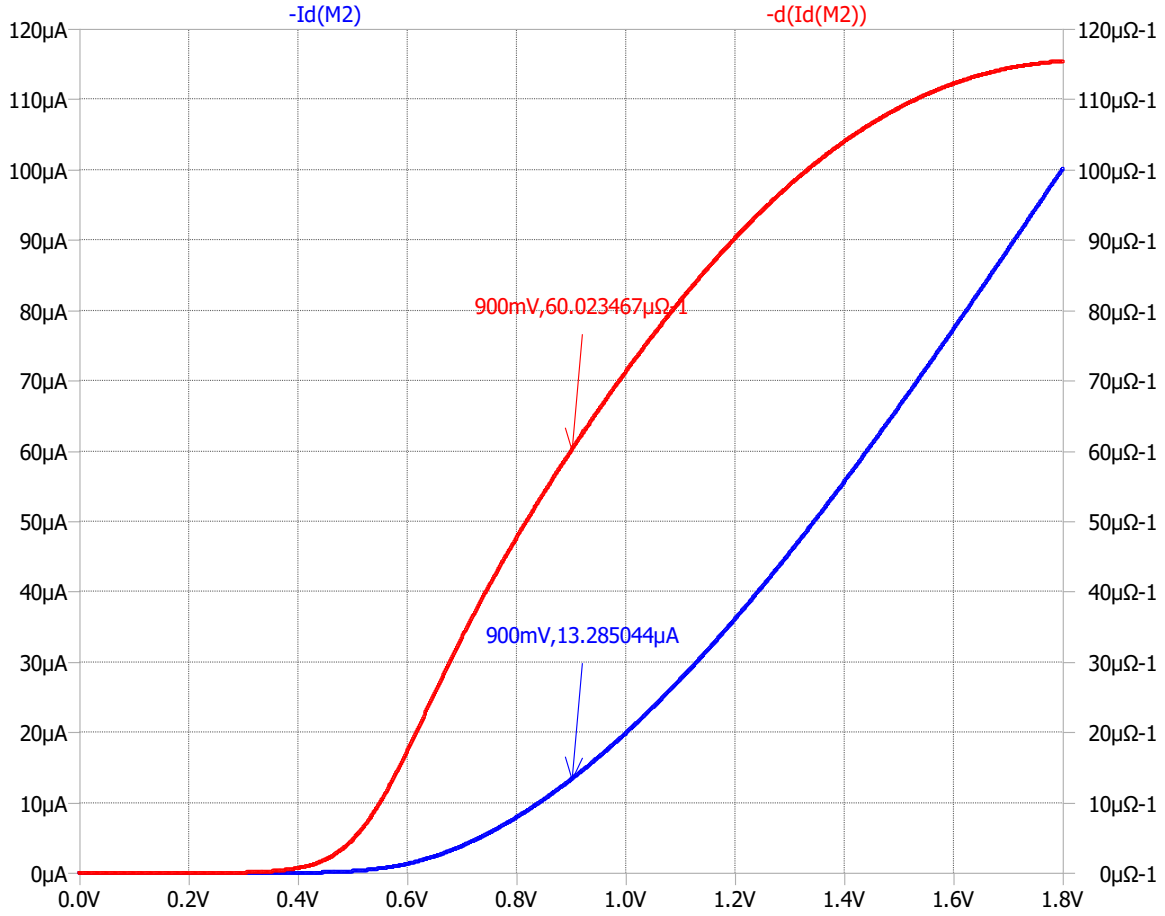
2nd Stage

Design Budgeting

- Common source amplifier
- Design parameters:
  - V_{gs}(for second stage)
    - $V_{gs} = V_{DD} - V_{CMRef}$ = 1.8V-0.9V = 0.9V
  - $A_{v,req}$(Required gain) $\sim 25dB$ = 17.78
- Calculation:
  - $A_{v,req}$= 17.78 = $g_m * R_{out}$
  - *(2.22m) * (8kΩ)* = 17.78
  - $R_{out} \sim 8k\Omega$
  - $g_m \approx 2.22mS$

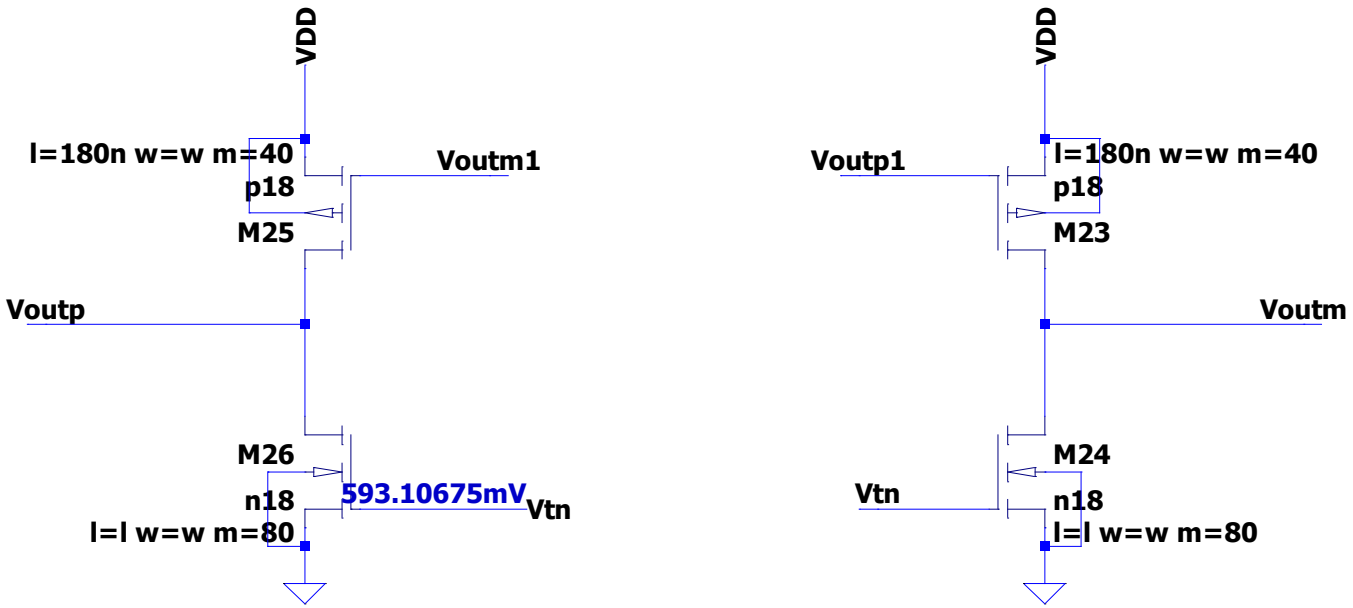
PMOS Characterization





- Scaling factor(multipliers) = $\frac{2.22mS}{60.023467\mu S}$ = 36.98 ≈ 37

2nd Stage Design



2nd Stage Circuit

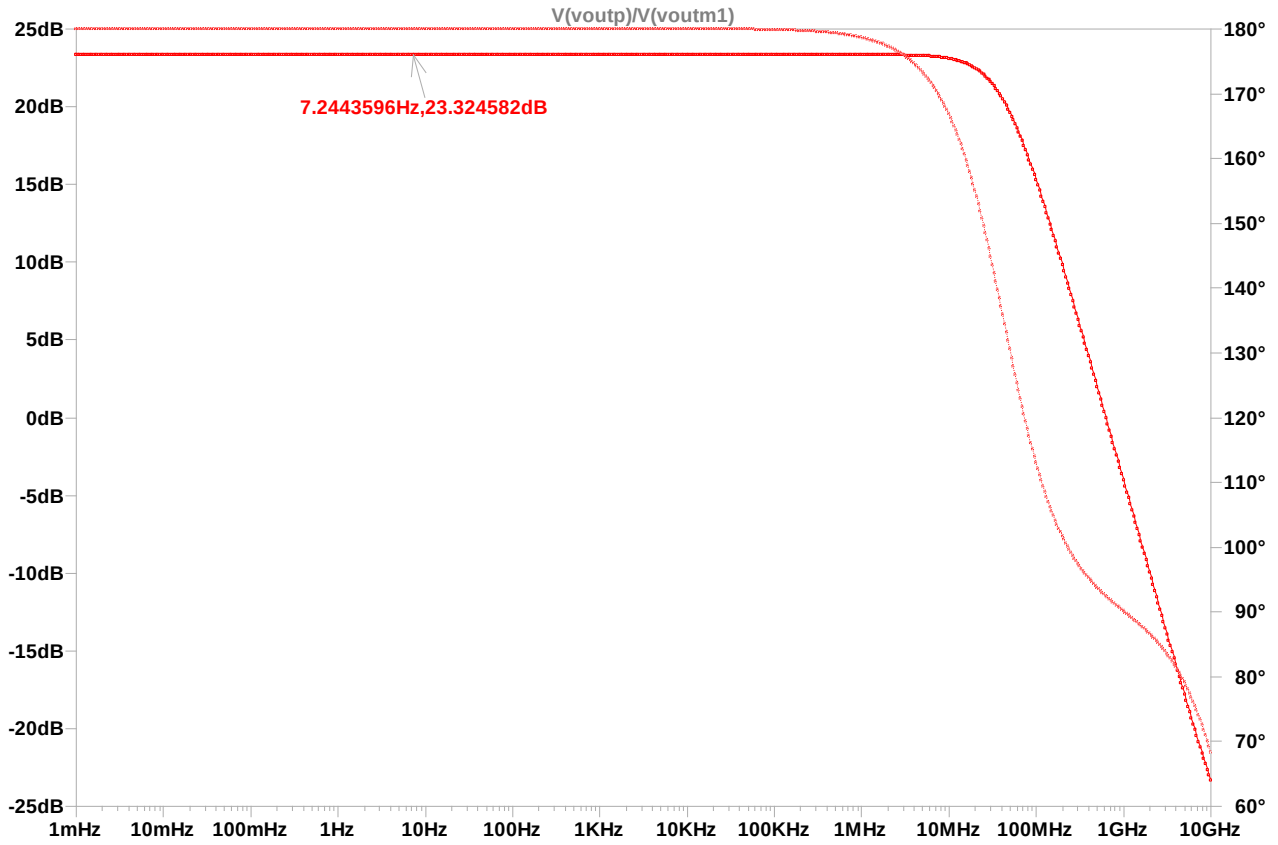
Name:	m6	m25	m23	m17	m16
Model:	n18	p18	p18	p18	p18
Id:	1.54e-04	-4.30e-04	-4.30e-04	-2.85e-07	-2.08e-07
Vgs:	6.76e-01	-8.98e-01	-8.98e-01	-3.94e-01	-3.94e-01
Vds:	7.02e-01	-6.57e-01	-6.57e-01	-1.16e+00	-3.94e-01
Vbs:	-2.01e-01	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	5.19e-01	-5.14e-01	-5.14e-01	-5.11e-01	-5.16e-01
Vdsat:	1.54e-01	-3.00e-01	-3.00e-01	-3.91e-02	-3.89e-02
Gm:	1.50e-03	2.04e-03	2.04e-03	6.47e-06	4.75e-06
Gds:	4.15e-05	9.37e-05	9.37e-05	1.09e-07	9.38e-08

Operating Point

Simulation Results

- g_m = 2.04mS
- R_{out} = 10.672kΩ
- Gain(A_v) = 23.32dB
- Cut-off Frequency(f_c)

$$\frac{1}{2\pi RoutCout} = 29.83\text{MHz}$$



Gain Plot

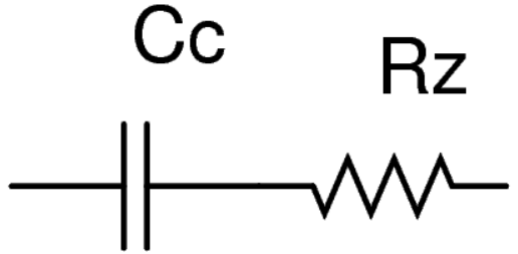
Phase Compensation(Miller compensation)

- Resistor Calculation:

  $R_z > \frac{1}{g_m}$

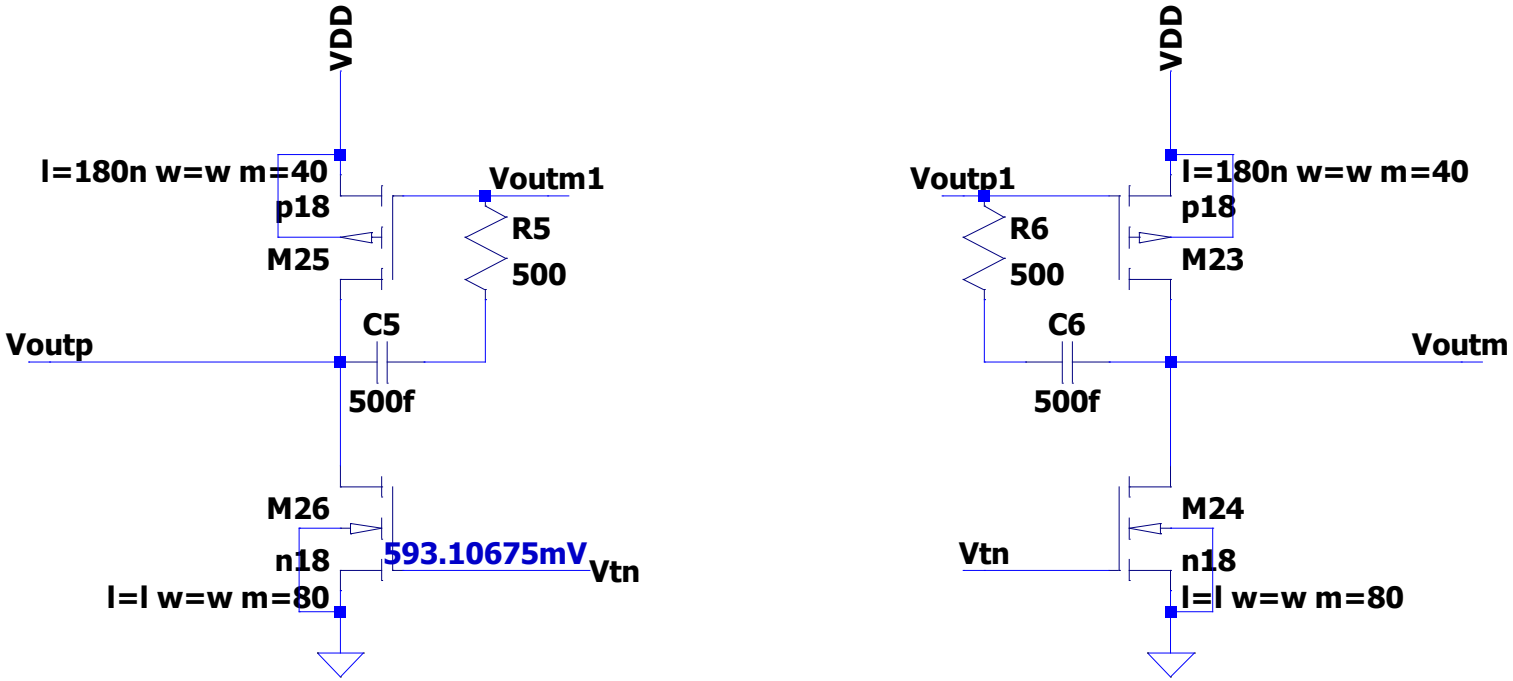
  $\frac{1}{g_m}$ = 490.196Ω

  Taking R_z=500Ω



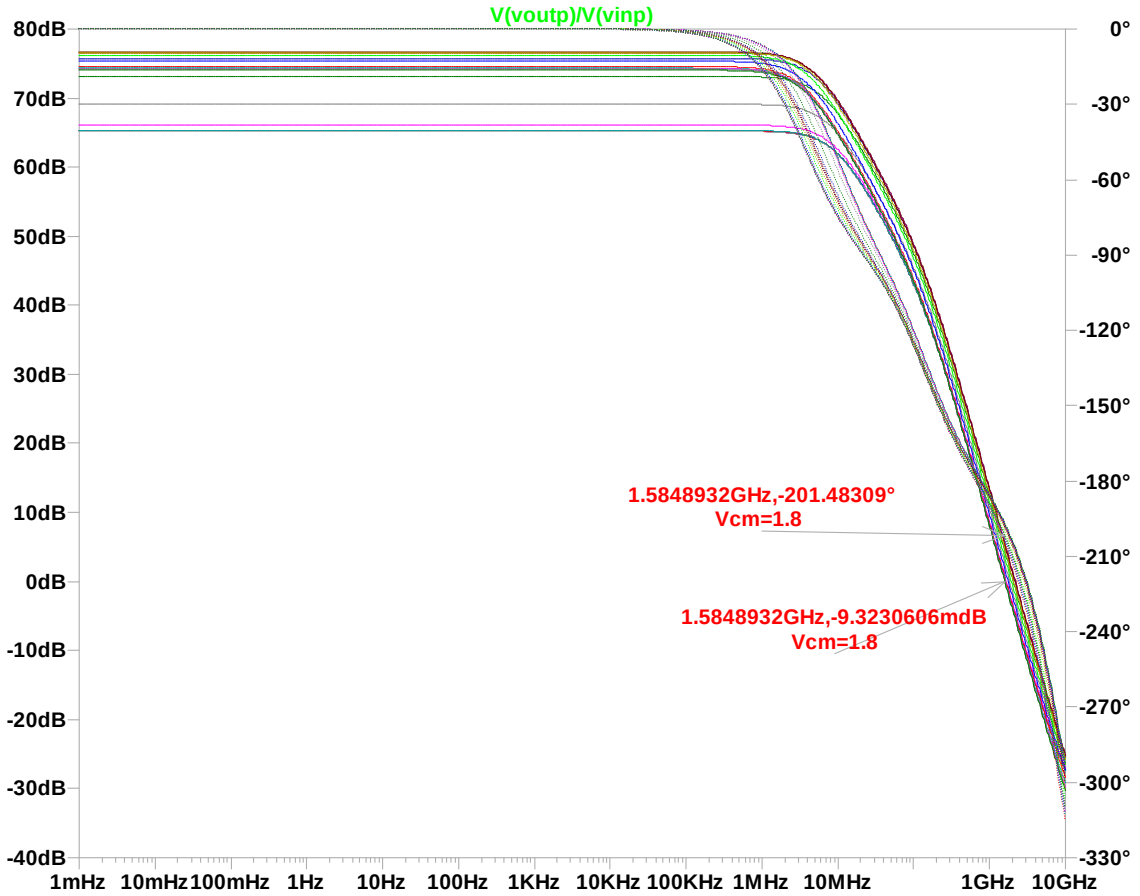
- Taking arbitrary value for capacitor c_c = 500fF

Circuit Design



2nd Stage with miller compensation(between 1st and 2nd stage)

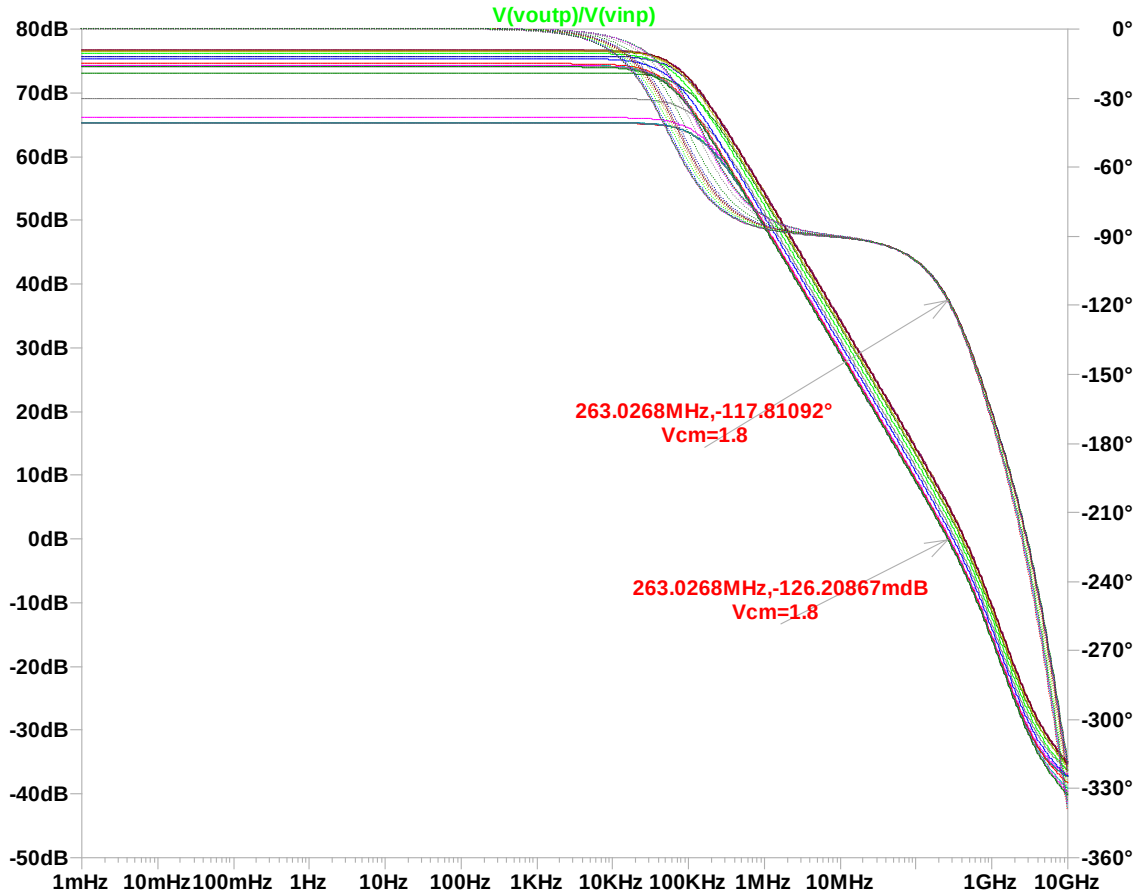
Simulation result



Without Miller Compensation

Gain Cross-over frequency = 1.584GHz

Phase margin = -201.48+180 = -21.48(Unstable)



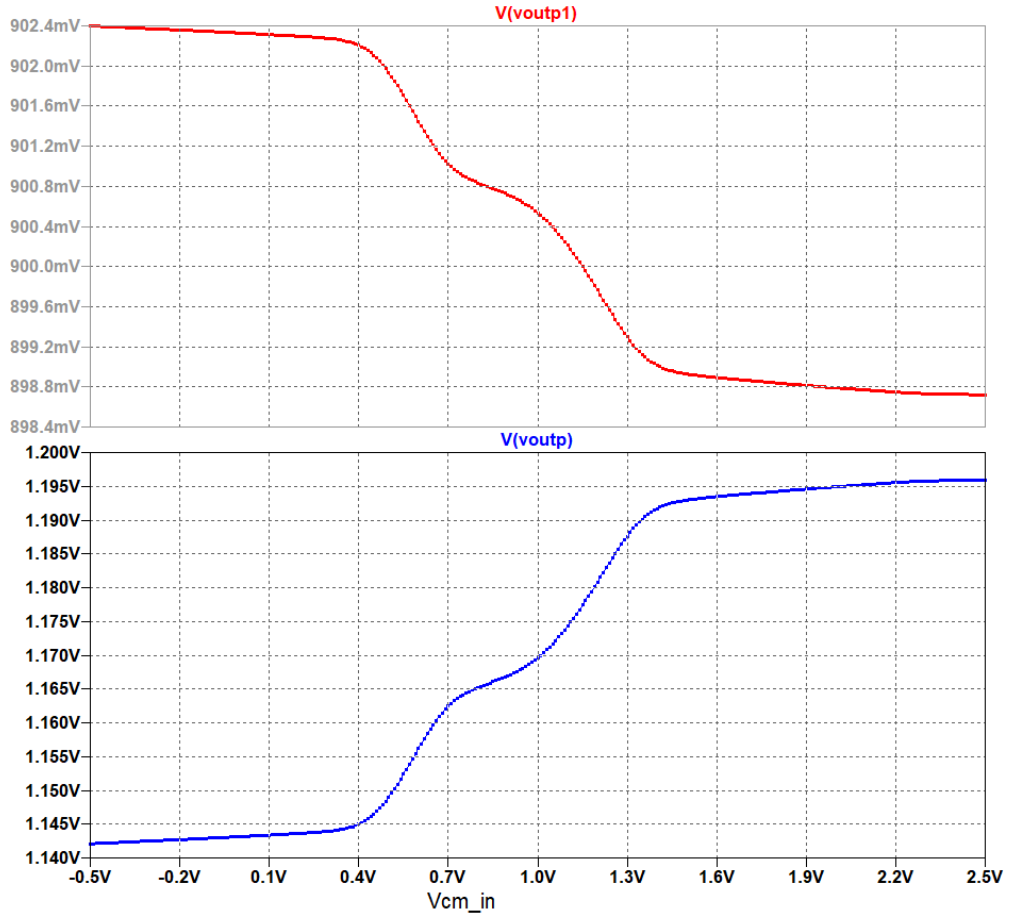
With Miller Compensation

Gain Cross-over frequency = 263.02 MHz

Phase margin = -117.81+180 = 62.19(stable)

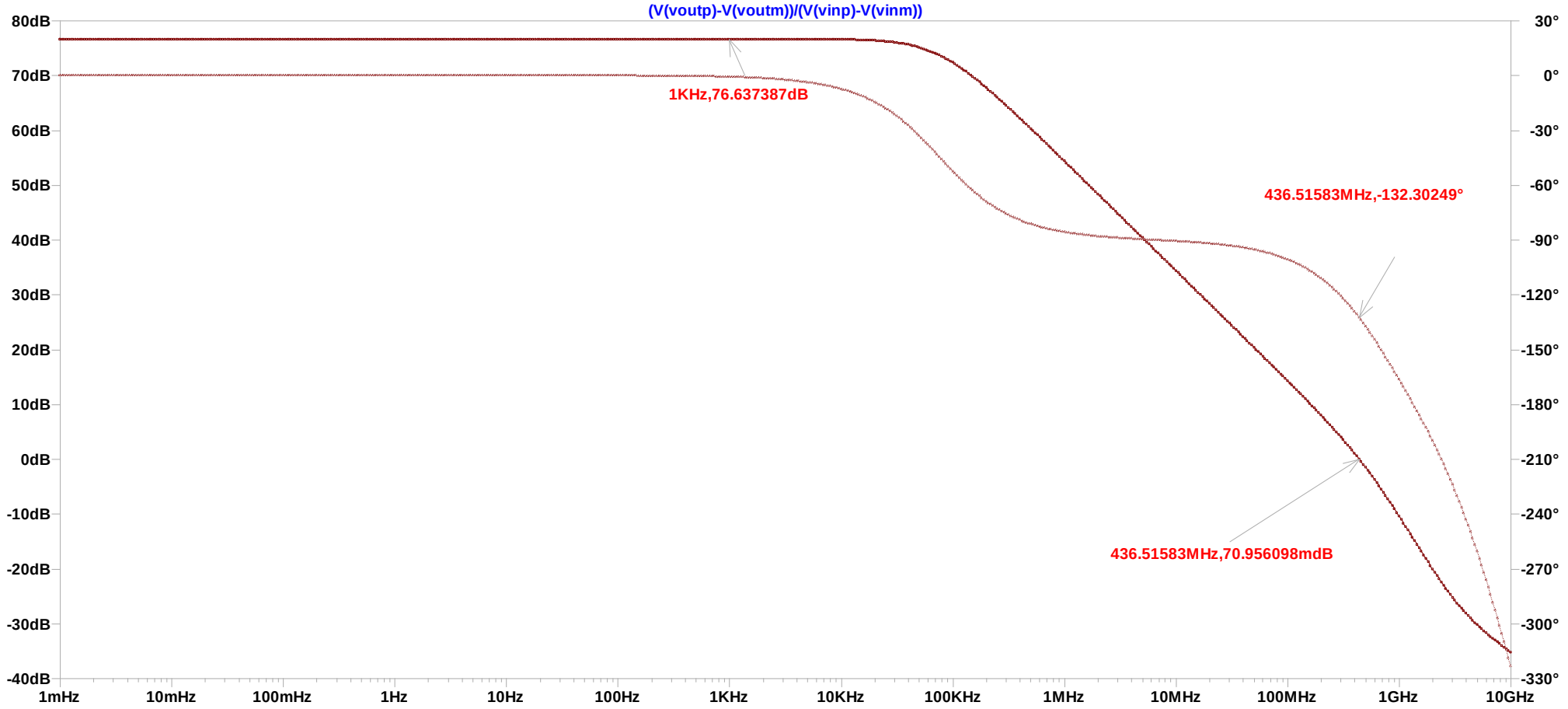
Results

DC Analysis

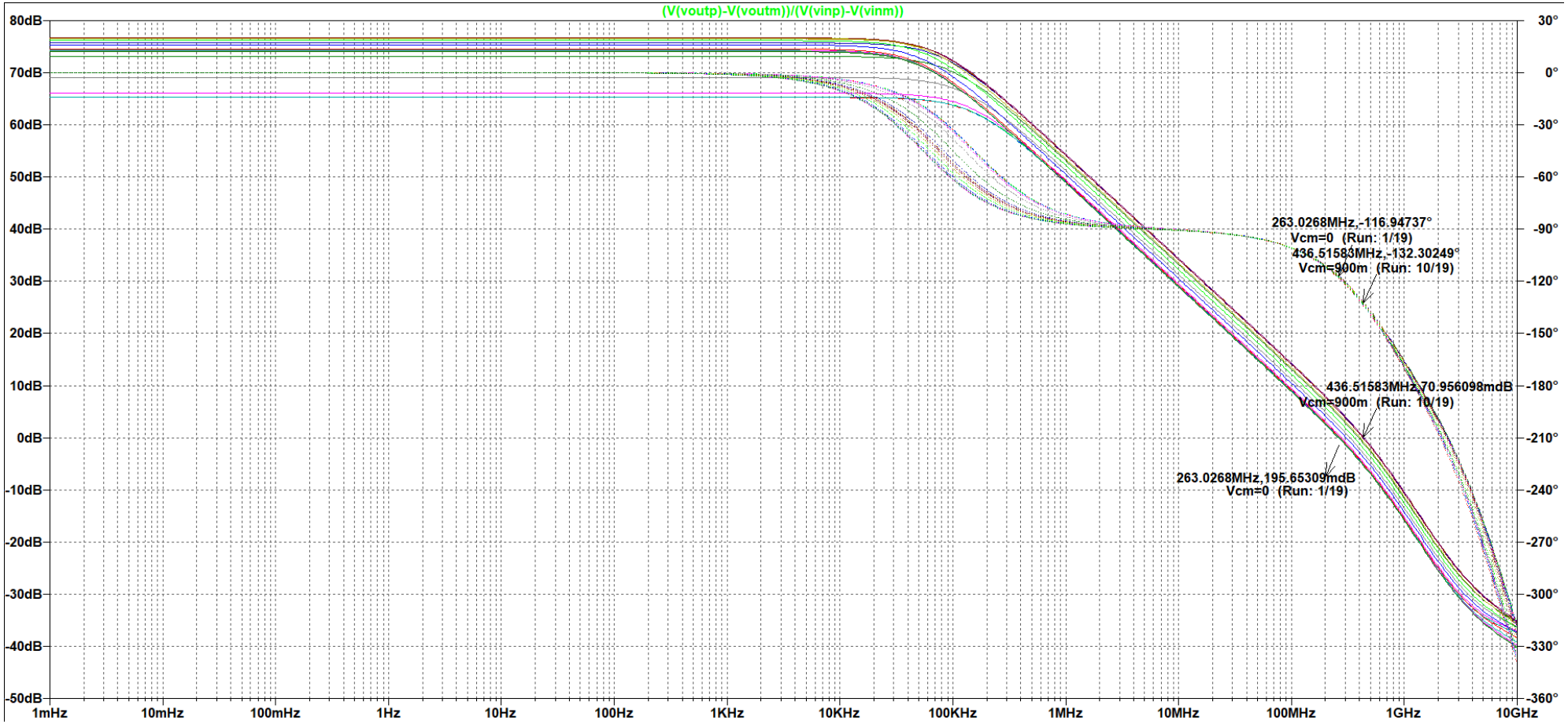


- Input CM Voltage
  - Sweep from -0.5V to 2.5V
- Output DC Voltage of Stage-1
  - Range: 0.4V to 1.4V
  - Not much variation
- Output DC Voltage of Stage-2 (Final O/P)
  - Range: 0.4V to 1.4V
  - Not much variation
- Rail to Rail working capability
  - Input CM voltage – Full Range

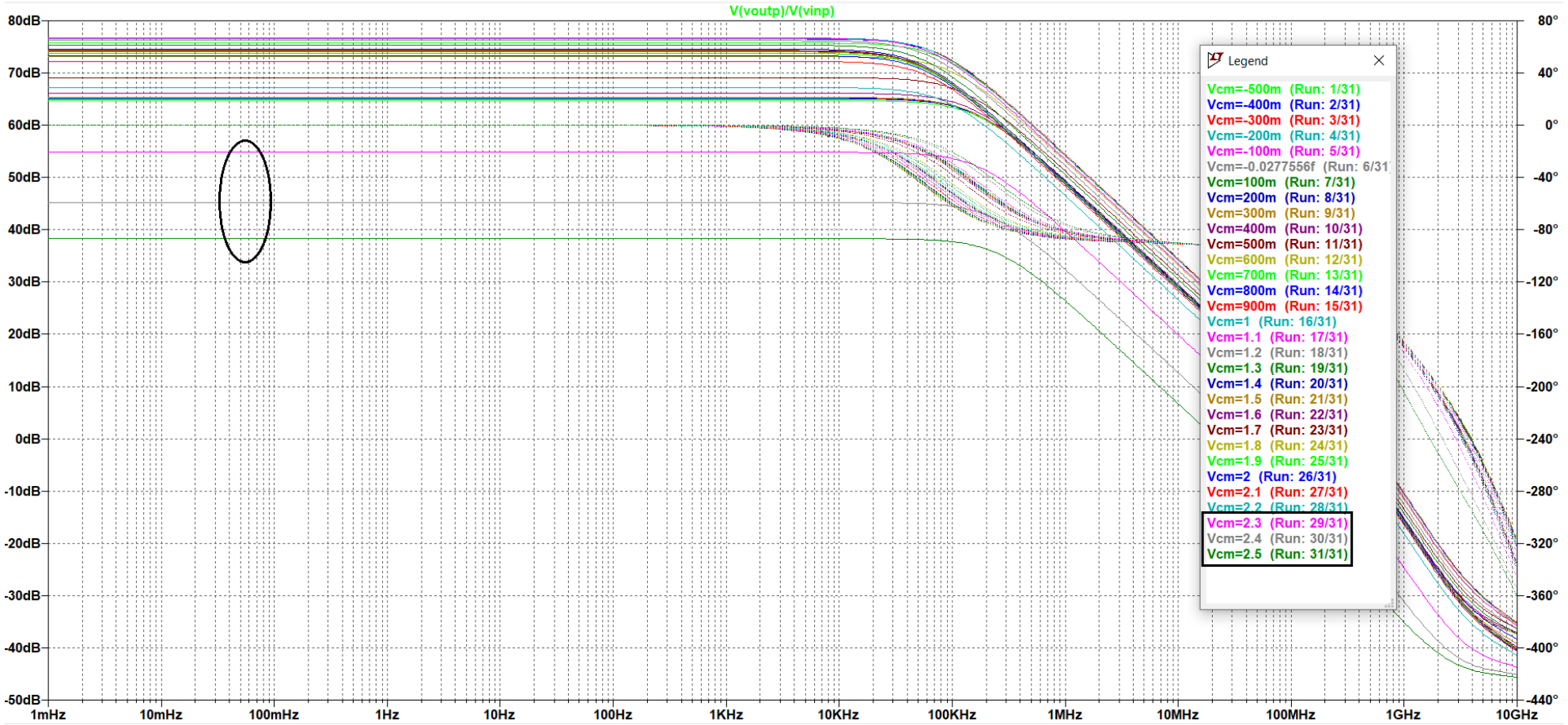
AC Analysis (V_{CM} = 0.9V)



AC Analysis (V_{CM} sweep)



AC Analysis (V_{CM} sweep)



Results & Conclusion

- Gain
  - 65.3 dB to 76.63 dB
- BW
  - 156.055 kHz to 77.16 kHz
- UGF
  - 263 MHz to 436.5 MHz
  - UGF > 100 MHz
- Phase margin
  - 48° to 63°
- Power Consumption (Overall)
  - 1.8*1.37m = 2.467mW
- Power Consumption (w/o bias)
  - 1.8*1.33m = 2.39mW
- Input common mode range
  - Rail-to-Rail
- CMFB
  - Working

Improvements

- Rail-to-Rail input capabilities in stage-1 (folded cascode)
- Gm Calibration
- Overall Gain Improvements

References

- Design of Analog CMOS Integrated Circuits, B. Razavi
- ECEN474/704: (Analog) VLSI Circuit Design (Spring 2018), Sam Palermo Analog & Mixed-Signal Center, Texas A&M University
  - Lecture 15: Fully Differential Amplifiers & CMFB
  - Lecture 17: Fully Differential Amplifiers & CMFB
- Lecture notes

THANK YOU!