SUMS

1. The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is _____.

   (A) 1.26
   (B) 1.68
   (C) 2.46
   (D) 4.52

   The question is to find the time taken for,

   "100 fetch operation and 60 operand red operations and 40 memory

   operand write operations"/"total number of instructions".

   Total number of instructions= 100+60+40 =200

   Time taken for 100 fetch operations(fetch =read)

   = 100*((0.9*1)+(0.1*5)) // 1 corresponds to time taken for read

   // when there is cache hit

   = 140 ns //0.9 is cache hit rate

   Time taken for 60 read operations = 60*((0.9*1)+(0.1*5))

   = 84ns

   Time taken for 40 write operations = 40*((0.9*2)+(0.1*10))

   = 112 ns

// Here 2 and 10 the time taken for write when there is cache

// hit and no cahce hit respectively

So,the total time taken for 200 operations is = 140+84+112

= 336ns

Average time taken = time taken per operation = 336/200

= 1.68 ns

2. A cache memory unit with capacity of N words and block size of B words is to be designed. If it is designed as direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a 16-way set-associative cache, the length of the TAG field is _____ bits.

   Note: This questions appeared as Numerical Answer Type.
   (A) 12
   (B) 14
   (C) 16
   (D) 18

   Type of mapping is direct map; for this direct map, 10 bits are required in itss Tag.

   It is updated to 16 way set Associative map then new tag field size = 10 + $\log_2 16$ = 14 bits, because for k way set associative map design, $\log_2 k$ bits are additionally required to the number of bits in tag field for Direct map design.

3. A block-set associative cache memory consists of 128 blocks divided into four block sets . The main memory consists of 16,384 blocks and each block contains 256 eight bit words.

   1.How many bits are required for addressing the main memory?
   2. How many bits are needed to represent the TAG, SET and WORD fields?

- Number of blocks in cache memory = 128
- Number of blocks in each set of cache = 4
- Main memory size = 16384 blocks
- Block size = 256 bytes
- 1 word = 8 bits = 1 byte

Size of main memory

= 16384 blocks

= 16384 x 256 bytes

= 2^{22} bytes

Thus, Number of bits required to address main memory = 22 bits

We have-

Block size

= 256 bytes

= 2^{8} bytes

Thus, Number of bits in block offset or word = 8 bits

Number of sets in cache

= Number of lines in cache / Set size

= 128 blocks / 4 blocks

= 32 sets

= 2^{5} sets

Thus, Number of bits in set number = 5 bits

Number of bits in tag

= Number of bits in physical address – (Number of bits in set number + Number of bits in word)

= 22 bits – (5 bits + 8 bits)

= 22 bits – 13 bits

= 9 bits

Thus, Number of bits in tag = 9 bits

4. A 4-way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is _____.

Given-

- Set size = 4 lines
- Cache memory size = 16 KB
- Block size = 8 words
- 1 word = 32 bits = 4 bytes
- Main memory size = 4 GB

We have,

Main memory size

= 4 GB

= 2^{32} bytes

Thus, Number of bits in physical address = 32 bits

We have,

Block size

= 8 words

= 8 x 4 bytes

= 32 bytes

= 2^{5} bytes

Thus, Number of bits in block offset = 5 bits

Number of lines in cache

= Cache size / Line size

= 16 KB / 32 bytes

= 2^{14} bytes / 2^{5} bytes

= 2^{9} lines

= 512 lines

Thus, Number of lines in cache = 512 lines

Number of sets in cache

= Number of lines in cache / Set size

= 512 lines / 4 lines

= 2^9 lines / 2^2 lines

= 2^7 sets

Thus, Number of bits in set number = 7 bits

Number of bits in tag

= Number of bits in physical address – (Number of bits in set number + Number of bits in block offset)

= 32 bits – (7 bits + 5 bits)

= 32 bits – 12 bits

= 20 bits

Thus, number of bits in tag = 20 bits