

## Experiment No: 01

Experiment Name: Generation of Amplitude Shift Keying.

Objective: The objectives of this experiment is to generate Amplitude Shift keying (ASK) signals without data coding.

Theory: Amplitude shift keying - ASK - in the context of digital communications is a modulation process which imparts to a sinusoid two or more discrete amplitude levels. These are related to the number of levels adopted by the digital message.

For a binary message sequence there are two levels, one of which is typically zero. Thus the modulated waveform consists of bursts of a sinusoid.

### Modulation :

■ Modulation is the process of converting data into radio-waves by adding information to an electronic or optical carrier signal.

■ A carrier signal is one with a steady waveform -- constant height or amplitude & frequency.

### Amplitude Shift Keying :

Amplitude Shift Keying (ASK) is a form of amplitude modulation that represents digital data as variations in the amplitude of a carrier wave.

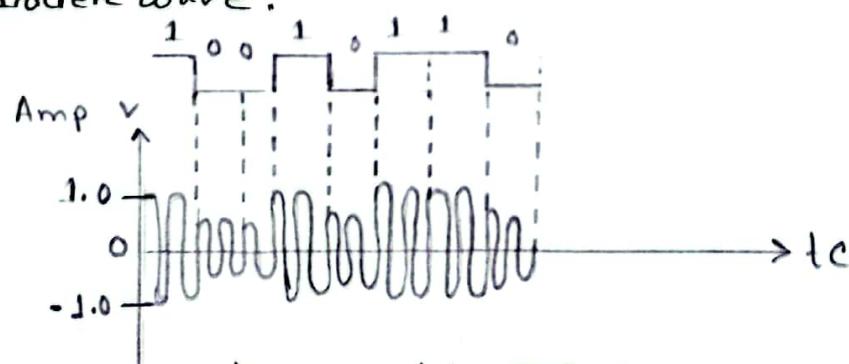


Fig: Amplitude Shift Keying

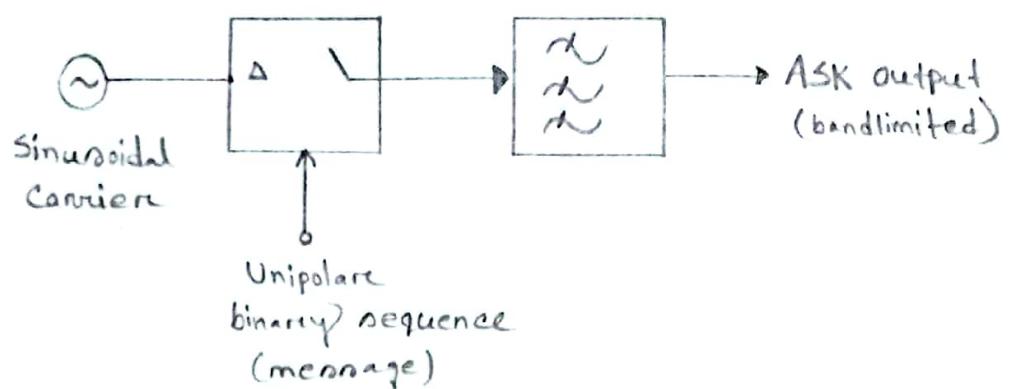


Fig: The principle of ASK generation

### Apparatus :

1. CMOS - 4016
2. Inverters/Transistors - 74LS04
3. Registers - MINRES1K
4. Generators - i) SINE  
ii) Pulse
5. Ground
6. Oscilloscope .

### Design :

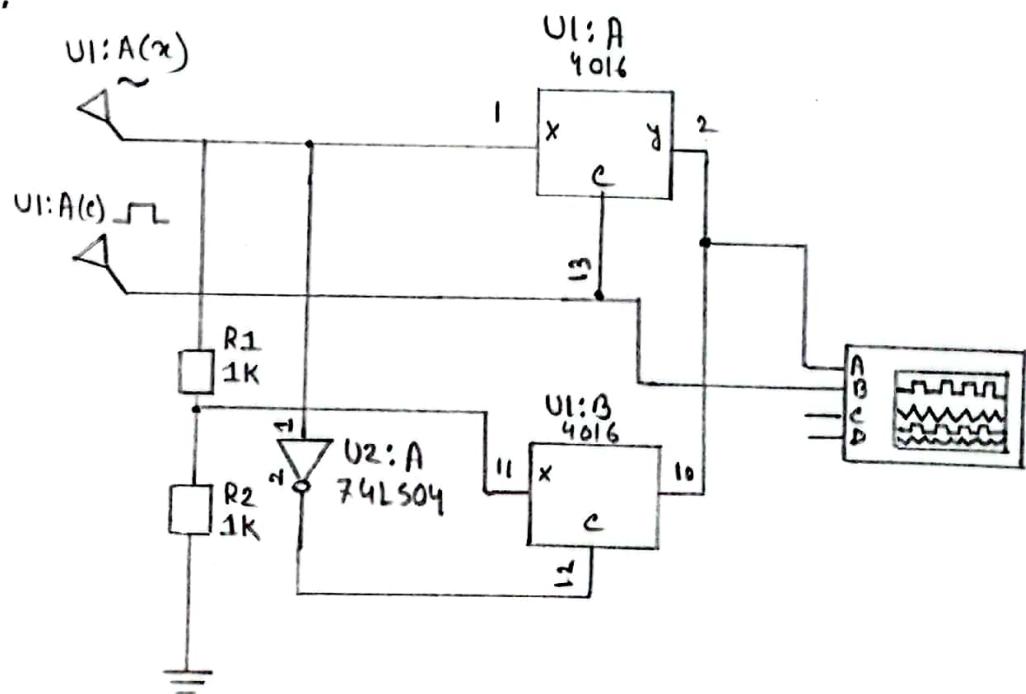


Fig: ASK (Design)

### Working Procedure:

1. Connect pin 2 and Pin 10.
2. Oscilloscope pin A will be added with pin 2.
3. Oscilloscope pin B will be added with Pin 13.
4. Pulse generator will be connected with Pin 13.
5. Sine generator will be connected with 74LS04 transistor and input side along with pin 1 of 4016 CMOS.
6. first sine wave generator will be connect with Pin 1.
7. Second sine wave generator will be connect the resistors R<sub>1</sub> & R<sub>2</sub> and it also connect will pin 11.
8. The registers will be grounded.
9. Output of the transistors will be connected with Pin 12.
10. And finally we will adjust the amplitude = 5 and frequency = 100 .

By this we will have our desire waveform

Discussion: In this experiment , we can design amplitude shift keying signal .

Experiment NO: 02

Experiment Name: Frequency Shift keying (FSK) modulation technology.

Objectives : The objective of this experiment is to generate Frequency shift keying (FSK) modulation technology signals without data coding.

Theory : Frequency Shift keying (FSK) is a frequency modulation scheme in which digital information is transmitted through discrete frequency changes of carrier signal.

Modulation :

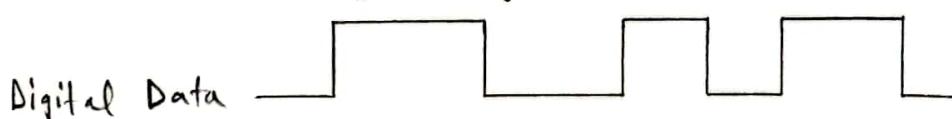
■ Modulation is the process of converting data into radio waves by adding information to an electric or optical carrier signal.

■ A carrier signal is one with a steady waveform constant height or amplitude and frequency.

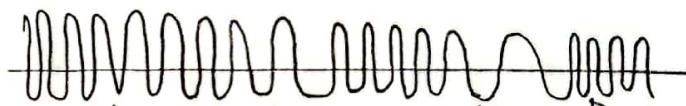
Frequency Shift Keying (FSK):

■ FSK of a SAW oscillator can be achieved by switching a capacitance in and out of the tuned circuit in step with the modulation.

■ We can also use a transistor instead of a diode to do the switching or use the voltage and varicap diode, whose capacitance changes with the voltage. The effect of changing the capacitance in the tuned circuit is to pull the oscillation frequency away from its static value.

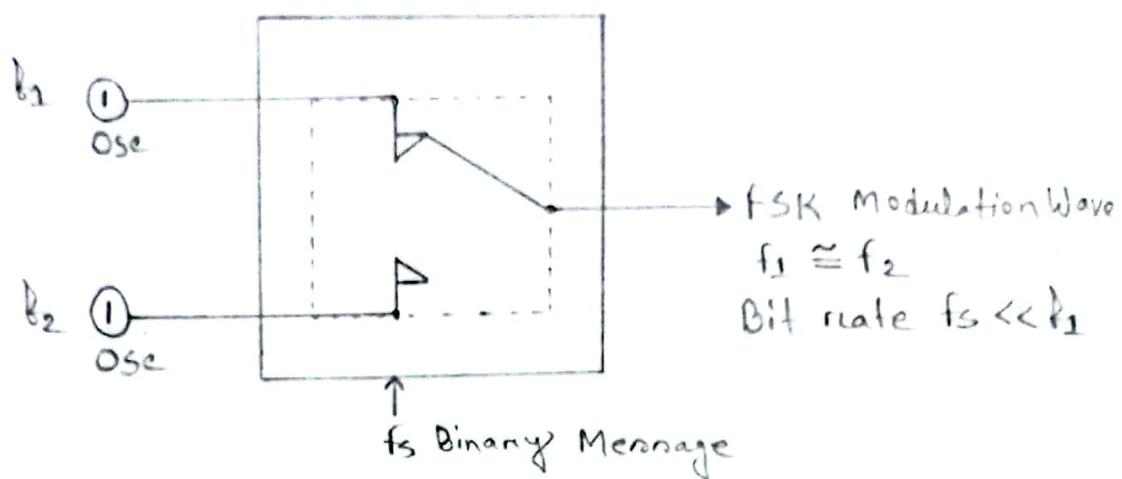


FSK



Mark-Frequency fig: FSK signal the message .

FSK Modulator: The FSK modulator block diagram comprises of two oscillators with a clock & the input binary sequence.



- Apparatus:
1. CMOS - 4016
  2. Inverters / Transistors - 74LS04
  3. Registers - MINRES1K
  4. Generators - 1) SINE, 2) Pulse
  5. Oscilloscope.

Design:

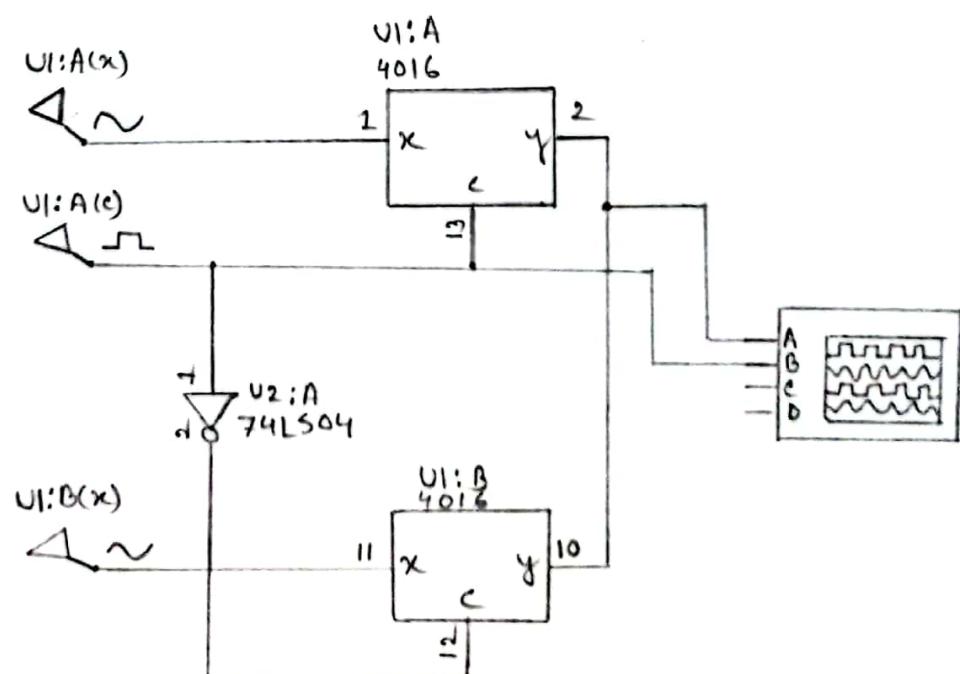


Fig: FSK (Design)

### Working Procedure :

1. Connect Pin 2 & Pin 10.
2. Oscilloscope pin A will be added with Pin 2.
3. Oscilloscope pin B will be added with Pin 13.
4. Here in two. Sine generators. One will be connected with Pin 1 & other will be connected with Pin 12.
5. Pulse generator will be connected with Pin 13 & transistor 74LS04 input side along with Pin 12 of CMOS-4016(ULB)
6. Output of the transistor 74LS04 will be connected Pin 12.
7. And lastly we will adjust the amplitude = 1.  
frequency = 500 & pulse = 5 for pulse value.
8. In 1st sine wave amplitude = 1 & frequency = 1000  
& 2nd sine wave amplitude = 1 & frequency = 1000.  
By this we will have own desire waveform.

Discussion: In this experiment, we can design frequency shift keying signal.

### Experiment No: 03

Experiment Name: Generation of Binary phase Shift keying.

Objective : The objectives of this experiment is to generate of binary phase shift keying (BPSK) signals without data coding.

Theory : Phase - shift keying (PSK) is a digital modulation process which conveys data by changing (modulating) the phase of a constant frequency reference signal (the carrier wave). The modulation is accomplished by varying the sine and cosine inputs at a precise time.

BPSK is also called as 2-phase PSK or phase Reversal keying. In this technique, the sine wave carrier takes two phase reversals such as  $0^\circ$  and  $180^\circ$ .

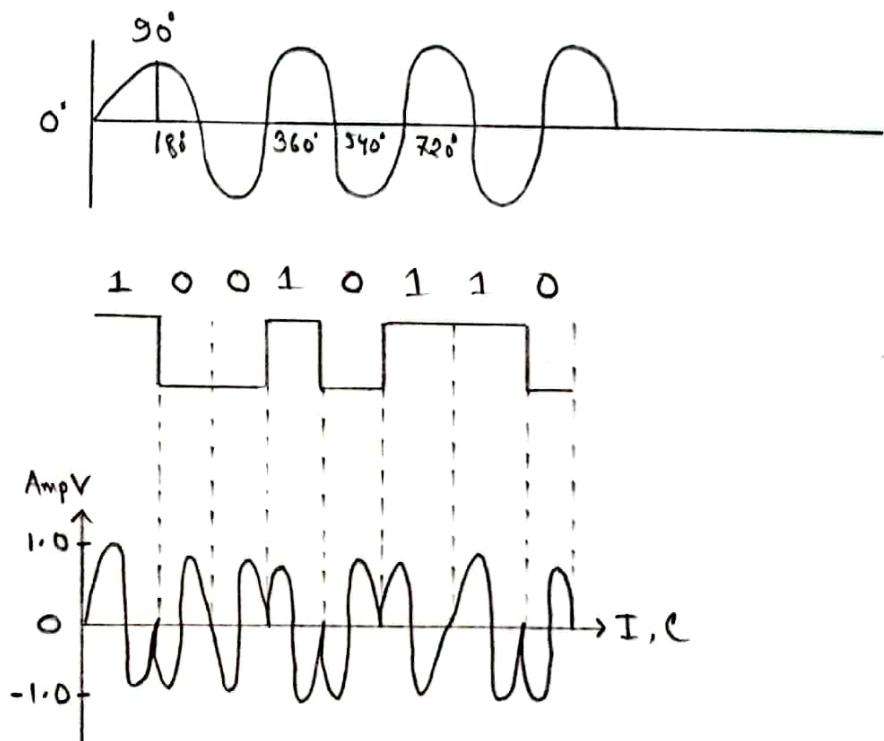


Fig: Phase shift keying (PSK)

## Apparatus:

1. Operational Amplifiers - 741
2. Power (2)
3. Ground
4. Resistors - MINRES 10K (2)
5. Input
6. Generators SINE
7. Amplifiers - LF398A
8. Output
9. SW - SPDT (switch)
10. Oscilloscope.

## Design:

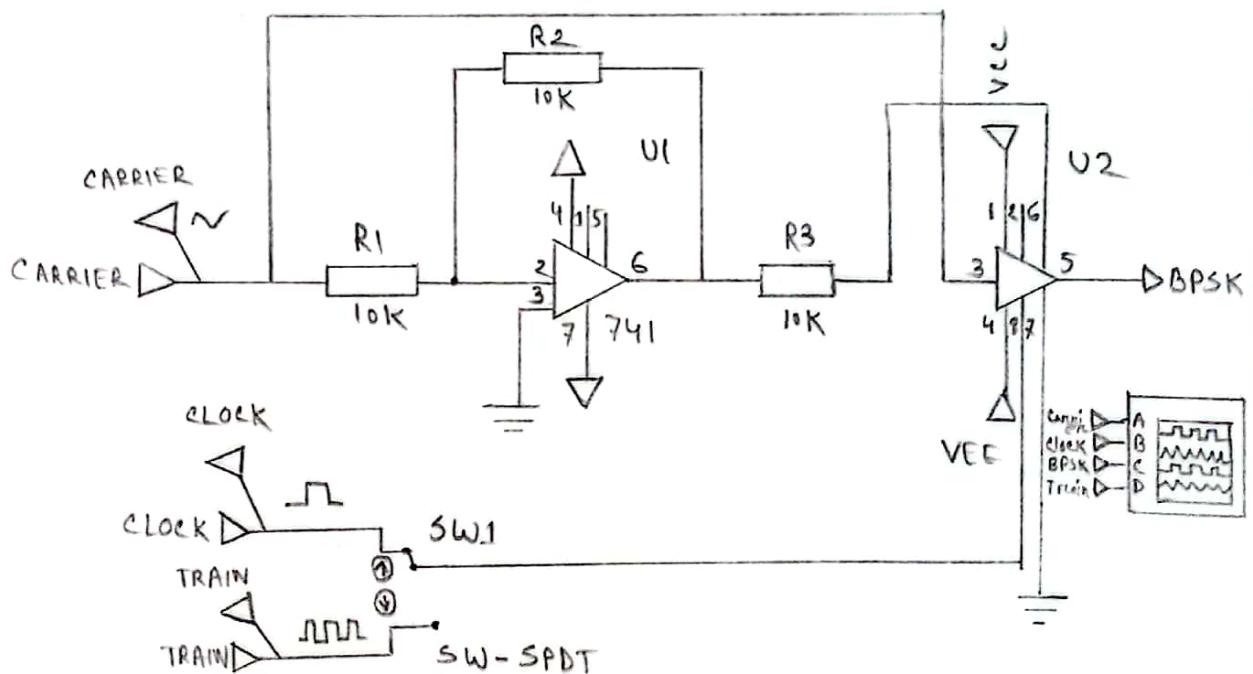


fig: BPSK (Design)

### Working Procedure:

1. After opening proteus, we will select Design then we will select Configure power Rails. Here, we will select in power supply VCC/VDD (voltage common collector) & fixed its voltage = 12. After that we will select VEE & fixed its voltage = -12.
2. Then select Component & take an operational Amplifier 741 & set it.
3. From terminal, we will took two powers & connect them with pin 4 & pin 7 of the 741.
4. Then connect ground with pin 3.
5. Select resistors R1 & R2. And connect R2 with Pin 6. R1 & R2 will be connected together with pin 2.
6. Select an input. And named it carrier.
7. Sine generator will be fixed up in carrier. And set amplitude = 12V & Frequency = 50Hz.
8. Select a amplifier - LF398N and connect its pin 6 with resistor R3. R3 resistor also will connect with 741's pin 6.
9. Take two input. Connect one with pin 1 & another with pin 4 of the amplifier LF398N.
10. The input VCC is connected with pin 1 & The input VEE is connected with pin 4.
11. Take a ground and connect with pin 7.
12. Select a output & connect it with pin 5 & named the ground as BPSK.
13. Amplifier LF398N's pin 3 will be connected with input carrier.

14. Taking two inputs & named them Clock & Train.
15. Selecting device SW-SPDT. And connected with inputs Clock & Train.
16. Select a pulse generator & connect it with clock and select pulsed (High) voltage = 10 & Frequency = 25
17. Select a pattern generator & connect it with train and select pulse width (Secn) = 20m.
18. The oscilloscope pin A will connected with input name CARRIER , pin B connected with input clock , pin C will connected with output named BPSK , pin D will connected with input TRAIN .

By this, we will have our desire waveform.

Discussion: In this experiment, we can design Binary Phase Shift keying signal.

## Experiment No: 04

Experiment Name: Design 4:1 multiplexer device.

Objective: The objectives of this experiment to design 4:1 multiplexer device without data coding.

Theory: The multiplexer is a combinational logic circuit designed to switch one of several input line to a common single output line.

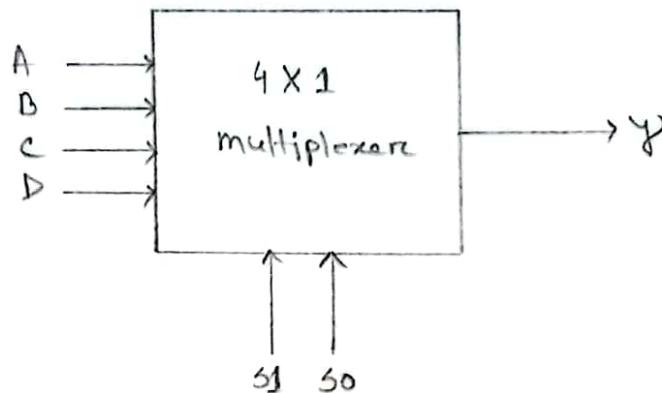


Fig: 4x1 multiplexer design .

It has four data inputs such as - A, B, C, D , two select line - S<sub>1</sub>, S<sub>0</sub> and output Y .

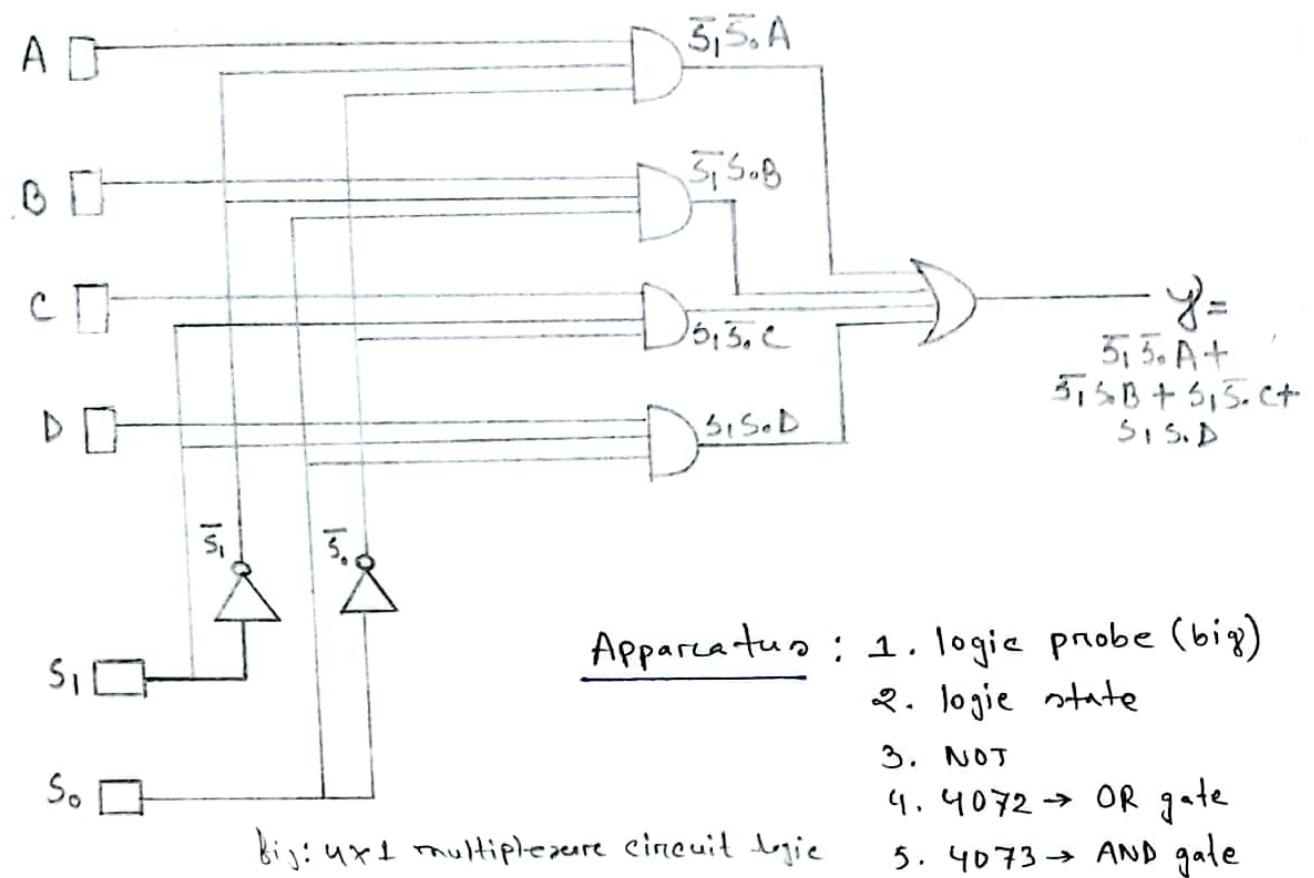
The input data goes to any one of the four input at a given time for a particular combination of select lines .

It has four inputs, two select lines and one output line.

Timing Diagram for input / output :

S <sub>1</sub>	S <sub>0</sub>	Y
0	0	A
0	1	B
1	0	C
1	1	D

## Design:



## Working principle:

1. In the child sheet we will take four AND gate & one OR gate with two NOT gate.
2. Each AND gate has three inputs part. All first input will connect with the random input each.
3.  $S_1$  will connect third & and fourth AND gate with third and fourth inputs.
4.  $\bar{S}_1$  will be connected first and second AND gate with first and second inputs.
5.  $S_0$  will be connected second and fourth AND gate with second and fourth inputs.
6.  $\bar{S}_0$  will connect first and third AND gate with first and fourth inputs.
7. All four AND gates will be added with the OR gate input. It means all four output of AND gate are the inputs of OR gate.

Discussion: In this experiment, we can design 4:1 multiplexer device.

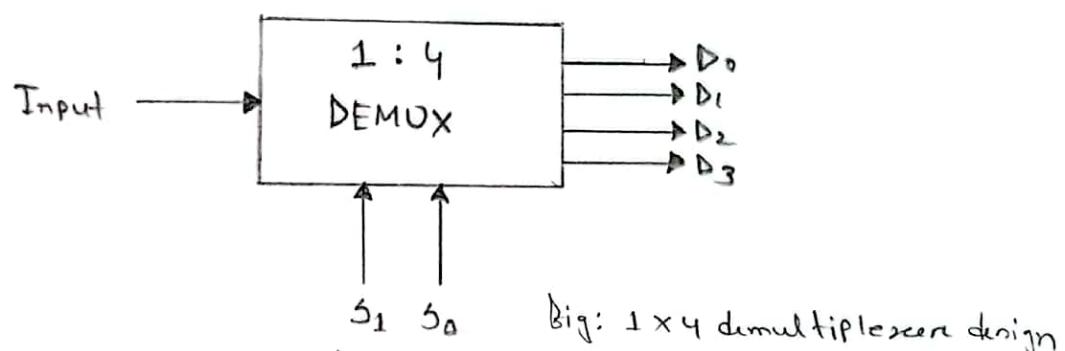
## Experiment No: 05

Experiment Name: Design 1 to 4 Demultiplexer.

Objectives : The objective of this experiment is to design 1 to 4 Demultiplexer without data coding.

### Theory :

- A demultiplexer (or demux) is a device that takes a single input line and returns it to one of several digital output lines.
- A demultiplexer of  $2^n$  output has  $n$  select lines, which are used to select which output line to send the input.
- A demultiplexer is also called a data distributor.



### Truth table :

S <sub>1</sub>	S <sub>0</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Apparatus:

- i) Logic probe (big)
- ii) Logic state
- iii) NOT gate
- iv) AND gate (4073)

Design:

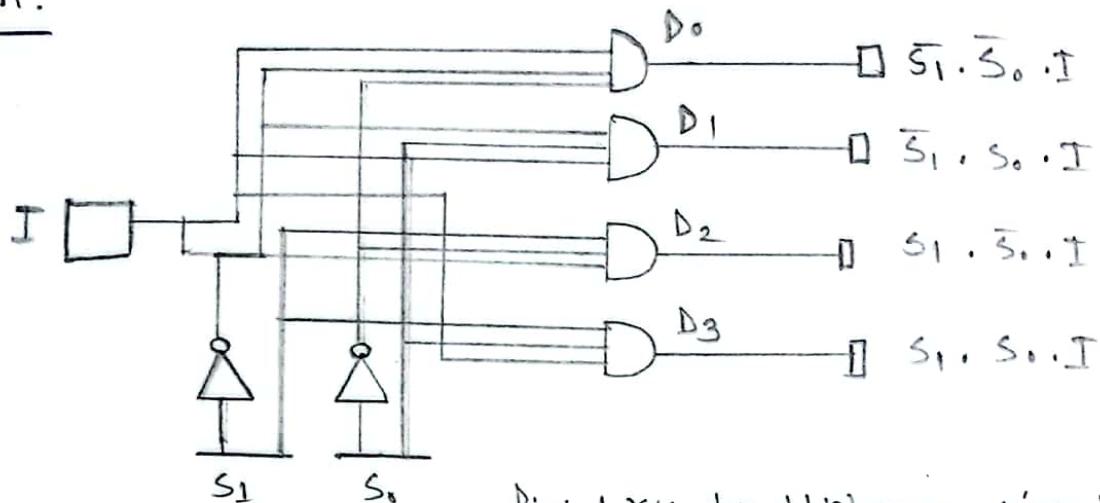


Fig: 1x4 demultiplexer circuit logic

Working principle:

1. Data will be added with every AND gate's first input port.
2. Two not gate will also the input port here.
3.  $S_1$  will be added third and forth AND gate's third and forth input port.
4.  $S_0$  will be added second and forth AND gate's second and forth input port.
5.  $\bar{S}_1$  will be added first and second AND gate's first and second input ports.
6.  $\bar{S}_0$  will be added first and third AND gate's first and third input ports.
7. The outputs will be connected with four AND gate's.

Discussion: In this experiment, we can design 1 to 4 Demultiplexers.

Experiment No : 06

Experiment Name : Generation of Hamming Code.

Objectives: The objective of this experiment is to generate of hamming code without data coding.

Theory: Hamming code is a set of error correction code that can be used to detect and corrects the errors that can be occur when the data is stored or moved from the sender to receiver.

Parity bit is a bit appended to data of binary bits to ensure that the total numbers of 1's in the data is even or odd.

Encoding a message by Hamming Code :

Step 1 → Calculation of the number of redundant bits.

Step 2 → Positioning the redundant bits.

Step 3 → Calculating the values of each redundant bits.

Apparatus :

1. Logic toggle
2. X-OR gate
3. LED - 81By
4. Ground

## Design:

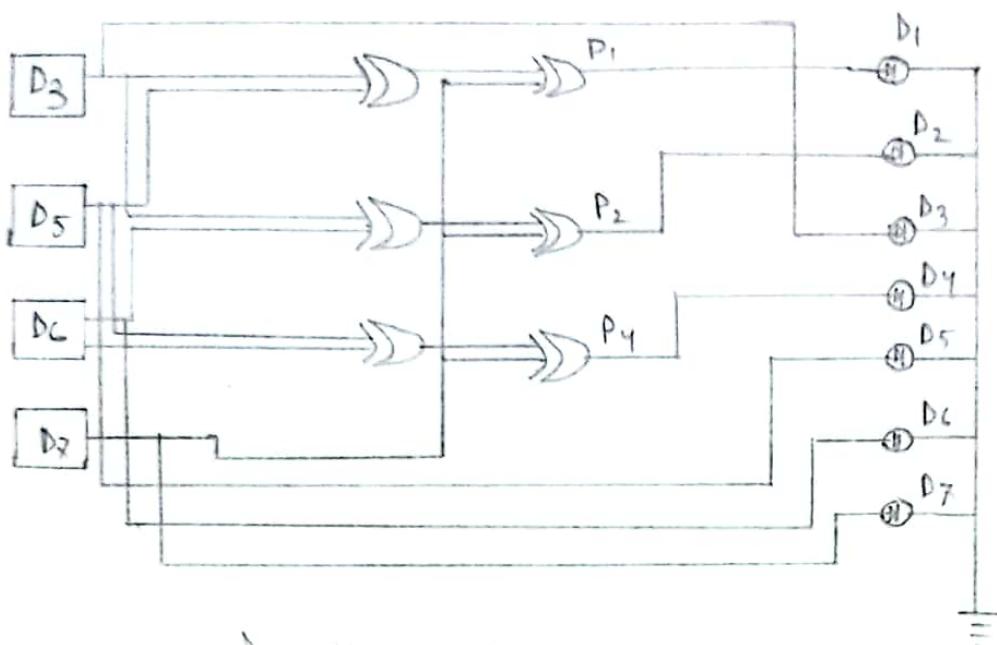


Fig: Hamming Code generation

## Working principle:

1. first we will connect logic toggle.
2. Toggle 1 will connect first X-OR gate.
3. Toggle 2 will connect second and 4th X-OR gate.
4. Toggle 3 will connect third and 4th X-OR gate.
5. Toggle 4 will connect second, 5th and 6th X-OR gate.
6. LED-Biby light will be connected with toggle of X-OR gates.
7. 2nd , 4th & 5th X-OR gate will connect to the first, second and forth LED-Biby Respectively.
8. All the LED will be connected to the ground.

Discussion: In this Experiment, we can generate Hamming Code.

Experiment No: 07

Experiment Name: Hamming Code generation and error detection.

Objectives: The objective of this experiment is to generate hamming code and errors detection.

Theory: In computer science and telecommunication, Hamming codes are a family of linear error-correcting codes.

Parity: Hamming code is a set of error correction codes that can be used to detect and correct the errors that can occur when data is moved or recorded from sender to receiver.

Parity bit: A parity bit is a bit appended to data of binary bits to ensure that the total number of 1's in the data is even or odd.

Truth table:

	P <sub>4</sub>	P <sub>2</sub>	P <sub>1</sub>
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Apparatus: (I) 74LS138      (IV) LED - Red  
                  (II) XOR gate      (V) Logic toggle  
                  (III) NOT gate

circuit diagram :

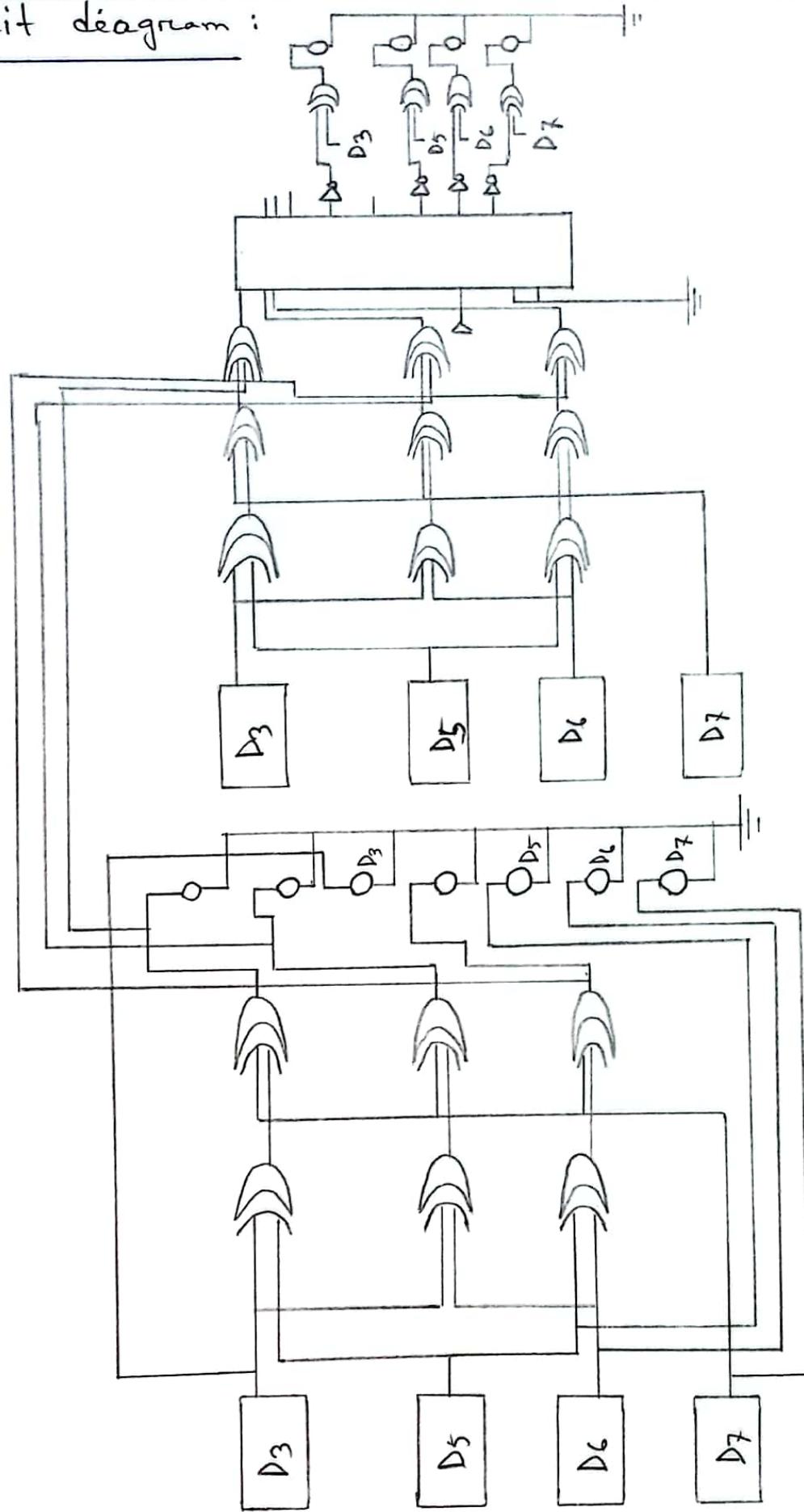


Fig : Hamming code generation and error detection

Working Principle: After hamming code generation we will detect the errors.

1. Toggle  $D_{12}$ ,  $D_{13}$  and  $D_{14}$  will connect to the 7<sup>th</sup>, 8<sup>th</sup> & 9<sup>th</sup> XOR gate.
2. Toggle  $D_{15}$  will connect with 10<sup>th</sup> & 12<sup>th</sup> X-OR gate.
3. Output of 10<sup>th</sup>, 11<sup>th</sup> & 12<sup>th</sup> XOR gate will be pass through another three XOR gate.
4.  $P_1, P_2, P_4$  will connect with the 13<sup>th</sup>, 14<sup>th</sup> & 15<sup>th</sup> XOR gate.
5. Encoder 1, 2 & 3 pin will connect with 13<sup>th</sup>, 14<sup>th</sup> & 15<sup>th</sup> XOR gate.
6. An input is passed through pin 6 and pin 4 & 5 are connected to the ground and pin 1, 2, 3, 7 are also connected to the ground.
7. Encoder 12<sup>th</sup>, 10<sup>th</sup>, 9<sup>th</sup> & 7<sup>th</sup> pin are connected with 17<sup>th</sup>, 18<sup>th</sup>, 19<sup>th</sup> & 20<sup>th</sup> NOT gate.
8. NOT gate are sequentially connected with 21<sup>st</sup>, 22<sup>nd</sup>, 23<sup>rd</sup> & 24<sup>th</sup> XOR gate.
9. All the XOR gates are connected with  $D_3, D_5, D_6, D_7$ .
10. The output are connected to the LED-red and other pin are grounded.

Here, the input is 1011 and the output is 1011. So, no bits are changed here.

Discussion: In this experiment, we can generate hamming code and error detection easily.

## Experiment No: 08

Experiment Name: Design and configuration different types of network topology.

Objectives: The objective of this experiment is to design and configuration different types of network topology.

### Theory :

Network Topology: Network topology is the arrangement of the element of communication network. Network topology is the topological structure of a network may be depicted physically or logically. There are six types of Network topology -

- |                 |                   |
|-----------------|-------------------|
| ① Bus topology  | ④ Tree topology   |
| ② Ring topology | ⑤ Mesh topology   |
| ③ Star topology | ⑥ Hybrid topology |

They are describe below :

① Bus topology : A bus topology is multipoint. One long cable acts as a backbone to link all the device in a network.

② Ring topology : In a ring topology, each device has a dedicated point-to-point connection with only the two device on either side of it.

③ Star topology : In a star topology, each device has a dedicated point-to-point link only to a central controller, usually called a hub.

- IV) Tree topology : Tree topology integrate multiple star topologies together onto a bus.
- V) Mesh topology : Mesh topology , a device has a dedicated point - to - point link to every other device .
- VI) Hybrid topology : All other topology are connected in a device with network is called hybrid topology .

IP address : IP address is a unique address that identifies a device on network or communication system .

Apparatus :

- ① End - device (pc)
- ② Switch
- ③ Hub
- ④ Crossover - straight through
- ⑤ Copper cross over

Diagram:

- ① Bus topology :

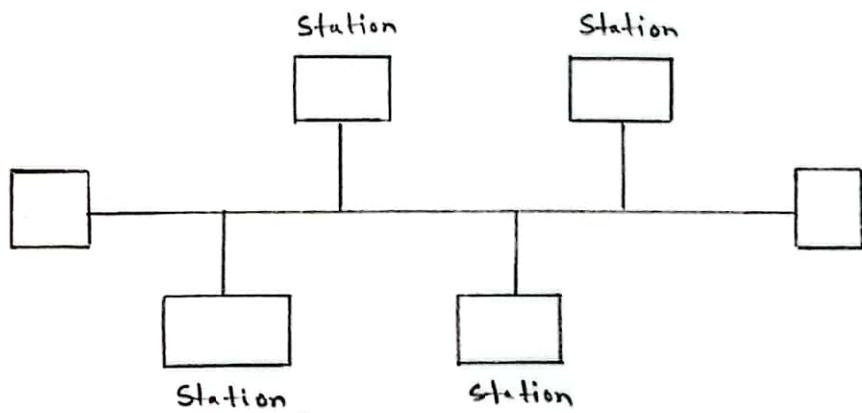


fig: Bus topology

## II) Ring topology :

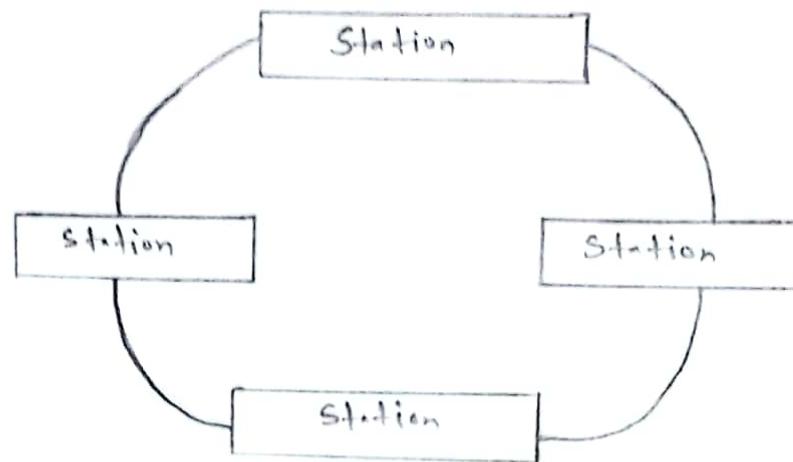


fig: Ring topology

## III) Star topology :

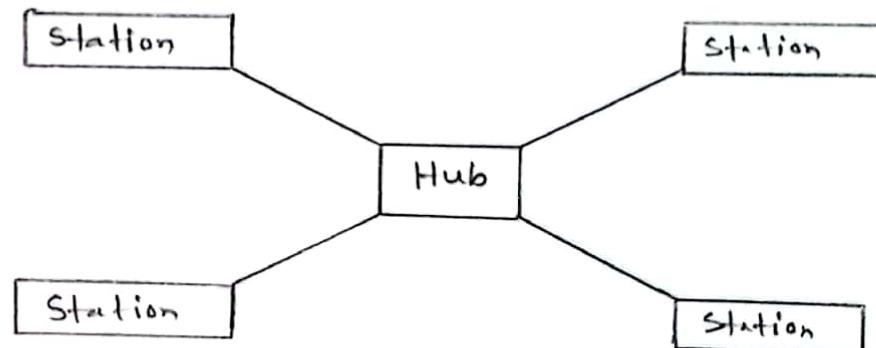


fig: Star topology

(IV) Tree topology :

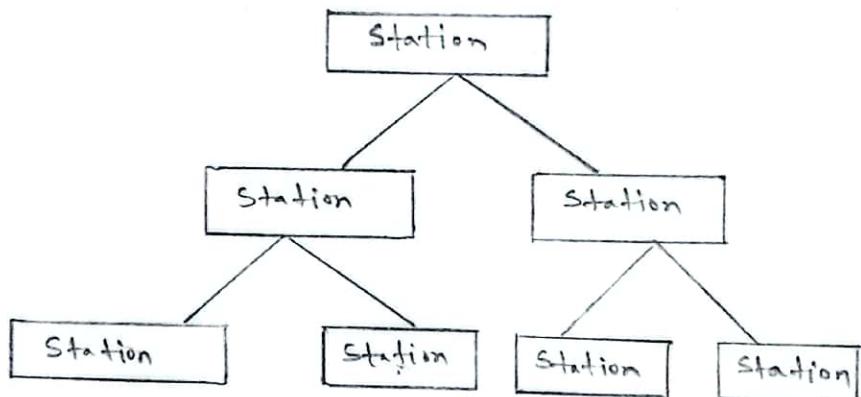


fig: tree topology

(V) Mesh topology :

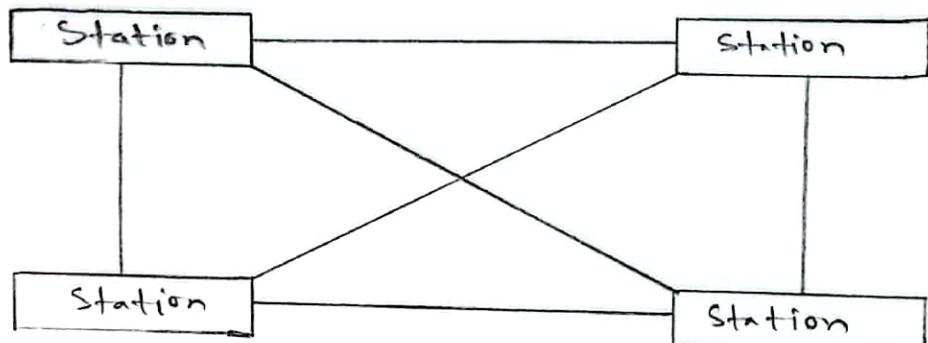


fig: mesh topology

(VI) Hybrid topology :

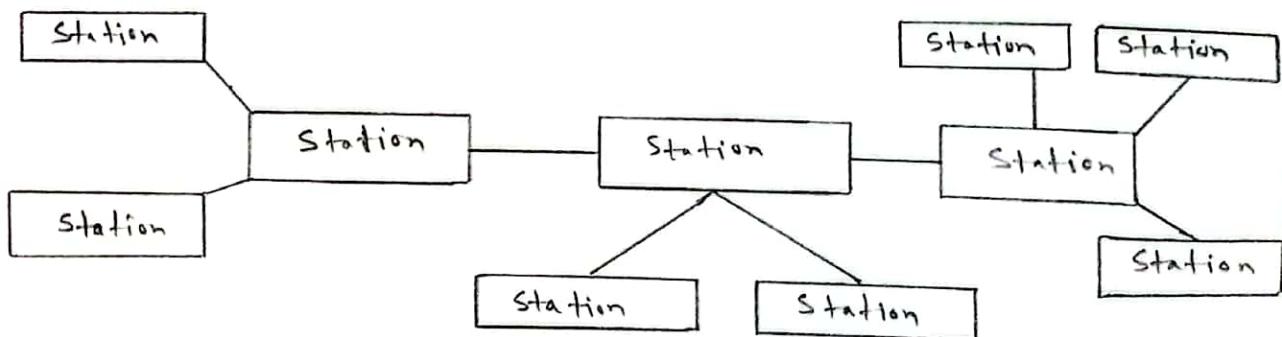


fig: hybrid topology

## Working principle:

### I Bus topology :

- Pick four end device pc and four switch.
- Configure the IP configure of the pc's as 192.168.10.1, 192.168.10.2, 192.168.10.3 and 192.168.10.4.
- Connect PC-0 with switch-0, PC-1 with switch-1 PC-2 with switch-2 and PC-3 with switch-3 with the crosses straight through.
- Connect all the switch with copper cross-over.
- Pass message through PC0 to PC2, P1 to PC0 output is shown in fig 1.a.1.

### II Ring topology:

- Connect all the component as like bus topology.
- Connected the two end switch with copper cross-over.
- Pass message PC3 to PC2, PC1 to PC0 and PC0 to PC2. output is shown in fig:2.a.1.

### III Star topology:

- Pick four end device (pc) and IP configure as 192.168.10.1, 192.168.10.2, 192.168.10.3 and 192.168.10.4
- Connect all the pc with Hub through copper-straight through.
- Pass message through PC 2 to PC-1 , PC 3-PC 2 , PC 0 to PC 3 .  
output is shown in fig 3.a.1 .

#### IV Tree topology :

- Pick pc from end device and IP configure 192.168.10.1 and others sequentially.
- Connect PC-0, PC-1, PC-2 with switch-0 through copper straight through.
- Connect PC-3, PC-4, PC-5 with switch -1 through copper straight through.
- Connect switch -0, switch -1 and switch -2 through copper cross-over.
- pass message PC3 to PC4, PC0 to PC1. Output is shown in fig 4.a.1,

#### V Mesh topology :

- Connect or arrange like Ring topology.
- Connect all the switch simultaneously.
- pass message through PC0 to PC3, PC2 to PC0, PC1 to PC3 . output is shown in fig 5.a.1.

#### VI Hybrid topology:

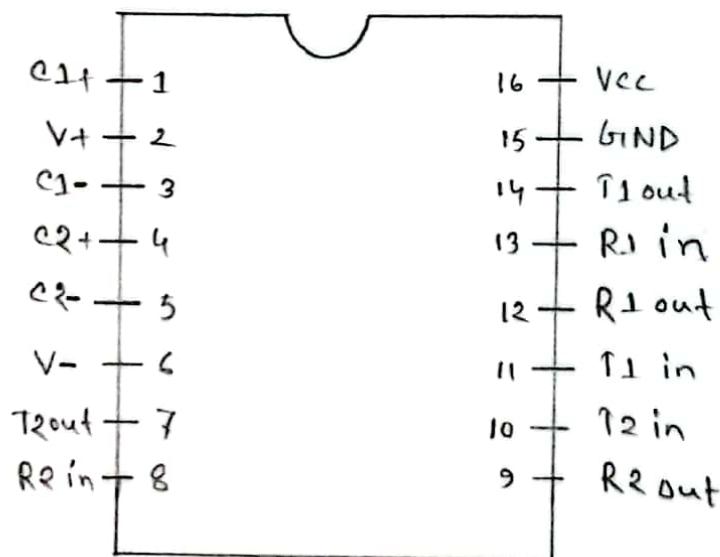
- Connect PC-0, PC-1, PC-2 through switch-0.
- Connect PC-3 with switch -1, PC-4 and PC-5 with switch -2 and PC-6, PC-7, PC-8 with switch -3. through copper - straight through.
- Connect all the switch through copper cross over
- pass message PC-8 to PC-7, PC-6 to PC-3 and PC-1 to PC-3. output is shown in fig 6.a.1.

## Experiment No : 09

Experiment Name : Implementation of RS-232 serial communication.

Objectives : The objective of this experiment is to design RS-232 serial communication.

Theory : RS-232 is a standard protocol used for serial communication. It is used for connecting computers and its peripheral device. From DTE sources, the RTS generates the request to send data. From DCE, the CTS clears the path for receiving data. After clearing a path it will give a signal to RTS of DTE sources to send signal. Then bits are transmitted from DTE to DCE. DCE sources, the request can be generate by RTS and CTS of DTE source.



fig; pin configuration

Apparatus :

- ① Max - 232      ⑪ Cap - elec      ⑫ Jumper  
⑬ Compin      ⑭ virtual terminal

Circuit diagram:

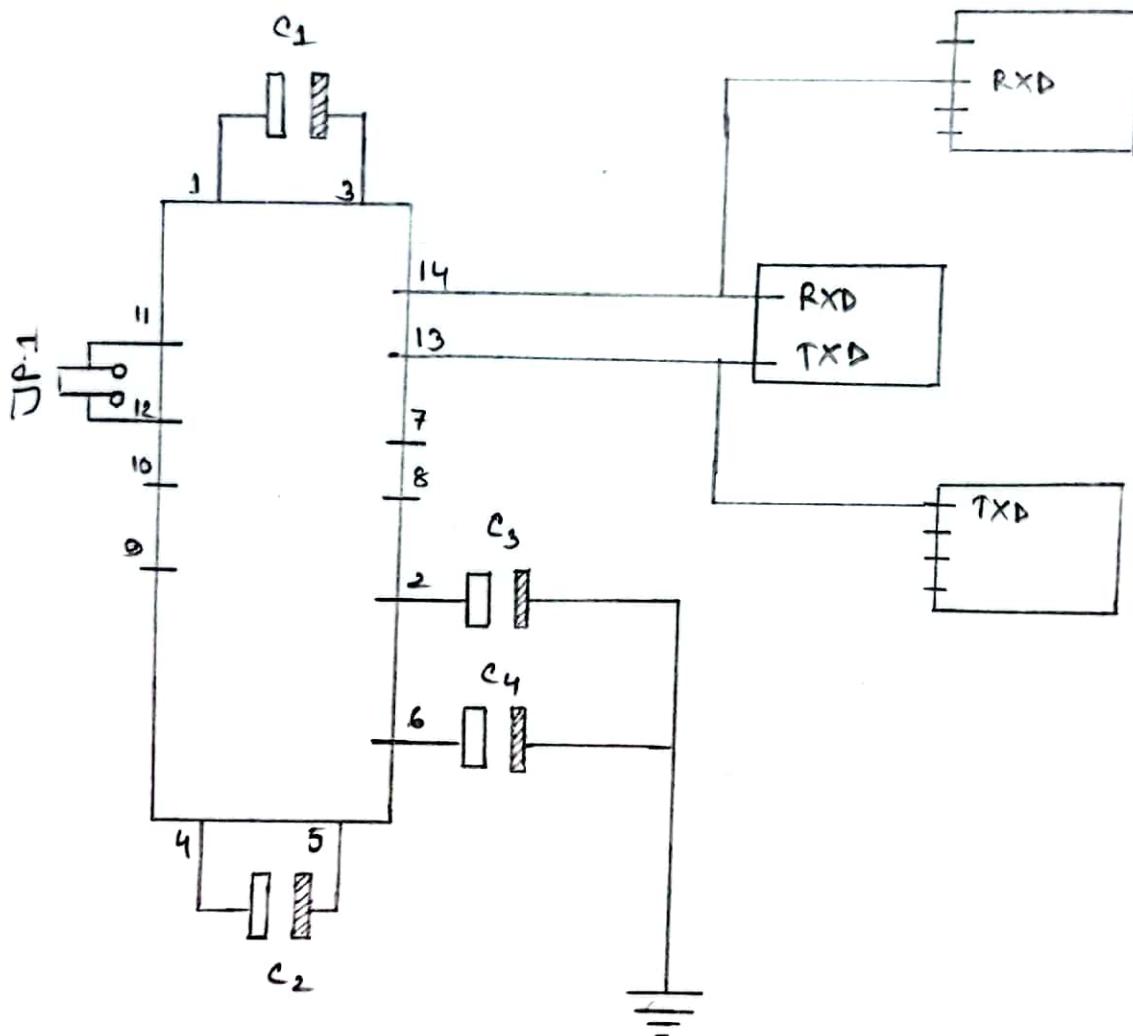


fig: RS-232 circuit diagram

### Working principle :

- ① Pick the max 232 and connect pin 11 and 12 with Jumper.
- ② Take four capacitors  $C_1, C_2, C_3, C_4$  and connect pin 1 and 3, 4 and 5, 6, 2 sequentially.
- ③ Capacitors  $C_3$  and  $C_4$  will connect with ground.
- ④ Virtual terminal will be connect with 14, which is RXD.
- ⑤ Port 13 will be connected with TXD.
- ⑥ We will take another two virtual terminal and pin 14 will be connected with the upper terminals RXD and pin 1 will be connected with the lower terminal TXD.
- ⑦ Then we will run the simulation and find our desire message.
- ⑧ If we want to see message in both terminal. Then set echo input character.
- ⑨ By inputting hexa value, we will receive character.