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Experiment No: 01

Experiment Name: Generation of Amplitude Shift Keying.

Objective: Generation of an amplitude shift keyed (ASK) signal.

Theory: Amplitude shift keying - ASK - in the context of digital communications is a modulation process which imparts to a sinusoid two or more discrete amplitude levels. These are related to the number of levels adopted by the digital message.

For a binary message sequence there are two levels, one of which is typically zero. Thus the modulated waveform consists of bursts of a sinusoid.

Modulation:

■ Modulation is the process of converting data into radio waves by adding information to an electronic or optical carrier signal.

■ A carrier signal is one with a steady waveform - constant height, or amplitude & frequency.

Amplitude-shift keying:

Amplitude-shift keying (ASK) is a form of amplitude modulation that represents digital data as variations in the amplitude of a carrier wave.

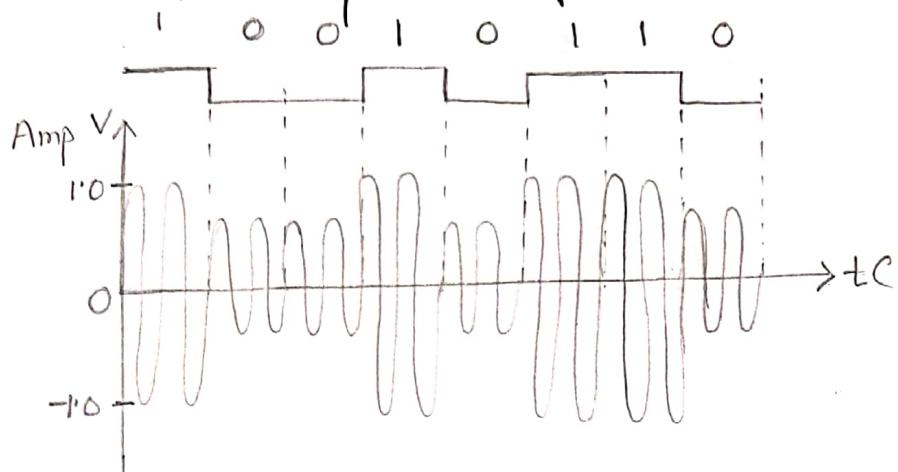


fig: Amplitude Shift Keying

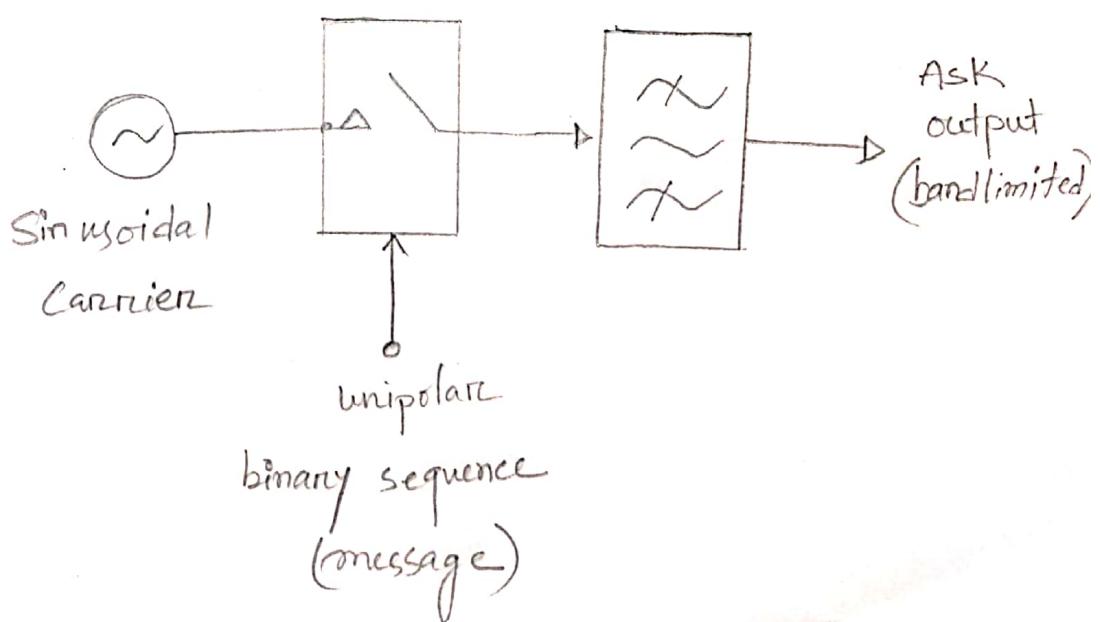
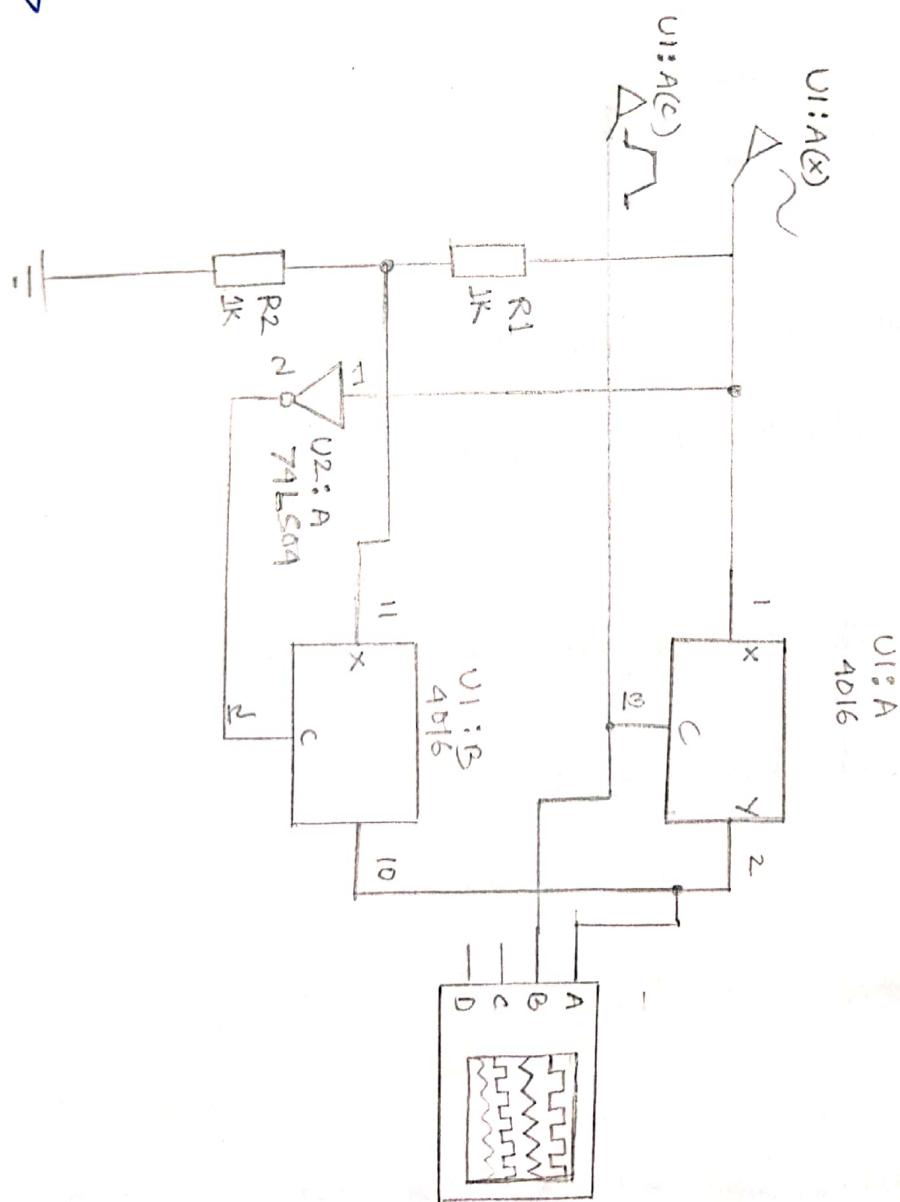


Fig: The principle of ASK generation

Apparatus:

1. CMOS - 4016
2. Inverter / Transistor - 74LS04
3. Register - MINRESIK
4. Generator - i) SINE
ii) Pulse
5. Ground
6. Oscilloscope

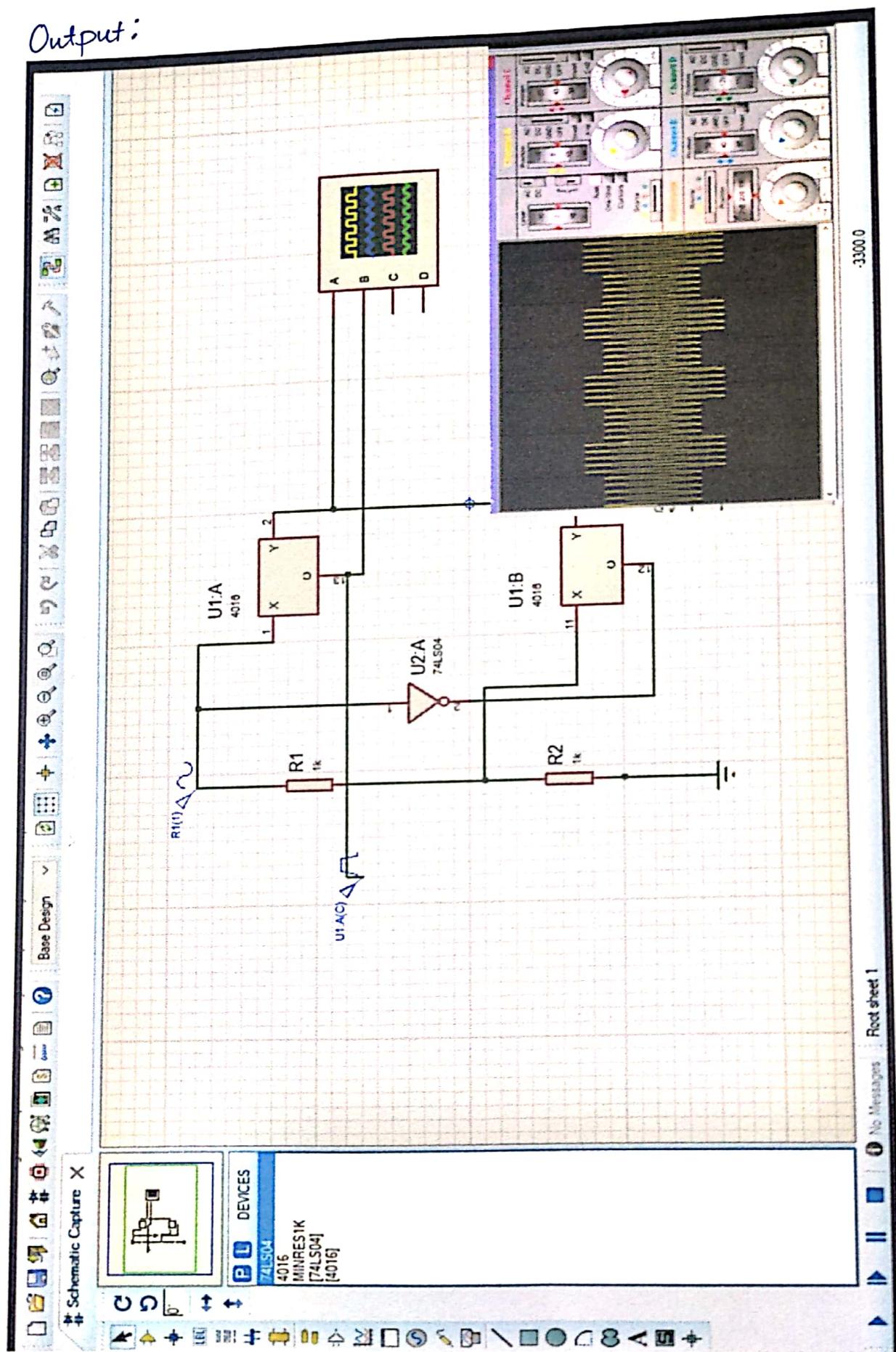
Design



Working Procedure :-

1. Connect pin 2 and pin 10.
 2. Oscilloscope pin A will be added with pin 2.
 3. Oscilloscope pin B will be added with pin 13.
 4. Pulse generator will be connected with pin 13.
 5. Sine generator will be connected with 74LS04 transistor input side along with pin 1 of 4016 CMOS.
 6. First sine wave generator will be connect with pin 1.
 7. Second sine wave generator will be connect with the resistors R_1 & R_2 and it also connect with pin 11.
 8. The resistors will be grounded.
 9. Output of the transistor will be connected with pin 12.
 10. And lastly we will adjust the amplitude = 5 and Frequency = 1000.
- By this we will have our desire waveform.

Output:



Experiment No: 02

Experiment Name: Generation of Frequency Shift Keying.

Objective : Generation of an frequency shift keyed (FSK) signal

Generation : Frequency-shift keying (FSK) is a frequency modulation scheme in which digital information is transmitted through discrete frequency changes of a carrier signal.

Modulation :

■ Modulation is the process of converting data into radio waves by adding information to an electronic or optical carrier signal.

■ A carrier signal is one with a steady waveform - constant height, or amplitude, and frequency.

FSK - Frequency Shift Keying :

■ FSK of a SAW oscillator can be achieved by switching a capacitance in and out of the tuned circuit in step with the modulation.

■ You can also use a transistor instead of a diode to do the switching, or use a varicap diode, whose capacitance changes with the voltage. The effect of changing the capacitance in the tuned circuit is to pull the oscillation frequency away from its static value.

FSK - Frequency Shift keying:

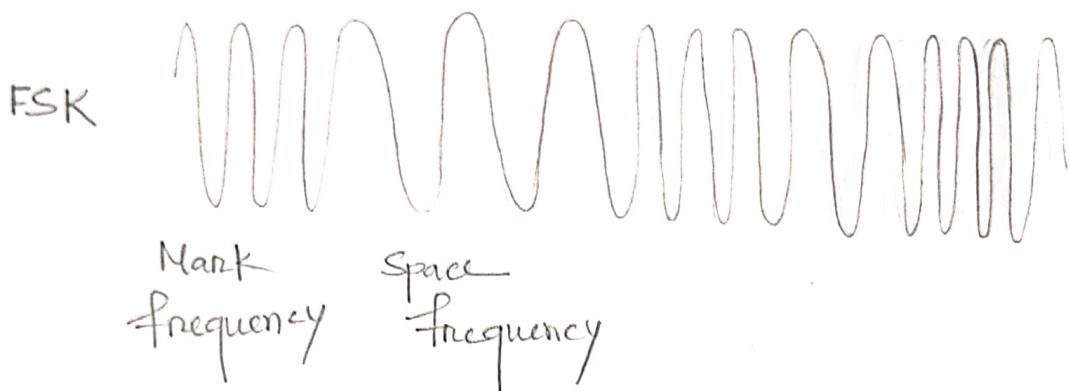
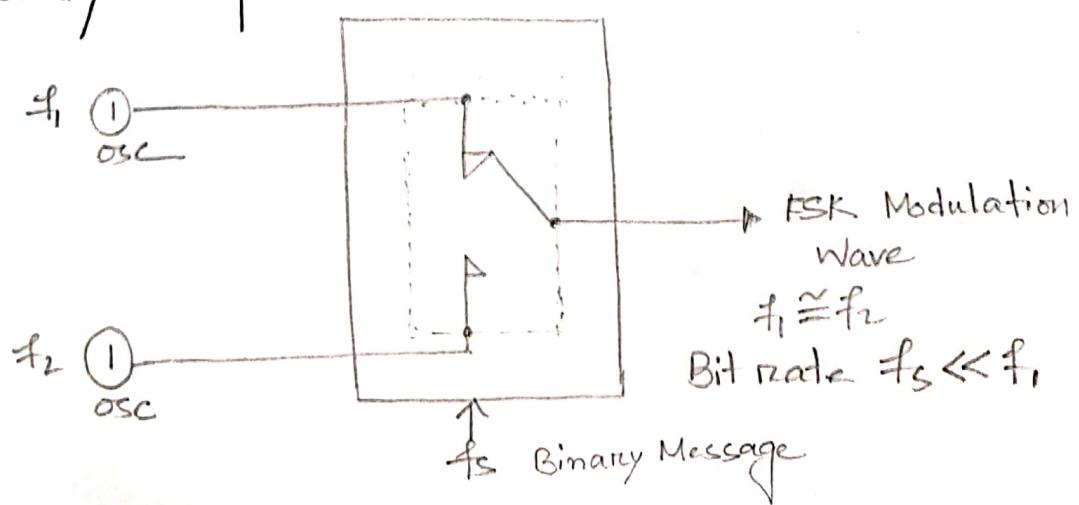


fig: an FSK signal (below) & the message (above)

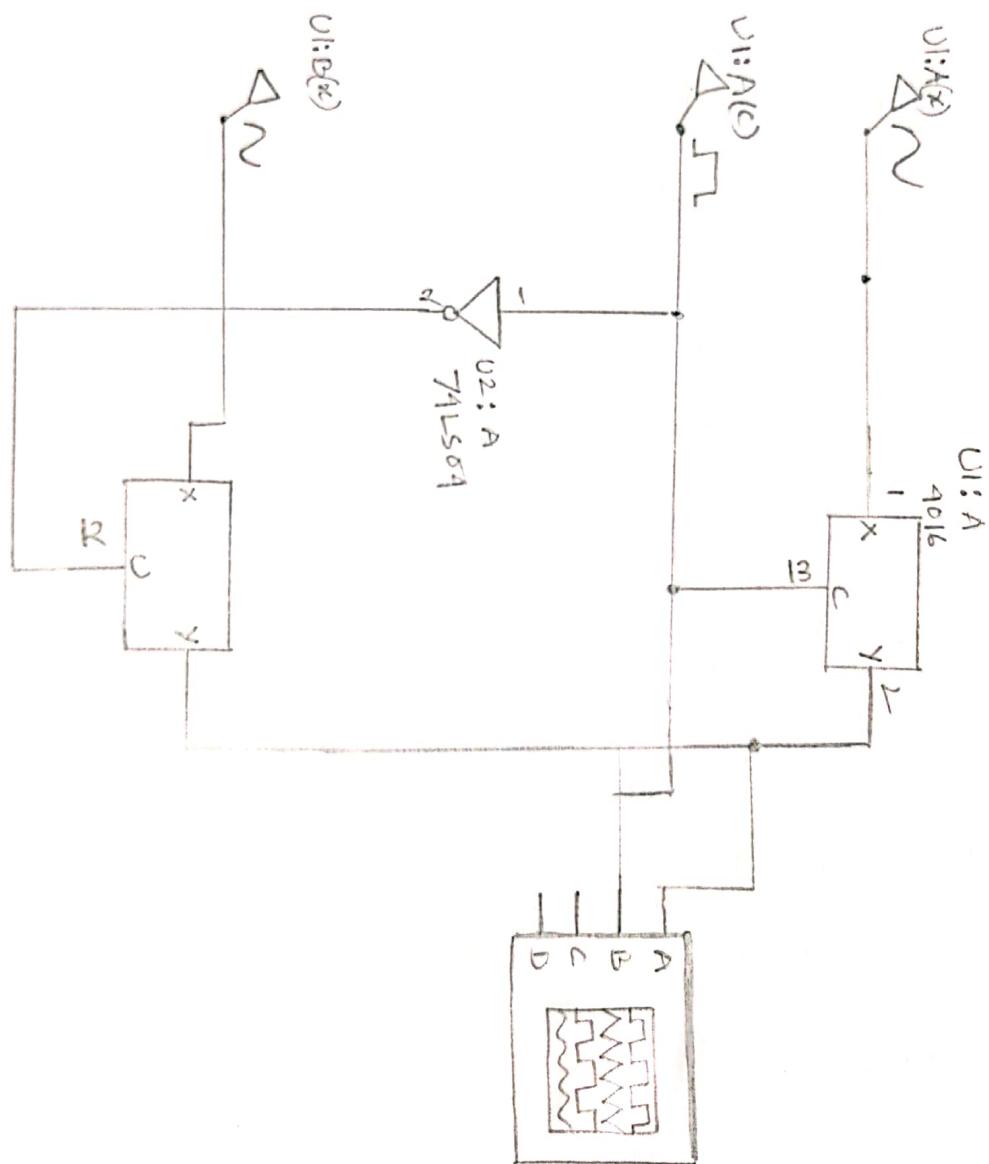
FSK Modulator : The FSK modulator block diagram comprises of two oscillators with a clock & the input binary sequence.



Apparatus :

1. CMOS - 4016
2. Inverter / Transistor - 74LS04
3. Register - MINRESIK
4. Generator - 1) SINE , 2) Pulse
5. Oscilloscope .

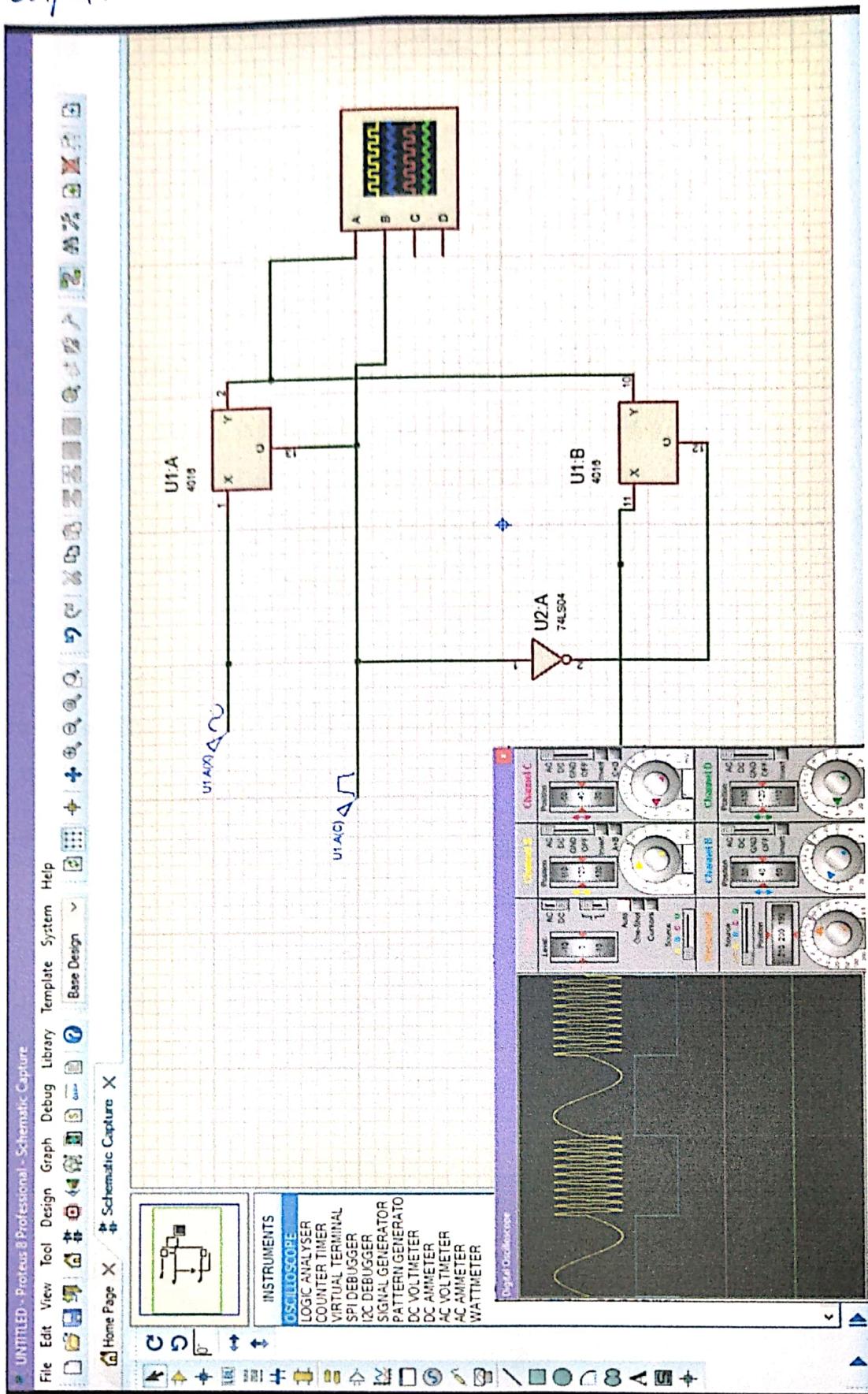
Design :



Working Procedure :

1. Connect pin 2 & Pin 10.
2. Oscilloscope pin A will be added with pin 2.
3. Oscilloscope pin B will be added with pin 13.
4. There is two Sine generator, one will be connected with pin 1 & other will be connected with pin 11.
5. Pulse generator will connected with pin 13 & transistor 74LS04 input side alonge with pin 12 of CMOS-4016 (V1:B)
6. Output of the transistor 74LS04 will be connected to pin 12.
7. And lastly we will adjust the amplitude = 1' Frequency = 500 & pulse = 5 for pulse wave.
8. In 1st sine wave amplitude = 1 & frequency = 1000
& 2nd sine wave amplitude = 1 & frequency = 10000 .
By this we will have our desire wave form.

Output:



Experiment No.: 03

Experiment Name: Generation of Binary Phase Shift Keying

Objective: The objective of the experiment is to design Binary Phase Shift Keying Modulators.

Theory: Phase-Shift Keying (PSK) is a digital modulation process which conveys data by changing (modulating) the phase of a constant frequency reference signal (the carrier wave). The modulation is accomplished by varying the sine and cosine inputs at a precise time.

BPSK is also called as 2-phase PSK or Phase Reversal Keying. In this technique, the sine wave carrier takes two phase reversals such as 0° and 180° .

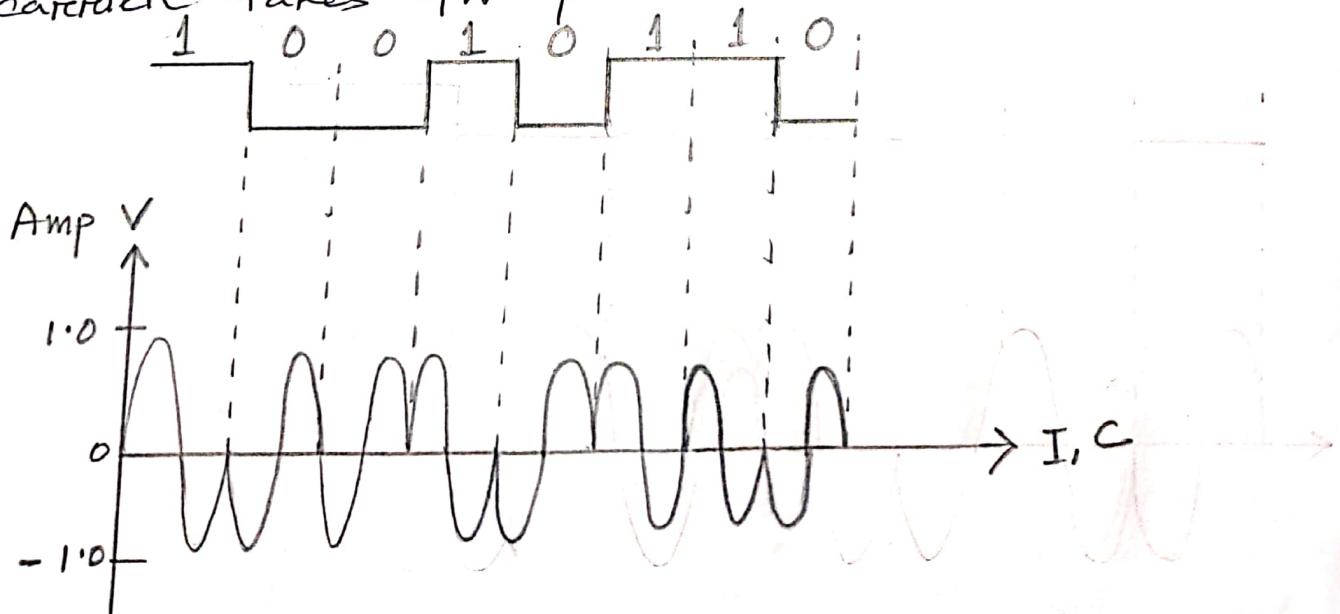
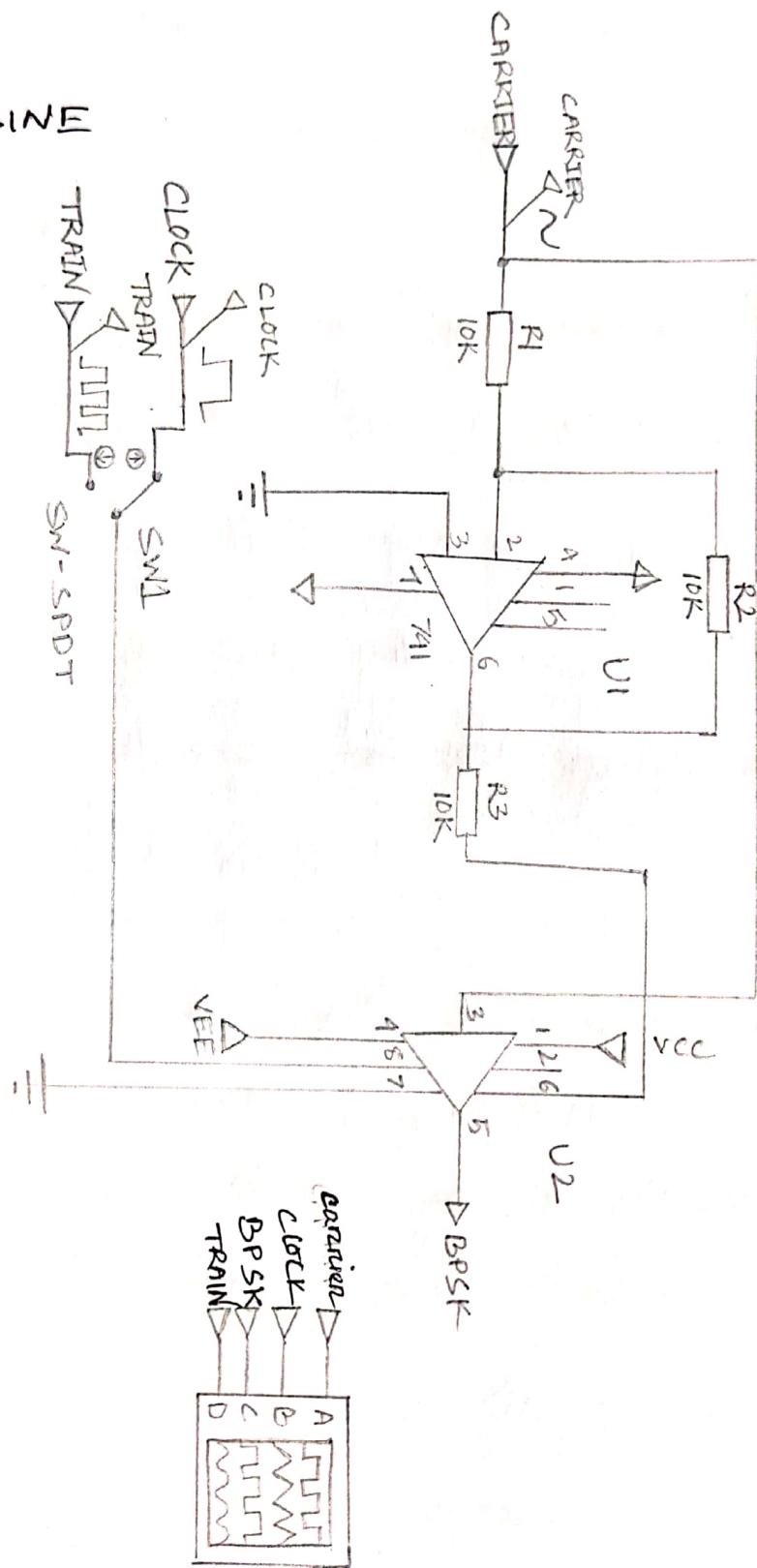


Fig: Phase Shift keying (PSK)

Apparatus :

1. Operational Amplifier - 741
2. Power (2)
3. Ground
4. Resistors - MINRES10K (2)
5. Input
6. Generator SINE
7. Amplifier - LF398A
8. Output
9. SW-SPDT (switch)
10. Oscilloscope

Design :



Working Procedure :

1. After opening proteus, we will select Design, then we will select configure Power Rails. Hence we will select in power supply VCC/VDD (voltage common collector) & fixed its voltage = 12. After that we will select VEE & fixed its voltage = -12.
2. Then select component & take an operational amplifier 741 & set it.
3. From terminal, we will took two power. & connect them with pin 4 & pin 7 of the 741.
4. Then connect ground with pin 3.
5. Select resistors R₁ & R₂. And connect R₂ with pin 6. R₁ & R₂ will be connected together with pin 2.
6. Select an input. And named it carrier.
7. Sine generator will be fixed up in carrier. And set amplitude = 12V & frequency = 50 Hz.
8. Select a amplifier - LF398N. and connect its pins with resistor R₃. R₃ resistor will connect with 741's pin 6.
9. Take two input. connect one with pin 1 & another with pin 4 of the amplifier LF398N.

10. The input VCC is connected to pin 1 & the input VEE is connected with pin 4.
11. Take a ground and connect with pin 7.
12. Select a output & connect it with pin 5 & named the ground as BPSK.
13. Amplifier LF398N's pin 3 will be connected with input Carrier.
14. Taking two inputs & named them Clock & Train
15. Selecting device SW-SPDT. And connected with inputs Clock & Train.
16. Select a pulse generator & connect it with clock. And select pulsed (High) voltage = 10 & frequency = 25.
17. Select a pattern generator & connect it with Train. And select pulse width (secs) = 20m.
18. The Oscilloscope pin A will connected with input name CARRIER, pin B connect with input CLOCK. Pin C will connected with output named BPSK. Pin D will connected with input TRAIN.

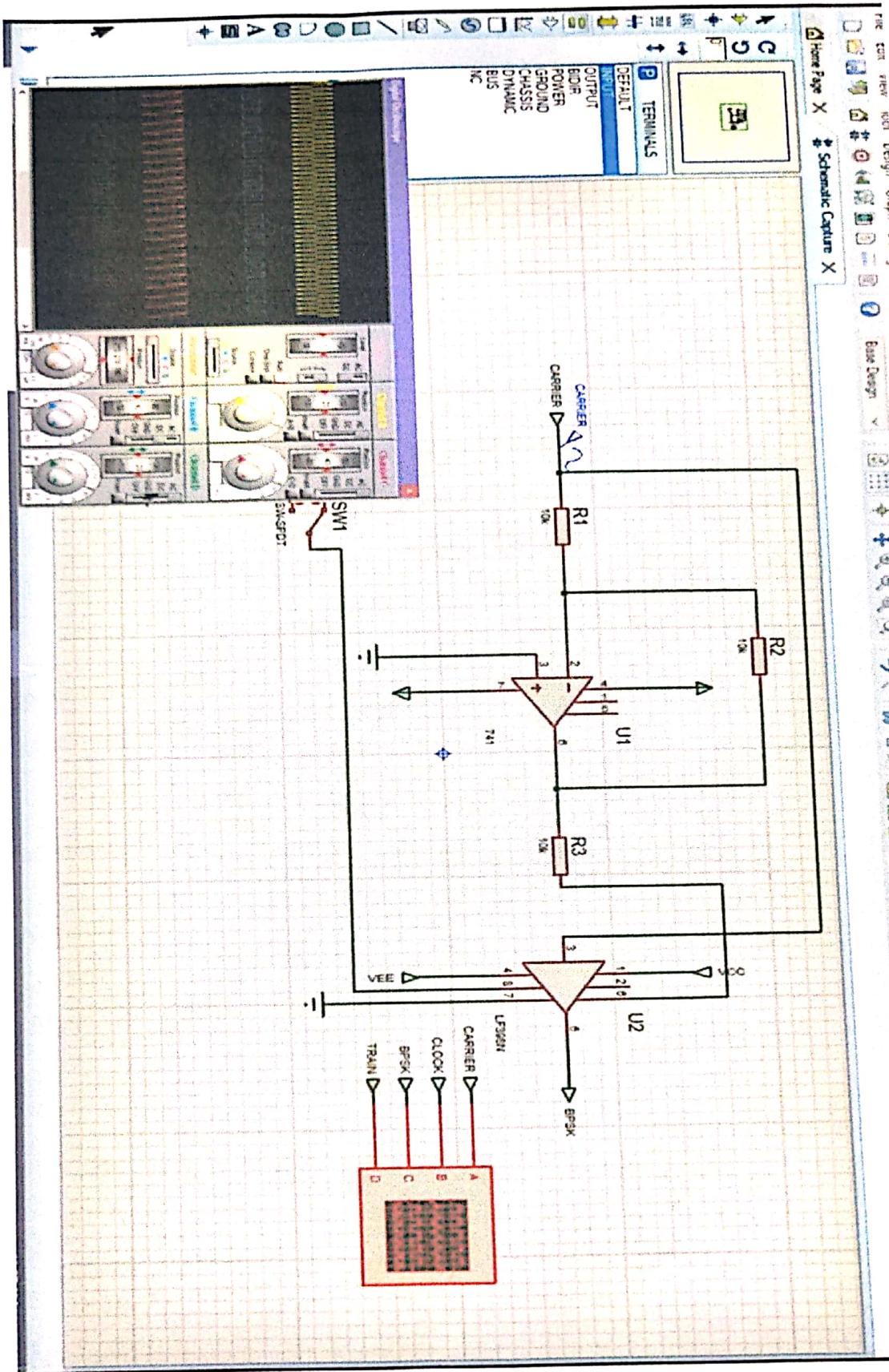
By this, we will have our desire wave form.

AND

AND

D

OR



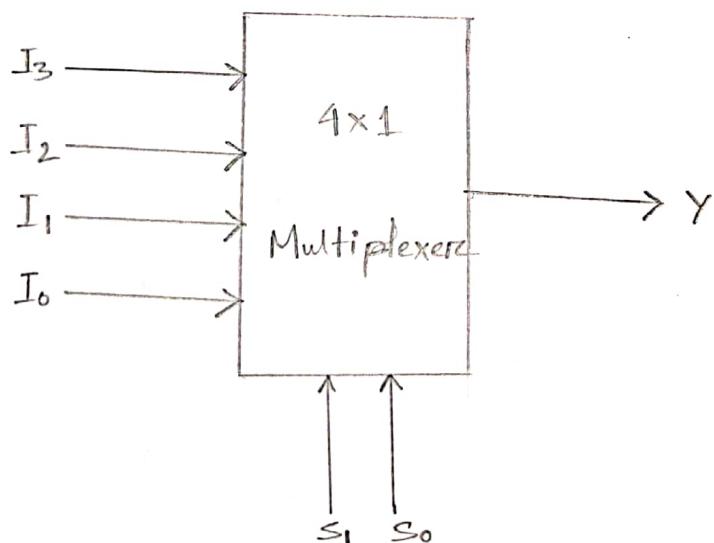
(A)

Experiment No. 04

Experiment Name: Design 4 to 1 Multiplexer.

Objective: The objective of the experiment is to design 4 to 1 multiplexer.

Theory: The multiplexing divides the capacity of the communication channel into several logical channels one for each message signal or data stream to be transferred. A reverse process, known as demultiplexing, extracts the original channels on the receiver end.



Multiplexer is abbreviated as MUX.

A 4:1 multiplexer has a single input (D), two selection lines (S_1 and S_0) and output Y .

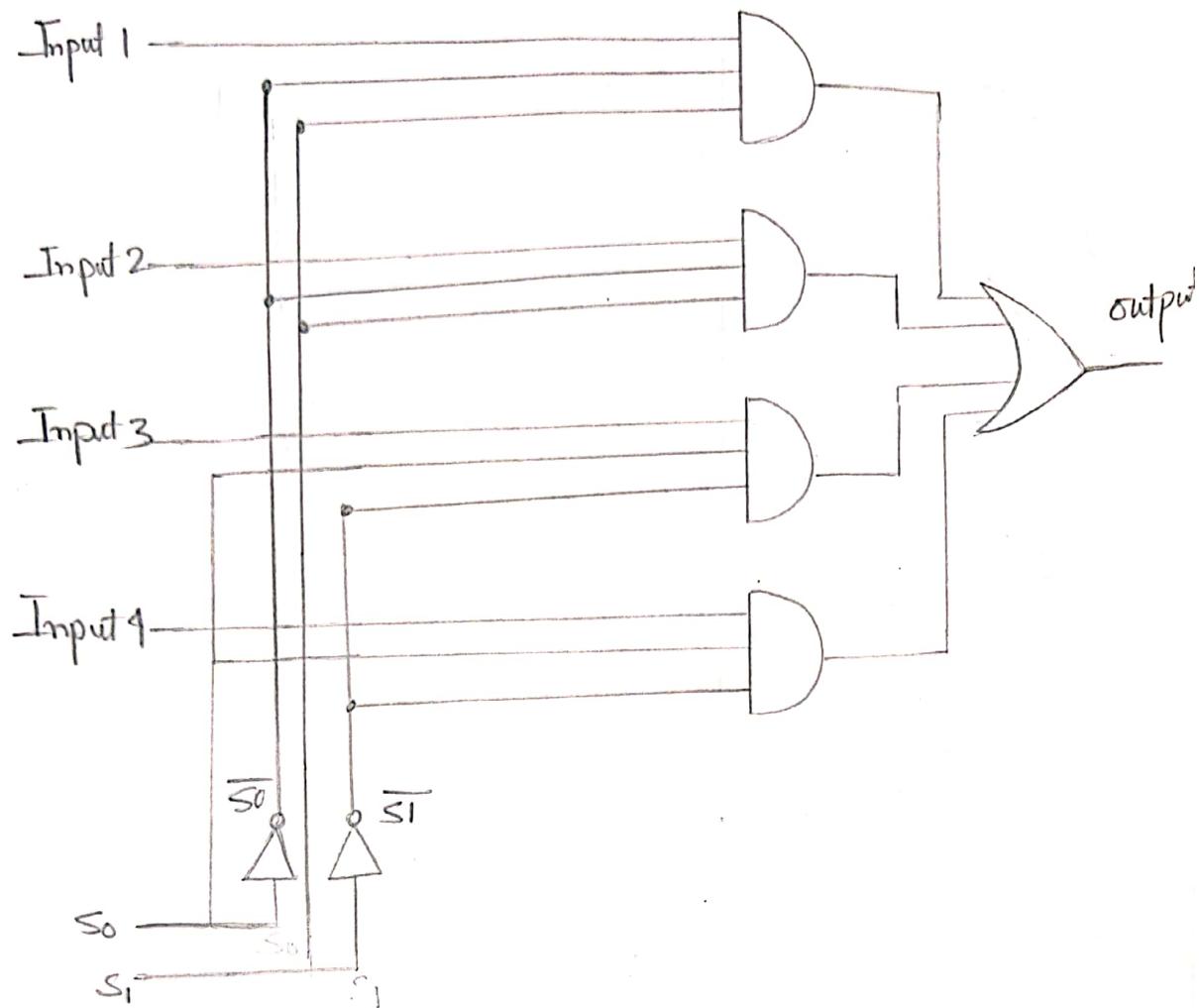
The input data goes to any one of the four input at a given time for a particular combination of select lines.

It has four select lines and 1 output line.

Timing Diagram for input /output :

S_0	S_1	D_0	D_1	D_2	D_3	Y (output)
0	0	0	x	x	x	0
0	0	1	x	x	x	1
0	1	x	0	x	x	0
0	1	x	1	x	x	1
1	0	x	x	0	x	0
1	0	x	x	1	x	1
1	1	x	x	x	0	0
1	1	x	x	x	1	1

Design:



Working Principle:

- ① In the child sheet we will take four AND Gate & one OR Gate with two NOT Gate.
- ② Each AND Gate has three inputs port. All first input will connect with the random input each.
- ③ \bar{S}_1 will connect with first and third AND Gates third input.

④ s_1 will be connected with second & fourth AND Gate's third input.

⑤ s_0 will be connected with third & fourth AND Gate's second input.

⑥ \bar{s}_0 will be connected with first & second AND Gate's second input.

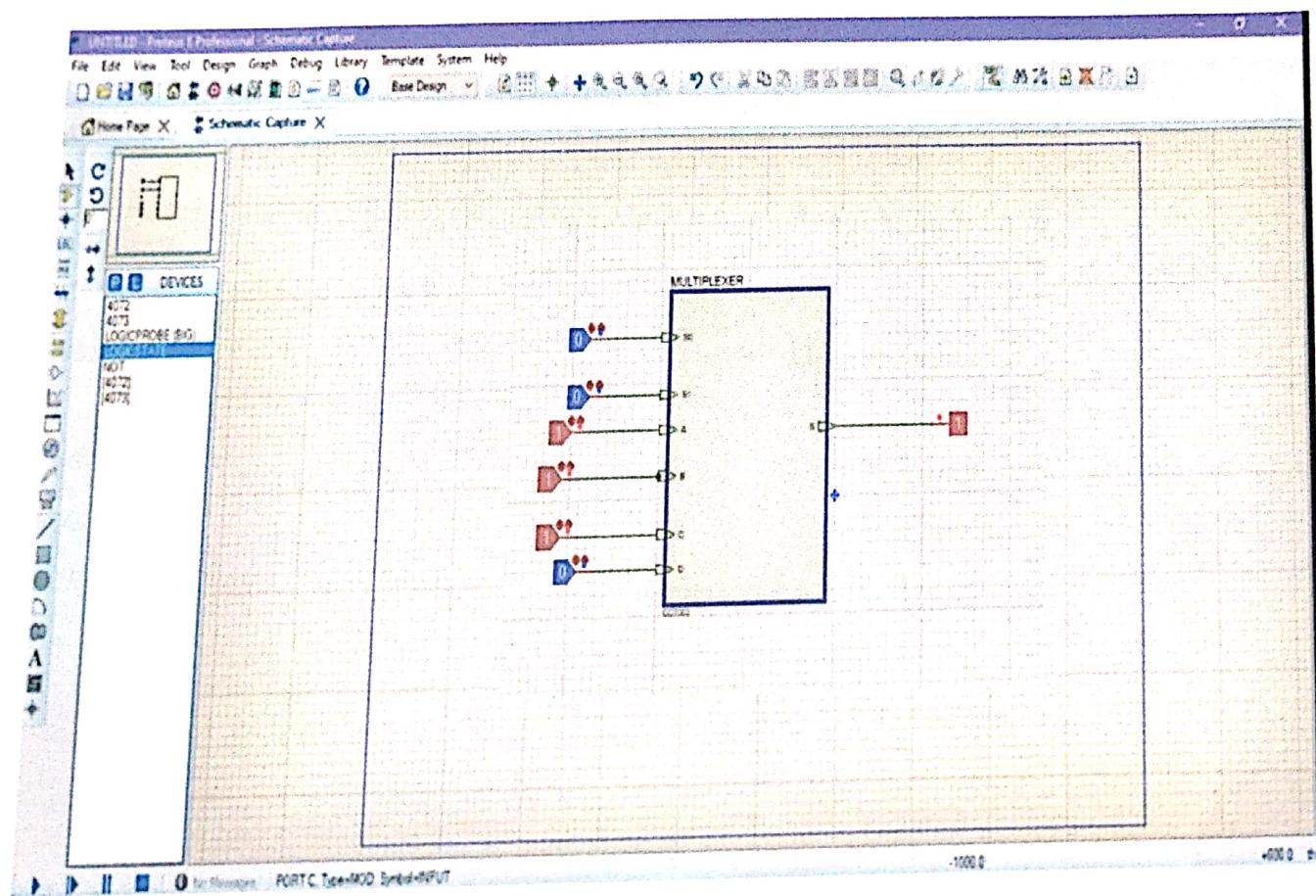
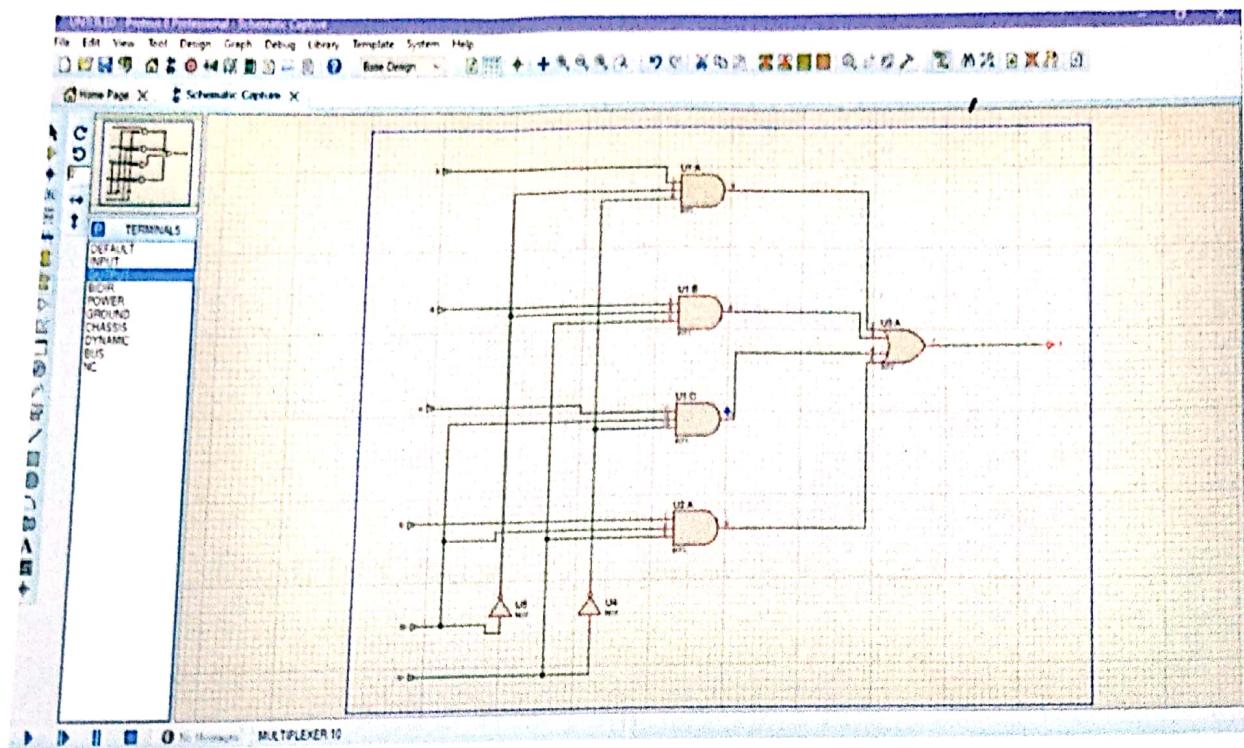
⑦ All four AND Gate will be added with the OR Gate input. It means all four output of AND Gate are the inputs of OR Gate.

By this we will get our output.

Output: We have shown here only one example,
where,

$$\begin{aligned} s_0 &= 1 \\ c &= 1 \end{aligned} \quad \left. \begin{array}{l} \text{ } \\ \text{ } \end{array} \right\} \text{among six inputs.}$$

As a result the output becomes '1'.



Experiment No: 05

Experiment Name: Design 1 to 4 Demultiplexer.

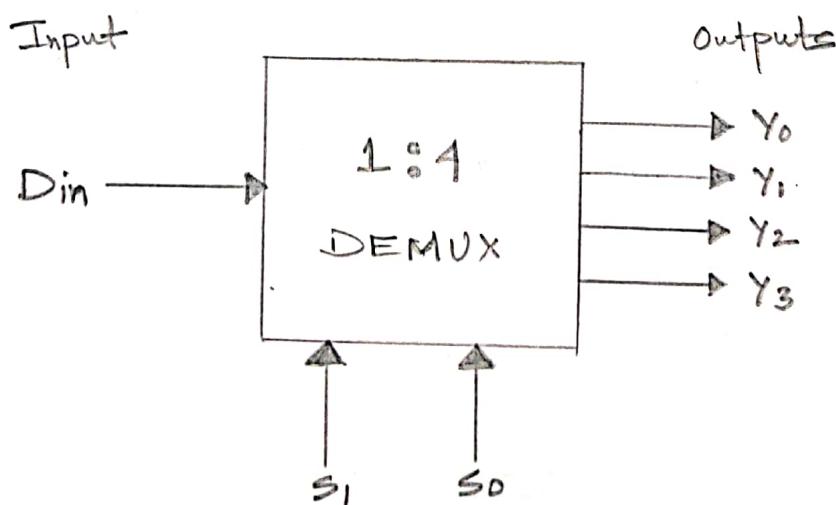
Objective: The objective of the experiment is to design 1 TO 4 Demultiplexer.

Theory :

■ A demultiplexer (or demux) is a device that takes a single input line and routes it to one of several digital output lines.

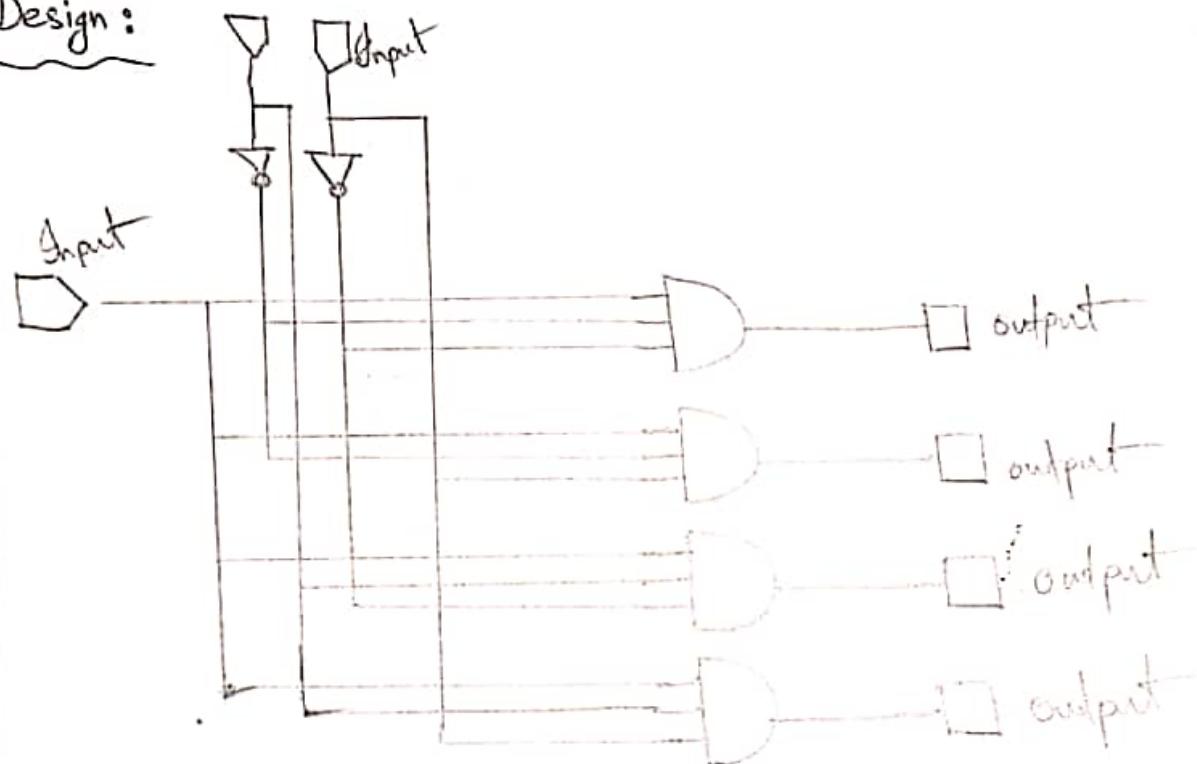
■ A demultiplexer of 2^n output has n select lines, which are used to select which output line to send the input.

■ A demultiplexer is also called a data distributor.



Truth Table:

S1	S0	D	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Design:Fig: 1:4 De-mux Circuit Design.

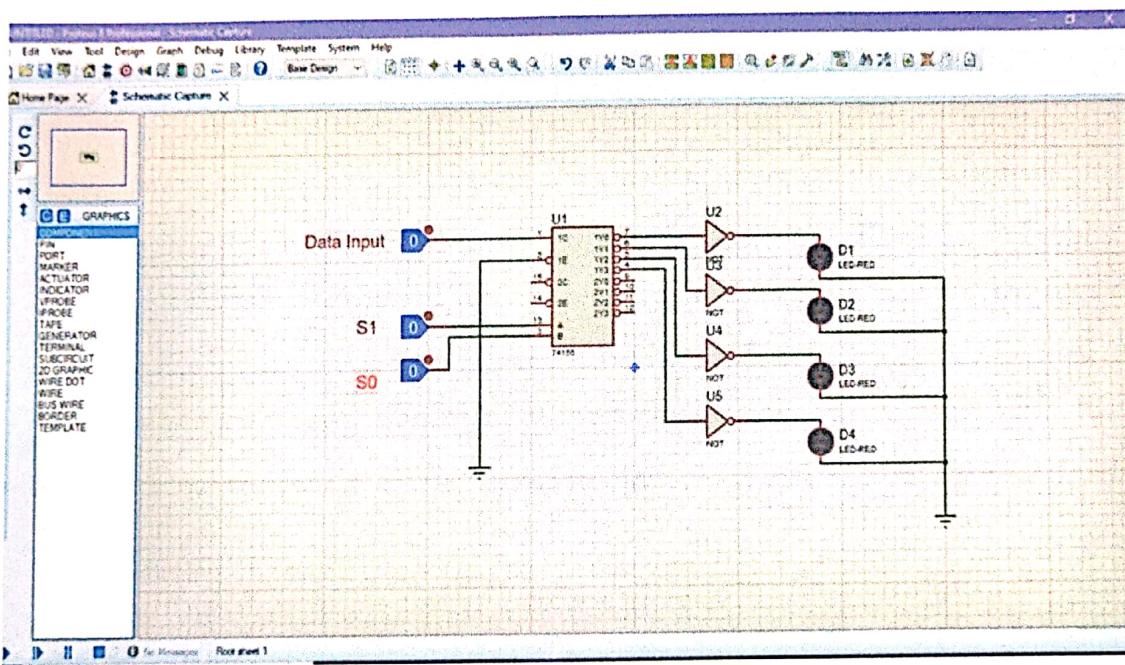
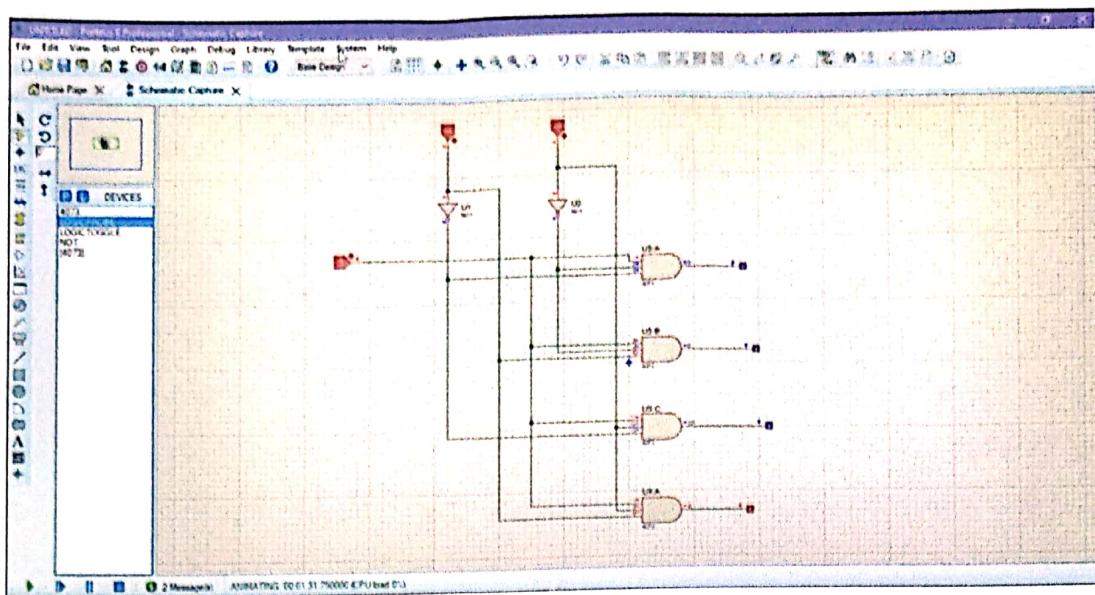
Working principle :-

- ④ Data will be added with every AND gate's first input part.
- ⑤ Two not gate will also the input part here.
- ⑥ $\overline{S_1}$ will be added 'two and fourth' AND gate's third input part.
- ⑦ $\overline{S_1}$ will be added 'one and third' AND gate's third input part.
- ⑧ So will be added with 'three and fourth' AND gate's second input part.
- ⑨ So will be added with 'first and third' AND gate's second input part.
- ⑩ ~~Each and so~~ The outputs will be connected with four AND Gates.

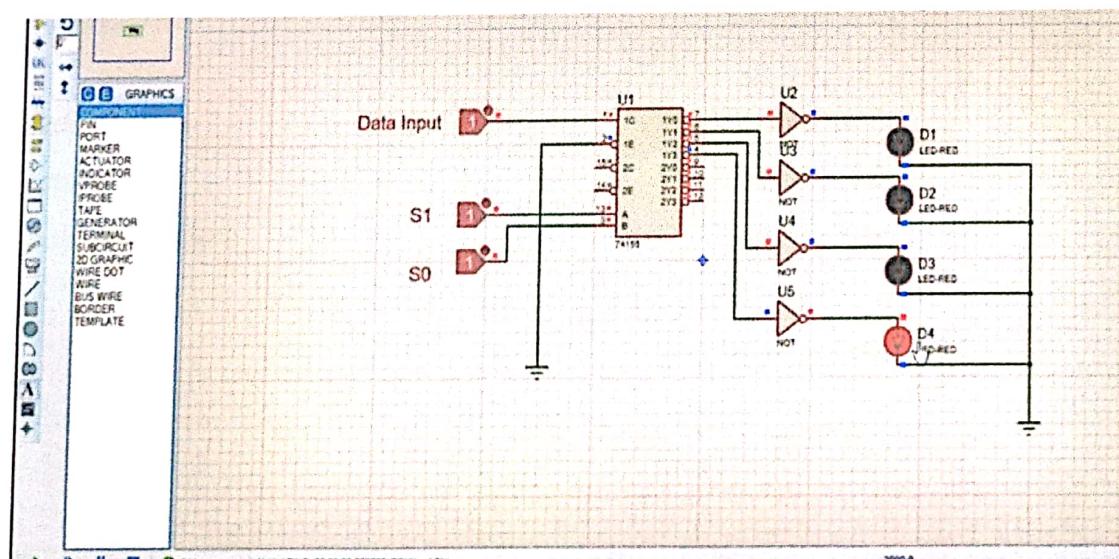
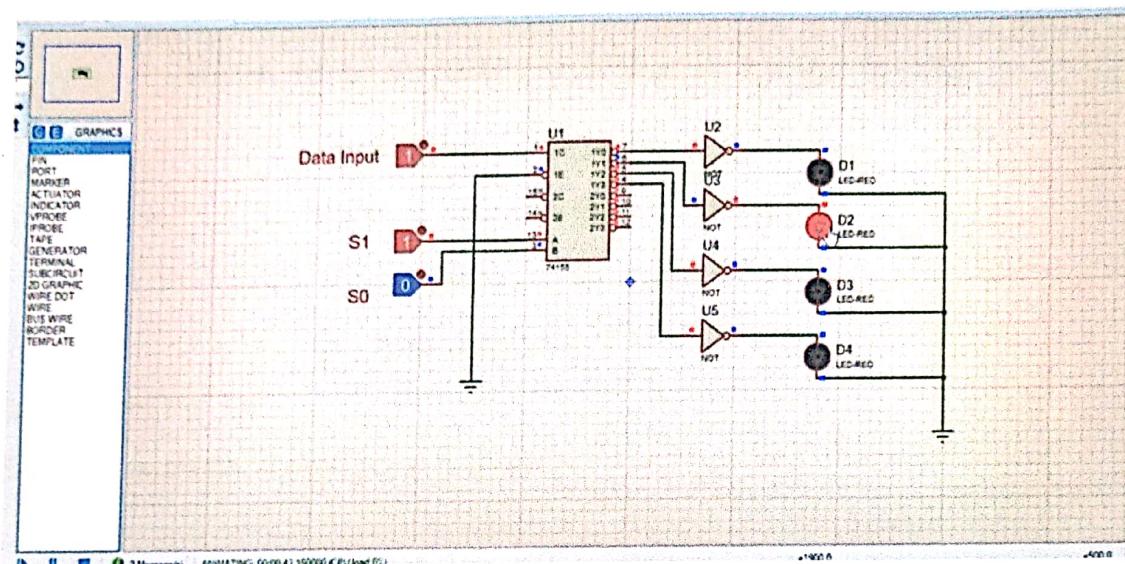
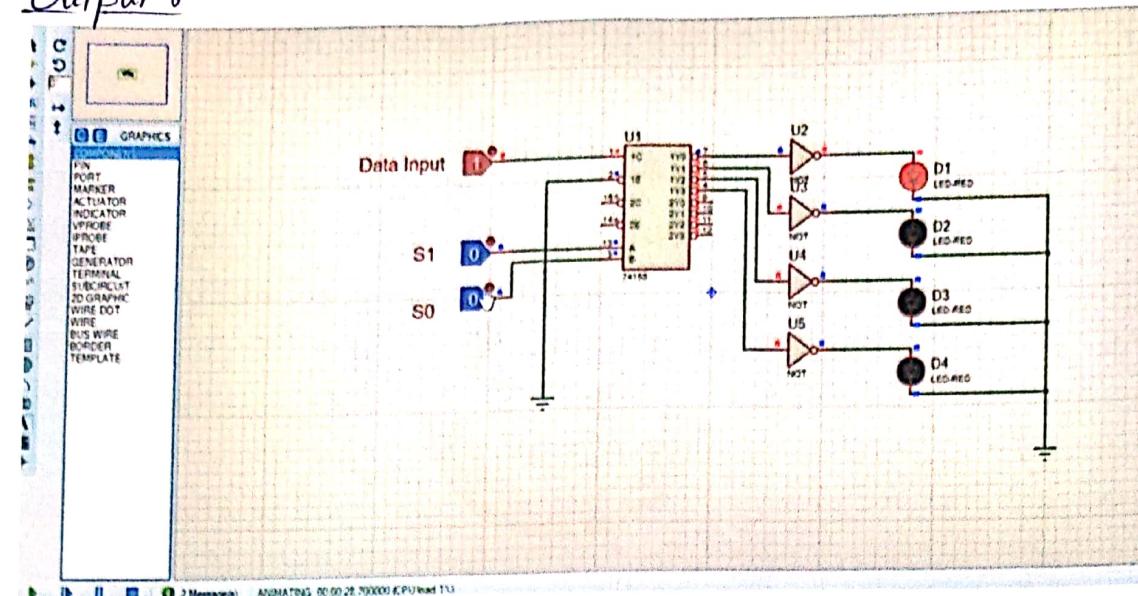
By this way we will get out output.

Output: Here, we have shown only one example.

$$\begin{aligned} D &= 1 \\ S_1 &= 1 \\ S_0 &= 0 \end{aligned} \quad \left\{ \text{---} \right. \quad \text{Output will be '1' in } Y_2 \text{ output and others remain zero (0).}$$



Output :



Experiment No: 06.

Experiment Name: Generation of Hamming Code.

Theory: Hamming code is a block code that is capable of detecting up to two simultaneous bit errors and correcting single-bit errors. In this coding method, the source encodes the message by inserting redundant bits within the message. These bits are extra bits that are generated and inserted at specific positions in the message itself to enable error detection and correction.

Encoding a message by Hamming Code:

Step 1 → Calculation of the number of redundant bits.

Step 2 → positioning the redundant bits.

Step 3 → calculating the values of each redundant bit.

Aparatus :

- ④ Logic Toggle .
- ④ X-OR Gate
- ④ LED-BLUE .
- ④ Circound .

Circuit Design :

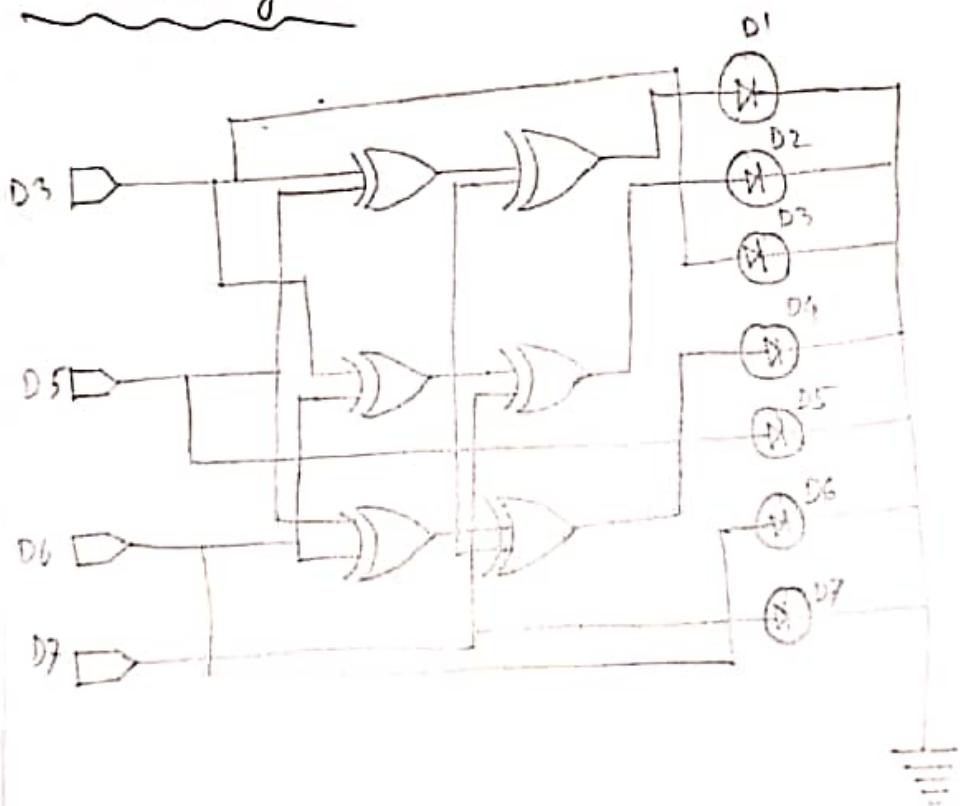
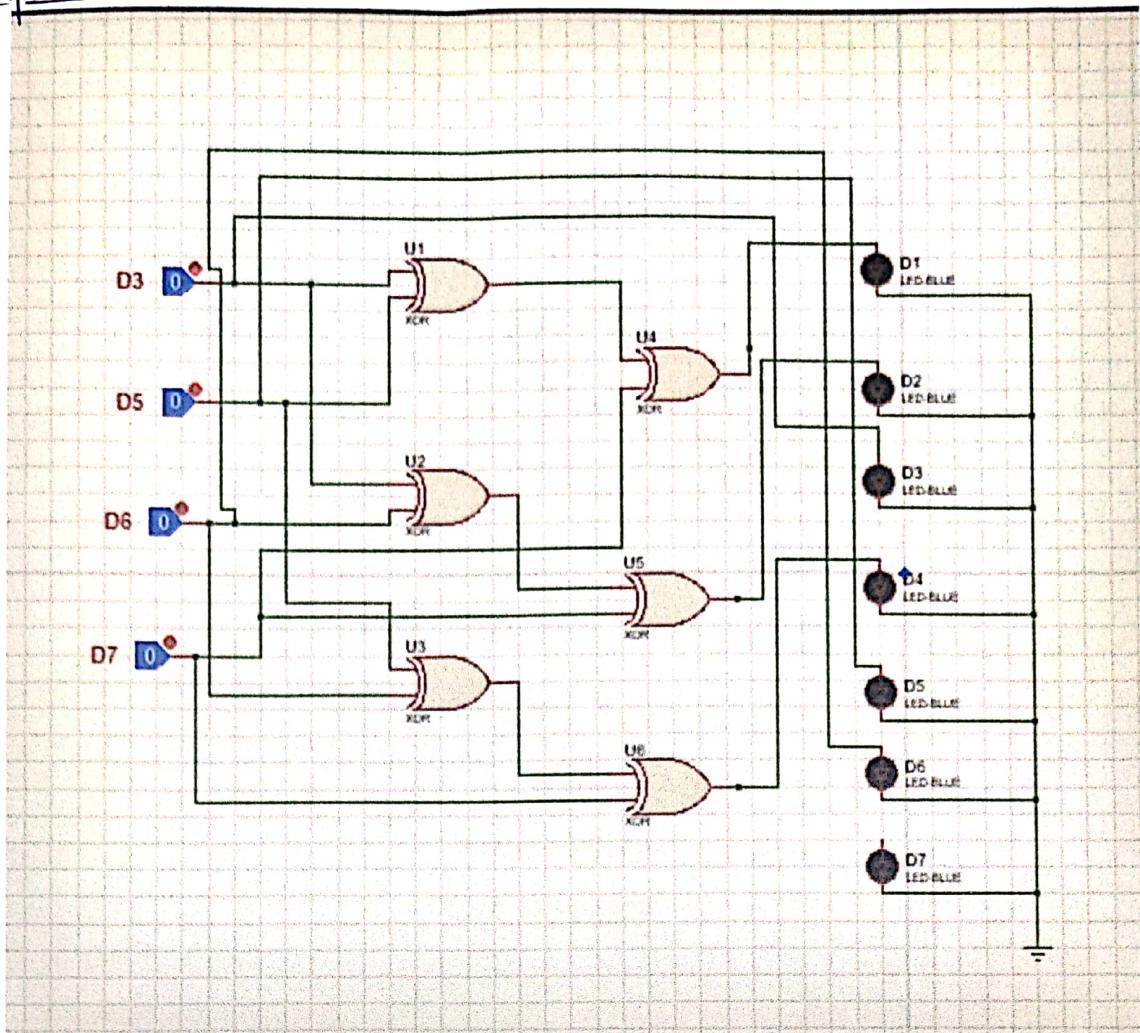


Fig: Hamming Code Generation .

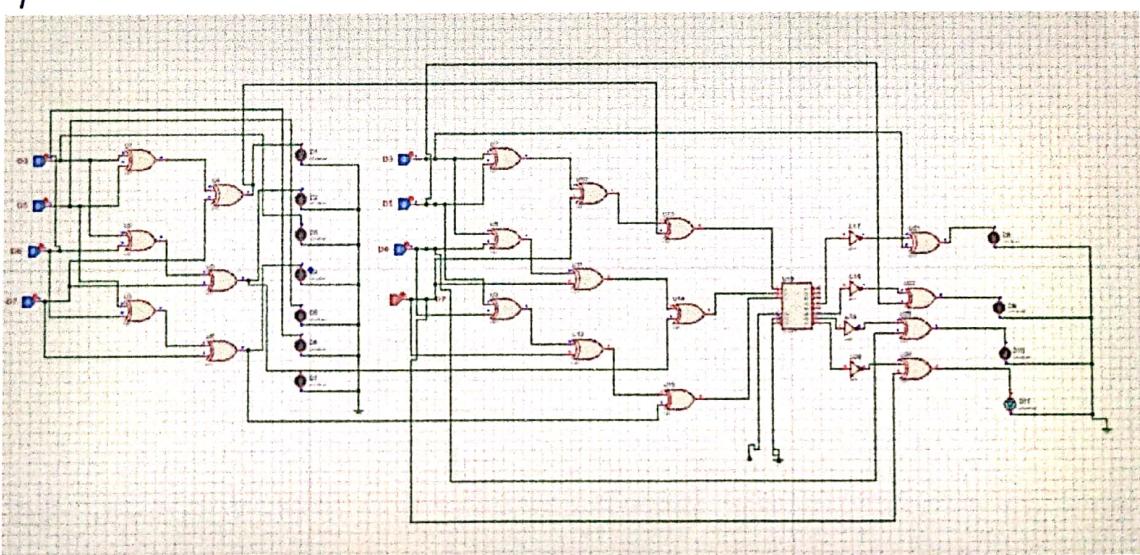
Working Principle :

1. First we will connect logic for
2. Toggle 1 will connect first X-OR Gate.
3. Toggle 2 will connect 2nd and 4th X-OR gate.
4. Toggle 3 will connect 3rd and 4th X-OR Gate.
5. Toggle 4 will connect 2nd, 5th and 6th X-OR Gate.
6. LED - Blue light will be connected with Toggle 2 X-OR gates.
7. 2nd, 1st & 5th X-OR Gate will connect to the first, 2nd & 4th LED BLUE Respectively.
8. All the LED will be connected to the Ground.
Then we will get our output.

Input :



Output :



Experiment No : 07

Experiment Name : Hamming Code Generation and Error Detection.

Objective : The objective of the experiment is to design Hamming code generation and error detection.

Theory : In computer science and telecommunication, Hamming codes are a family of linear error-correcting codes. Hamming codes can detect up to two-bit errors or correct one-bit errors without detection of uncorrected errors.

If these errors are not corrected & detected then the data will lost. For effective communication, system data should transfer with high accuracy!

This will be done by first identifying the errors & then correcting them.

Three types of error detection codes are:

- ① Parity checking.
- ② Cyclic Redundancy Check (CRC)
- ③ Longitudinal Redundancy Check (LRC).

-Types of Errors:

- ① Single bit errors
- ② Multiple bit errors
- ③ Burst errors .

0	1	1	0

0	0	1	0

Single error

0	1	0	1

0	0	0	0

Multiple errors

1	0	1	0

0	1	0	0
↑	↑	↑	

Burst Errors

Appliances:

1. Logic Toggle .

2. Not Gate .

3. X - OR Gate .

4. LED - BLUE

5. 74LS - 138 encode .

Working Principle: After Hamming Code generation we will detect the errors.

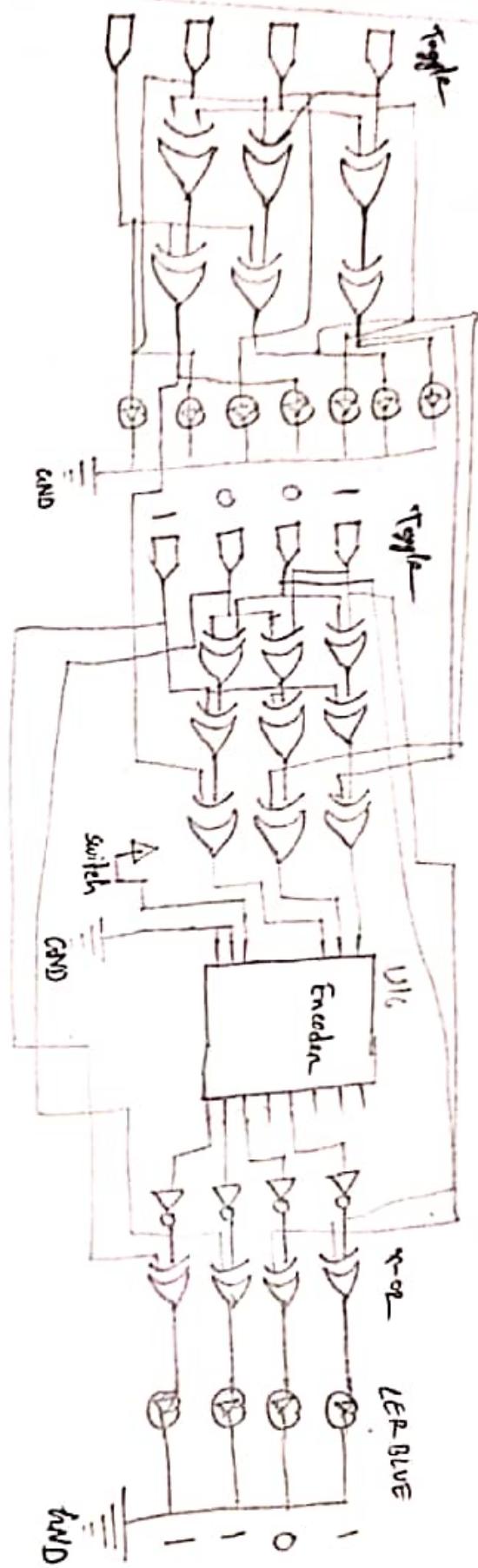
- ① Toggle one, two & third will connect with 7th, 9th, 10th X-OR gate.
- ② Toggle 4 will connect with 8th, 11th & 12th X-OR gate.
- ③ Encoder's pin 1, 2, 3 will be added to the 13th, 14th & 15th X-OR Gate Respectively.
- ④ Encoder's 12, 10, 9, 7th pin will connect with First 2nd, 3rd & 4th not Gate Respectively.
- ⑤ All the LED-BLUE will be added with Ground.
- ⑥ Here we, shown only one error.

Input is 1001 but the output is 1011. Only one bit change here.

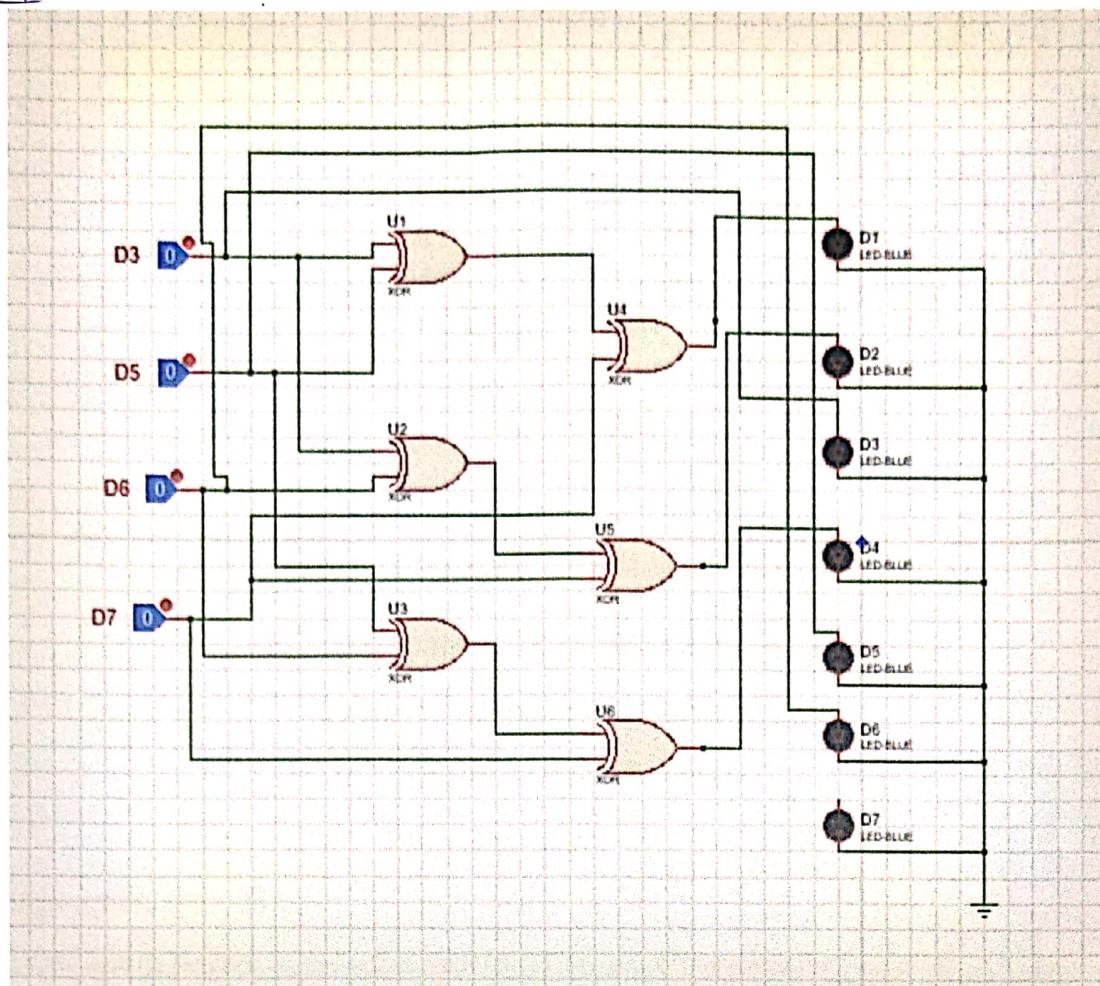
7-3

Circuit Design :

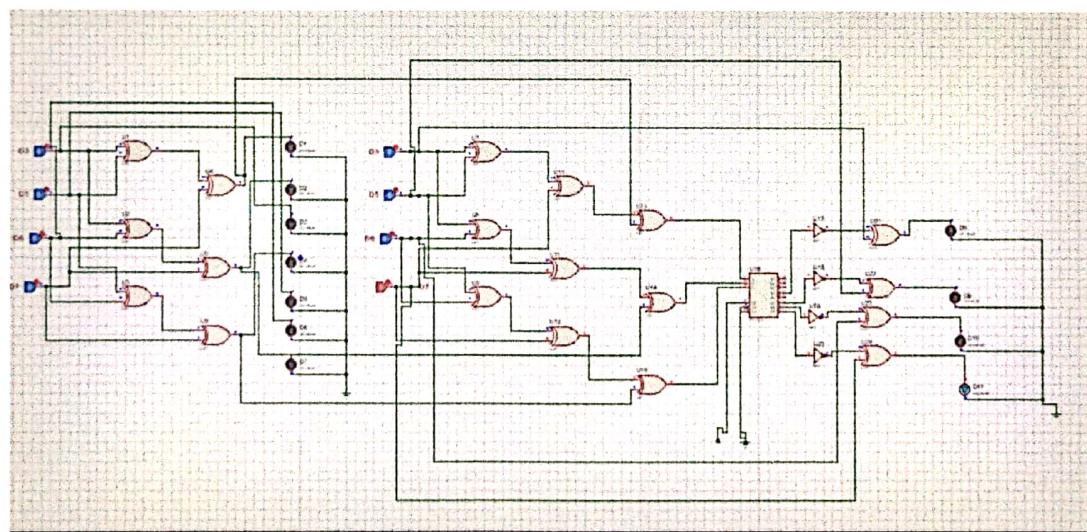
Fig: Circuit Design of Error Detection .



Input :



Output :



Experiment No: 08

Experiment Name: Implementation of RS-232 serial communication.

Objective: The objective of the experiment is to design RS-232 Serial Communication.

Theory:

Serial Communication: In telecommunication, the process of sending data sequentially over a computer bus is called as serial communication, which means the data will be transmitted bit by bit. While in parallel communication the data is transmitted in a byte (8 bit) or character on several data lines or buses at a time. Serial communication is slower than parallel communication but useful for long data transmission due to lower cost and practical reasons.

RS-232 RS232 is a standard protocol used for serial communication, it is used for connecting computer and its peripheral devices to allow serial data exchange between them. As it obtains the voltage for the path used for the data exchange between the devices. It is used in serial communication up to 50 feet with the rate of 1.92 kbps. As EIA defines, the RS232 is used for connecting Data Transmission Equipment (DTE) and Data Communication Equipment (DCE).

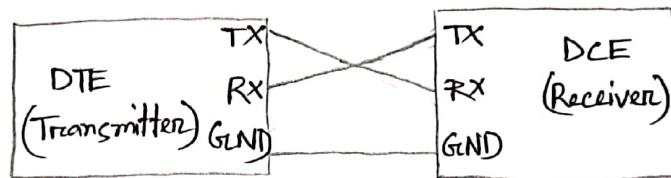
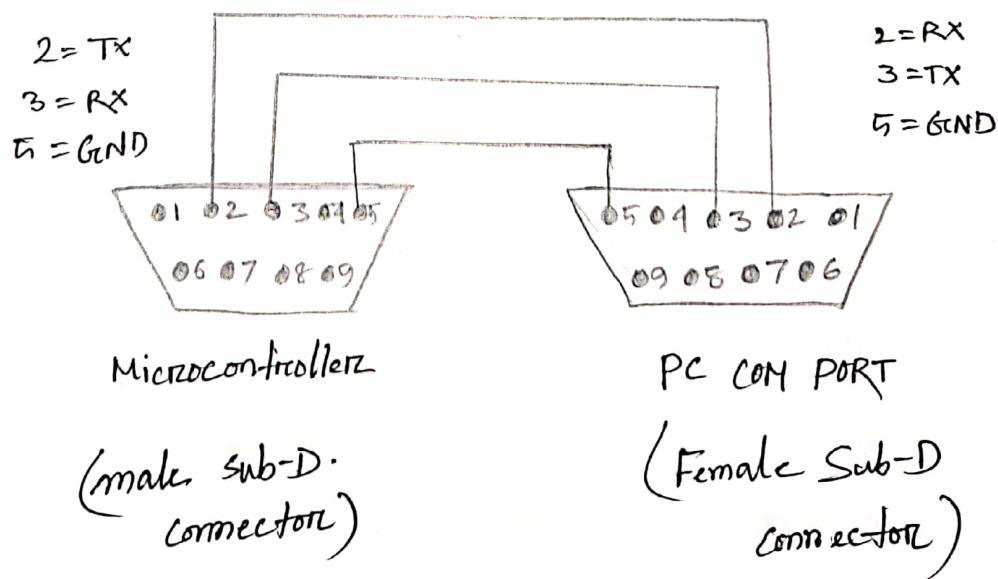


fig: RS232 protocol

RS232 Cable



PIN Description:

PIN No.	PIN Name	PIN Description
1.	CD (Carrier Detect)	Incoming signal from DCE
2.	RD (Receive Data)	Receives incoming data from DTE.
3.	TD (Transmit Data)	Send outgoing data to DCE
4.	DTR (Data Terminal Ready)	Outgoing handshaking signal
5.	GND (Signal ground)	Common reference voltage
6.	DSR (Data Set Ready)	Incoming handshaking signal
7.	RTS (Request to Send)	Outgoing signal for controlling flow
8.	CTS (Clear to Send)	Incoming signal for controlling flow
9.	RI (Ring Indicator)	Incoming signal from DCE

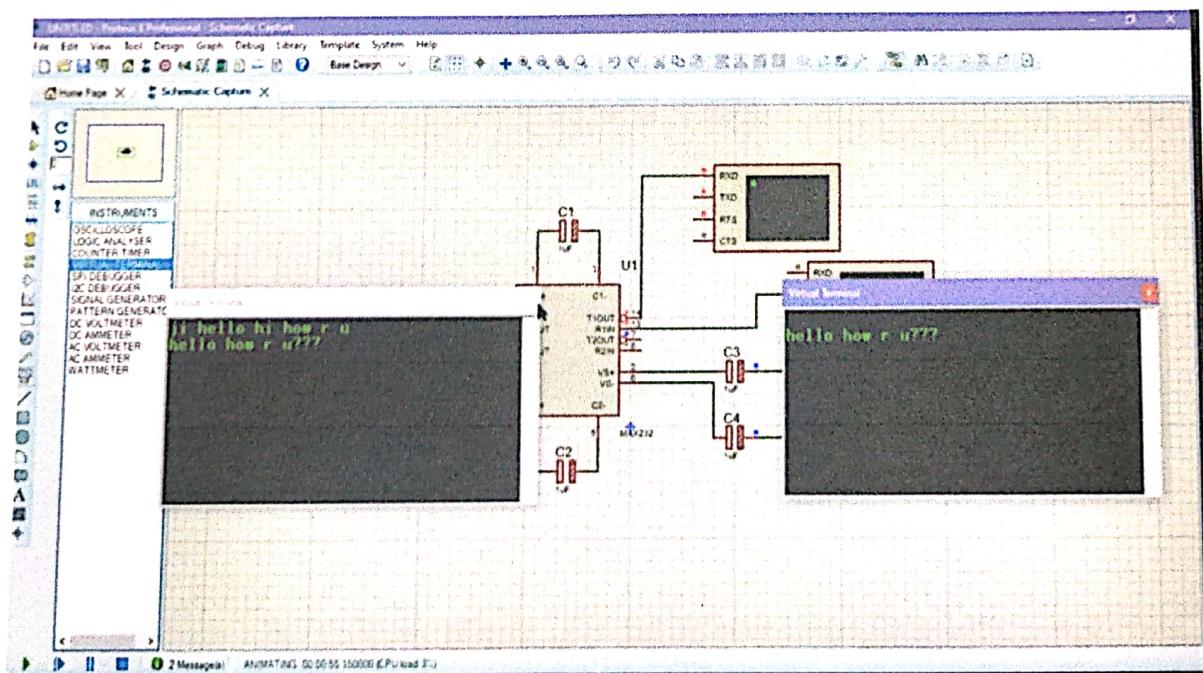
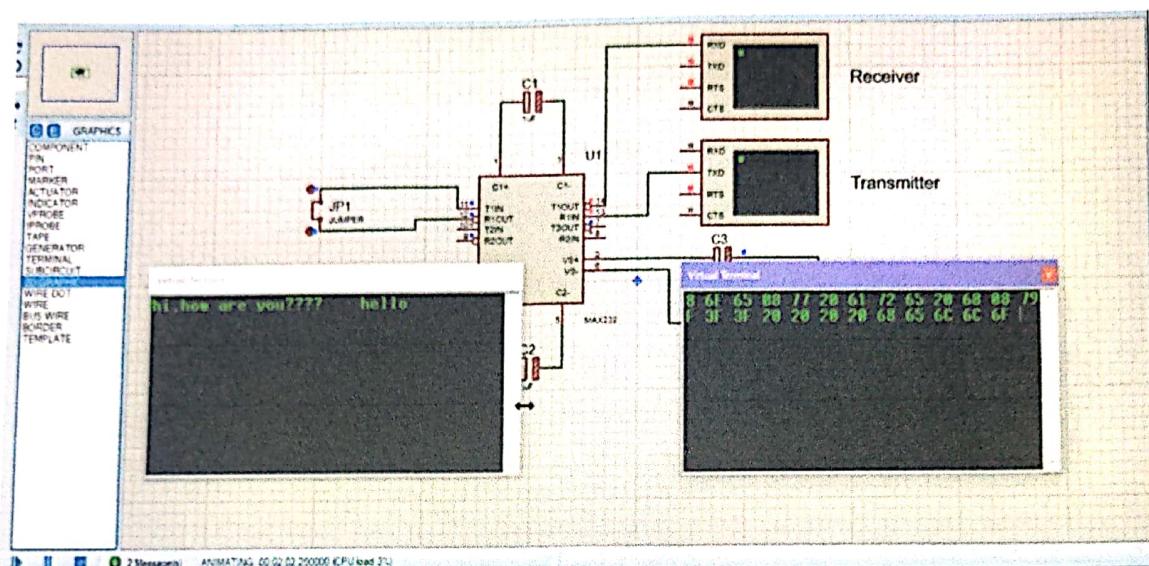
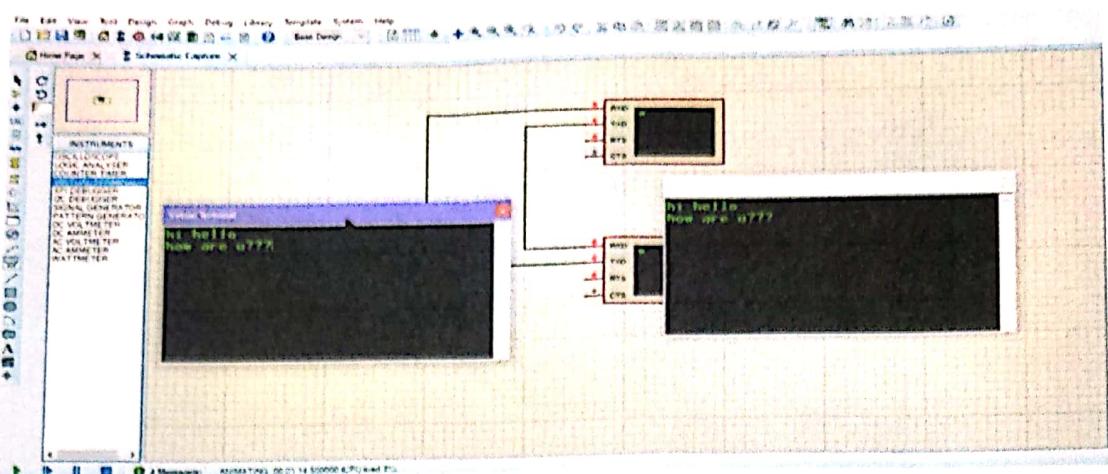
Apparatus:

- ① Virtual Terminals
- ② RS-232 → Max 232
- ③ Capacitors
- ④ Jumper
- ⑤ Ground

Working Principle:

1. First we will take Max 232. Then we will connect it with (jumper) JPI in pin 11 & pin 12 which will help to transmit & receive Data.
2. 4 capacitors will be C_1, C_2, C_3 & C_4
3. C_1 will connect with pin 1 & pin 3.

4. C_2 will connect with pin 4 & 5
5. C_3 will connect with pin 2 & C_9 will connect with pin 6.
6. Capacitor C_5 & C_9 will connect with ground.
7. Virtual terminals will be connected with 14 which will be Receiver (RXD). Then port 13 will be connected with another terminal which will be Transmitter (TXD). We need to active jumper.
8. Then we will run the simulation, And find our desire message.
9. If we want to see message in both terminal Then set echo typed character.
10. By inputting hexa value, we will receive character.
input \rightarrow 68 69 2C 68 6F 65 08 77 20 61 72 65
2C 6F 75 3F 3F 3F 20 20 20 .68 65
6C 6C 6C .
output \rightarrow hi, how are you ??? hello

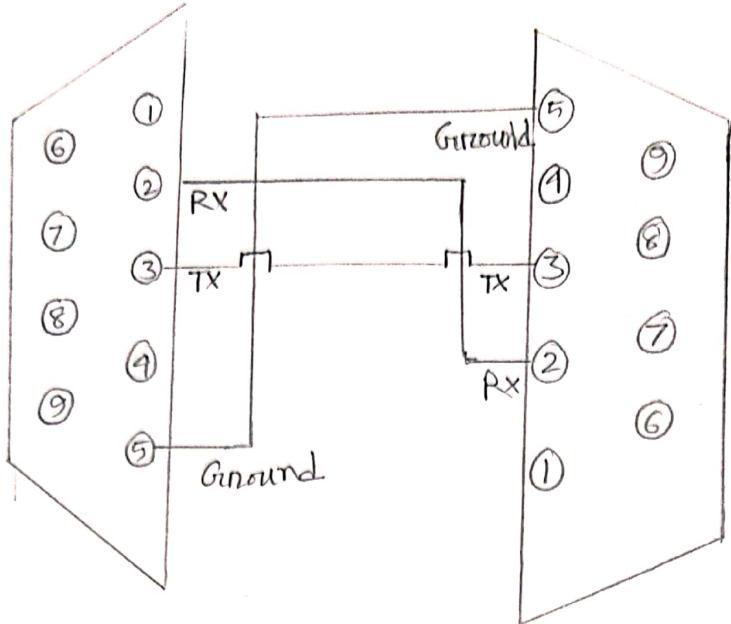


Experiment No.: 09

Experiment Name: Implementation of null modem communication.

Objective: The objective of the experiment is to implement the null modem communication.

Theory: Null modem is a communication method to directly connect two DTEs (computer, terminal, printers, etc.) using an RS-232 serial cable. With a null modem connection the transmit and receive lines are crosslinked. A null modem serial cable (frequently called a crossover cable) is used to connect two DTE devices together without the use of a DCE device in between. For this to happen, the Transmit (TXD) and Receive (RXD) pins on one of the serial connectors are flipped.



Apertures :

- | | |
|--------------------|----------|
| ① Virtual terminal | ⑤ Jumper |
| ② COMPIIM | ⑥ Ground |
| ③ RS 232 - MAX 232 | |
| ④ Capacitors | |

Working Principle :

- ① We need to open software virtual serial Port emulator, Then we need to connect with device. Named it COM 9.
- ② Max-232 will connected with capacitor c₁, c₂, c₃, & c₉,

- ③ Then we will connect the Jumper JPI with port 11 & 12.
- ④ C1 will be connected with port 1 & 3. C2 will be connected with port 4 & 5.
- ⑤ C3 will be connected with port 2 & C4 will be connected with port 4.
- ⑥ C3 & C4 will connect with ground.
- ⑦ COMPIM will connect with MAX-232. Port 2 RXD & port 3 TXD of COMPIM will connect respectively with Max-232 port 1A & port B.
- ⑧ COMPIM physical port name need to be correct.
- ⑨ Virtual terminal Receiver RXD will connect with Max-232 port 1A & Transmitter TXD will connect with Max-232 port B.
- ⑩ Activate both jumper.
- ⑪ Simulate the Null mode/ then receive the desire message.

