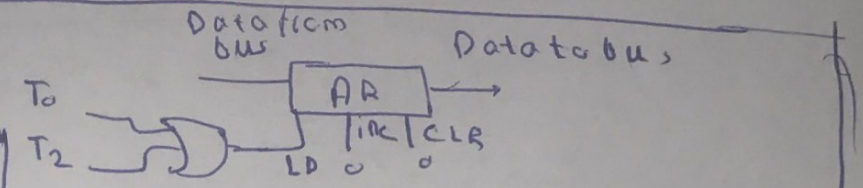
Design

1) Resistels (AR, PC, AC, DR, EC, IR)

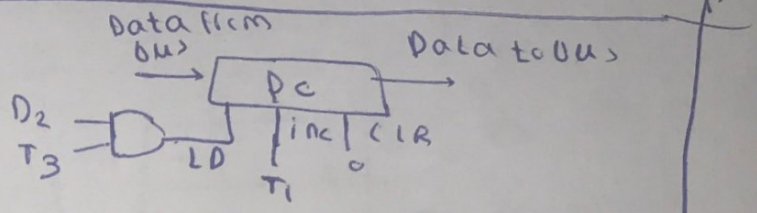
1) AR

- load → T_0: AR ← PC
- CLR → 0
- inc → 0
- T_2: AR ← IR(0-5)



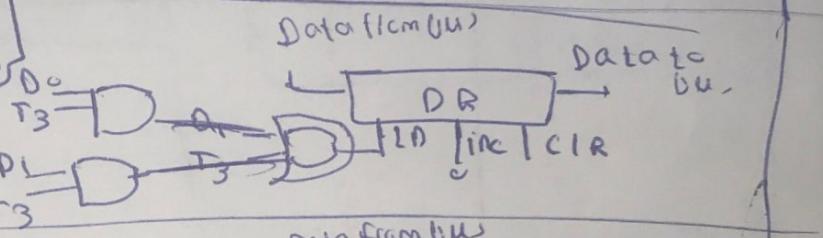
2) PC

- load → D_2T_3: PC ← AR
- CLR → 0
- inc → T_1: PC ← PC+1



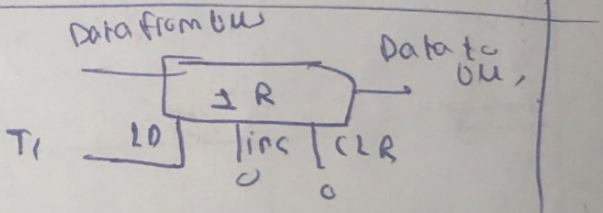
3) DR

- load → D_iT_3: DR ← M[AR]
- CLR → 0
- inc →



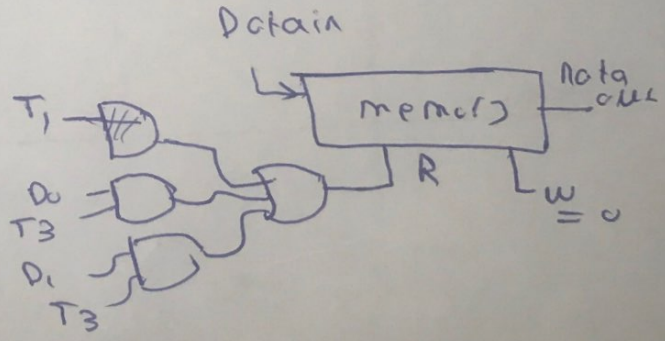
4) IR

- load → T_1: IR ← M[AR]
- CLR → 0
- inc → 0



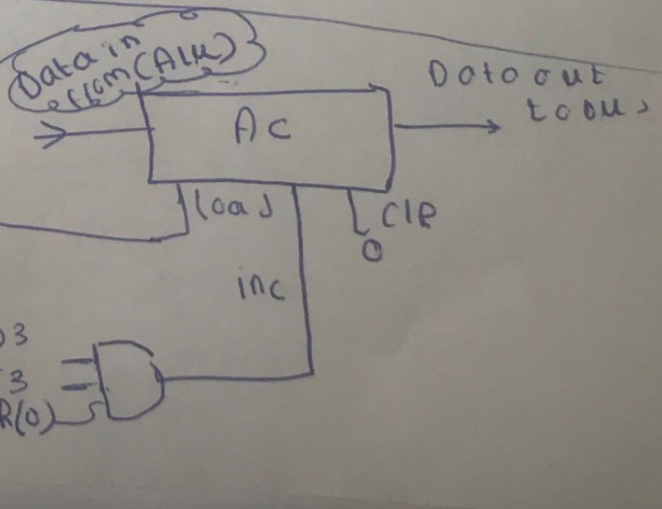
5) M[AR]

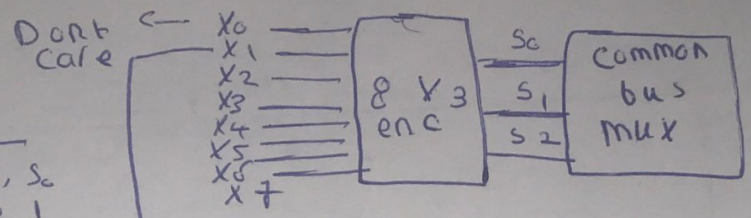
- W → 0
- R → T_1: IR ← M[AR]
- → D_0T_3: DR ← M[AR]
- → D_1T_3: DR ← M[AR]



6) AC

- load → D_0T_4: AC ← AC ∧ DR
- → D_1T_4: AC ← AC + DR
- → $D_3T_3IR(1)$: AC ← $\overline{AC}$
- CLR → 0
- inc → $D_3T_3IR(0)$: AC ← AC+1





① $X_1 = 1$ :: $S_2\ S_1\ S_0$ = 0 0 1

AR to Comm bus

$X_1 = D_2T_3$ (D_2, T_3)

② $X_2 = 1$ $S_2\ S_1\ S_0$ = 0 1 0

PC to comm bus

$X_2 = T_0$

② $X_3 = 1$ $S_2\ S_1\ S_0$ = 0 1 1

PR to comm bus

$X_3 = 0$

③ $X_4 = 1$ $S_2\ S_1\ S_0$ = 1 0 0

AC to comm bus

$X_4 = 0$

④ $X_5 = 1$ $S_2\ S_1\ S_0$ = 1 0 1

IR to Comm bus

~~$X_6 = T_2$~~ $X_5 = T_2$

⑤ $X_6 = 1$ $S_2\ S_1\ S_0$ = 1 1 0

TR to Comm bus

$X_5 = 0$

⑤ $X_7 = 1$ $S_2\ S_1\ S_0$ = 1 1 1

M[AR] to comm bus

$X_7 = T_1 + D_0T_3 + D_1T_3$

reg to comm bus

S_2	S_1	S_0	
0	0	0	none
0	0	1	AR
0	1	0	PC
0	1	1	DR
1	0	0	AC
1	0	1	IR
1	1	0	TR
1	1	1	memory