Report 5 : 95%
Prelab 5 : 100%
Prelab 6 : 99%

Jacobs University Bremen

CO-526-B
Electronics Lab

Fall Semester 2021

Lab Experiment 5 : Metal Oxide Field Effect Transistor

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Contents

1 Introduction

1.1 Theory

The objective of experiment is to familiarize with the basic characteristics and applications of Field Effect Transistors (MOSFETs). The lab includes an investigation of the I-V characteristics and the implementation of MOSFETs as amplifiers and switches.

The most common transistor types are the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and the Bipolar Junction Transistors (BJT). The BJTs are mainly used for specific applications like analog circuits, high-speed circuits or power electronics. The two main differences between BJTs and FETs are that FETs are charge-controlled devices while BJTs are current or voltage controlled devices and the input impedance of the FETs is very high while that of BJT is relatively low. As for the FET transistors, there are two main types: the junction field-effect transistor (JFET) and the metal oxide semiconductor field effect transistor (MOSFET). The power dissipation of a JFET is high in comparison to MOSFETs. Therefore, JFETs are less important if it comes to the realization of ICs, where transistors are densely packed. The combination of n-type and p-type MOSFETs allow for the realization of the Complementary Metal Oxide Semiconductor (CMOS) technology, which is nowadays the most important technology in electronics. All microprocessors and memory products are based on CMOS technology. The very low power dissipation of CMOS circuits allows for the integration of millions of transistors on a single chip..

1.2 Prelab Field Effect Transistor

1.2.1 Problem 1 : Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

Question 1

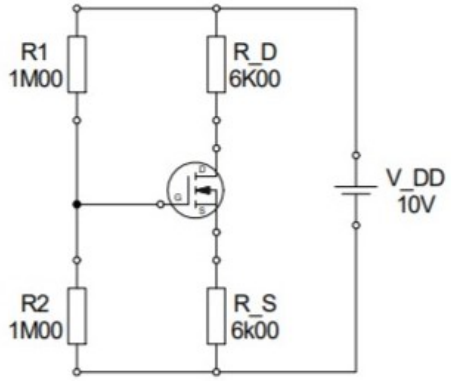
The difference between en enhanced and a depletion MOSFET is the conduction channel. For an enhanced MOSFET, the channel does not initially exist and is induced, so the channel is generated by applying a voltage greater than the threshold voltage at the gate terminals. Whereas in a depletion MOSFET, the channel is permanently fabricated during the construction of the MOSFET by doping

Question 2

The main difference between NMOS and PMOS is that, in NMOS, the source and the drain terminals are made of n-type semiconductors whereas, in PMOS, the source and the drain are made of p-type semiconductors. That is, the current flowing through NMOS is an electron current and the current flowing through a PMOS is a hole current.

1.2.2 Problem 2 : MOSFET as Amplifier

Considering the following circuit:



Question 1

Calculating the gate-source voltage:

$$V_G = V_D \frac{R_2}{R_1 + R_2} = 10 \times \frac{1}{2} = 5V$$

$$I_{DS} = k(V_{GS} - Vth)^2 = \frac{V_G - V_{GS}}{R_S}$$

$$\Rightarrow \quad \frac{5 - V_{GS}}{6000} = 0.0005(V_{GS} - 1)^2$$

$$\Rightarrow \quad V_{GS} = 2V$$

Calculating the drain-source voltage:

$$V_S = V_G - V_{GS} = 5 - 2 = 3V$$

$$I_D = \frac{V_S}{R_S} = \frac{3}{6000} = 0.5mA$$

$$V_D = V_{DD} - R_D I_D = 10 \times (5 \times 10^{-4} \times 6000) = 7V$$

$$\Rightarrow \quad V_{DS} = V_D - V_S = 7 - 3 = 4V$$

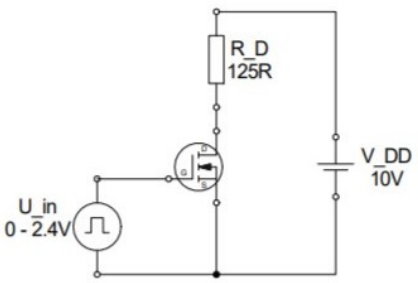
Question 2

$$V_{DS} - V_{GS} > V_{th} \quad \Leftrightarrow \quad 4 - 2 > 1$$

The condition above is fulfilled; which proves that the MOSFET is indeed operating in the saturation region.

1.2.3 Problem 3 : MOSFET as Switch

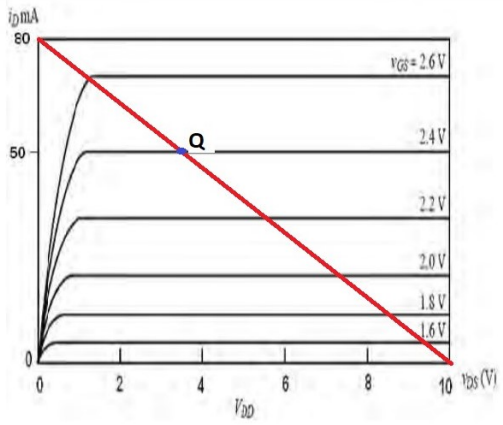
Consider the following circuit:



By performing a DC analysis on the circuit above we obtain the following equation, which we use to determine the operating points for $0V$ and $2.4V$ input.

$$V_{DS} = V_{DD} - I_D R_D$$

For $V_{DS} = 0V$, $I_D = 80mA$ and for $I_D = 0mA$, $V_{DS} = 10V$.
Using the DC line, we can determine the Q-point on the characteristic below.



At $2.4V$ input, $I_D(Q) = 50mA$

$$V_{DS}(Q) = V_{DD} - I_D(Q)R_D$$

$$\Rightarrow \quad V_{DS}(Q) = 3.75V$$

At $0V$ input, $I_D(Q) = 0mA$

$$\Rightarrow \quad V_{DS}(Q) = 0V$$

At $2.4V$ input, the MOSFET operates in saturation mode. At $0V$ input the MOSFET operates in cut-off mode.

2 Experimental Setup and Results

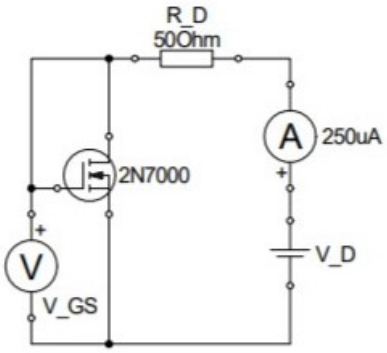
Workbench No 4:
Used tools and instruments:

- AC Voltage Generator
- TENMA multimeter
- Oscilloscope
- BNC-to-Kleps cable
- Voltage probes
- breadboard
- diode
- capacitor
- resistor

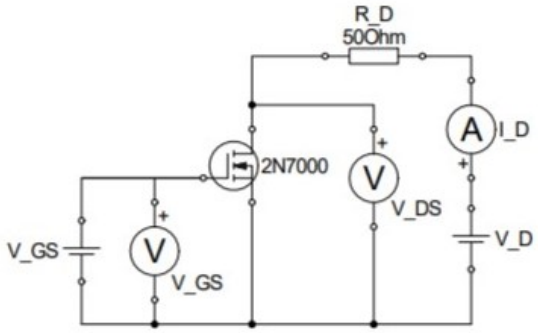
2.1 Problem 1 : I/V Characteristic of a MOSFET

2.1.1 Part 1: Setup

The two following circuits were implemented on the breadboard.



(a) Circuit used to determine U_{th}



(b) Circuit used to determine the transfer characteristics

2.1.2 Part 2: Execution and results

V_{th} and I_D obtained through the first circuit.

$$U_{th} = 2.1532V \qquad I_D = 249\mu A$$

From the second circuit:

The drain source voltage is kept constant at $V_{DS} = 5V$, and the gate source voltage is scanned from $0V$ to $3V$.

V_{GS} [V]	I_D [mA]	V_{DS} [V]
0	0	5,017
1,0339	0	5,016
1,5873	0	5,017
2,057	0,07805	5,072
2,106	0,14371	5,035
2,205	0,452	5,013
2,302	1,2537	5,003
2,403	3,1466	4,995
2,521	7,901	5,009
2,601	13,762	5,008
2,705	25,298	4,973
2,808	41,47	4,996
2,912	62,12	5,0009

The gate source voltage is kept constant at $V_{GS} = 2V$, and the gate source voltage is scanned from $0V$ to $4V$.

V_{GS} [V]	V_{DS} [V]	I_D [mA]
2,017	0,0047	0,00000
2,017	0,5058	0,04394
2,017	1,0096	0,04416
2,017	1,5051	0,04395
2,017	2,0191	0,04428
2,017	2,5096	0,04473
2,017	3,0052	0,04483
2,017	3,5025	0,04513
2,017	4,0350	0,04579

The gate source voltage is kept constant at $V_{GS} = 2.2V$, and the gate source voltage is scanned from $0V$ to $4V$.

V_{GS} [V]	V_{DS} [V]	I_D [μA]
2,209	0,0008	7,8
2,209	0,5082	415,4
2,209	1,0099	428,8
2,209	1,5069	435,2
2,209	2,0134	440,6
2,209	2,5039	445,9
2,209	3,0012	448,6
2,209	3,5150	454,0
2,209	4,0170	460,5

The gate source voltage is kept constant at $V_{GS} = 2.4V$, and the gate source voltage is scanned from $0V$ to $4V$.

V_{GS} [V]	V_{DS} [V]	I_D [mA]
2,401	0,0000	0,000
2,401	0,5076	2,812
2,401	1,0211	2,762
2,401	1,5027	2,806
2,401	2,0040	2,854
2,401	2,5034	2,894
2,401	3,0888	2,940
2,401	3,5034	2,974
2,401	4,0060	3,012

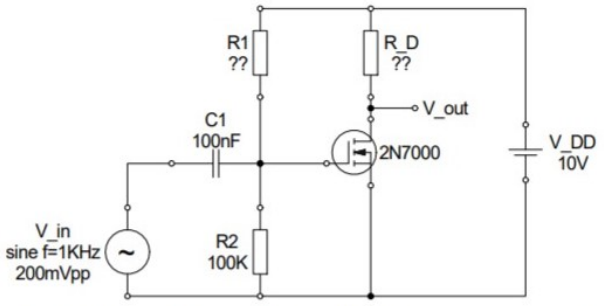
The gate source voltage is kept constant at $V_{GS} = 2.6V$, and the gate source voltage is scanned from $0V$ to $4V$.

V_{GS} [V]	V_{DS} [V]	I_D [mA]
2,602	0,0000	0,000
2,602	0,5020	10,877
2,602	1,0004	11,386
2,602	1,5069	11,801
2,602	2,0222	11,994
2,602	2,5024	12,236
2,602	3,0212	12,574
2,602	3,5124	12,799
2,602	4,0490	13,161

2.2 Problem 2 : MOSFET as Amplifiers

2.2.1 Part 1: Setup

The following circuit was implemented on the breadboard.



$V_{GS} = 2.7\,\mathrm{V}$, $V_{DS} = 5\,\mathrm{V}$, $k = 72.2\,\mathrm{mA/V^2}$, U_{th} = use measured value!

2.2.2 Part 2: Execution and results

The values for R_1 and R_D were determined as:

$$R_1 = 270k\Omega \qquad R_D = 191\Omega$$

calculation?

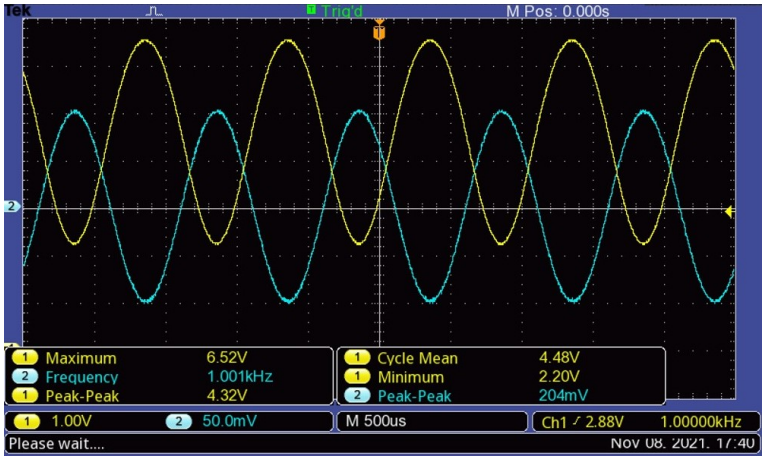
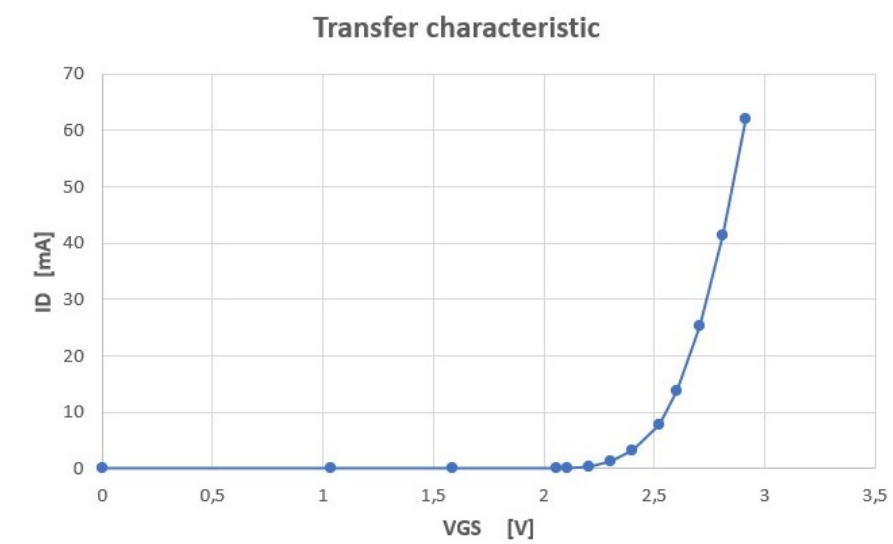


Figure 2: input and output signals + phase relation

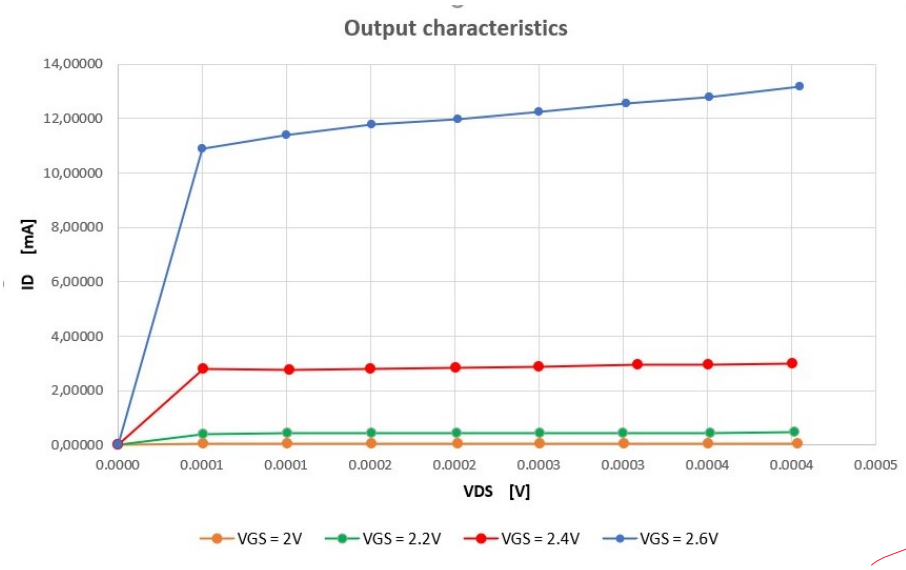
3 Evaluation

3.1 Problem 1 : I/V Characteristic of a MOSFET

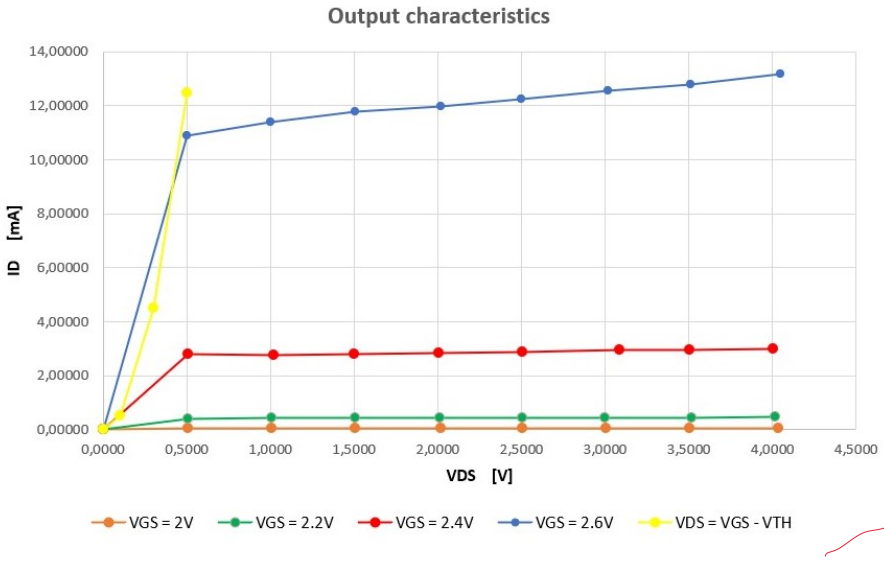
3.1.1 Question 1



3.1.2 Question 2



3.1.3 Question 3



3.2 Problem 2 : MOSFET as Amplifiers

3.2.1 Question 1

V_{out} is dependent on the current flowing through R_D. Since in the saturation mode the output depends only on the gate source voltage, then the MOSFET is operating in the saturation mode during the amplification.

3.2.2 Question 2

The maximum input voltage can be determined by obtaining the maximum drain source voltage. For every voltage magnitude bigger than $V_{DS} = V_{DD} = 10V$, the MOSFET will operate in cutoff mode - no current is flowing through the drain resistance -. For an input voltage of $0.2V$, the drain source voltage is $5V$. It is safe to assume that the maximum input voltage would be $0.4V$.

3.2.3 Question 3

Theoretical voltage gain of the circuit:

$$A = \frac{V_{out}}{V_{in}} = \frac{V_{DD} - I_D \times R_D}{V_{pp}} = \frac{V_{DD} - k(V_{GS} - V_{th})^2 \times R_D}{V_{pp}}$$

$$= \frac{10 - 0.0722(2.7 - 2.1)^2 \times 190}{0.2} = 25.31$$

3.2.4 Question 4

Experimental voltage gain of the circuit:

$$A = \frac{V_{out}}{V_{in}} = \frac{4.32}{0.204} = 21.18$$

The experimental voltage gain is smaller than the theoretical one. This could be due to the tolerance of the components used to implement the circuit as well as the precision of the measurement device.

3.2.5 Question 5

The phase shift between the input and output is $180°$. This is a consequence of the inverse proportionality between the output voltage and the gate source voltage. As the gate source voltage increases the current going through the drain resistance increases and the voltage drop over the resistor increases which decreases the output voltage, so when the input is at its highest peak value the output is at its lowest.

4 Conclusion

The objective of experiment was to familiarize with the basic characteristics and applications of Field Effect Transistors (MOSFETs). The lab included an investigation of the I-V characteristics and the implementation of MOSFETs as amplifiers and switches.

In the first part of the experiment, the I/V characteristics of the MOSFET were investigated. The V_{th} and drain current were determined. Then the drain source to gate source voltage relationship was displayed in graphs using the experimental results.

In the second part of the experiment, the MOSFET was implemented as an amplifier. The gain and the input/output voltage phase relationship was determined experimentally.

The experimental results were slightly different from the theory. That may be due to the tolerance of the components and the precision of the measurement devices.

5 References

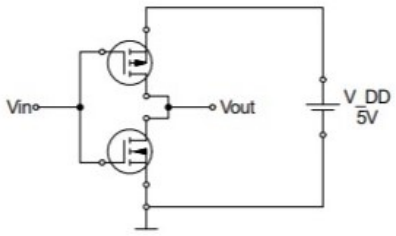
- Electronics Lab Manual (Uwe Pagel)
- http://www.faculty.jacobs-university.de/upagel/

6 Appendix

6.1 Prelab CMOS Inverters and Logic Gates

6.1.1 Problem 1 : Voltage Transfer Characteristic of a CMOS inverter

The following circuit was simulated using LTSpice.



Question 1

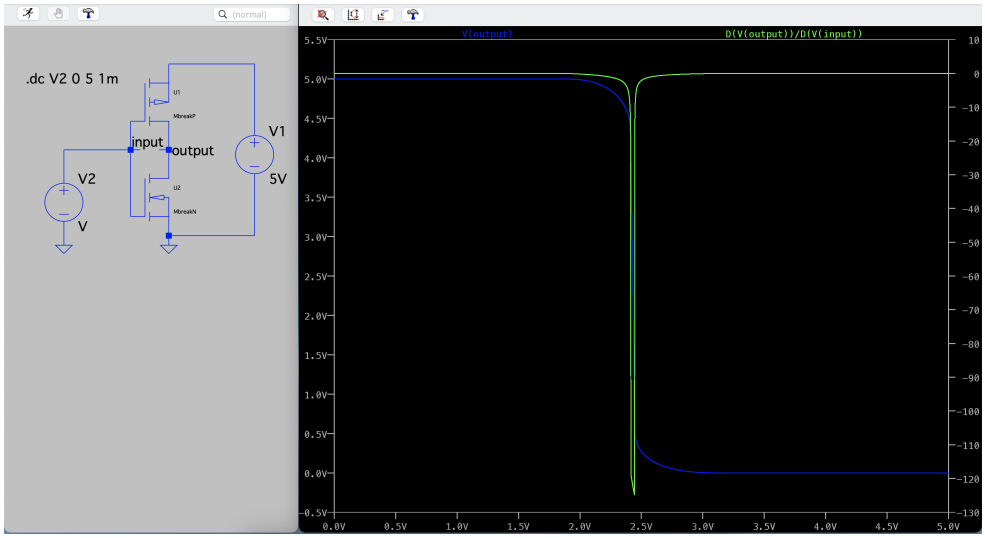


Figure 3: Voltage transfer curve (VTC) of the CMOS inverter

V_{OH}, V_{OL}, V_{IH}, V_{IL}, NM_L, NM_H, and V_{th} were determined using the cursors. The results were collected in the following table:

V_{OH}	4.8713117V
V_{OL}	159.32721mV
V_{IH}	2.58V
V_{IL}	2.235V
NM_L	128.68834mV
NM_H	159.32719mV
V_{th}	2.4299065V

Question 2

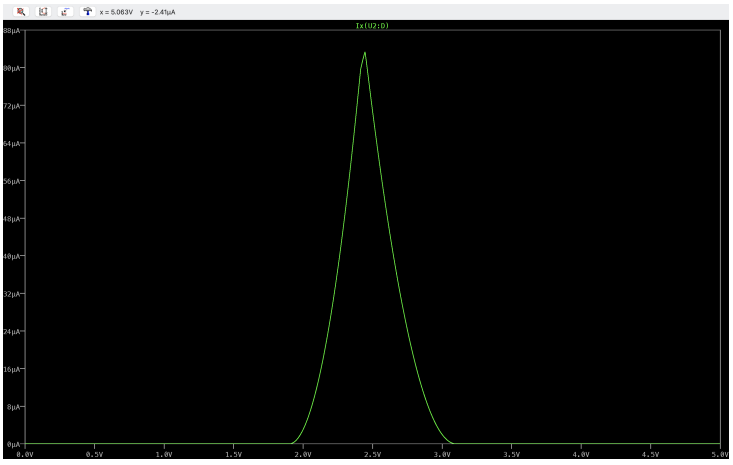


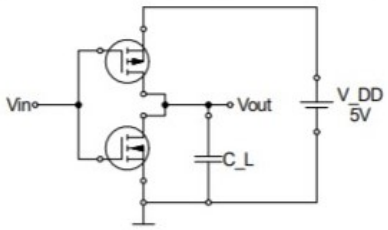
Figure 4: Current flowing through the inverter

Question 3

The peak current was determined from the simulation in the previous question as $83.348844\mu A$. When the input and output voltages are equal, both NMOS and PMOS transistors are on so that the current reaches its maximum level.

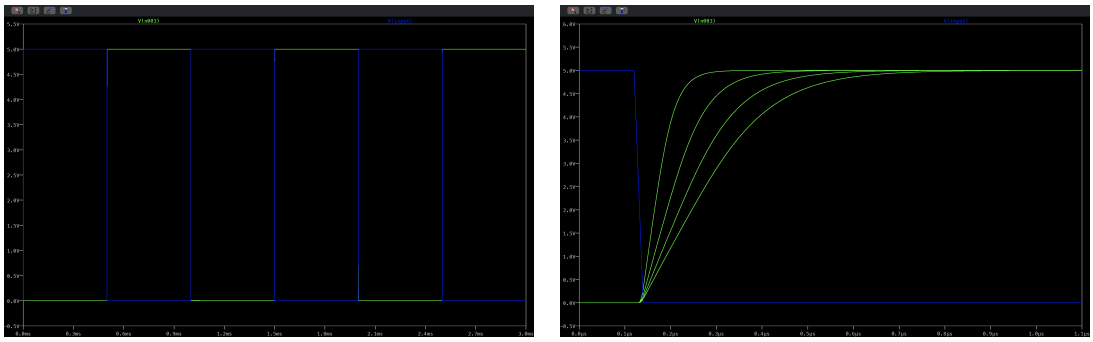
6.1.2 Problem 2 : CMOS Inverter with Capacitive Load

The following circuit was simulated using LTSpice.



Question 1

The capacitive load was varied from $25pF$ to $100pF$ in $25pF$ steps. The input signal was set to a 1 KHz square wave with a $20ns$ rise and fall time and $5V$ the power supply V_{DD}.



(a) Initial graph (b) Zoomed graph

Figure 5: Input and output voltages

The propagation delays were determined using the cursors.
The results were collected in the following table:

Capacitance	$t_{PLH} = t_{PHL}$
25pF	42.563242ns
50pF	76.959085ns
75pF	111.28402ns
100pF	145.3822ns

It can be observed from the table above that, the time delay increases as the capacitance increases.

Question 2

The dynamic power dissipation can be determined as follows:

$$P_D = f \times C \times V_{DD}^2 = 1000 \times 25 \times 10^{-12} \times 5^2 = 0.625\mu W$$

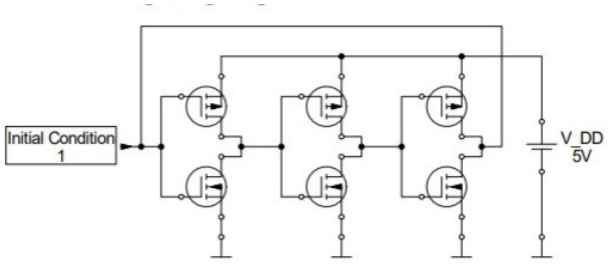
$$P_D = f \times C \times V_{DD}^2 = 1000 \times 50 \times 10^{-12} \times 5^2 = 1.250\mu W$$

$$P_D = f \times C \times V_{DD}^2 = 1000 \times 75 \times 10^{-12} \times 5^2 = 1.875\mu W$$

$$P_D = f \times C \times V_{DD}^2 = 1000 \times 100 \times 10^{-12} \times 5^2 = 2.50\mu W$$

6.1.3 Problem 3 : Propagation Delay of an Inverter Stage

The following circuit was simulated using LTSpice.



Question 1

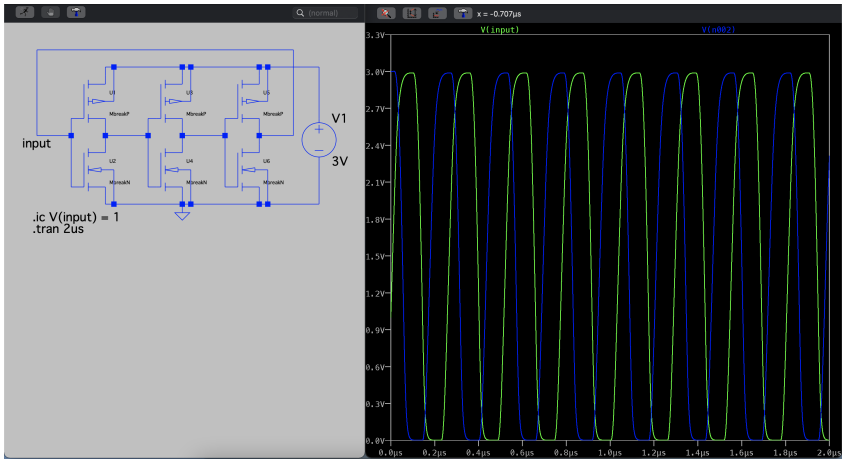


Figure 6: Input and output voltage of the first inverter

Supply voltage	Frequency
3V	3.880MHz
5V	23.688MHz
7V	55.092MHz
9V	122.134MHz

The delay of each individual inverter stage can be determined,

$$t_d = \frac{1}{2 \times N \times f}$$

where f is our obtained frequency and N is the number of inverter stages.

$$t_d = \frac{1}{2 \times 3 \times 3.880 \times 10^6} = 42.955ns$$

$$t_d = \frac{1}{2 \times 3 \times 23.688 \times 10^6} = 7.036ns$$

$$t_d = \frac{1}{2 \times 3 \times 55.092 \times 10^6} = 3.025ns$$

$$t_d = \frac{1}{2 \times 3 \times 122.134 \times 10^6} = 1.365ns$$

Question 2

$$P_D = f \times C \times V_{DD}^2 = 3.880 \times 10^6 \times 5 \times 10^{-12} \times 9 = 0.1746mW$$

$$P_D = f \times C \times V_{DD}^2 = 23.688 \times 10^6 \times 5 \times 10^{-12} \times 25 = 2.961mW$$

$$P_D = f \times C \times V_{DD}^2 = 55.092 \times 10^6 \times 5 \times 10^{-12} \times 49 = 13.50mW$$

$$P_D = f \times C \times V_{DD}^2 = 122.134 \times 10^6 \times 5 \times 10^{-12} \times 100 = 61.067mW$$

Question 3

A $50pF$ capacitor was added to each inverter.$f = 1.416MHz$ is recorded using the cursors.

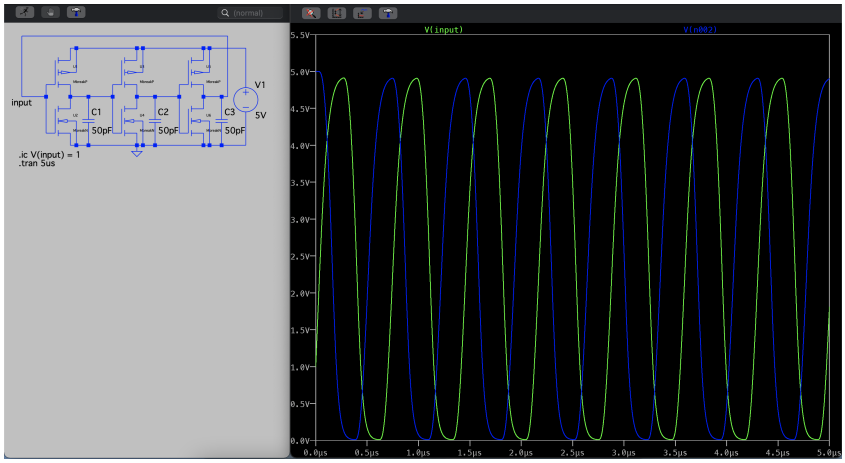


Figure 7: Input and output voltages

The delay of an individual inverter stage can be determined as:

$$t_d = \frac{1}{2 \times N \times f} = \frac{1}{2 \times 3 \times 1.416 \times 10^6} = 117.702ns$$

where f is our obtained frequency and N is the number of inverter stages. The dynamic power dissipation can be found as follows:

$$P_D = f \times C \times V_{DD}^2 = 1.416 \times 10^6 \times 50 \times 10^{-12} \times 5^2 = 1.77mW$$

Question 4

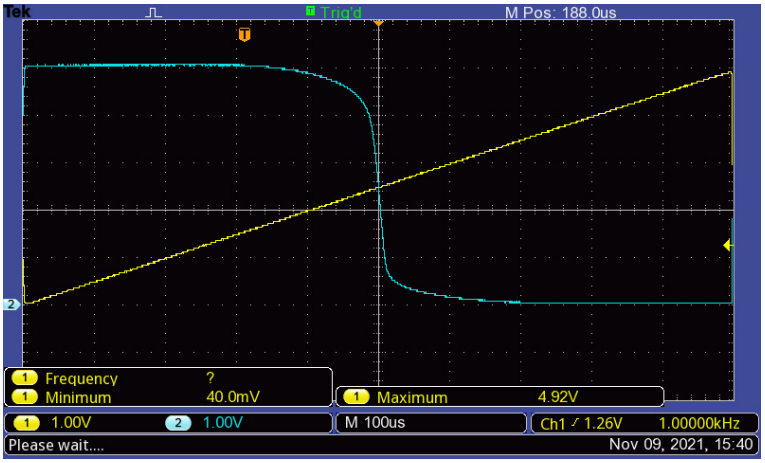
The presence of the capacitor increases the delay and decreases the frequency.

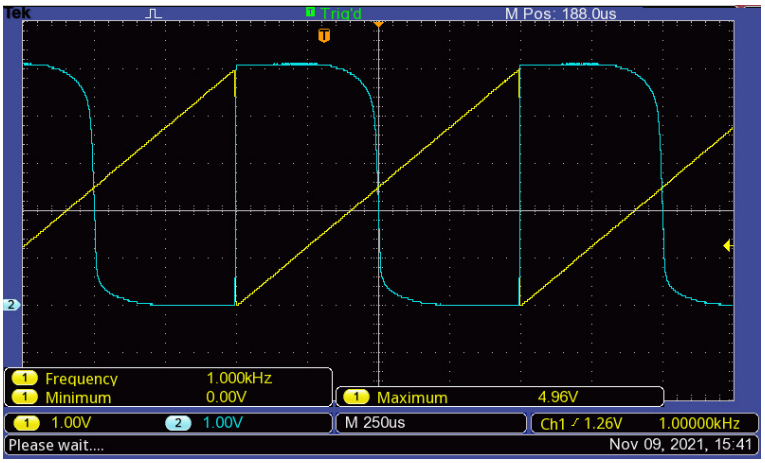
Question 5

Since the power dissipation is proportional to the frequency and the capacitor decreases the frequency the power dissipation decreases. The power supply is also proportional to the power dissipation, increase in supply power increases dissipation. By using the load capacitor power dissipation is lowered without changing the voltage supply

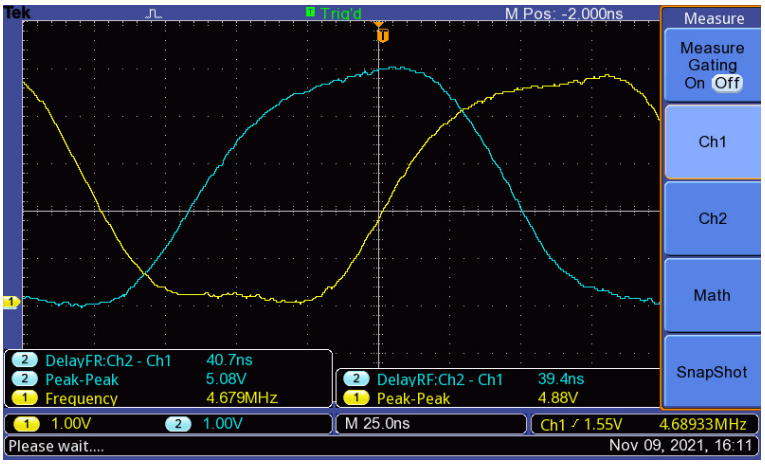
6.2 Experiment Data

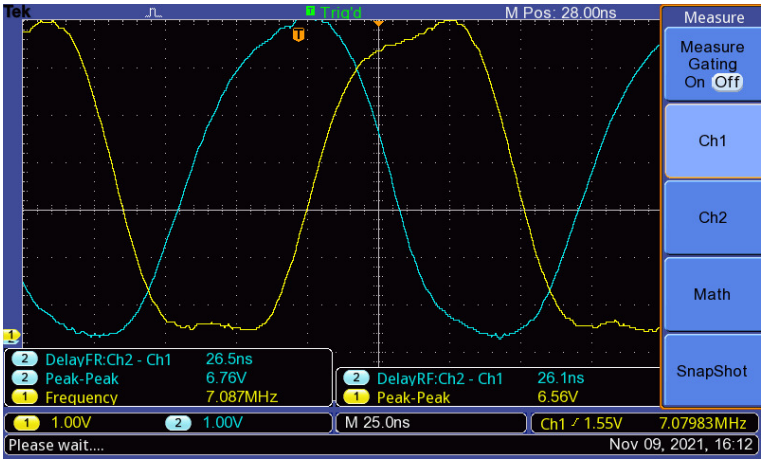
6.2.1 Problem 1 : Voltage transfer characteristic of an Inverter

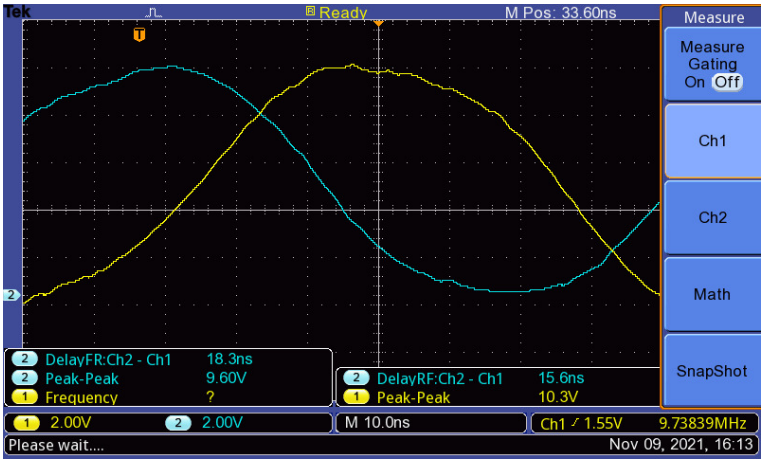


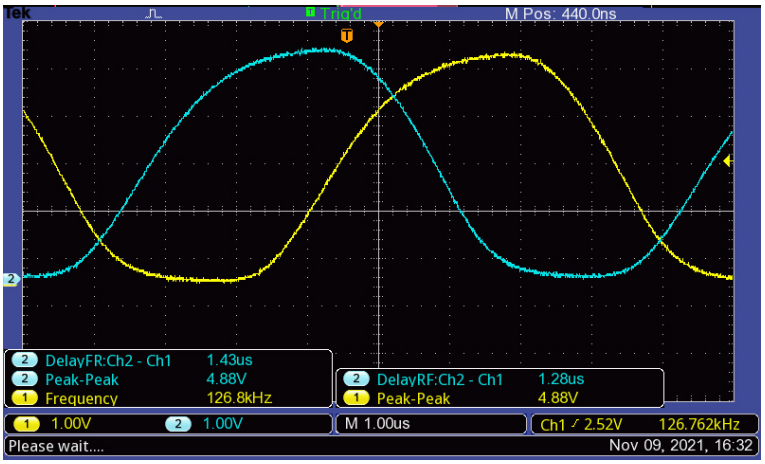


6.2.2 Problem 2 : Propagation Delay of an Inverter






Tek
Ready
M Pos: 33.60ns
Measure
Measure Gating On Off
Ch1
Ch2
Math
SnapShot
2 DelayFR:Ch2 - Ch1 18.3ns
2 Peak-Peak 9.60V
1 Frequency ?
2 DelayRF:Ch2 - Ch1 15.6ns
1 Peak-Peak 10.3V
1 2.00V 2 2.00V
M 10.0ns
Ch1 ⟋ 1.55V 9.73839MHz
Please wait....
Nov 09, 2021, 16:13


Tek
Trig'd
M Pos: 440.0ns
2 DelayFR:Ch2 - Ch1 1.43us
2 Peak-Peak 4.88V
1 Frequency 126.8kHz
2 DelayRF:Ch2 - Ch1 1.28us
1 Peak-Peak 4.88V
1 1.00V 2 1.00V
M 1.00us
Ch1 ⟋ 2.52V 126.762kHz
Please wait....
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