Jacobs University Bremen

Natural Science Laboratory
Electrical Engineering Module II

Fall Semester 2021

Lab 3 – Bipolar Junction Transistor

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Place of execution : Teaching Lab EE
Date of execution : November 1, 2021

Objective:

The main objective of the experiment is to study the properties of Bipolar junction transistors and its use in modern day electronic designs. Initially, the bipolar transistor itself was studied and the type of transistor was identified and also the emitter, base and collector junction pins were verified. Similarly, the biasing and operation active mode of the BJT was analyzed and the bias circuit was constructed. The voltage across different critical nodes and bias points were measured using multimeter and it was compared with the theoretical value from the simulation. Moreover, BJT circuit in its active mode of operation was used for amplification of small signal model for varying range of frequencies and input amplitude. Furthermore, the bandwidth of BJT amplifier circuit was measured using the oscilloscope and signal generator (in SWEEP mode).

Prelab: Bipolar Junction Transistor

Problem 1: Biasing of Bipolar Junction Transistors

Analyze the following common emitter circuit:

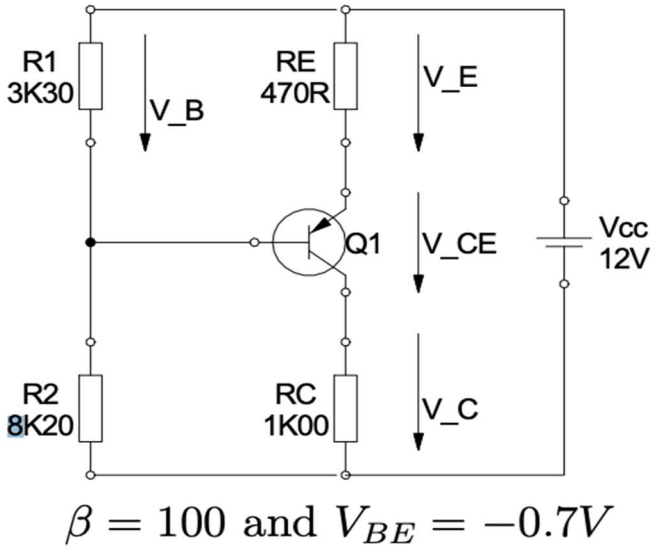


Figure 1: Common Emitter Circuit

1) (a) Calculate $V_B, V_E, V_{CE}, and\ V_C$.
   (b) Calculate $I_B, I_E\ and\ I_C$.

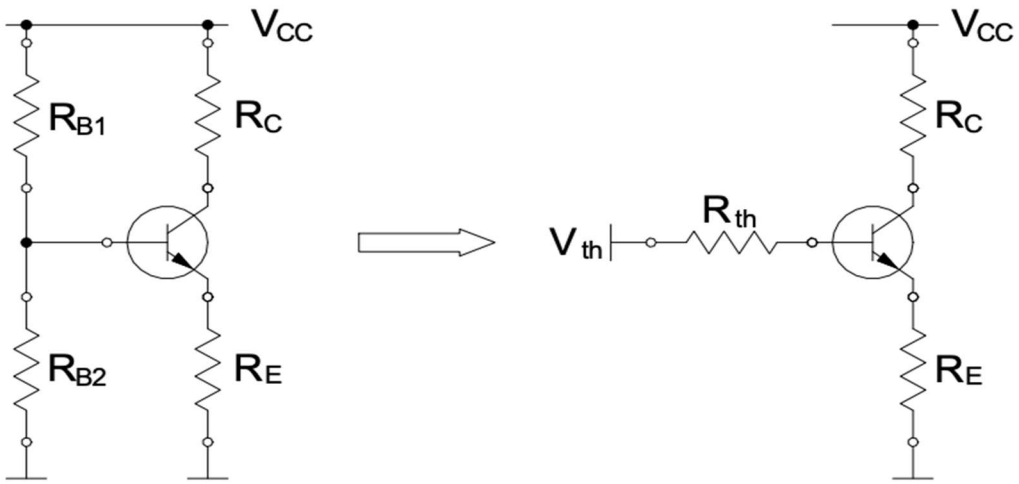


Figure 2: Thevenin Circuit

$V_B = V_{th} = \frac{R2}{R1+R2} \cdot V_{CC} = \frac{8200\Omega}{3300\Omega+8200} \cdot 12V = 8.557\ V$

$R_{th} = \frac{R1 \cdot R2}{R1+R2} = 2353\ \Omega$

Using KVL:

$12 - I_E R_E - V_{EB} - I_B R_{th} - V_{th} = 0$

Also, assuming BJT is operating in the active mode:

$I_c = \beta I_B = 100 I_B$ and

$I_E = (\beta + 1) I_B = 101 \cdot I_B$

So now,

$12 - 47470 \cdot I_B - 0.7 - 2353 \cdot I_B - 8.557 = 0$

$I_B = 55.05\ \mu A$

Now, $I_c = 100 I_B = 5.505\ mA$ and $I_E = 101 \cdot I_B = 5.561\ mA$

Similarly,

$V_E = I_E R_E = 5.561 \cdot 10^{-3} \cdot 470 = 2.614\ V$

$V_C = I_C R_C = 5.505 \cdot 10^{-3} \cdot 1000 = 5.505\ V$

Now, using KVL again,

$12 - V_E - V_{EC} - V_C = 0$

$V_{CE} = -2.614 + 12 - 5.505 = 3.881\ V$

Thus, the results can be tabulated as:

Quantity	Value
V_B	8.557 V
V_E	2.614 V
V_{CE}	3.881 V
V_C	5.505 V
I_B	55.05 µA

I_E	5.561 mA
I_C	5.505 mA

2) Use the same circuit. Calculate the necessary biasing resistors (R_1, R_2, R_C and R_E) under the assumption that $V_{CEQ} = 8V$ and $I_{CQ} = 8mA$. The transistor operates in the active mode. Other parameters: $V_{CC} = 20V,\ \beta = 150, V_E = 4V\ , R_{th} = 0.1\beta R_E$.

Using KVL,

$V_E + V_{CE} + V_C = V_{CC}$

$V_C = 20 - 8 - 4 = 8\ V$

$R_C = \frac{V_C}{I_{CQ}} = \frac{8}{0.008} = 1000\ \Omega$

If the transistor is operating in the active mode:

$I_B = \frac{I_c}{\beta} = \frac{8mA}{150} = 53.33\ \mu A$

$I_E = (\beta + 1) \cdot I_B = 8.053\ mA$

$R_E = \frac{V_E}{I_E} = \frac{4V}{8.053mA} = 496.71\ \Omega$

Given, $R_{th} = 0.1\beta R_E = 0.1 * 150 * 496.71 = 7450.64\ \Omega$

Using KVL again,

$20 - V_E - V_{EB} - I_B R_{th} - V_{th} = 0$

$V_{th} = 20 - 4 - 0.7 - 53.33 \cdot 10^{-6} \cdot 7450.6$

$V_{th} = 14.903\ V$

Also,

$V_{th} = \frac{R2}{R1+R2} \cdot 20\ V$

$\frac{R2}{R1+R2} = 0.7451$ (I)

and

$R_{th} = \frac{R1 \cdot R2}{R1+R2}$

$\frac{R1 \cdot R2}{R1+R2} = 7450.64$ (II)

Dividing equation (I) by (II):

$$R_1 = 9999.5\ \Omega \approx 10\ k\Omega$$

$$R_2 = 29229.7\ \Omega \approx 29.2\ k\Omega$$

The values can be tabulated as:

Biasing Resistor	Value
R_1	$10\ k\Omega$
R_2	$29.2\ k\Omega$
R_C	$1000\ \Omega$
R_E	$496.7\ \Omega$

Problem 2: Constant Current Source

1) Given is following constant current circuit:

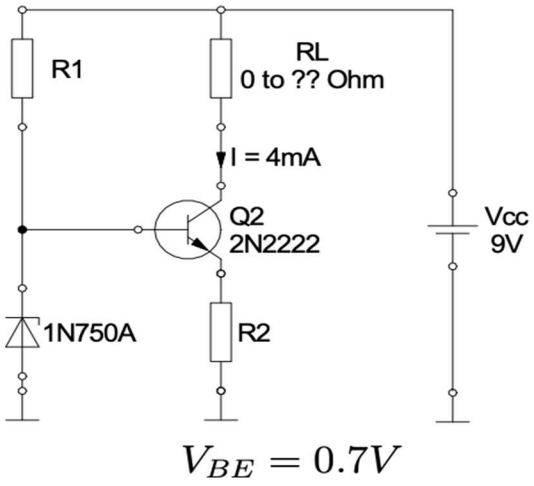


Figure 3: Constant Current Circuit

2) Find the values for R1 and R2 to get a constant current of $I_C \approx 4mA$
From the datasheet $V_Z = 4.7\ V$
$I_E = I_{R2} = \frac{V_Z - V_{BE}}{R_2}$
As the current is operating in the active mode, we can assume:
$I_{R2} = I_E \approx I_C \approx 4mA$

$R_2 = \frac{4.7-0.7}{4*10^{-3}} = 1000\ \Omega$

For the diode a current greater than 5mA could be chosen for biasing,
So, for the diode $I_Z = 10\ mA$

$R_1 = \frac{V_{CC}-V_Z}{10\ mA} = \frac{9-4.7}{10*10^{-3}} = 430\ \Omega$

3) What is the maximum value for R_L to still get $I_C \approx 4mA$?
Approximating $I_E \approx I_C \approx 4mA$
$V_L + V_{R2} = V_{CC} - V_{CE}$
$V_L = 9 - 4 * 10^{-3} \cdot 1000 - 1V = 4\ V$
$R_L = \frac{V_L}{I} = \frac{4\ V}{4mA} = 1000\ \Omega$

4) Implement the circuit in LT Spice and verify your calculations! Use the '.step' command to vary R_L.

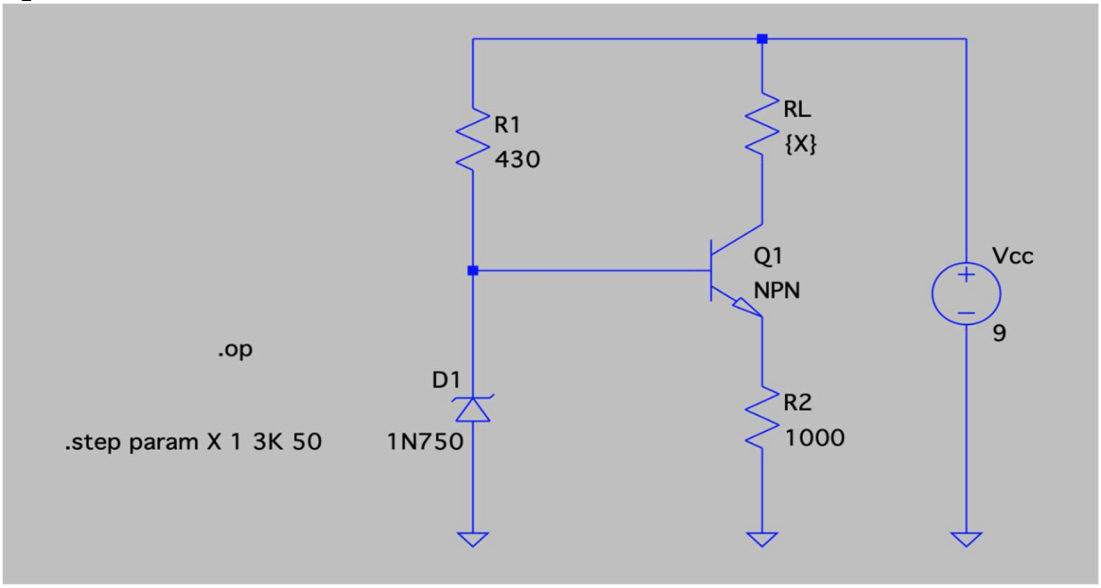


Figure 4: Circuit for variable R_L

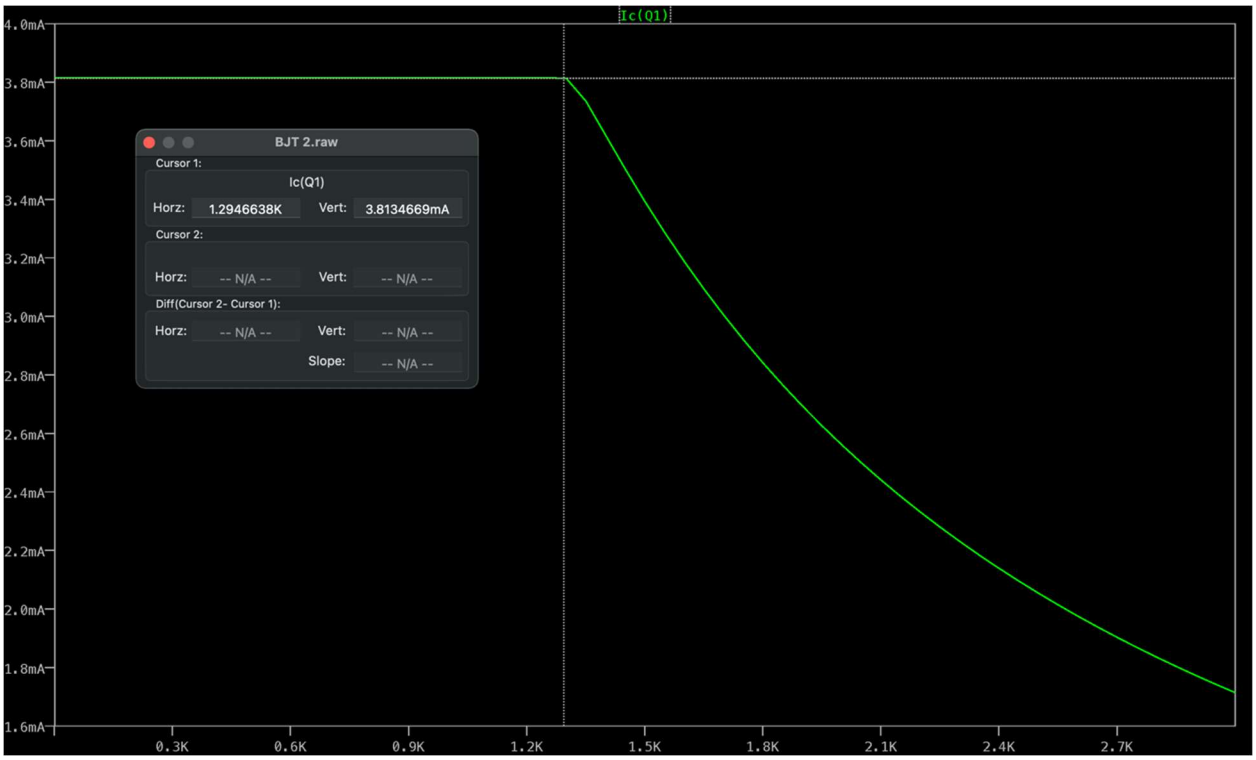


Figure 5: Plot of I_C with varying R_L

From the plot, it can be seen that constant 3.8mA I_C current is flowing until the value of R_L reaches 1295 Ω. So, during our value of 1000Ω resistance current is still constant. This value

(1295Ω) is close to the calculated value and the difference could be due to the different value of V_{CE} used by the LT Spice than in our calculation.

5) Explain the function principle of the circuit!
   In this circuit with the bipolar transistor (BJT), a Zener diode is used as a voltage stabilizer. The constant voltage across the Zener diode is 4.7 V in this case. It also maintains constant voltage across $R1$ and hence the current through it is almost constant. The external floating resistor ($R2$) is connected to the collector and it is varied. It is also assumed that the same magnitude of current flows through the resistor $R2$ and $R3$, i.e., same current through the collector and emitter. The transistor $Q1$ adjusts the output current at the floating resistor. So as to maintain constant voltage drop across the emitter resistor. As a result, the output current across the emitter resistor is almost constant even though the collector resistor varies.

Problem 3: Amplifier Circuit

1) Use LT Spice to implement the following circuit:

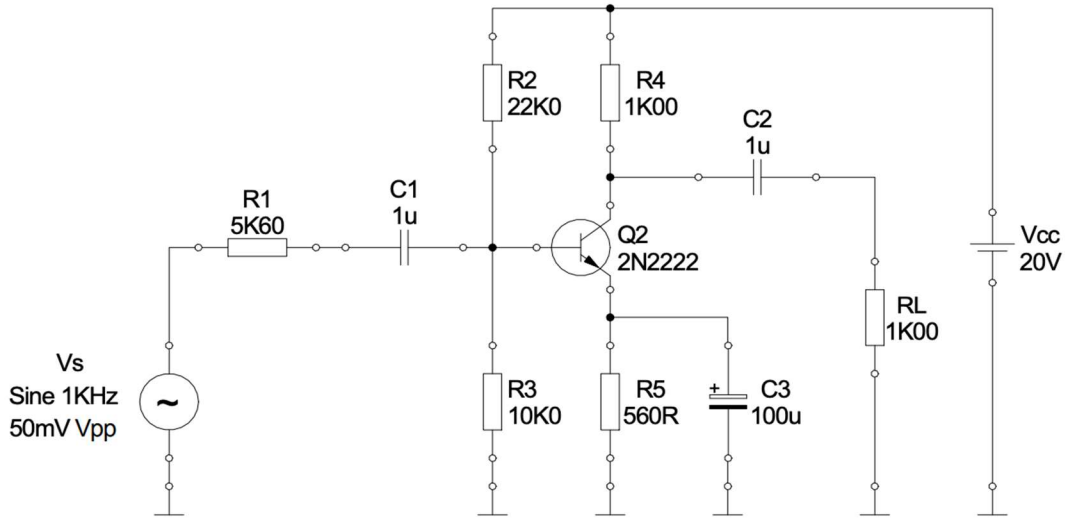


Figure 6: Amplifier Circuit

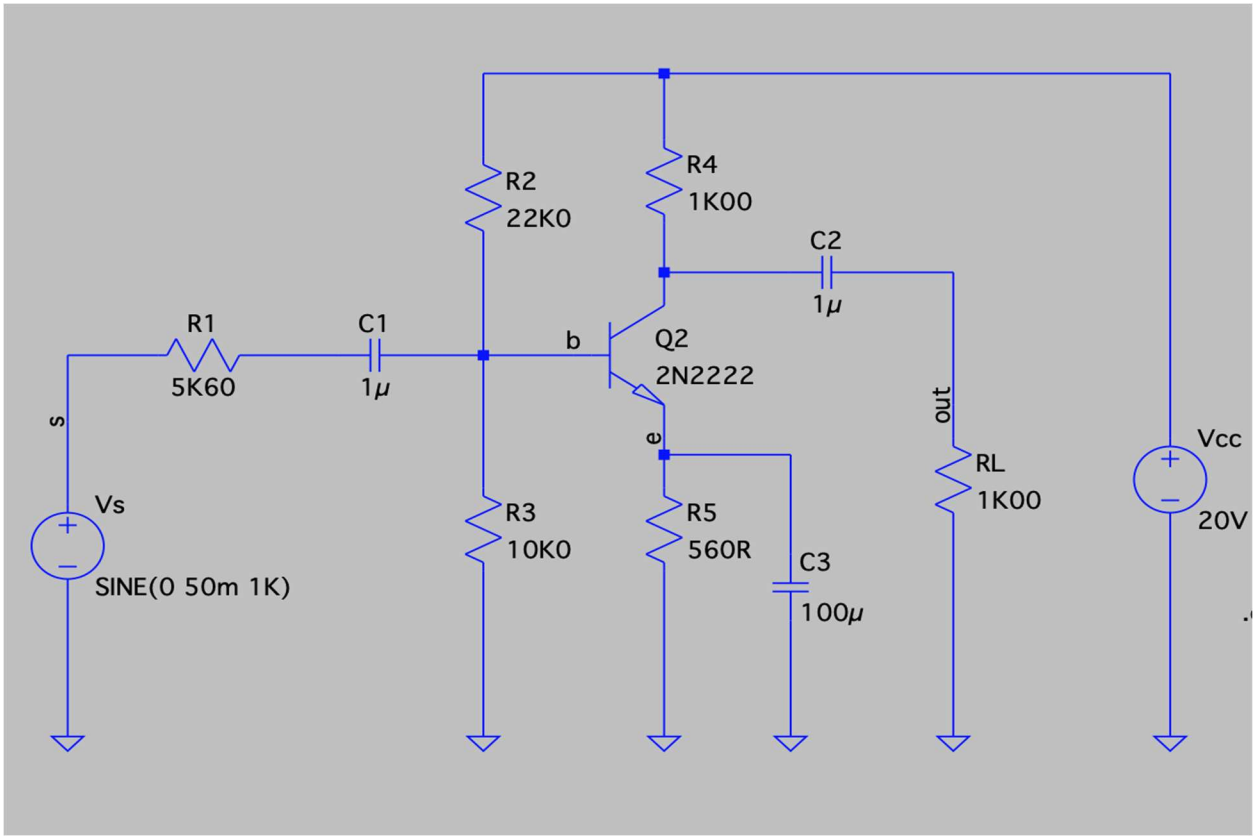
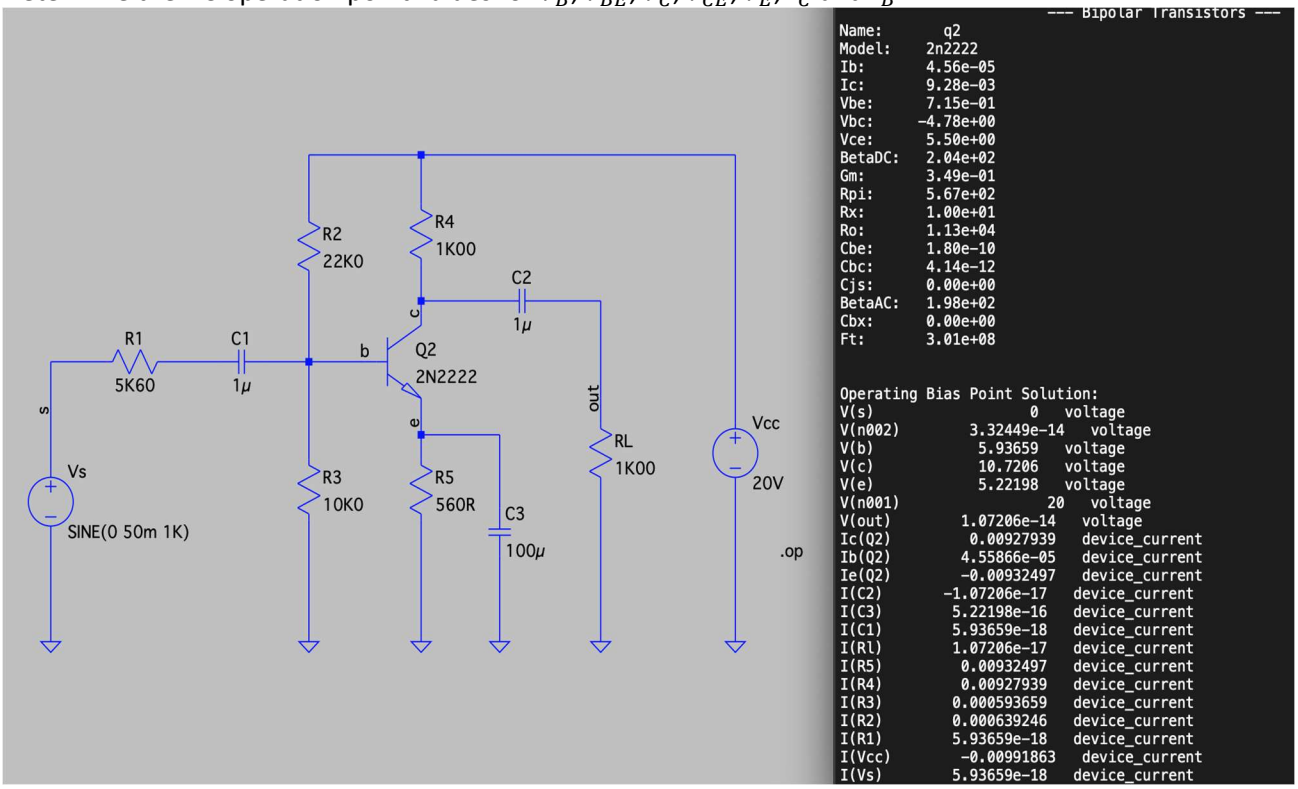


Figure 7: Amplifier Circuit Implemented in LT Spice

2) Determine the DC operation point values for V_B, V_{BE}, V_C, V_{CE}, V_E, I_C and I_B.




```
                                --- Bipolar Transistors ---
Name:       q2
Model:      2n2222
Ib:         4.56e-05
Ic:         9.28e-03
Vbe:        7.15e-01
Vbc:       -4.78e+00
Vce:        5.50e+00
BetaDC:     2.04e+02
Gm:         3.49e-01
Rpi:        5.67e+02
Rx:         1.00e+01
Ro:         1.13e+04
Cbe:        1.80e-10
Cbc:        4.14e-12
Cjs:        0.00e+00
BetaAC:     1.98e+02
Cbx:        0.00e+00
Ft:         3.01e+08


Operating Bias Point Solution:
V(s)                    0   voltage
V(n002)          3.32449e-14   voltage
V(b)              5.93659   voltage
V(c)              10.7206   voltage
V(e)              5.22198   voltage
V(n001)                20   voltage
V(out)           1.07206e-14   voltage
Ic(Q2)            0.00927939   device_current
Ib(Q2)           4.55866e-05   device_current
Ie(Q2)           -0.00932497   device_current
I(C2)           -1.07206e-17   device_current
I(C3)            5.22198e-16   device_current
I(C1)            5.93659e-18   device_current
I(Rl)            1.07206e-17   device_current
I(R5)             0.00932497   device_current
I(R4)             0.00927939   device_current
I(R3)            0.000593659   device_current
I(R2)            0.000639246   device_current
I(R1)            5.93659e-18   device_current
I(Vcc)            -0.00991863   device_current
I(Vs)            5.93659e-18   device_current
```

Figure 8: DC Operational Point Simulation

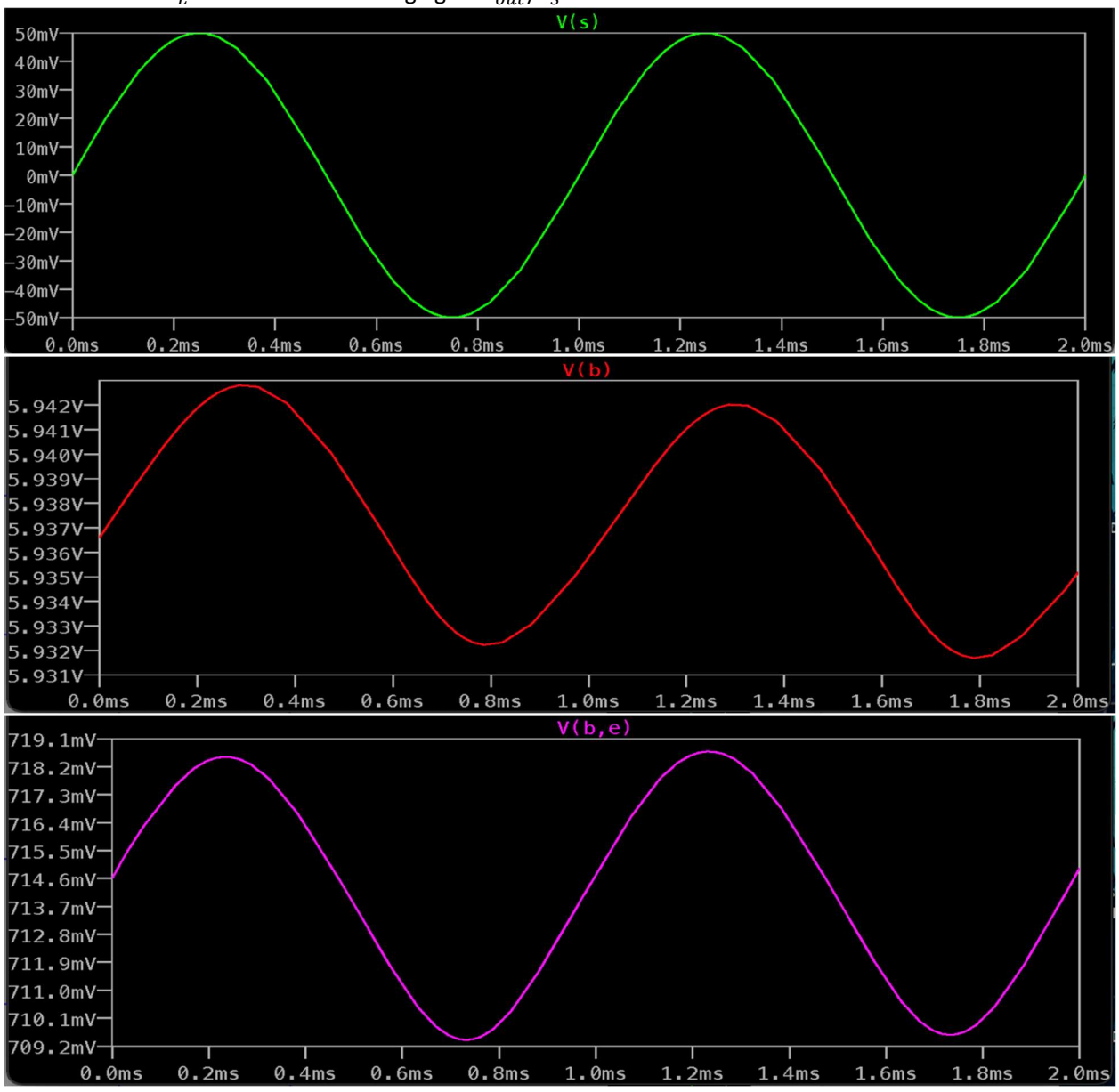
- The values are:

DC operation point Voltages	Voltage [V]
V_{CC}	20
V_B	5.937
V_{BE}	0.715
V_C	10.72
V_{CE}	5.50
V_E	5.222

DC operation point Currents	Current
I_C	9.279 mA

I_B	45.59 µA

3) Perform a transient analysis for about 2 cycles of a sinusoidal input signal.
Use $V_S = 50\ mV_{PP}$ input amplitude and $f = 1\ KHz$. Display V_S, V_B, V_{BE}, and the voltage across the load resistance R_L. Determine the voltage gain V_{out}/V_S.



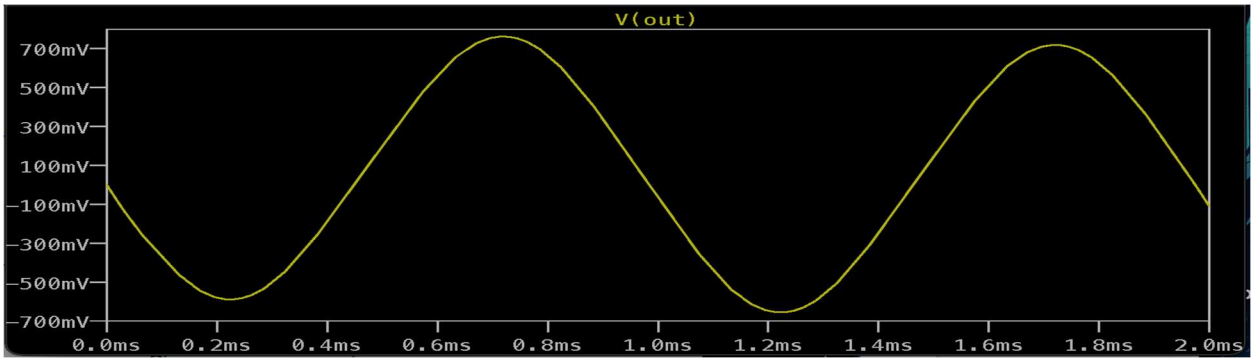


Figure 9: Plot of V_S, V_B, V_{BE} and V_{out}

- Peak Voltage of Output Voltage across the load $V_{out} = 762.68\ mV$
  Peak Voltage of Input Voltage $V_s = 49.98\ mV$
  Gain $G = \frac{V_{out}}{V_s} = \frac{762.68}{49.98} = 15.26$
  Gain in dB: $20 \cdot \log_{10} 15.26 = 23.7\ dB$

4) Determine the quality of the amplified signal at RL. Use the '.step' command to vary Vs by $10\ mV_{PP}, 20\ mV_{PP}, 50\ mV_{PP}, 100\ mV_{PP}$, and $200\ mV_{PP}$. Use a FFT or determine the harmonic distortion to give a statement.

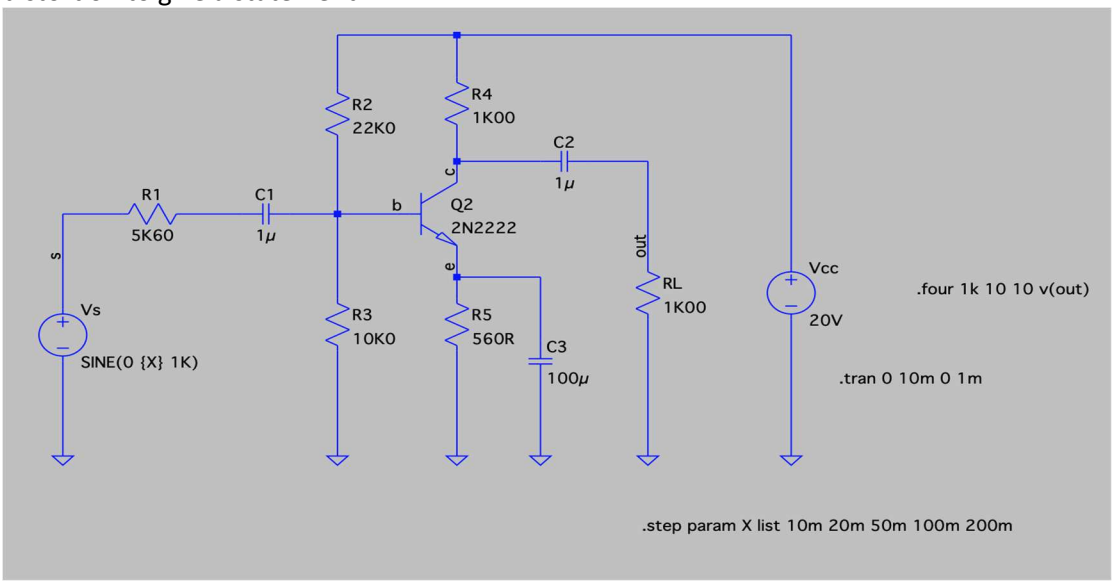


Figure 10: Amplifier Circuit with change in input amplitude

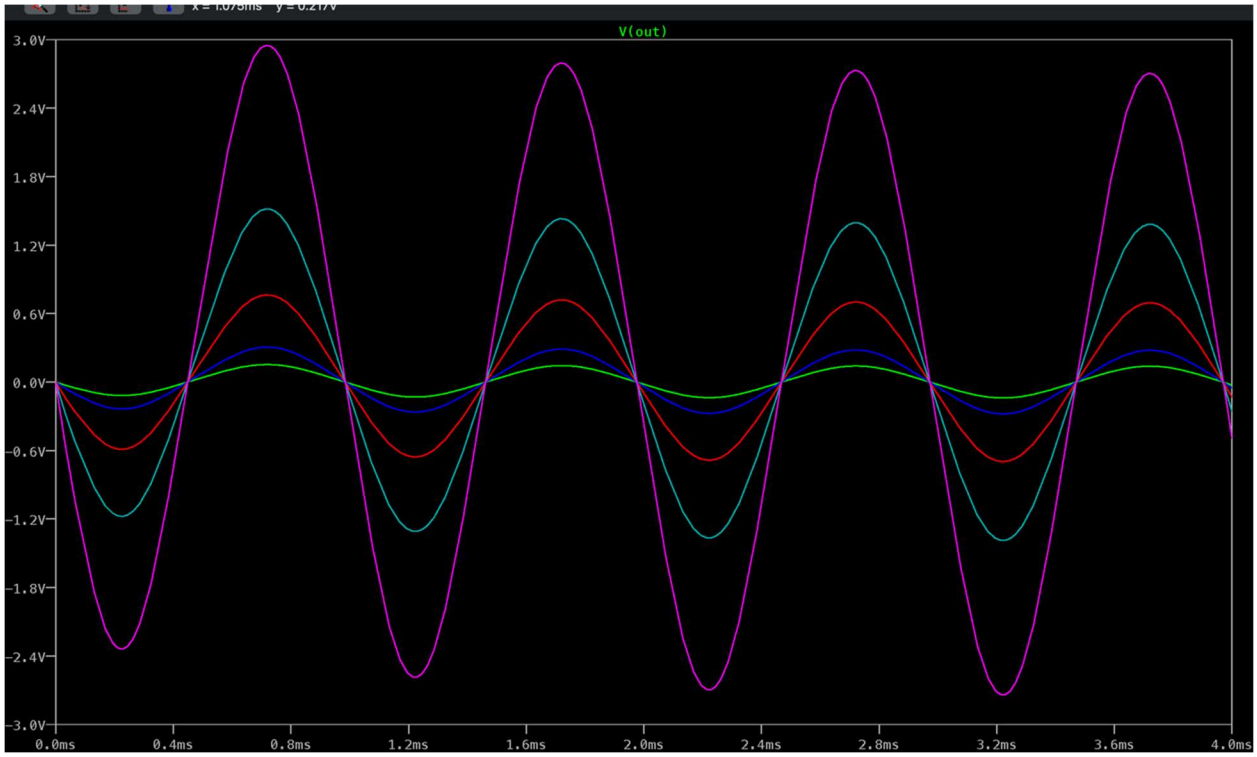


Figure 11: Plot of V_{out} with varying amplitude

- The FFT:

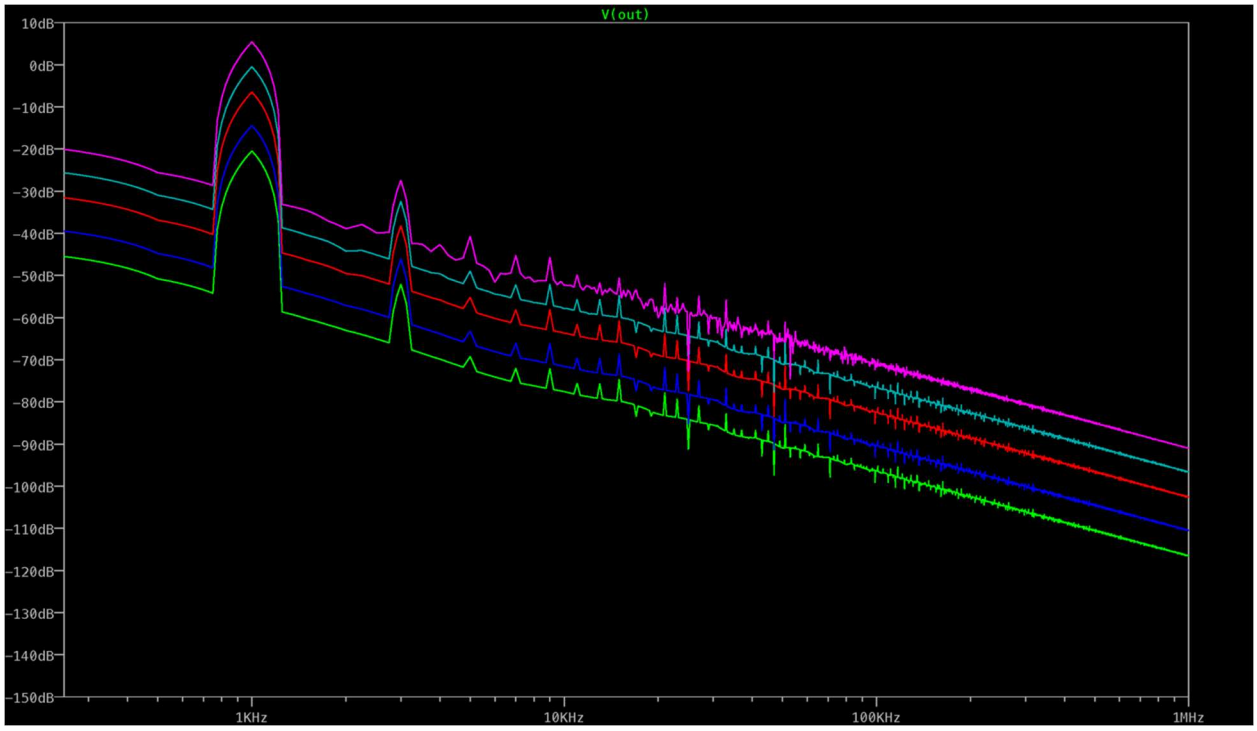


Figure 12: FFT of different V_{out}

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+3	1.358e-1	1.000e+0	-169.53°	0.00°
2	2.000e+3	3.861e-4	2.844e-3	-3.34°	166.19°
3	3.000e+3	3.207e-3	2.362e-2	27.31°	196.84°
4	4.000e+3	1.798e-4	1.325e-3	-10.25°	159.27°
5	5.000e+3	3.042e-4	2.241e-3	28.58°	198.11°
6	6.000e+3	1.098e-4	8.087e-4	-3.77°	165.76°
7	7.000e+3	2.080e-4	1.532e-3	11.32°	180.85°
8	8.000e+3	8.636e-5	6.361e-4	2.68°	172.21°
9	9.000e+3	2.567e-4	1.891e-3	49.46°	218.98°
10	1.000e+4	7.372e-5	5.430e-4	2.91°	172.44°

Total Harmonic Distortion: 2.408681%(6.189334%)

Figure 13: Harmonic Distortion 10 mV_{pp}

- The Harmonic Distortions for different V_s are:

V_s $[mV_{pp}]$	Harmonic Distortions
10	2.408681%
20	2.415563%
50	2.587046%
100	2.825338%
200	2.967771%

It can be seen from the FFT that there are a greater number of peaks than 1 and the magnitude of the peaks are higher with high amplitude. This shows the deviation of the signal from pure sinusoidal signal which only has one peak.

Similarly, the harmonic distortions increased with increase in amplitude. This implies that the quality of the signal is decreasing with the increase in V_{pp} of the input signal.

5) Perform an AC analysis. Keep the amplitude of the input signal constant at $50\ mV$. Vary the frequency from $100Hz$ to $1MHz$ with 10 points per decade and display the voltage across the load resistance R_L.

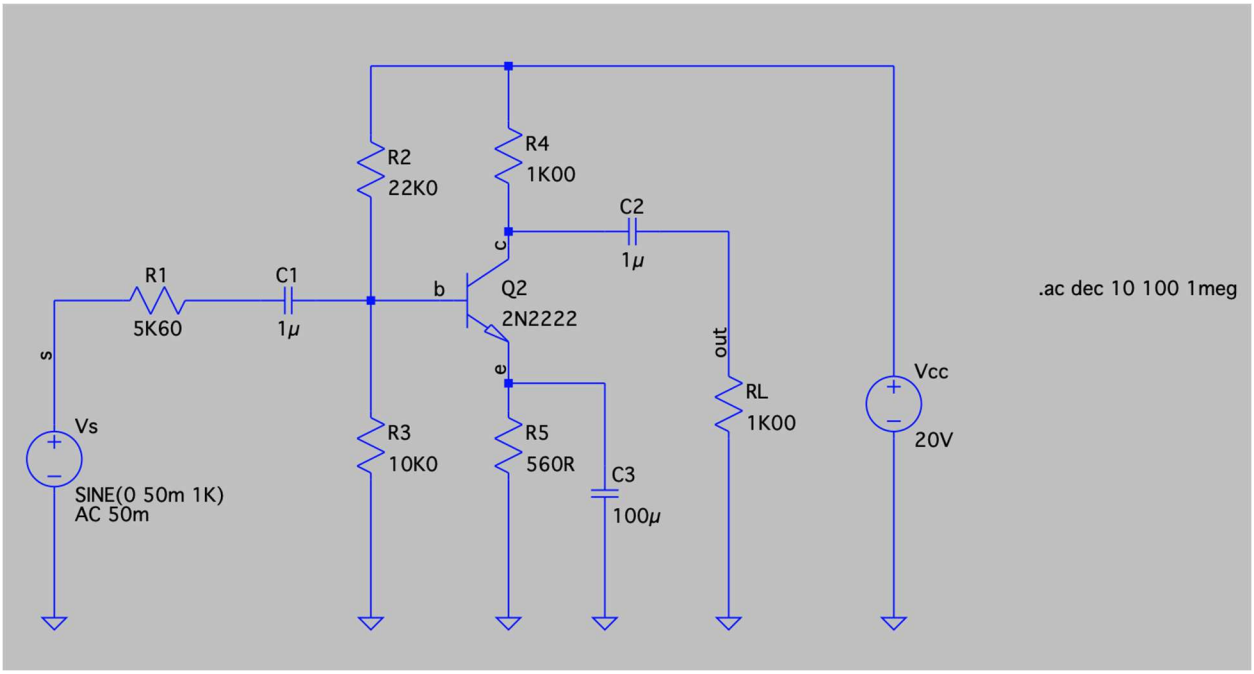


Figure 14: Amplifier Circuit for AC Analysis

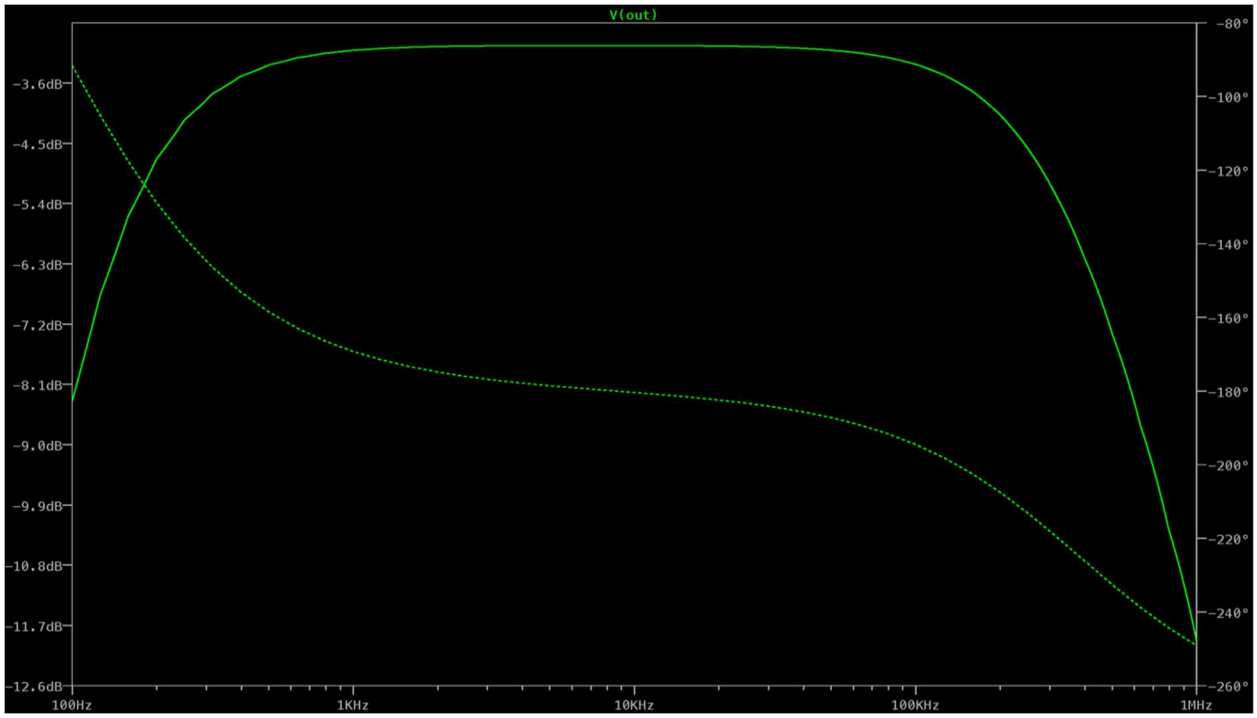


Figure 15: LT Spice Plot for AC Analysis

6) Use the LT Spice '. MEASURE' command to determine the lower and upper −3 dB frequencies and the bandwidth.

```
Direct Newton iteration for .op point succeeded.

tmp: MAX(mag(v(out)))=(-3.03794dB,0°) FROM 100 TO 1e+06
bw=384725 FROM 145.154 TO 384870


Date: Sun Nov  7 18:14:48 2021
Total elapsed time: 0.017 seconds.

tnom = 27
temp = 27
method = trap
totiter = 4
traniter = 0
tranpoints = 0
accept = 0
rejected = 0
matrix size = 12
fillins = 0
solver = Normal
Matrix Compiler1:      36 opcodes
Matrix Compiler2:      74 opcodes
```

Figure 16: Spice Log for AC Analysis

From the spice log:

Lower -3dB frequencies $\left(f_{-3db,L}\right) = 145.154\ Hz$
Upper -3dB frequencies $\left(f_{-3db,U}\right) = 384870\ Hz$
Bandwidth $(BW) = 384725\ Hz$

1 Execution

1.1 Experimental set-up:

Workbench Number 8

- Signal Generator
- Oscilloscope
- BNC Cable
- Resistors (22K0 Ω, 5K60 Ω, 10K0 Ω, 1K00, 560 Ω)
- Capacitors (1 μF, 100 μF)
- BJT (2N2222)
- Tenma Multimeter

1.1.1 Part 1: Determine Type and Pin Assignment of a Bipolar Transistors:

In this experiment the task was to determine the collector, emitter and base of a transistor. Firstly, pin numbers were assigned to the Bipolar transistors and a multimeter was connected across the two terminals. The voltage across the terminals were measured and recorded. Similarly, the terminals of the multimeter were changed and the output across the same terminals were measured again. If we observed the output voltage across both the terminals forward and reversed be .0L then the remaining terminal can be used as base and similar steps are followed to determine emitter and collector. Also, the type of transistor can also be determined using the similar procedure.

Test Circuit:

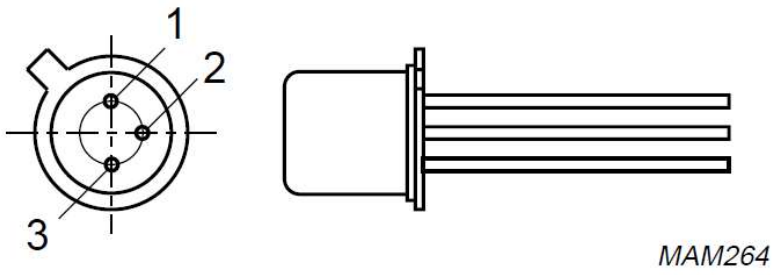


Figure 1: Circuit diagram for determining pins and type of transistor

1.1.2 Part 1-Execution and Results:

- The following table presents the voltage measured across different pins using a multimeter.

Terminal	Ground	Diode Check Value [V]
1	2	.0LL
2	1	0.7460 V
1	3	.0L
3	1	.0L
2	3	0.7412 V
3	2	.0L

Table 1: Measurement of voltage across different pins

- Determining the base terminal
    - As both the terminals (1,3) and (3,1) resulted into .0L diode check value, the remaining pin 2 is the base.

- Determining the type of transistor
    - When the common lead of the multimeter was connected to the base terminal and the positive lead was connected to the remaining pins one after another, the diode check value came out to be .0L. This confirms that it is a 'NPN' Bipolar transistor.

- Determining the Emitter and Collector terminal:
    - When the multimeter was connected to the base terminal so that the diode undergoes forward voltage drop across each of the other pins, the lower voltage drop was measured across the 3-2 terminal junction. So, it was concluded that 3- 2 terminal junction is the base-collector junction. While, a higher voltage drop was measured across 1-2 terminal junction and it was verified that it is the base-emitter junction.

Transistor Type	NPN pin
Base Terminal	2
Emitter Terminal	1
Collector Terminal	3

Table 2: Summary of the transistor type and terminals description

1.1.3 Part 2: Operating Point of BJTs:

- The experiment helps to confirm if the BJT is correctly biased to work in the active mode of operation. In this problem, only the electronic configuration inside the black box was assembled to observe the DC operating points of BJTs. The circuit was assembled as according to the circuit diagram below and the voltage across different points were measured using a TENMA Multimeter
- Test Circuit:

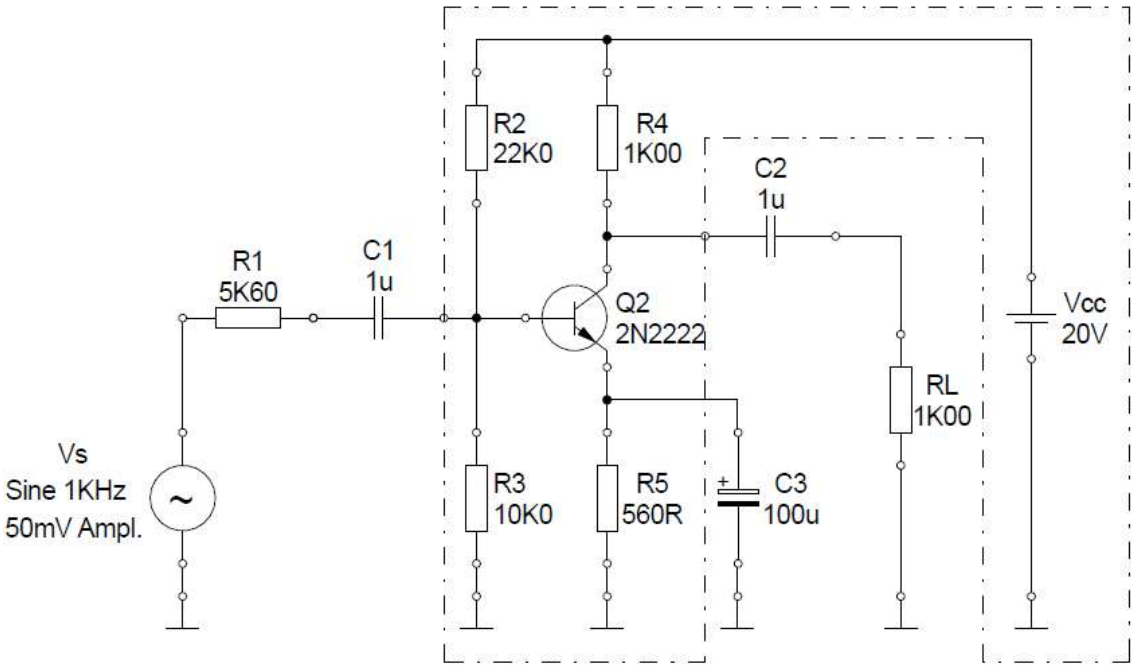


Figure 2: Circuit diagram of BJT

1.1.4 Part 2-Execution and Results:

The measurement of DC Operating points for different nodes were measured using TENMA Multimeter and the results are tabulated below:

Voltage across different points	Voltage from Multimeter [V]
V_{CC} [V]	20.056
V_B [V]	5.958
V_{BE} [V]	0.6515
V_C [V]	10.611
V_{CE} [V]	5.293
V_E [V]	5.32

Table 3: Measurement values for operating points on BJT

1.1.5 Part 3-Common Emitter Circuit:

This experiment demonstrates the amplification of small signal by BJT when the bipolar transistor is correctly biased to work in the active mode of operation. This problem is similar to the previous problem but the remaining part of the circuit is assembled here. The output voltage was observed using an Oscilloscope and is presented below:

Test Circuit:

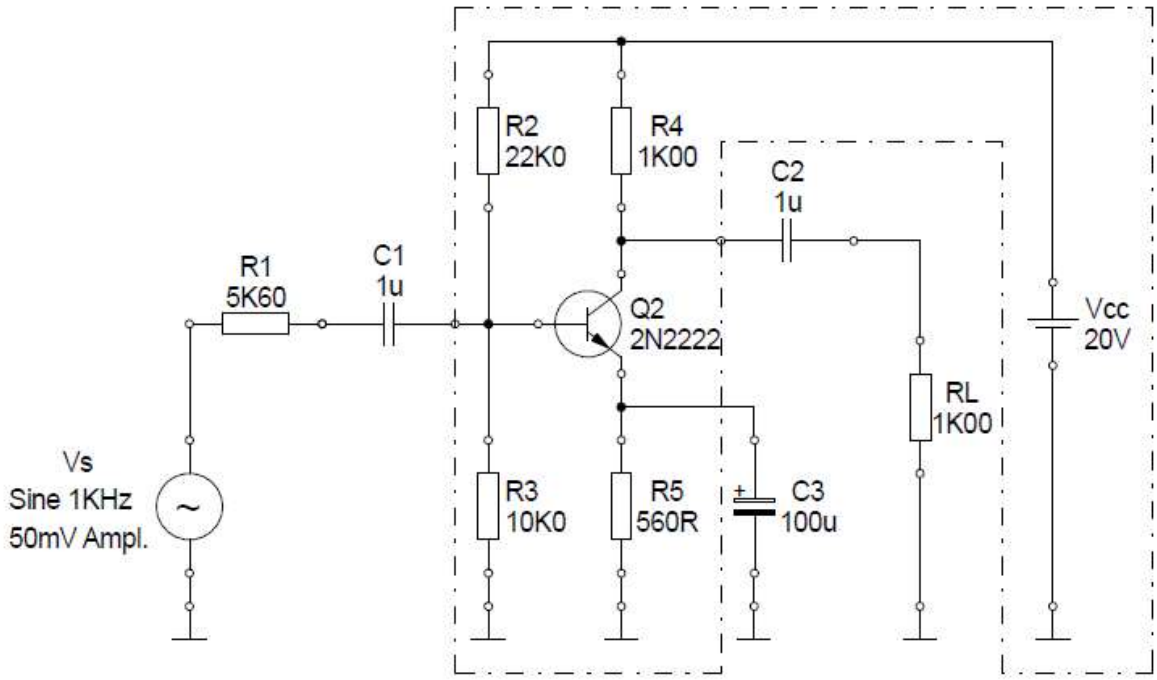


Figure 3: Circuit diagram for common emitter

- Experimental findings
  For Vs = 50 mVpp

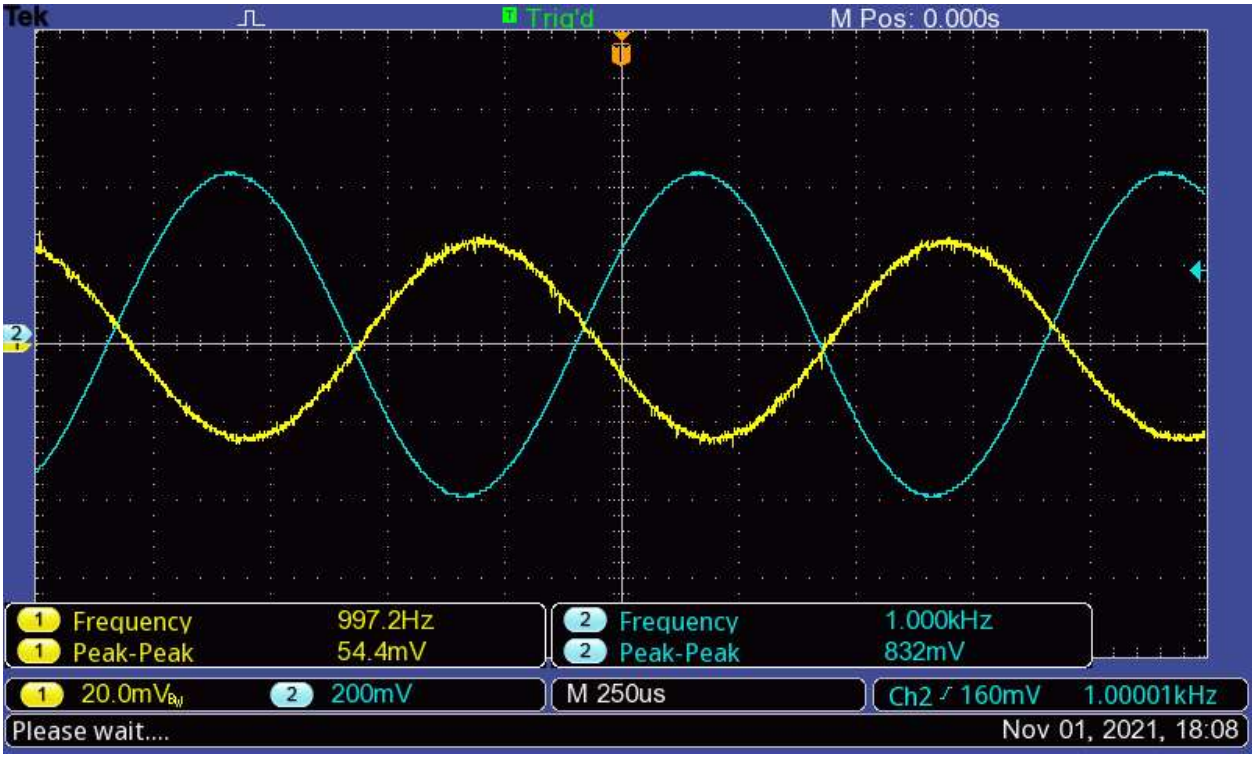


Figure 4: Figure for input and output at Vs = 50 mVpp

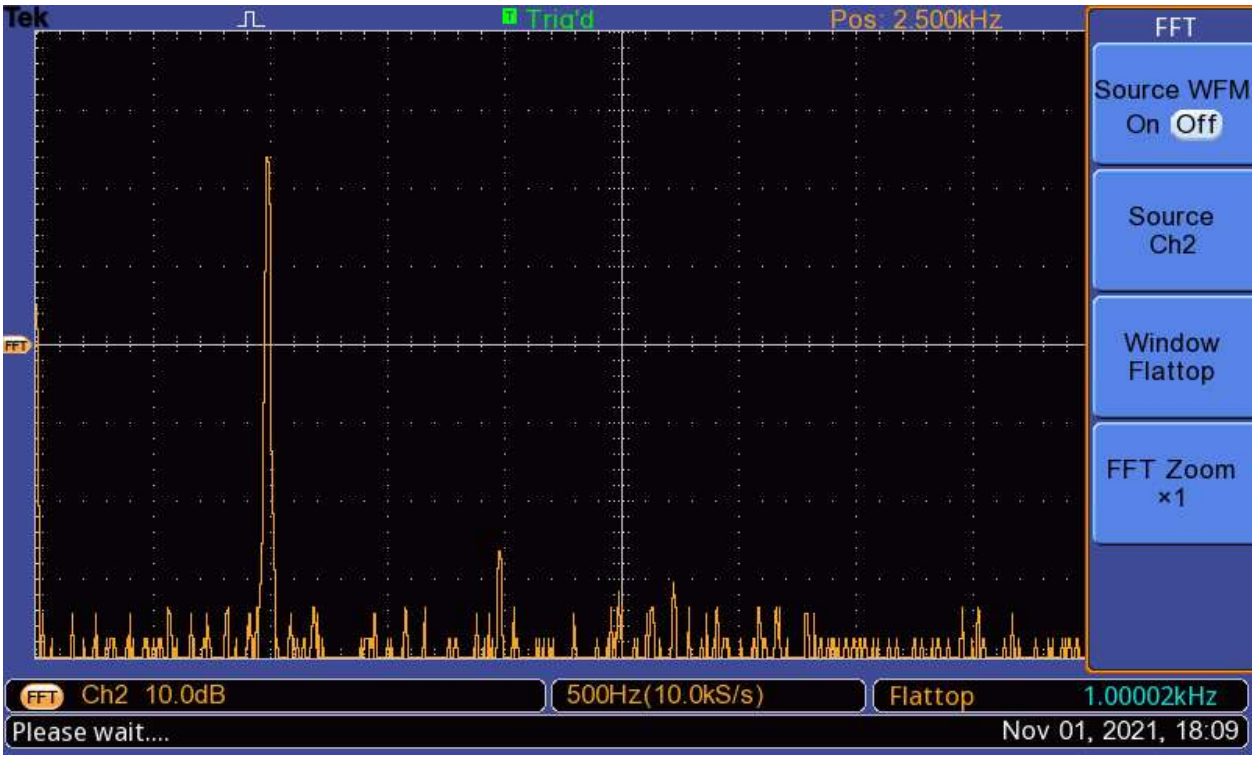


Figure 5: FTT of output at Vs = 50 mVpp

For Vs = 100 mVpp

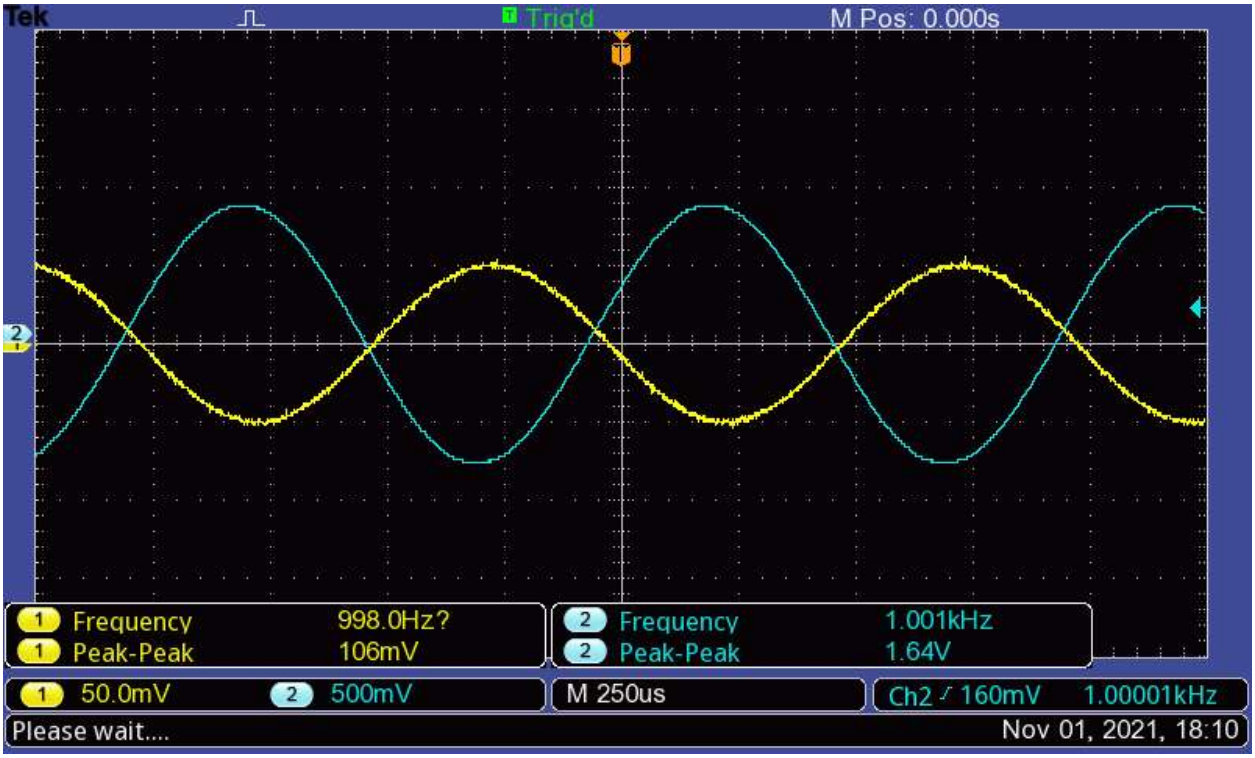


Figure 6: Figure for input and output at Vs = 100 mVpp

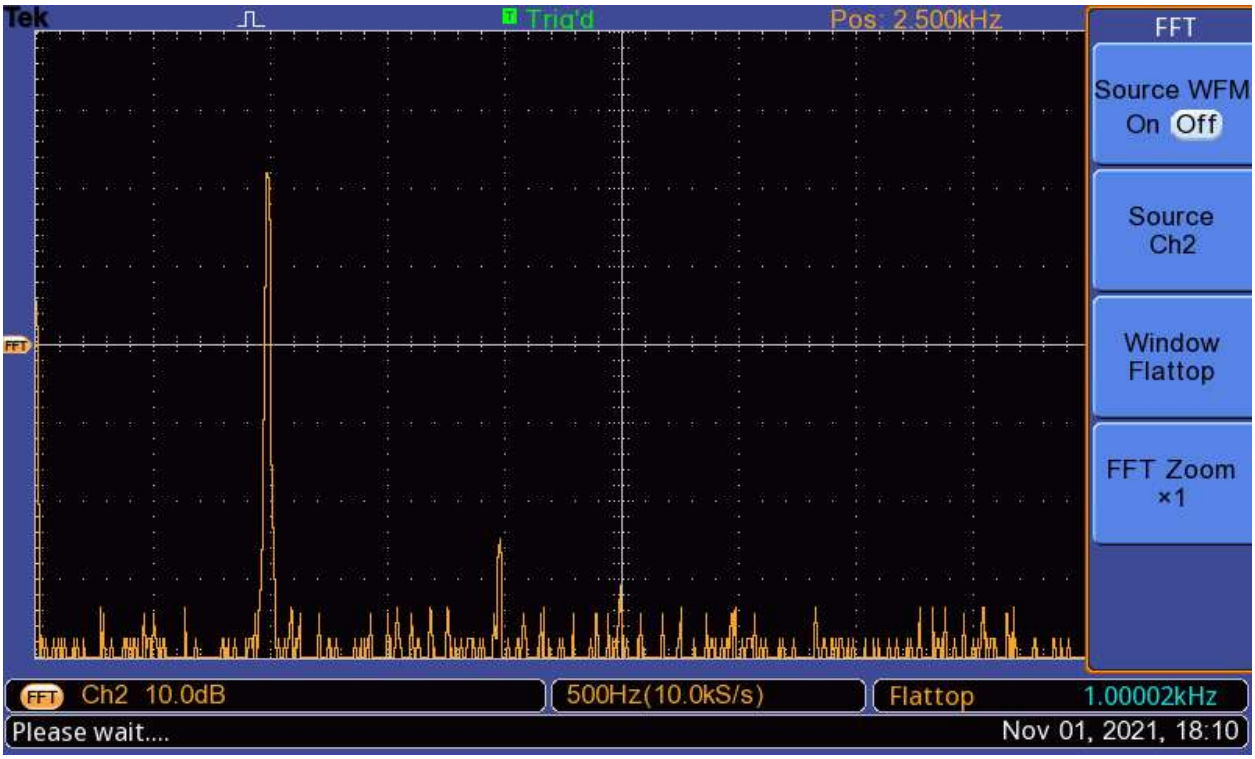


Figure 7: FFT of output at Vs = 100 mVpp

For Vs = 200 mVpp

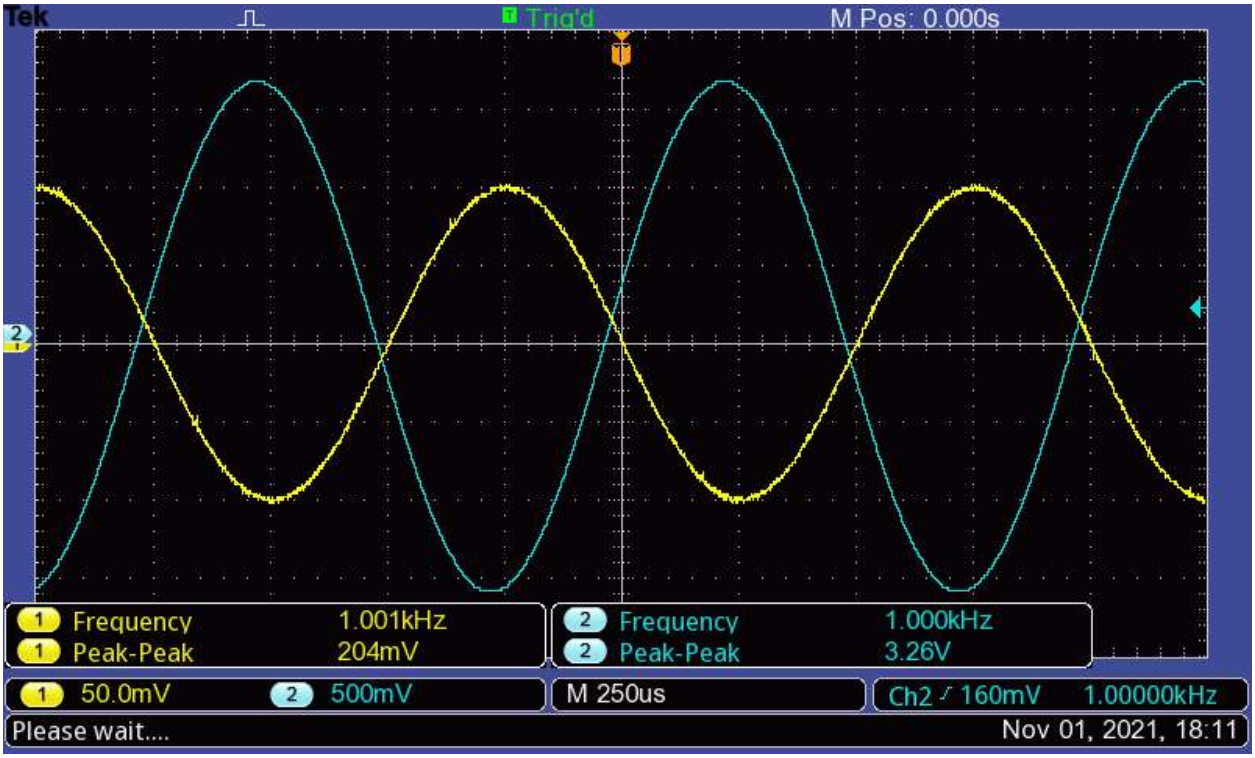


Figure 8: Figure for input and output at Vs = 200 mVpp

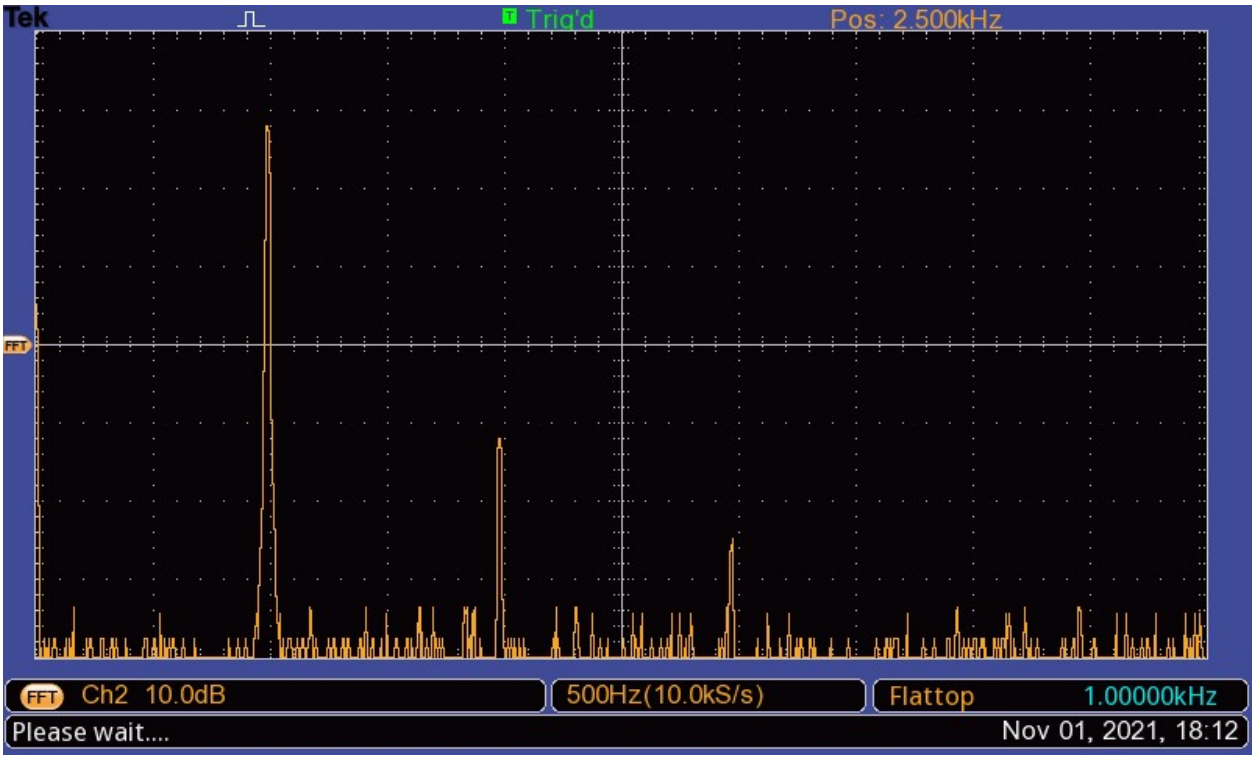


Figure 9: FFT of output at Vs = 200m Vpp

1.1.6 Part 4: Bandwidth of amplifier circuit:

- This experiment demonstrates the way to determine the bandwidth of the BJT amplifier circuit and to observe the effect of changing frequency of the input signal on the voltage gain of a BJT. In this experiment, the signal generator was set to 50m Vpp and the sweep mode of the signal generator was enabled. In sweep mode the following updates were made:
  START F: 100 Hz
  STOP F: 1 MHz
  SWP TIME: 500 ms
  SWP MODE: Logarithmic
  Note: SYNC output of the generator as trigger source for the oscilloscope

1.1.7 Part 4: Execution and results:

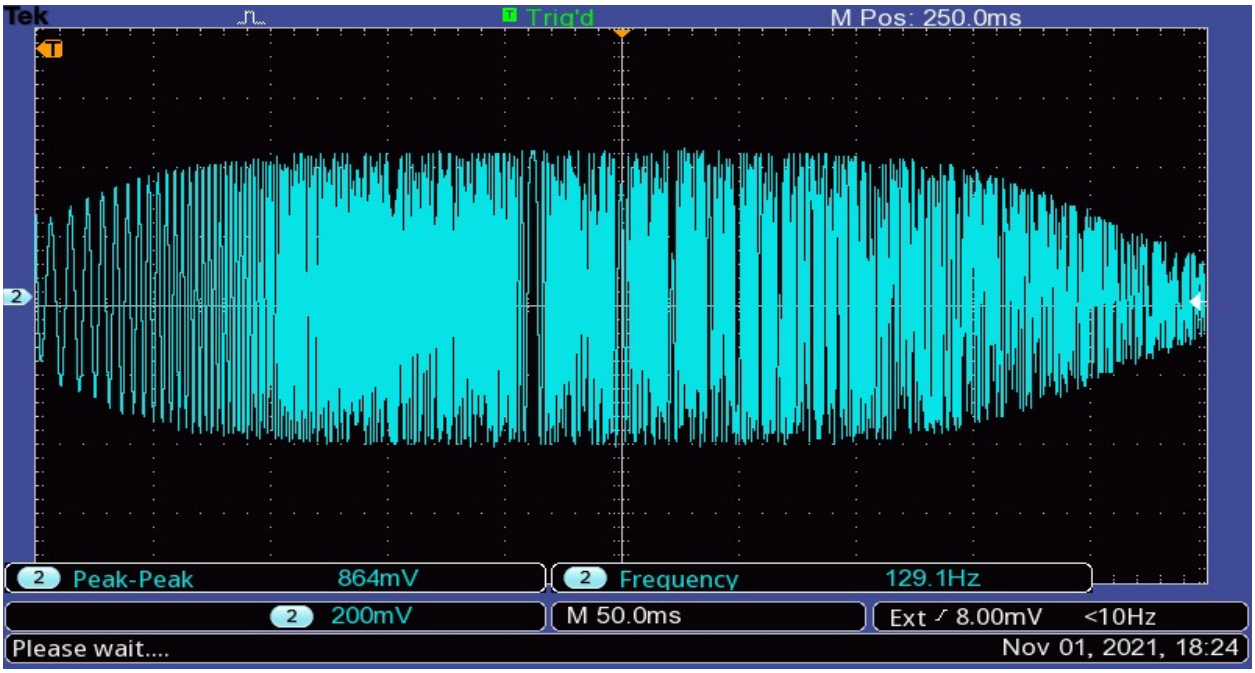


Figure 10: Full sweep mode of output signal

- The amplitude for -3dB frequencies would be: $\frac{864\ mV_{pp}}{\sqrt{2}} = 610.9\ mV_{pp}$

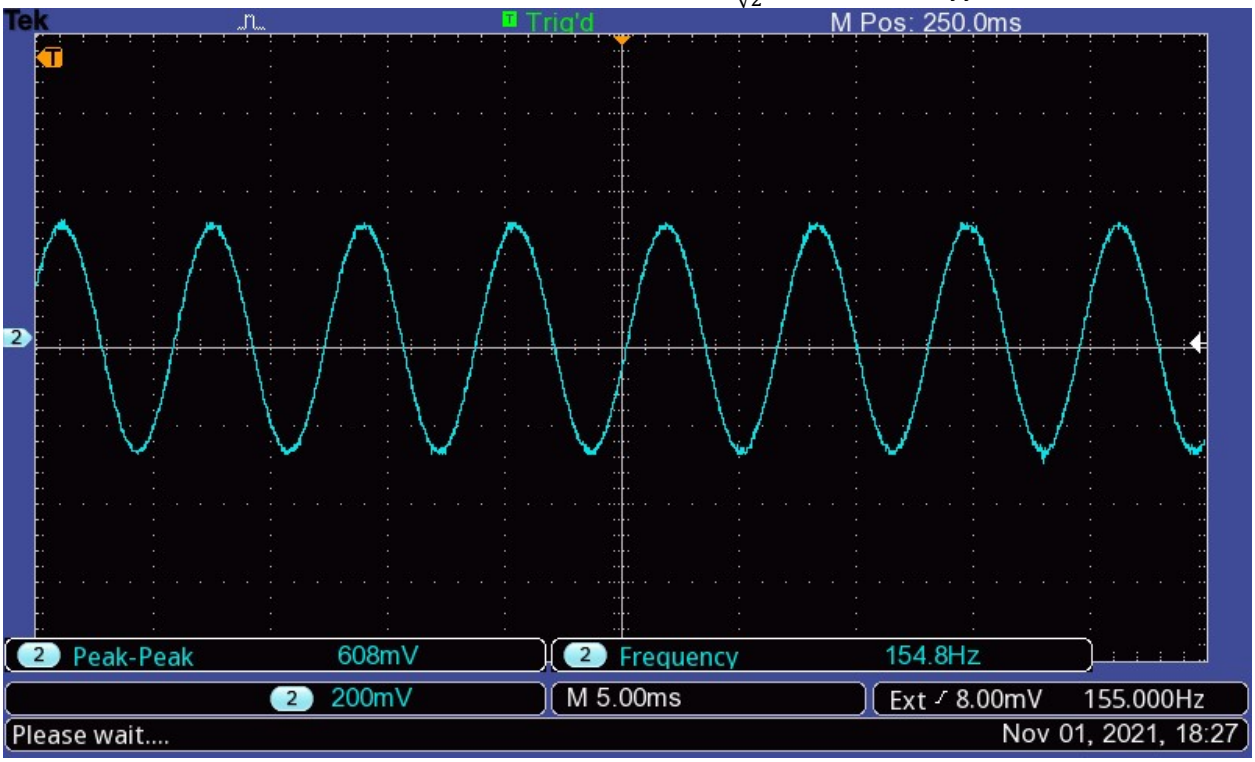


Figure 11: Lower -3 dB frequency of output signal

In the oscilloscope measure function was used to determine lower -3dB frequency and it is clear from the figure above that lower -3 dB frequency is,

$f_{low,-3\ dB} = 154.8\ Hz$

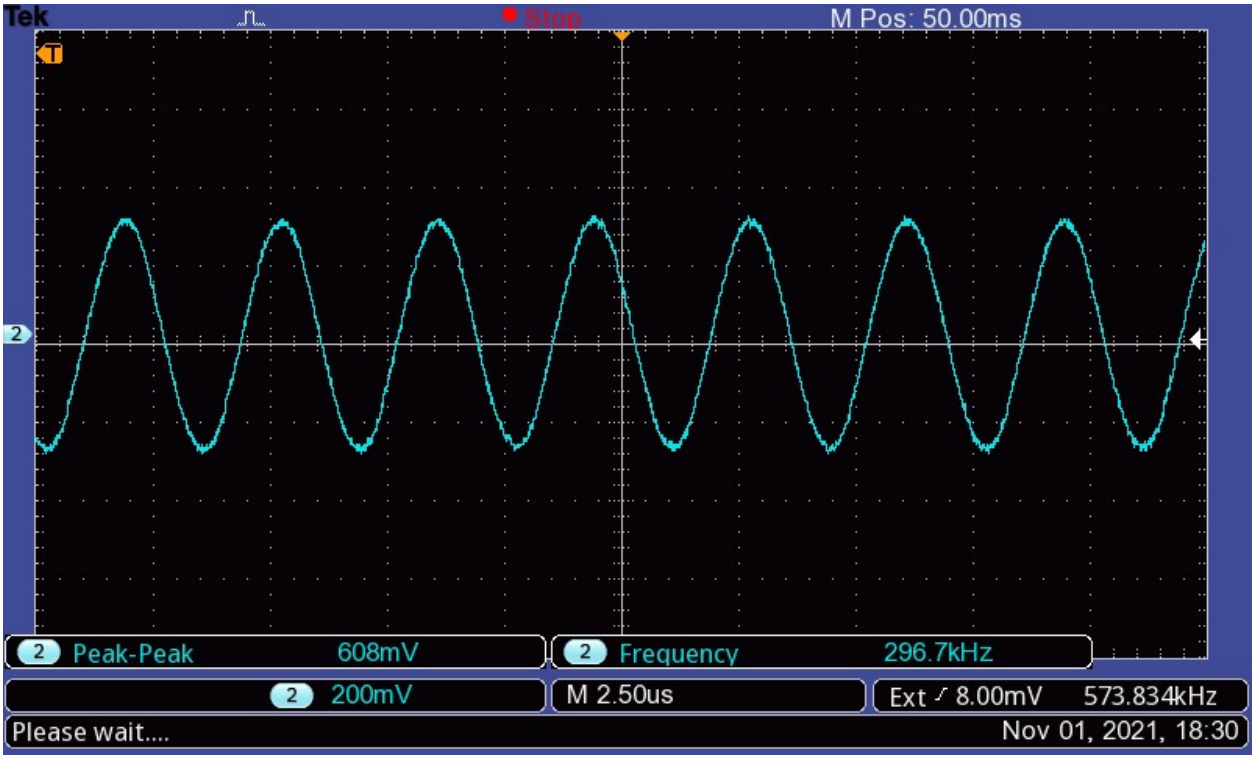


Figure 12: Upper -3 dB frequency of output signal

In the oscilloscope measure function was used to determine upper -3dB frequency and it is clear from the figure above that upper -3 dB frequency is,

$f_{upper,-3\ dB} = 296.7\ kHz.$

Hence, bandwidth of the output signal is:

Bandwidth (BW) = $f_{upper,-3\ dB} - f_{low,-3\ dB} = 296.7$ kHz – 154.8 Hz = 296.54 kHz

Thus, $Bandwidth = 296.54\ kHz$

2 Evaluation:

2.1 Evaluation Experiment Part 1

1) In Problem 6.3.1.(1), explain why the remaining terminal is the base when the other two terminals give overload .0L with both polarities of the multimeter applied?

- It is because transistor have same type of diode at its ends (1 and 3 terminal) either both of them are N-type or both are P-type. In between the transistor it has either a P-type or N-type at terminal 2. When the voltage is supplied across pins 1 and 3, there are two depletion layer that requires higher potential difference and moreover they are similar semiconductor type. But when voltage is applied with one of the two pins being pin 2, there is only one depletion layer to overcome and also are two different types of semiconductors in between. Hence, it conducts well and potential is developed.

2) Explain why Problem 6.3.1.(2) can be used to determine whether the transistor is 'NPN' or 'PNP'.

- When positive terminal of Multimeter's probe was connected to the central pin (base) and the negative to the rest two pins, one after another, we got OL, this helps us to determine that our central pin is P type and the rest of the two pins are N type transistor. Thus, the transistor is a NPN transistor.

3) Explain why Problem 6.3.1.(3) can be used to determine the collector and the emitter terminals.

- The emitter in an NPN transistor is the source of charge carriers. It has the maximum voltage out of all the other terminals. The emitter current when it flows towards the collector, only a part of the current reaches the collector. Hence, it can be analyzed that the maximum voltage drop would be measured across the emitter-base junction rather than collector-base junction. Therefore, the lower of the two readings would be base-collector junction and the higher one would be base-emitter junction.

2.2 Evaluation Experiment Part 2

1) Compare the measured values with the theoretical ones. Discuss the differences.

Voltage Points	Simulation / [V]	Multimeter/ [V]
V_{CC}	20	20.056
V_B	5.937	5.958
V_{BE}	0.715	0.6515
V_C	10.72	10.611
V_{CE}	5.50	5.293
V_E	5.222	5.32

Table 4: Comparison between Simulated and Measured values

The measured values with the multimeter correlates to the values from the simulation to high degree. However, there is still a slight difference as the simulation values assume every component including capacitor and transistor to work ideally which is not the case practically. There are some instrumental errors in the multimeter and there is 10% error in resistance, current and voltage values too, which gets propagated in the experiment. The major difference can be found in the base-emitter and collector-emitter voltages because the ideal BJT would have zero resistance between the collector and emitter resulting in maximum current flow, which is not the case practically. There might be some resistance between the collector and emitter which have caused the values to get fluctuated from simulated values.

2) Calculate the common emitter current gain β. Use only measured values!

$\beta = \frac{I_C}{I_B}$

$I_c = \frac{V_{CC}-V_C}{R_4} = \frac{20.056\,V - 10.611\,V}{1000\,\Omega} = 9.445\ \times 10^{-3} A$

$I_B = I_{R2} - I_{R3} = \frac{V_{CC}-V_B}{R_2} - \frac{V_B}{R_3}$

$I_B = \frac{20.056\,V - 5.958\,V}{22000\,\Omega} - \frac{5.958\,V}{10000\,\Omega} = 45.02\ \times 10^{-6} A$

$\beta = \frac{I_C}{I_B} = \ 209.8$

3) Determine the error sources with approximate values and -CALCULATE- the relative error of the calculated β. Check the plausibility of your previous calculated value by comparing it to the simulation. If the error is too high what is the reason and is there a way to avoid it?

Firstly, defining the errors for each value:

$\Delta V_{cc} = 0.05\% * 20.056 + 5 * 0.001 = \pm 0.015028\ V$

$\Delta V_c = 0.05\% * 10.611 + 5 * 0.001 = \pm 0.0103055\ V$

$\Delta V_B = 0.05\% * 5.958 + 5 * 0.001 = \pm 0.007979\ V$

$\Delta R_2 = 2\% * 22000 = \pm 440\ \Omega$

$\Delta R_3 = 2\% * 10000 = \pm 200\ \Omega$

$\Delta R_2 = 1\% * 1000 = \pm 10\ \Omega$

Now, calculating error propagation for I_c:

$$\Delta I_C = \left|\left(\frac{\partial\left(\frac{V_{CC}-V_C}{R_4}\right)}{\partial V_{cc}}\right)\cdot \Delta V_{cc}\right| + \left|\left(\frac{\partial\left(\frac{V_{CC}-V_C}{R_4}\right)}{\partial V_c}\right)\cdot \Delta V_c\right| + \left|\left(\frac{\partial\left(\frac{V_{CC}-V_C}{R_4}\right)}{\partial R_4}\right)\cdot \Delta R_4\right|$$

$\Delta I_C = \pm 0.096 \times 10^{-3} A$

Calculating error propagation for I_B:

$$\Delta I_B = \left|\left(\frac{\partial\left(\frac{V_{CC}-V_B}{R_2}-\frac{V_B}{R_3}\right)}{\partial V_{cc}}\right)\cdot \Delta V_{cc}\right| + \left|\left(\frac{\partial\left(\frac{V_{CC}-V_B}{R_2}-\frac{V_B}{R_3}\right)}{\partial V_B}\right)\cdot \Delta V_B\right| + \left|\left(\frac{\partial\left(\frac{V_{CC}-V_B}{R_2}-\frac{V_B}{R_3}\right)}{\partial R_2}\right)\cdot \Delta R_2\right| + \left|\left(\frac{\partial\left(\frac{V_{CC}-V_B}{R_2}-\frac{V_B}{R_3}\right)}{\partial R_3}\right)\cdot \Delta R_3\right|$$

$\Delta I_B = \pm 18 \times 10^{-6} A$

Finally, calculating error for β:

$$\Delta\beta = \left|\left(\frac{\partial\left(\frac{I_C}{I_B}\right)}{\partial I_C}\right)\cdot \Delta I_c\right| + \left|\left(\frac{\partial\left(\frac{I_C}{I_B}\right)}{\partial I_B}\right)\cdot \Delta I_B\right|$$

$\Delta\beta = \pm 81.6$

This is the error due to error propagation from the quantities used to calculate the β value.

Therefore, Relative Error from error propagation is: $\frac{\Delta\beta}{\beta} \times 100\% = 38.9\%$

Similarly, another way to calculate the relative error could be by comparing with the β value from the simulation:

In the simulation $\beta_{simulation} = \frac{I_C}{I_B} = \frac{9.279\ mA}{45.59\ \mu A} = 203.5$

So, Relative Error from comparison is: $\frac{209.8-203.5}{203.5} \times 100\% = 3.09\%$

The devices like capacitors and resistors, which are used for the measurement, has certain amount of error tolerance. Also, the experiment consisting of numerous nodes and connecting wires contributes to the increment of the error margin. However, these things are not taken into consideration while deriving the theoretical values. Similarly, the multimeter used for taking the readings were showing some kinds of fluctuating values initially and the multimeter reading also contributes to the error. All these sources are the responsible factors of the deviation of the value from the theoretical one. Usage of resistors with less error tolerance as well as high accuracy multimeter could decrease the error.

2.3 Evaluation Experiment Part 3

1) In what region of the output characteristic is the circuit for a distorted positive or negative amplitude? Explain!
   - In this experiment, a distorted negative amplitude was observed i.e., output has a phase difference of around 180°. In a signal amplifier it requires some form of DC Bias at its base in order to operate correctly without any distortion. A DC bias is required so that the amplifier can amplify the input signal over the entire cycle with the bias 'Q-point' set near to the load line. Thus, if the transistors have a correct biasing point, then the output waveform correlates with the input waveform. But in case of insufficient bias, the output waveform would have negative half of that of input waveform, just like the result in the experiment. Also, when the biasing voltage is set very low, the input voltage sets the output voltage during negative half of the cycle.

2) Using the measurements taken in the lab, calculate the voltage gain A_V of the amplifier. Compare to simulation.

→ Considering the result of one of the measurements, $V_{out} = V_{RL}$ = 832 mV
and $V_{in} = V_S$ = 50 mV
Then,
Gain (A_V) = $\frac{V_{out}}{V_{in}} = \frac{2832\ mV}{50\ mV}$ = 16.64

In dB scale, Gain (A_V) = 20 log (16.64) = 24.42 dB
From the simulation in prelab, the gain (A_V) = 23.7 dB

Factor	From Measurement / dB	From Simulation / dB
Gain (A_V)	24.42	23.7

Table 5: Comparison between gain by simulation and Measurement

The two values of gain obtained from measurement and simulation have high degree of correlation among each other.

3) Determine from the hard copies, what is the phase relationship between the input and the output signals? Explain the reason for such a relation.

→ The input and output signal have 180° phase relationship as can be seen from the hardcopies.

As the input voltage increases, the base current increases. We know that, $I_C = \beta \cdot I_B$, Hence the collector current also increases. As, the collector current increases the voltage drop over collector resistor i.e., R_4 also increases. So, the output voltage decreases. It can be referred as the output voltage decreases in response to an increasing voltage. Hence, it can be represented as a 180° phase shift.

4) Compare the FFTs with the different input signals to the simulation.

- The output signals resemble with a sine function at first glance, but when the FFT plot of the output is viewed, it has more than one frequency component, which deviates from the frequency spectrum of a sinusoid. So, the output signal is not a sinusoid. In the experiment 50mV_{PP} , 100mV_{PP} , 200mV_{PP} were used as the amplitude of input signal. It was seen that the number of peaks increased from 1 to 2 to 3 for 50mV_{PP} , 100mV_{PP} , 200mV_{PP} respectively, in the frequency domain.
  In the simulation, it was seen that all the input amplitudes had the peaks but the magnitude of the peak increased with increase of amplitude of the input signal. Thus, in the oscilloscope, with the increase in V_{PP} of input, the peaks for higher frequency were not hidden as their magnitude increased. This is the reason for seeing increased number of peaks in oscilloscope.

2.4 Evaluation Experiment Part 4:

1) In Problem 6.3.4.(2), explain your observation.

- In the figure (10), the voltage gain is very low at low frequency because the impedance of the capacitor is very high at low frequency and hence minimal part of signal passes to the output resistance and hence gain is low. As the frequency increases slightly the gain also increases because the impedance of the capacitor decreases. It is also to be noted that, the low frequency behaviour of gain is due to the external coupling capacitor, i.e., the capacitor in the circuits. But the high frequency behaviour is due to internal transistor capacitances. As when the frequency is on the higher range, the higher frequency reduces the current gain factor (β) and hence decreases the output voltage and the gain obviously. Also, when the frequency is higher, the breadboard and the circuit have an inductance behaviour which leads to increase in impedance at the collector resistor and hence decreases the gain.

2) Using the measurements taken in the lab, calculate the amplifier bandwidth

$f_{low,-3\ dB} = 154.8\ Hz$

$f_{upper,-3\ dB} = 296.7\ KHz$

Hence, bandwidth of the output signal is:

Bandwidth (BW) = $f_{upper,-3\ dB} - f_{low,-3\ dB} = 296.7$ kHz – 154.8 Hz $= 296.54$ kHz

Thus, bandwidth = 296.54 KHz

3) Compare to the simulation!

- From the simulation, the bandwidth is: 384.725 kHz

$BW_{simulation}$ **= 384.725 KHz**

$BW_{measurement}$ **= 296.54 KHz**

It can be noted that the bandwidth calculated from simulation and from lab measurement are close to each other. But still there is some difference between the two values of bandwidth. The possible reasons could be ideal behaviours of transistor in simulation. However, in practice, the transistor used in the lab have a variable value of current gain and does not behave ideally.

3 Conclusion:

This experiment dealt with studying the properties of Bipolar junction transistors and its use in modern day electronic designs. Initially, the bipolar transistor itself was studied and the type of transistor was identified and also the emitter, base and collector junction pins were verified. Similarly, the biasing and operation active mode of the BJT was analyzed and the bias circuit was constructed. The voltage across different critical nodes and bias points were measured using multimeter and it was compared with the theoretical value from the simulation. With the help of data for different parameters the common emitter current gain was calculated and was compared with the value from the simulation. Moreover, BJT circuit in its active mode of operation was used for amplification of small signal model for varying range of frequencies and input amplitude. Furthermore, the bandwidth of BJT amplifier circuit was measured using the oscilloscope and signal generator (in SWEEP mode). The lower and upper -3 dB frequency were measured and the bandwidth was calculated.

In the experiment a signal generator was used as an alternating voltage supply. The value of V_{PP} from the signal generator might not exactly resemble with the actual input voltage across the circuit. The capacitor used in the experiment has some tolerance and moreover the value of capacitance lies within the range of ± 10%. Moreover, the external capacitance and internal capacitance of transistor could contribute to the error in measurement and plot of output parameters. It should also be noted that the value of current gain (β) was not consistent for all the transistor and also all the transistor cannot be expected to have a perfect ideal model. This can be one of the reasons for the introduction of error in the experiment. Similarly, for some portions of the experiment very high frequencies were used and for that portion, the breadboard and other electrical component had some inductive effect within it, i.e., inductance and it could be the reason for varying value of measurement parameters compared to that of values from the simulation.

4 References:

- Electronics Lab Manual (Uwe Pagel)
- http://www.faculty.jacobs-university.de/upagel/
- https://www.electrical4u.com/bipolar-junction-transistor-or-bjt-n-p-n-or-p-n-p-transistor/

Experimental Findings: Operational Amplifier

(Forgot to copy the pictures from the oscilloscope, please consider the measured values)

1. Differential amplifier using a fixed emitter resistor

- Measurement of dc bias values:

	T1	T2
V_C [V]	5.315	5.349
V_B [V]	-0.0438	-0.0418
V_{BE} [V]	0.6323	0.6329
I_C [mA]	2.351	2.214
I_{RE} [mA]	4.256	

2. Implementing a circuit source

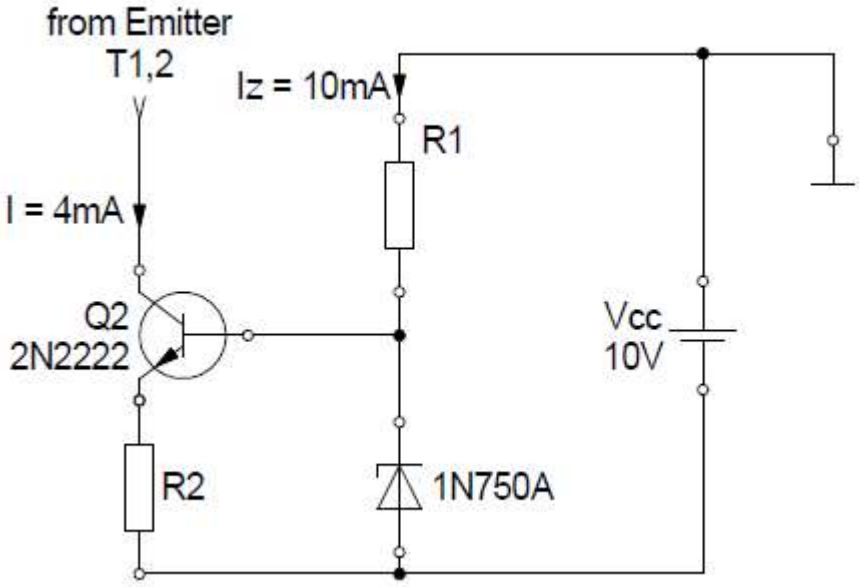


Figure 1: Test circuit for second problem

- Calculate R_1 and R_2 to get about the same I_{R_E} as in the circuit with the fixed emitter resistor.

In the left most loop,
$10 - 10\ \text{mA} \cdot R_1 - 4.7 = 0$
$\therefore \boldsymbol{R_1 = 530\ \Omega}$

Now, in the lower left loop,
$4.7 - 0.7 - 4\ \text{mA} \cdot R_2 = 0$
$\therefore \boldsymbol{R_2 = 1000\ \Omega}$

3. Differential amplifier using current source

- Measuring the dc bias values:

	T1	T2
V_C [V]	5.805	5.813
V_B [V]	-0.0394	-0.0383
V_{BE} [V]	0.6261	0.6347
I_C [mA]	1.991	2.002
I_{RE} [mA]	3.9	