Jacobs University Bremen

Natural Science Laboratory
Electrical Engineering Module II

Fall Semester 2021

Lab 3 – Metal Oxide Field Effect Transistor

Roshan Nepal

Experiment conducted by : Roshan Nepal and Aditya Ojha
Place of execution : Teaching Lab EE
Date of execution : November 10, 2021

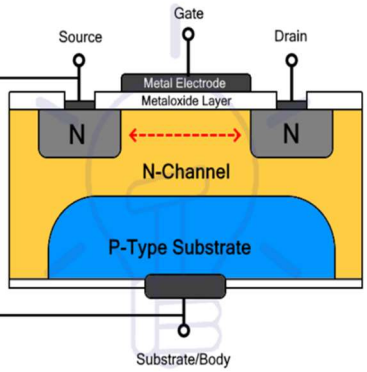
Objective:

The main objective of the experiment was to understand and execute the properties of MOSFET. The first part of the experiment focused in the I-V Characteristic of MOSFET its transfer characteristic. In the second part of the experiment, the output characteristic of MOSFET was analyzed. In this part, the drain-source voltage (V_{DS}) was measured and the output current at the drain (I_D) was recorded for different values of V_{GS}. From the output characteristic, different operation regions of the MOSFET were verified.

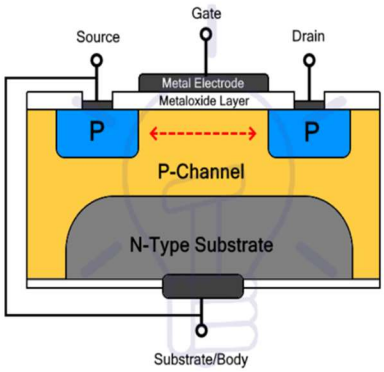
Prelab: Field Effect Transistor

Problem 1: Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

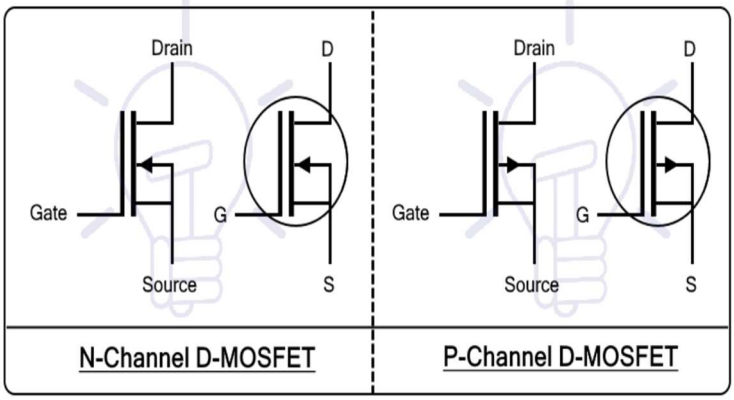
1) Explain the differences between an enhanced and depletion MOSFET.
   The differences between an enhanced and depletion MOSFET are:
   - Depletion MOSFET or D-MOSFET:



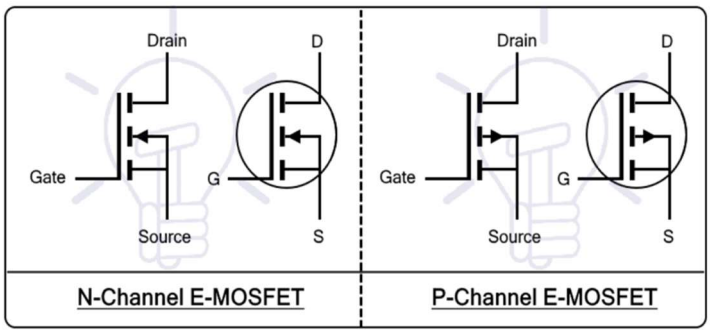
N-Channel D-MOSFET



P-Channel D-MOSFET



i) The channel depletes with the gate voltage in depletion MOSFET.
ii) The voltage from gate to the source (V_{GS}) can be positive or negative.
iii) The D-MOSFET can work in both depletion and enhancement mode.
iv) There is no threshold voltage for switching ON the D-MOSFET.
v) N-type semiconductors exist in the structure itself between source and drain.



vi) There are different types of biasing possible in D- MOSFET i.e., Gate Bias, Zero Bias, Self-Bias and Voltage divider Bias.

- Enhanced MOSFET or E-MOSFET:
  - i) The channel is enhanced or induced using the gate voltage in enhanced MOSFET.
  - ii) The voltage from gate to the source (V_{GS}) is always positive.
  - iii) The E-MOSFET can only work in enhancement mode.
  - iv) There is a threshold voltage at which the MOSFET switches ON.
  - v) There is no n-channel between source and drain.
  - vi) There are different types of biasing possible in E- MOSFET i.e., Gate Bias, Voltage divider Bias, Drain feedback Bias.

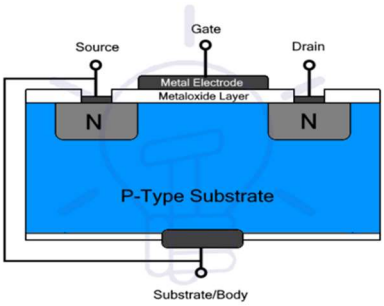
2) Explain the differences between an NMOS and PMOS transistor.
The differences between NMOS and PMOS can be characterized as:

i) Fabrication:
In NMOS, the source and the drain are made of n-type semiconductors while the bulk is made of a p-type semiconductor.
In PMOS, the source and the drain are made of p-type semiconductors while the bulk is made of an n-type semiconductor.

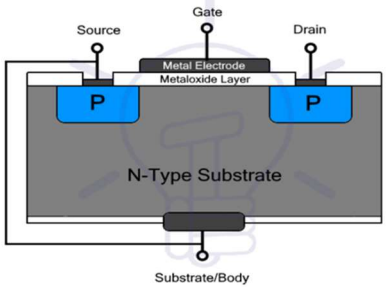
ii) Majority Carriers:
In NMOS, the majority carriers are electrons.
In PMOS, the majority carriers are holes.

iii) Size:
NMOS devices are comparatively smaller compared with PMOS devices with complimentary conducting properties. It is because NMOS transistor provides one-half of the impedance as provided by a PMOS.

iv) Operating Speed:



N-Channel E-MOSFET

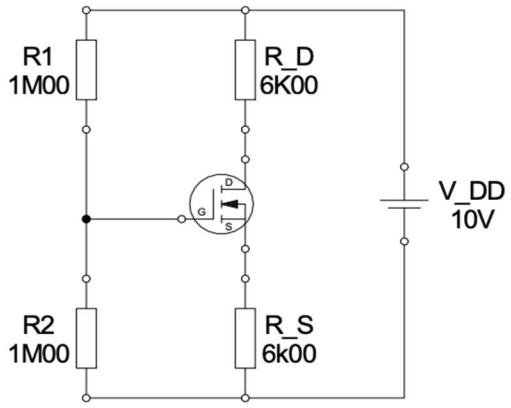


P-Channel E-MOSFET

NMOS devices can be switched faster compared to PMOS devices. It is because the charge carries of NMOS i.e., electrons can travel faster than the charge carries of NMOS i.e., holes.

v) Voltage Functionality:
NMOS conducts for a high voltage at the gate terminal.
PMOS conducts for a low voltage at the gate terminal.

Problem 2: MOSFET as Amplifier



It is assumed that the transistor operates in saturation, so that the drain source current can be described by:

$$I_{DS} = \mu_n C_G \frac{W}{2L}(V_{GS} - V_{th})^2 = k * (V_{GS} - V_{th})^2$$

The prefactor k is given by $k = 0.5\,\mathrm{mA/V^2}$. $V_{th} = 1\,\mathrm{V}$

1) Determine the gate-source and drain-source voltage and the drain current for the MOSFET amplifier.

From the circuit,
$V_{R2} = \frac{R_2}{R_1+R_2} \cdot V_{DD} = \frac{1}{2} \cdot 10\ V = 5\ V$
Gate Voltage $V_G = V_{R2} = 5\ V$

Given:
$I_{DS} = k * (V_{GS} - V_{th})^2$
$I_{DS} = 0.5 \times 10^{-3} * (V_{GS} - 1)^2$ (1)

Now using KVL:
$V_G = V_{GS} + I_{DS} \cdot R_S$
$I_{DS} = \frac{5 - V_{GS}}{6000}$ (2)

From equation (1) and (2):
$V_{GS} = 2\ V\ or - 0.333\ V$
Since it is an enhanced MOSFET, V_{GS} must be positive. So,
$V_{GS} = 2\ V$
Using that value, $I_{DS} = 0.5\ mA$.

Now using KVL again:
$V_{DD} - I_{DS} \cdot (R_D + R_S) - V_{DS} = 0$
$V_{DS} = 10 - 0.5 \times 10^{-3} \cdot 12000 = 4V$

So, Gate Source Voltage $V_{GS} = 2\ V$
Drain Source Voltage $V_{DS} = 4\ V$
Drain Current $I_D = 0.5\ mA$

2) Show that the MOSFET indeed operates in the saturation region.

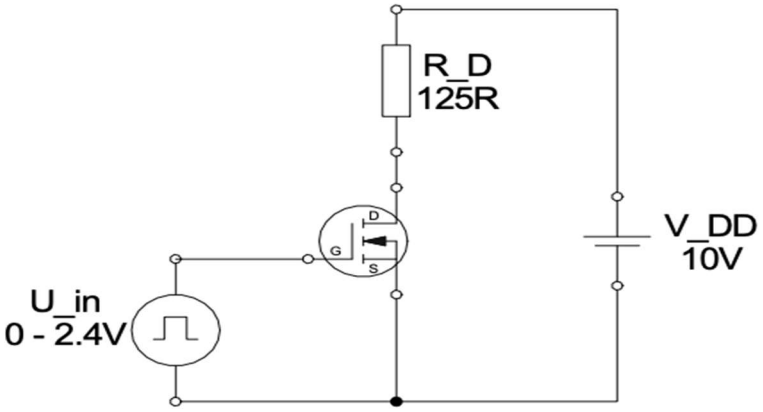
For the MOSFET to operate in the saturation region:
$V_{DS} > V_{GS} - V_{th}$

In this circuit, $V_{DS} = 4\ V$, $V_{GS} = 2\ V$ and $V_{th} = 1\ V$
So,
$4V > 2\ V - 1\ V = 1\ V$ (True)

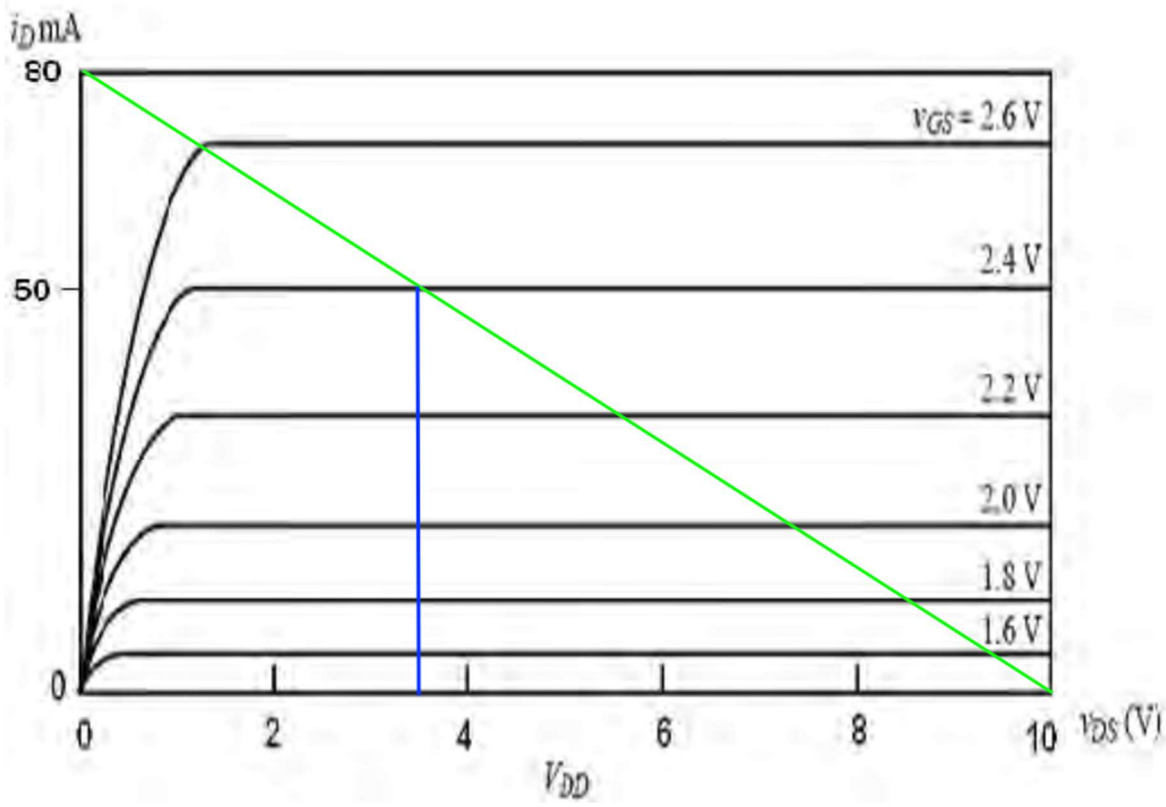
So, the MOSFET operates in the saturation region:

Problem 3: MOSFET as Switch

1) The MOSFET is used as a switch. The input signal of the circuit varies between 0 V and 2.4 V. Determine the operating point for both input voltages.



The operating point of the MOSFET is the bias point of the MOSFET. The biasing of MOSFET is done with a DC voltage so that maximum gain from the MOSFET could be achieved. In calculation, $V_{DD} = V_{DS} + I_D \cdot R_D$, the DC line is drawn based on the fact that $I_D = 80mA$ when $V_{DS} = 0$ and $I_D = 0\ A$ when $V_{DS} = 10\ V$. The slope of load line is $(-\frac{1}{R_D})$.



$V_{DS} = V_{DD} - I_D \cdot R_D = 10 - 50 \times 10^{-3} \cdot 125 = 3.75\ V$
For $V_{GS} = 0\ V$: Operating Point $V_{DS} = 0\ V$
For $V_{GS} = 2.4\ V$: Operating Point $V_{DS} = 3.75\ V$

From the graph, if a straight vertical line is drawn from the intersection of the line with slope of $(-\frac{1}{R_D})$ and $V_{GS} = 2.4\ V$ it has the value for $V_{DS} \approx 3.75\ V$, supporting our calculation.

1 Execution

1.1 Experimental set-up:

Workbench Number 8

- Oscilloscope
- Signal Generator
- ELABO Multimeter
- BNC Cable
- Resistors (50 Ω, 100 KΩ, 10K Ω, 560 Ω)
- Capacitors ($100nF$)
- MOSFET (2N7000)
- Tenma Multimeter

1.1.1 Part 1: I/V Characteristic of a MOSFET:

1. Use the following circuit to determine V_{TH}

A MOSFET has multiple terminals with major one being Gate, Source and Drain. All the MOSFET has its own operating / threshold voltage and in this experiment the threshold voltage for a particular value of drain current was determined. In particular, this was a NMOS which was subjected to test for determining the characteristic of current vs voltage. The drain current was maintained to be around 250μA and the gate to source voltage also the threshold voltage in this case was measured.

Test Circuit:

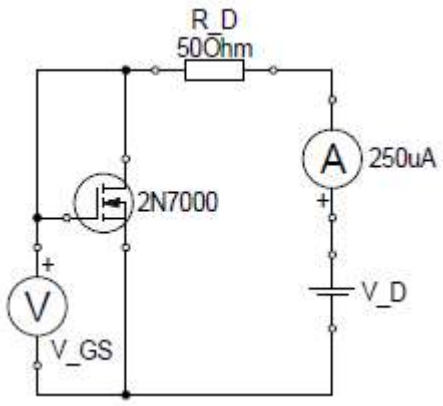


Figure 1: Circuit diagram for measuring threshold voltage and drain current

- The following table presents the voltage measured across the gate source terminal, i.e., V_{GS} which is the threshold voltage V_{TH}

Measurement Parameters	Magnitude
I_D	249.79 μA
V_{TH}	2.1065 V

Table 1: Measurement of threshold voltage and drain current

2. Use the following circuit to measure the transfer characteristic

- The same circuit from part 1 was used here with slight modification, i.e., a multimeter was set across the V_{GS} supply so as to measure the actual magnitude of gate-source voltage. Also, the voltage was measured across the drain-source terminal, i.e., V_{DS}. Moreover, the drain current was also measured for all variable value of V_{GS}.

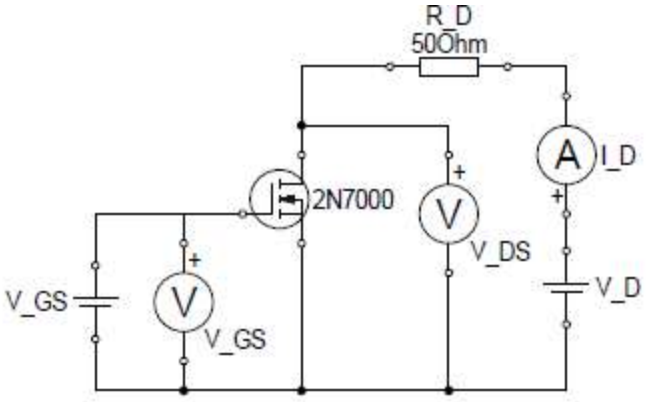


Figure 2: Circuit diagram for measuring transfer characteristics

- The following table presents the varying gate-source voltage (V_{GS}) and the measured drain current for the particular V_{GS}.

-

V_{GS} / V	I_D / mA
0	0
0.5656	0.000300
1.039	0.00031
1.55539	0.00043
1.7618	0.00723
1.8783	0.0237
1.9588	0.0539
2.0687	0.16936
2.2324	1.3922
2.3967	8.401
2.651	20.86
2.89542	43.38
3.0217	68.11

Table 2: Measurement values for V_{GS} and I_D

3. Use the circuit from before and measure the output characteristic for gate source voltages of 2 V, 2.2 V, 2.4 V, and 2.6 V. The drain source voltage should be scanned from 0 V to 4 V.

- The same circuit was used for this part of the execution. But now the output characteristic for different gate source was measured while drain source voltage was scanned from 0 V to 4 V. The results for the measurements are tabulated in the table below:

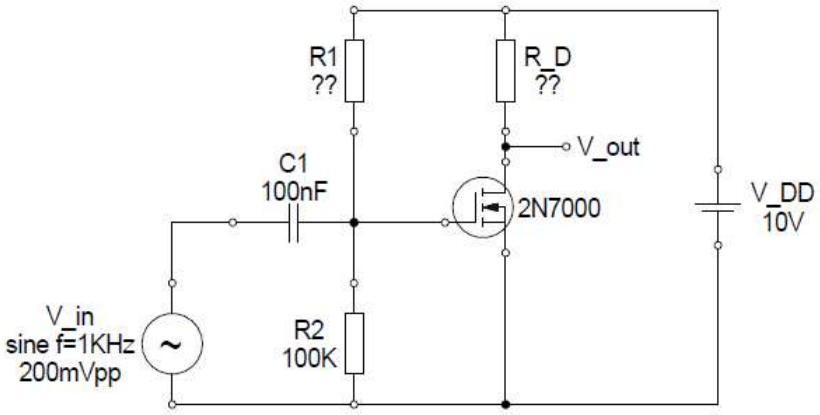
- The following table presents the varying gate-source voltage (V_{DS}) and the measured drain current (I_{DS}) for the particular V_{GS}.

V_{GS} = 2.0109 V		V_{GS} = 2.2018 V		V_{GS} = 2.4008 V		V_{GS} = 2.6084 V	
V_{DS} / V	I_{DS} / µA	V_{DS} / V	I_{DS} / µA	V_{DS} / V	I_{DS} / mA	V_{DS} / V	I_{DS} /m A
0.0040	0.00001020	0.00000	0.0000205	0.00000	0.0000073	0.00000	0.000730
0.5116	0.00005530	0.51590	0.0009330	0.50780	0.0045090	0.50290	0.009100
1.0210	0.00005700	1.08140	0.0013530	1.00090	0.0087800	0.99640	0.014390
1.5250	0.00005790	1.52580	0.0018650	1.51940	0.0121300	1.51050	0.018500
2.0183	0.00005880	2.09040	0.0020570	2.01590	0.0145100	2.03130	0.020200
2.5050	0.00005855	2.52020	0.0022320	2.49820	0.0159200	2.50170	0.021470
3.0159	0.00006011	3.52730	0.0030000	3.51600	0.0179400	3.50960	0.023430
4.0180	0.00006173	4.00900	0.0031800	4.04800	0.0180000	4.07000	0.024090
0.0040	0.00001020	0.00000	0.0000205	0.00000	0.0000073	0.00000	0.000730

Table 3: Measurement data for V_{DS} and I_{DS}

1.1.2 Part 2: MOSFET and an Amplifier:

- This experiment dealt with studying the amplifying nature of MOSFET. In this experiment firstly the value of resistance for a particular gain was calculated and then was used in the circuit.
- Test Circuit:



$V_{GS} = 2.7\,\mathrm{V},\ V_{DS} = 5\,\mathrm{V},\ k = 72.2\,\mathrm{mA/V^2},\ U_{th} =$ use measured value!

Figure 3: Circuit diagram for MOSFET amplifier

To calculate the values of R_1 and R_2:

$V_{GS} = \frac{R_2}{R_1+R_2} \cdot 10\ \text{V}$

$R_1 = \frac{R_2}{V_{GS}} \cdot 10\ \text{V} - R_2 = \frac{100000}{2.7} \cdot 10\ \text{V} - 100000 = 270\ \text{K}\Omega$

Now, $I_{DS} = \text{K} \cdot (V_{GS} - V_{th})^{\ 2} = 72.2\text{m} \cdot (2.7 - 2.102)^{\ 2} = 25.8\ \text{mA}$

Then, $R_D = \frac{V_{DD}-V_{DS}}{I_{DS}} = \frac{10-5}{25.8mA} = 194\ \Omega$

4. Take hard copies showing the input and the output signals and the phase relation between them

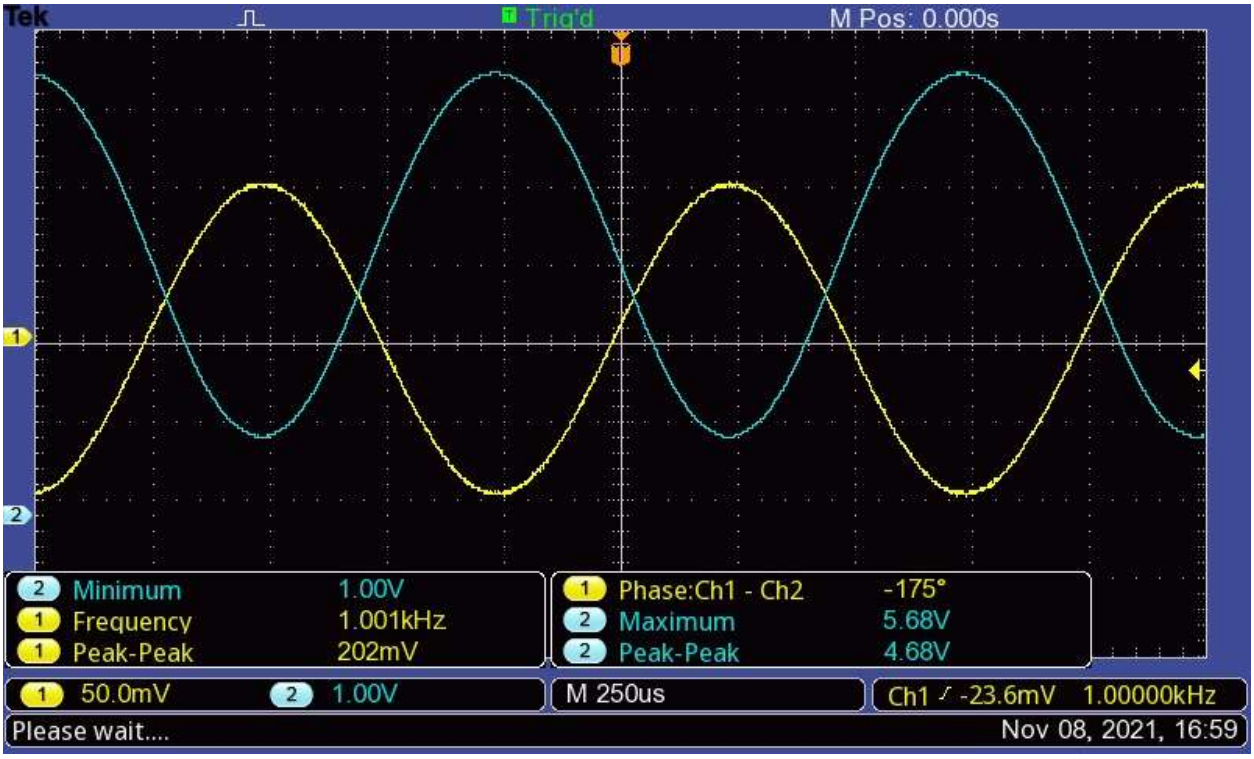


Figure 4: Hardcopy of input and output of MOSFET Amplifier

2 Evaluation:

2.1 Evaluation Experiment Part 1

1) Plot the measured transfer characteristic
   - The plot provides the information on the changing nature of output drain current I_{DS} with the altering value for input gate-source voltage. In general, the graph follows an exponential pattern after reaching the threshold voltage which is 2.102 V in this case.

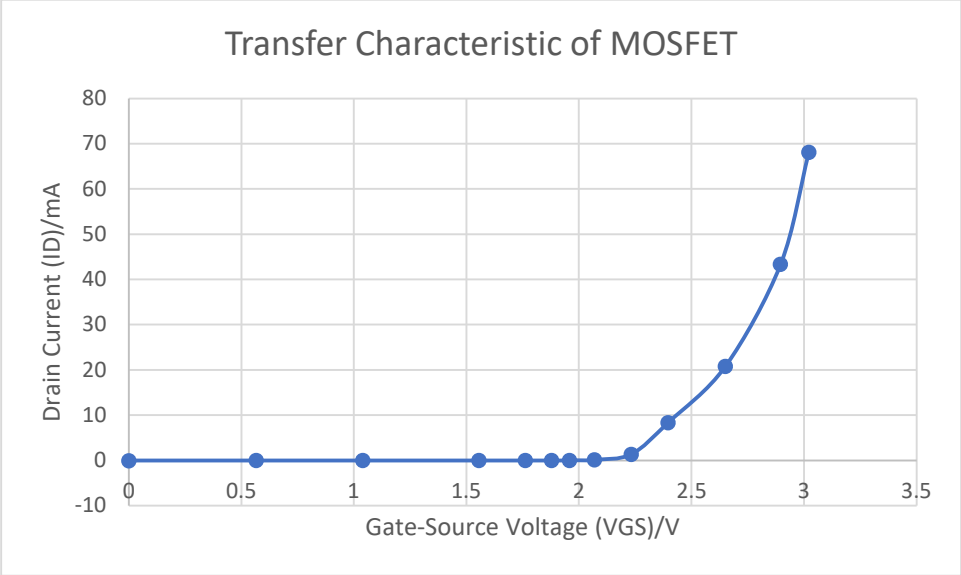


Figure 5: Plot of transfer characteristic of MOSFET

2) Plot the measured output characteristic for the different gate source voltages.

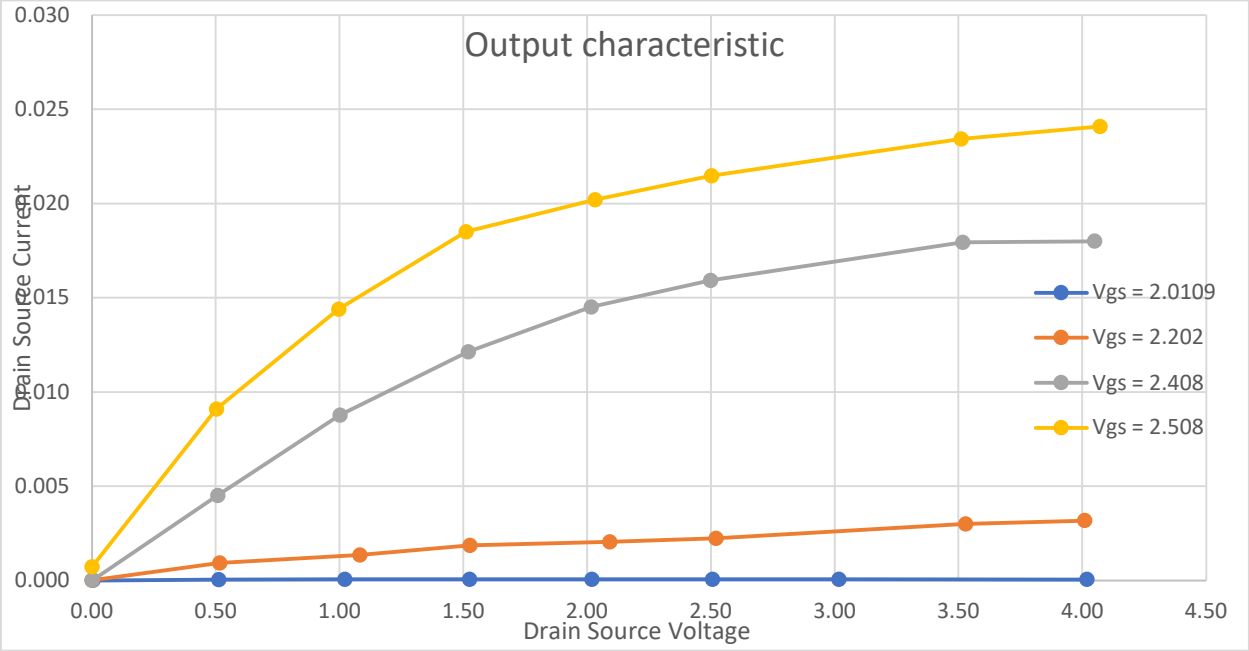


Figure 6: Plot for output characteristic for gate voltage

3. Insert the $V_{DS} = V_{GS} - V_{TH}$ line into the output characteristic.

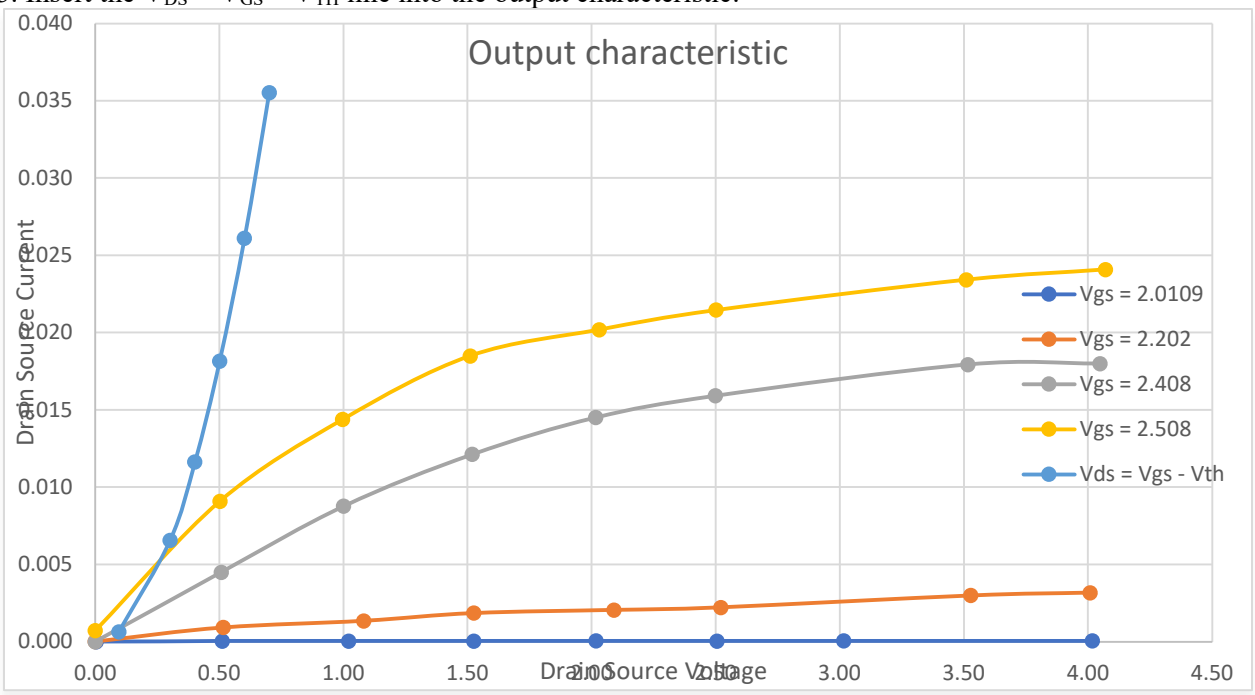


Figure 6: Plot for output characteristic for gate voltages with Vds = Vgs – Vth included

2.2 Evaluation Experiment Part 2

1. In which mode (linear or saturation) does the transistor operate during amplification? Provide an explanation.

   The transistor operates in saturation mode. It is because of the fact that output in saturation region depends only on the input Gate - Source Voltage (V_{GS}) and the V_{out} is dependent on the magnitude of current flowing through the resistor R_D. Here, the output is independent of the source-drain voltage and is a function of gate-source voltage only. In linear region, it is expected that the gain would be different since I_{DS} was changing linearly with the drain-source voltage.

2. If the amplitude of the sinusoidal input voltage is too large clipping of the output voltage is observed. Determine the largest possible input voltage for which no clipping is observed.

   From the hardcopies, we have:

   Gain- Measured $(G_{measured}) = \frac{V_{out}}{V_{in}} = \frac{4.68}{0.202} = 23.17$

   Now, maximum positive output voltage is calculated using the formula:

   $V_{out,max} = V_{DS} + \frac{1}{2} \cdot V_{out,(p-p)} = 5 + \frac{1}{2} \cdot 4.68 = 7.34$ V

Then,

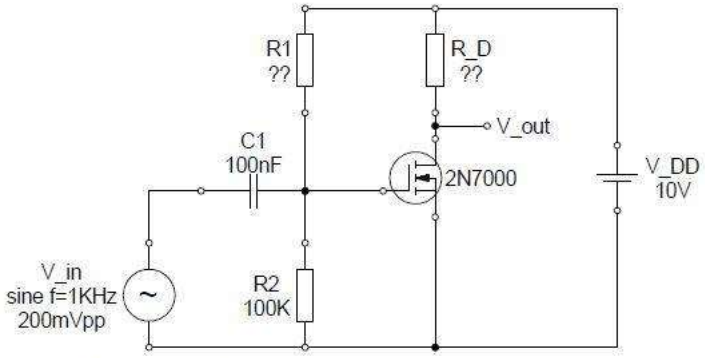
For this maximum output, the calculated value for maximum input is:

$V_{in,max} = \frac{V_{out,max}}{G_{measured}} = \frac{7.32}{23.17} = 316$ mV

∴ The maximum input voltage ($V_{in,max}$) without clipping is 316 mV.

3. Provide a mathematical expression for the voltage gain (theoretical voltage gain) of the circuit.

From the circuit,



$V_{GS} = 2.7V$, $V_{DS} = 5V$, $k = 72.2mA/V^2$, U_{th} = use measured value!

$V_{out} = V_{DS} = V_{DD} - I_D \cdot R_D$

Also, $I_D = I_{DS} = \mathrm{K} \cdot (V_{GS} - V_{TH})^2$

Then,

$V_{out} = V_{DD} - \mathrm{K} \cdot (V_{GS} - V_{TH})^2 \cdot R_D$

Then,

Gain (G) $= \frac{V_{out}}{V_{in}} = \frac{V_{DD} - \mathrm{K} \cdot (V_{GS} - V_{TH})^2 \cdot R_D}{V_{in}}$

4. Determine the measured voltage gain and compare the measured voltage gain with the theoretical voltage gain.

The measured voltage gain from the hardcopies is:

Gain- Measured ($G_{measured}$) $= \frac{V_{out}}{V_{in}} = \frac{4.68}{0.202} = 23.17$

Now, Gain in dB ($G_{measured,dB}$) = $20\ log(23.17) = 27.28\ dB$

Then, theoretical value of gain is:

Gain $(G_{theoretical}) = \frac{V_{out}}{V_{in}} = \frac{10 - 72.2\text{m} \cdot (2.7 - 2.1065)^2 \cdot 194}{0.2} = 25.33$

Now, Gain in dB $(G_{theoretica\ ,dB}) = 20\ log(25.33) = 28.073\ dB$

∴ Gain in dB $(G_{measured,dB})$ = 27.28 dB

∴ Gain in dB $(G_{theoretical,dB})$ = 28.073 dB

The theoretical and measured value of gain highly correlate to one another and there is only a slight difference between the two values. The slight difference might exist due to the tolerance of the resistor. The calculated value of resistance of R_D was 194 Ω. But, it was not possible to use 194 Ω in the circuit as it was not available. So a resistor of 200 Ω was used instead and this might have accounted for difference in the theoretical and measured gain.

5. Explain the phase relation between the input and the output.

The input and output have a phase difference of 173° in the experiment, close to the theoretical value of 180°. When the input signal's amplitude increases in positive direction, the drain-source current (I_{DS}) increases and it results in increase in potential drop across the resistor (R_D). Now since, $V_{out} = V_{DS} = V_{DD} - I_D \cdot R_D$, So increase in voltage across (R_D) implies that the voltage across V_{DS} would decrease and as $V_{DS} = V_{out}$. Hence, the amplitude of V_{out} would decrease and likewise for the increase in input signal's amplitude in negative direction, where the amplitude of V_{out} would increase. Finally, due to these facts there exist a phase relation of 180° between the input and the output.

3 Conclusion:

In this experiment, the main goal was to understand and execute the properties of MOSFET. The first part of the experiment focused in the I-V Characteristic of MOSFET its transfer characteristic. The relationship between V_{GS} and I_D was of exponential nature. In the second part of the experiment, the output characteristic of MOSFET was analyzed. In this part, the drain-source voltage (V_{DS}) was measured and the output current at the drain (I_D) was recorded for different values of V_{GS}. From the output characteristic, different operation regions of the MOSFET were verified. In the ohmic region, the MOSFET showed a linear dependence between V_{DS} and I_D. While, in the saturation region, the drain current (I_D) was nearly constant for increasing value of V_{DS}.

In this experiment, there were some minor sources of error and one of them being the heating effect of MOSFET. The MOSFET used in our experiment got heated up and it resulted into unreliable data for some of the measurements. So, for accuracy of measurements several readings were taken into consideration before taking the final note. Moreover, the resistance calculated in the execution section was not available for the use in the experiment. So, a resistor of resistance similar to the calculation was used for set-up of the circuit. Also, the value of constant pre-factor (k) was not accurate with the MOSFET used in the circuit. Hence it could have resulted into some systematic error in the experiment.

4 References:

- Electronics Lab Manual (Uwe Pagel)
- http://www.faculty.jacobs-university.de/upagel/
- https://en.wikipedia.org/wiki/MOSFET

Experimental Findings: CMOS inverters

1. Voltage transfer characteristic of an inverter

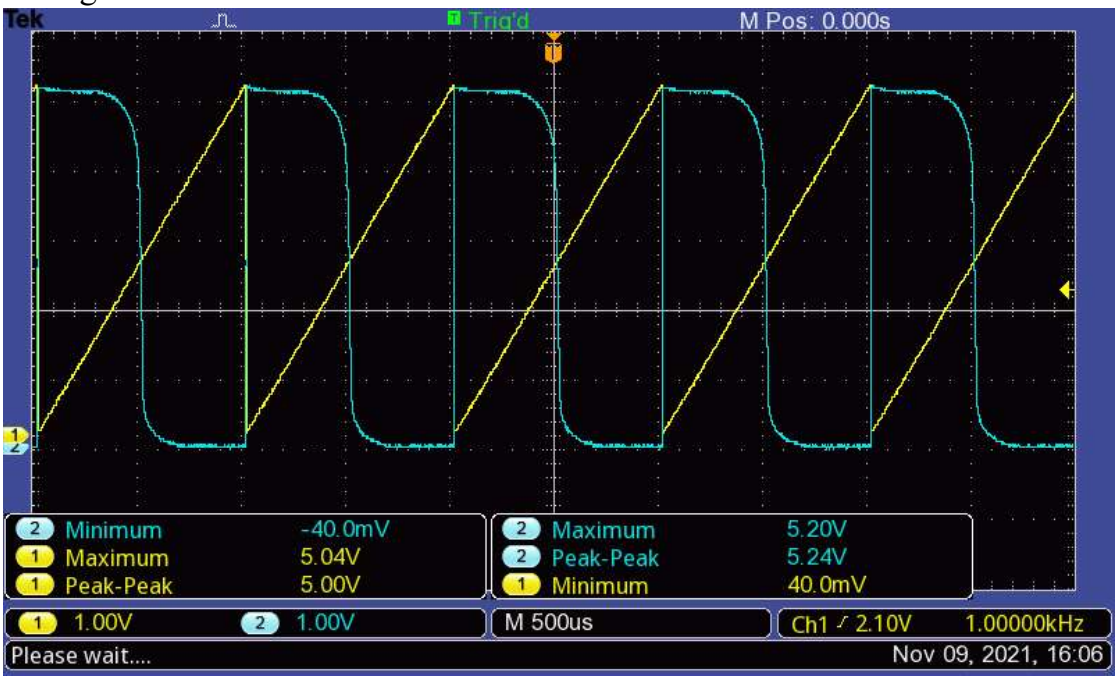


Figure 8: Output characteristic of an inverter

2. Propagation delay of an inverter
   a. For V_{DD} = 3V

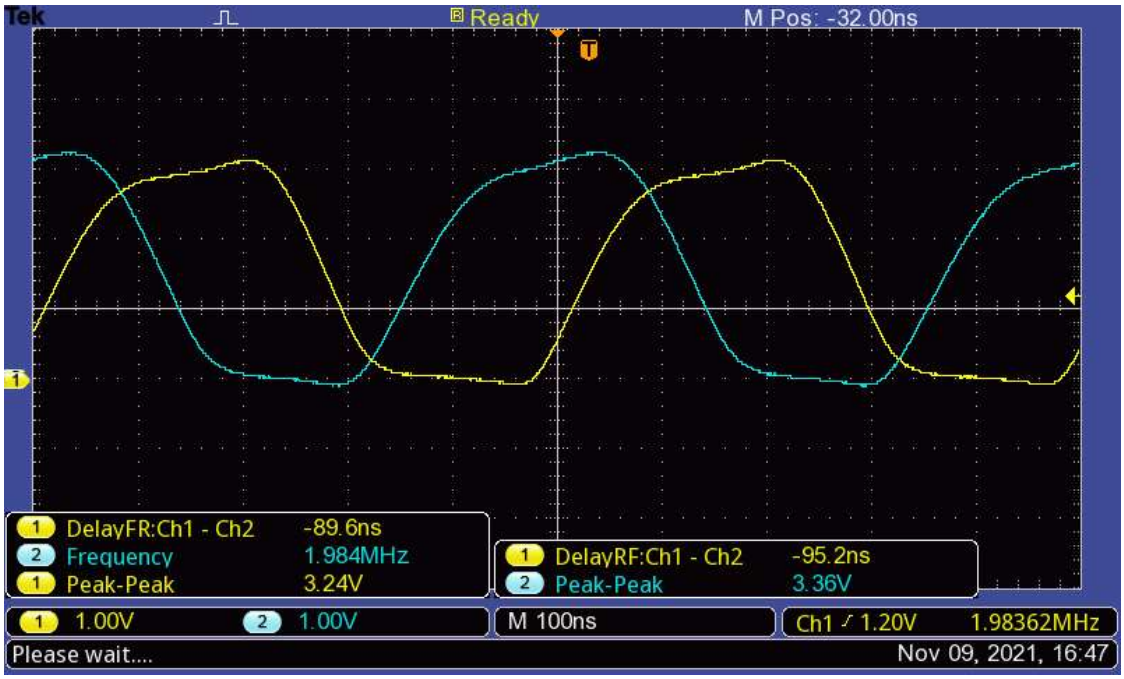


Figure 9: Propagation delay of inverter for V_{DD} = 3V

b. For V_{DD} = 5V

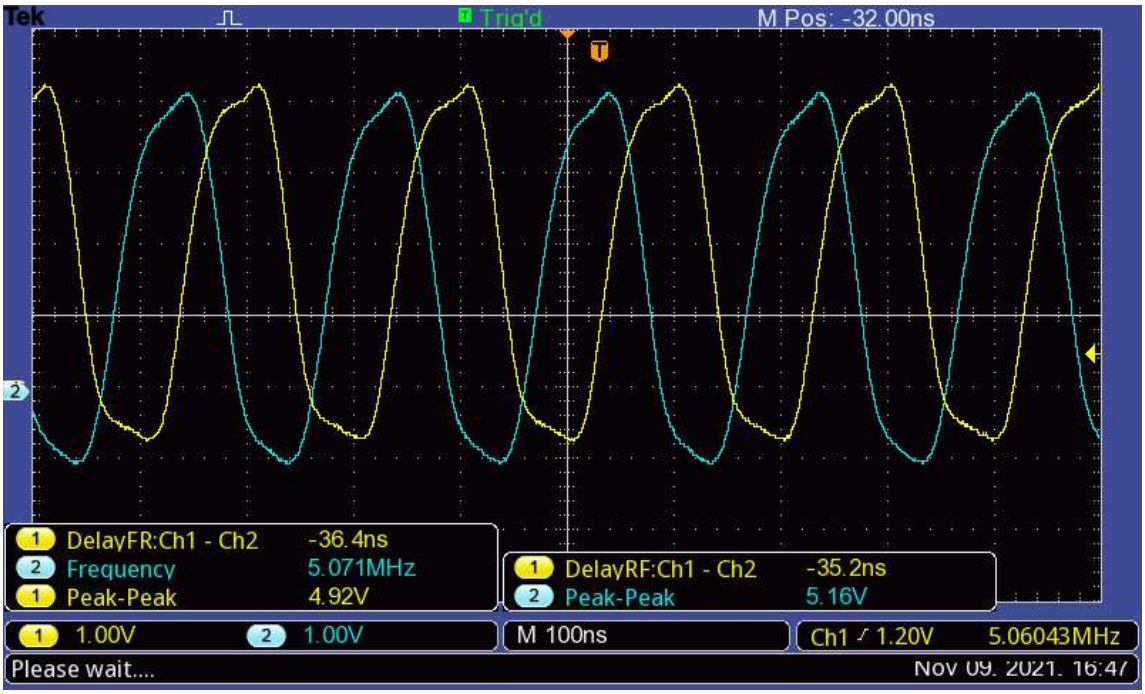


Figure 10: Propagation delay for V_{DD} = 5V

c. For V_{DD} = 7V

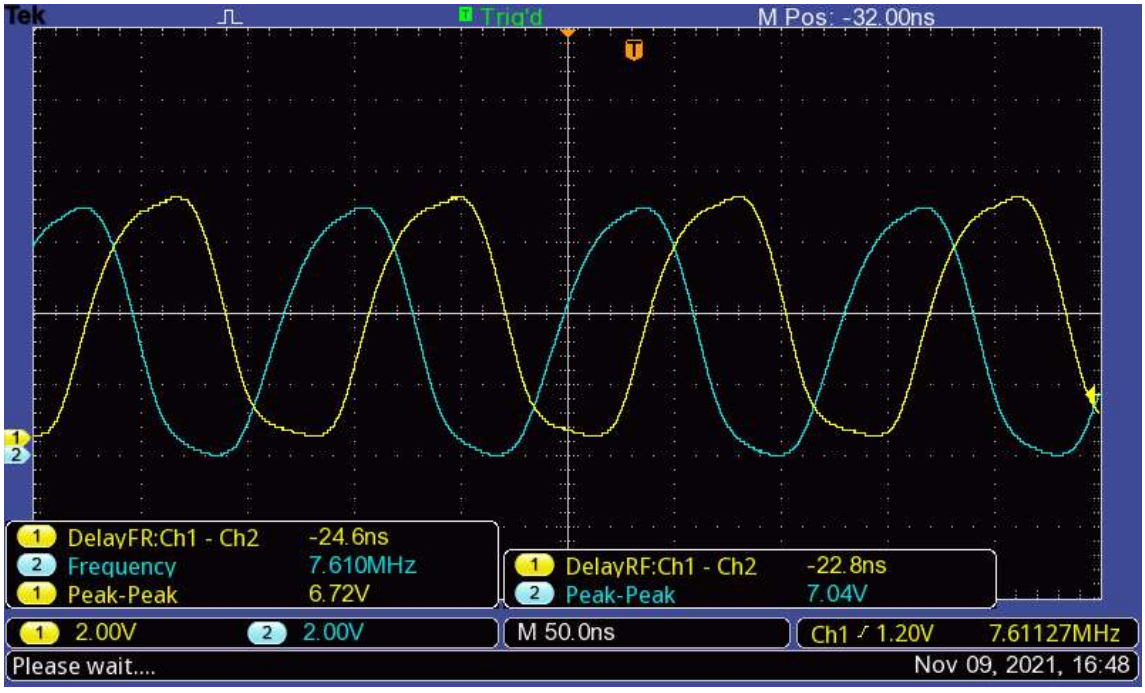


Figure 11: Propagation delay for V_{DD} = 7V

d. For V_{DD} = 9V

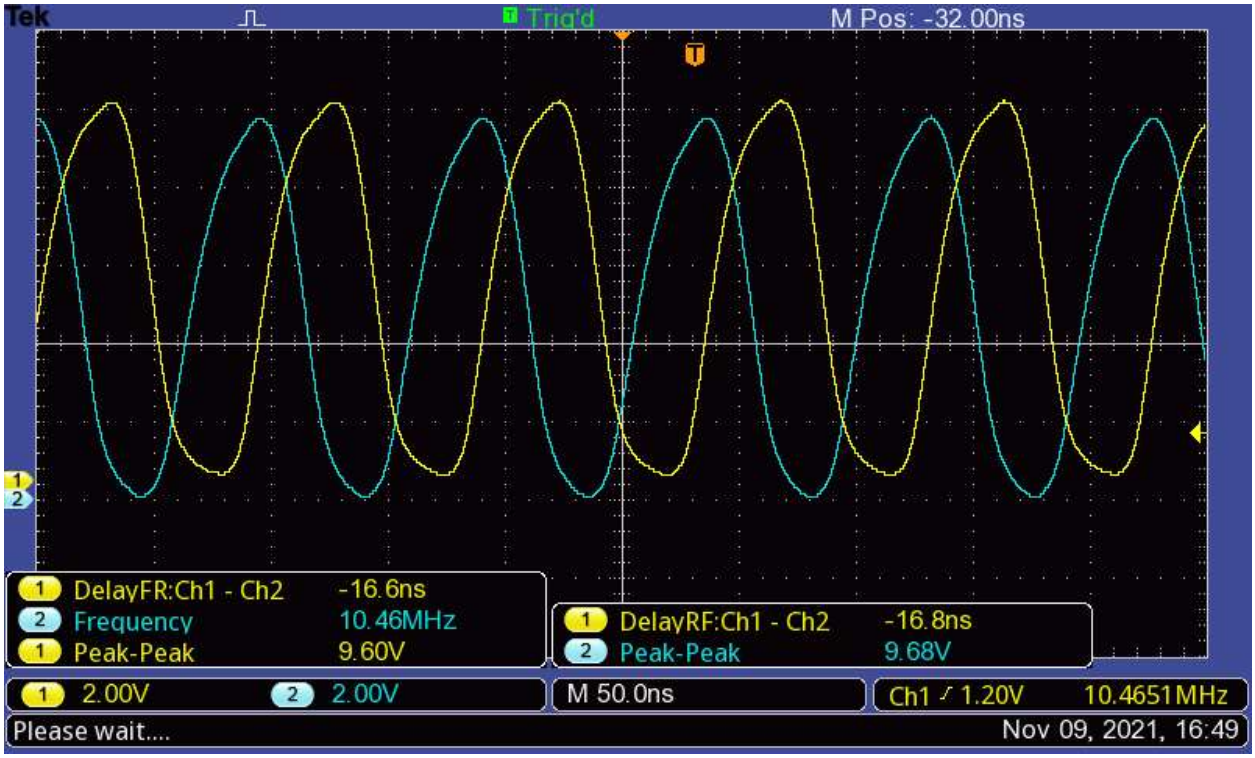


Figure 12: Propagation delay for V_{DD} = 9V