Jacobs University Bremen

CO-526-B: Electronics Lab

Fall 2021

Lab Experiment 3: Bipolar Junction Transistor

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Introduction

The objective of this experiment is to become familiar with the bipolar junction transistors (BJTs). A BJT is a three terminal semiconductor device, mainly used in analog circuits. They're used in high-speed amplifiers, for example. Three operating modes of BJTs are: active mode, cut-off mode and saturation mode. To apply as an amplifier, the BJT has to operate in active mode.

Theory

The BJT can be implemented as an NPN or a PNP transistor. In either case, the center region forms the base, while the external regions form the collector and emitter. The final structure looks as follows:

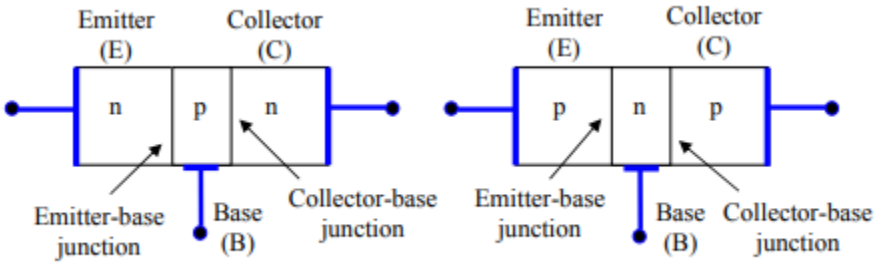


Figure: NPN and PNP BJT structures

Three ways a BJT could be configured:

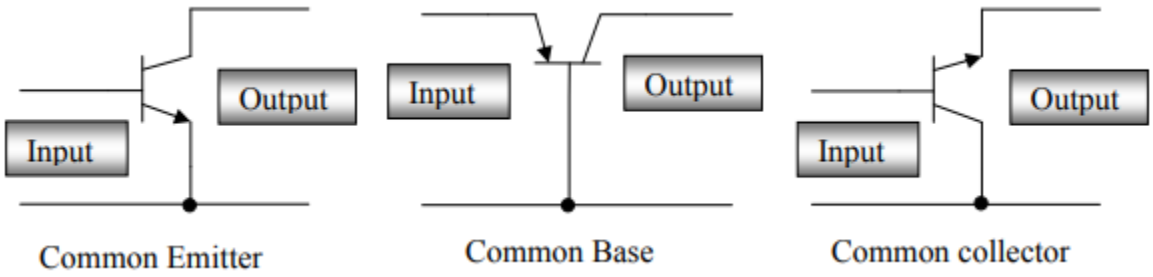


Figure: BJT configurations

The common emitter configuration can be used for voltage and current amplification. The common collector configuration can be used as an impedance matching device. The common base configuration is used for high frequency applications because the base separates the input and output, minimizing oscillations at high frequency. It has high voltage gain, low input impedance and high output impedance compared to the common collector.

Relations between terminal properties

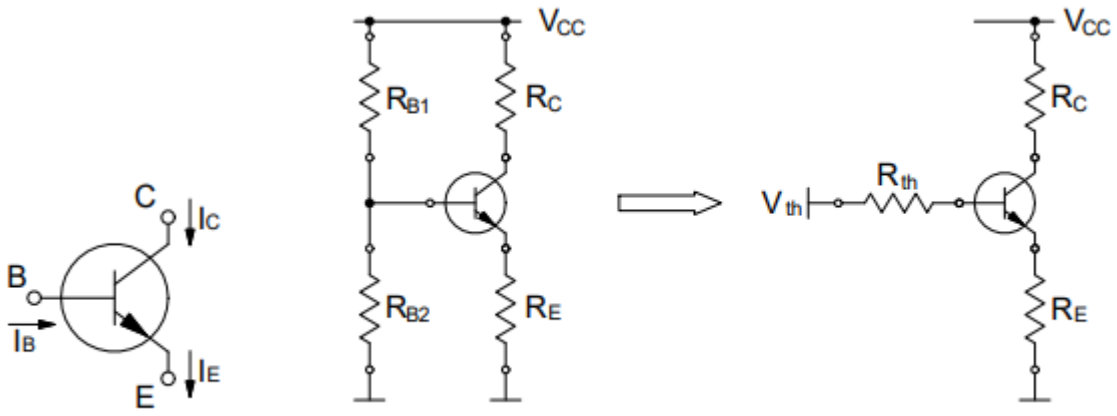


Figure: Transistor current relations and bias circuit structure

$$I_E = I_C + I_B$$

$$I_B \ll I_c$$

$$I_C \approx I_E$$

$$I_C = \beta I_B$$

$$V_{th} = V_{CC}\frac{R_{B2}}{R_{B1}+R_{B2}} \qquad R_{th} = \frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}}$$

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E = I_B(R_{th} + (\beta+1)R_E) + V_{BE}$$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E = I_C\left(R_C + \frac{R_E}{\alpha}\right) + V_{CE}$$

AC Analysis

We use the AC analysis to determine the voltage amplification (A_V), the current amplification (A_i), the input impedance (Z_i), the output impedance (Z_o) and the phase relation between the input voltage (V_i) and the output voltage (V_o).

The hybrid-π model can be used for AC analysis:

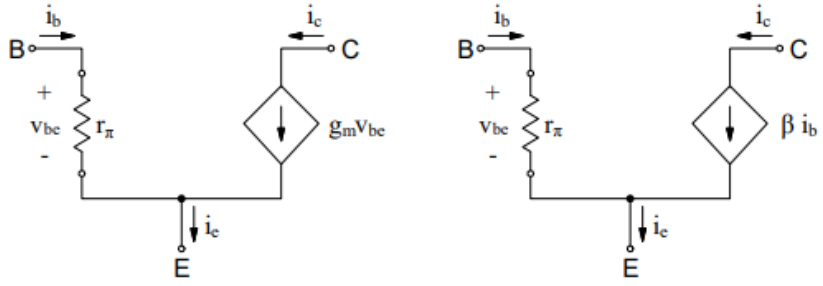


Figure: The hybrid-π model

$$g_m = \frac{I_C}{V_T}, \qquad V_T = \frac{kT}{q}, \qquad r_\pi = \frac{\beta}{g_m}$$

Prelab: BJT

Problem 1: Biasing of Bipolar Junction Transistors

Task 1

For this task we are required to analyze the following common emitter circuit:

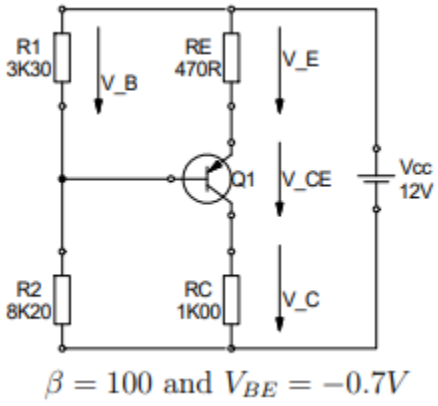


Figure: Common Emitter Circuit

In order to find the Thevenin voltage, we use the following circuit:

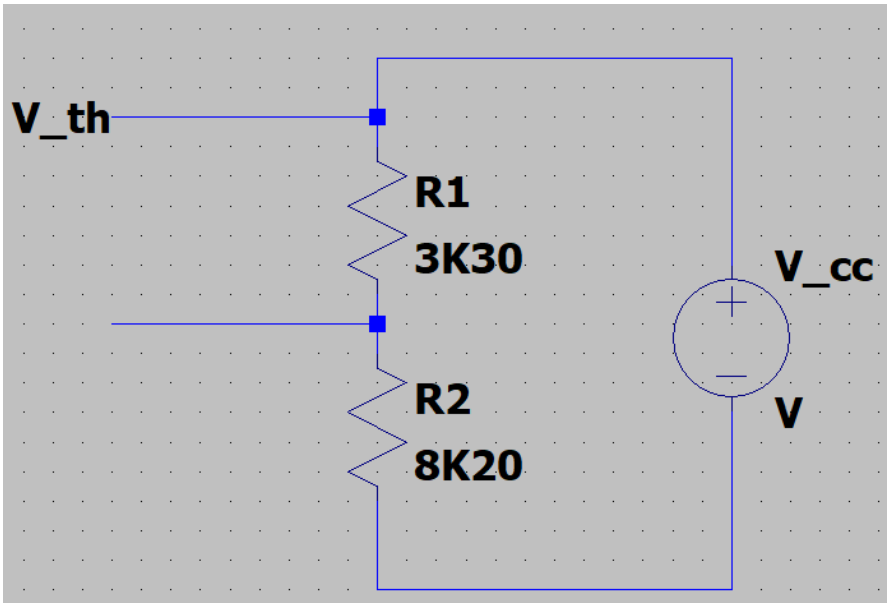


Figure: Thevenin Voltage and Resistance analysis

Use find the Thevenin resistance across the same nodes, but by suppressing the source.

We obtain the following values:

$$V_{Th} = \frac{R_1 V_{cc}}{R_1 + R_2} = \frac{3300 \times 12}{3300 + 8200} = 3.443V$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = 2353.043\Omega$$

The Thevenin equivalent looks as follows:

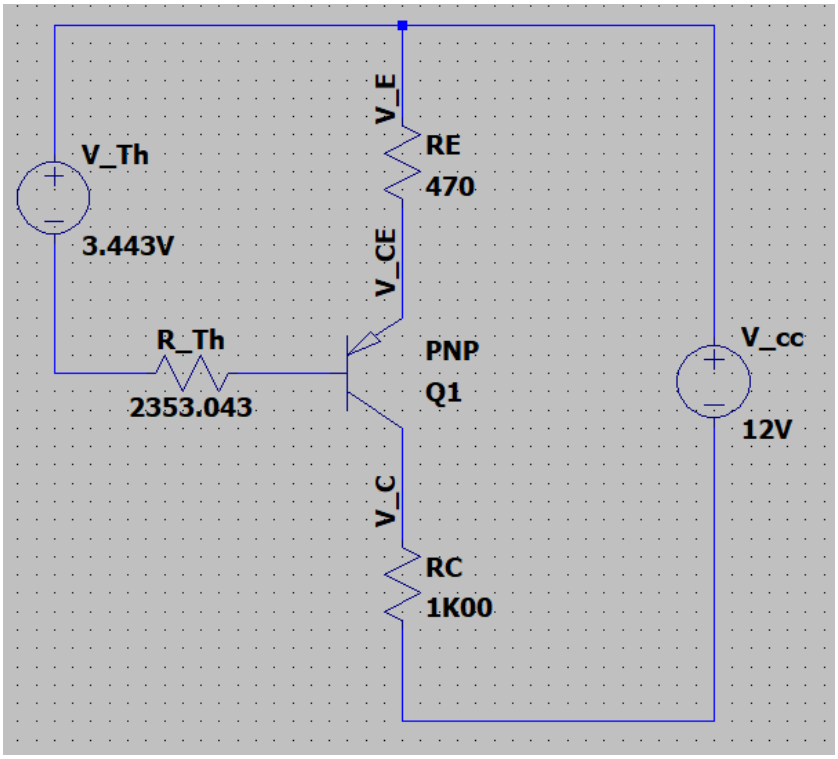


Figure: Thevenin equivalent circuit

Using the Thevenin equivalent circuit, we can obtain the terminal currents as follows:

$$-V_{Th} + V_E + V_{EB} + V_{R_{Th}} = 0$$

$$V_E + V_{EB} + V_{Th} = V_{R_{Th}}$$

$$(\beta + 1)\mathrm{I_B} R_E + V_{EB} + I_B R_{Th} = V_{Th}$$

$$I_B\big(R_{Th} + R_E(\beta + 1)\big) = V_{Th} - V_{EB}$$

$$I_B = \frac{V_{Th} - V_{EB}}{\big(R_{Th} + R_E(\beta + 1)\big)} = 5.485 \times 10^{-5} A$$

$$I_E = (\beta + 1) I_B = 5.54 \times 10^{-3} A$$

$$I_C = \beta I_B = 5.485 \times 10^{-3} A$$

$$V_E = I_E R_E = 5.54 \times 10^{-3} \times 470 = 2.604 V$$

$$V_C = I_C R_C = 5.485 \times 10^{-3} \times 1000 = 5.485 V$$

To find V_E and V_B, we use KCL:

For V_E:

$$V_E + V_{CE} + V_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - V_E - V_C = 12 - 2.604 - 5.485 = 3.911V$$

For V_B:

$$-V_B + V_E + V_{EB} = 0$$

$$V_B = 3.304V$$

Simulation circuit:

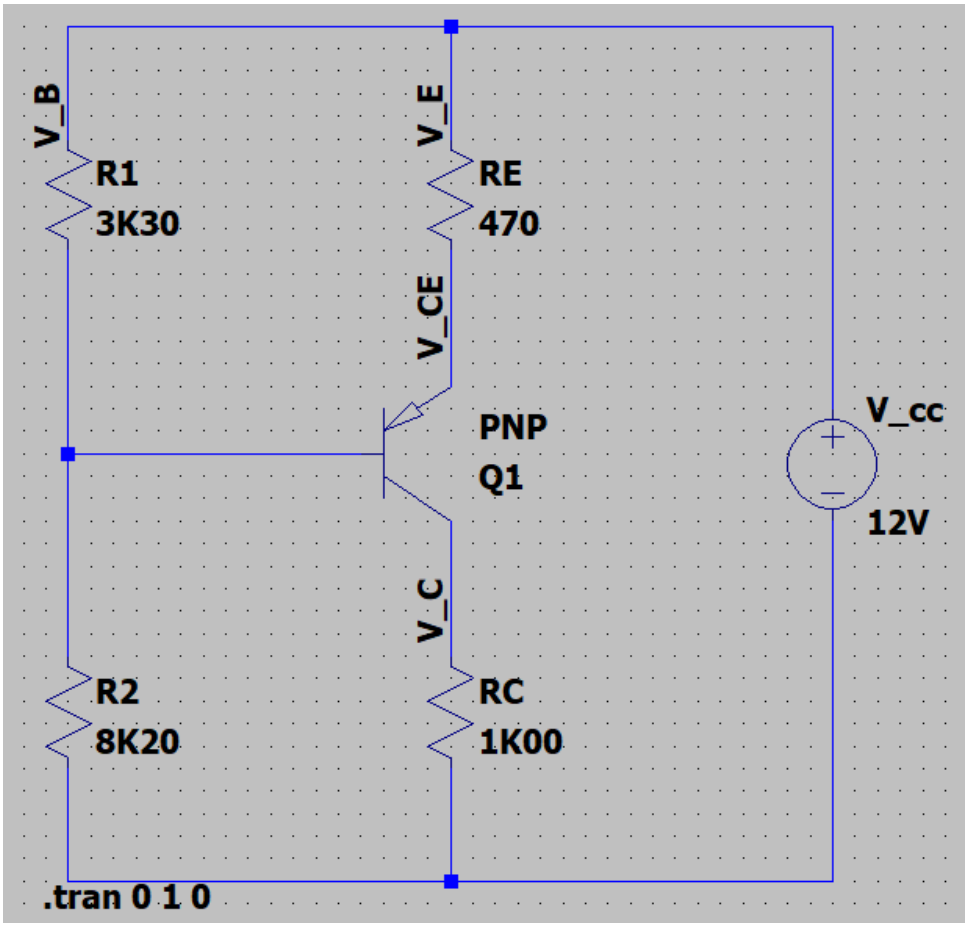


Figure: PNP Transistor circuit

Simulation values:

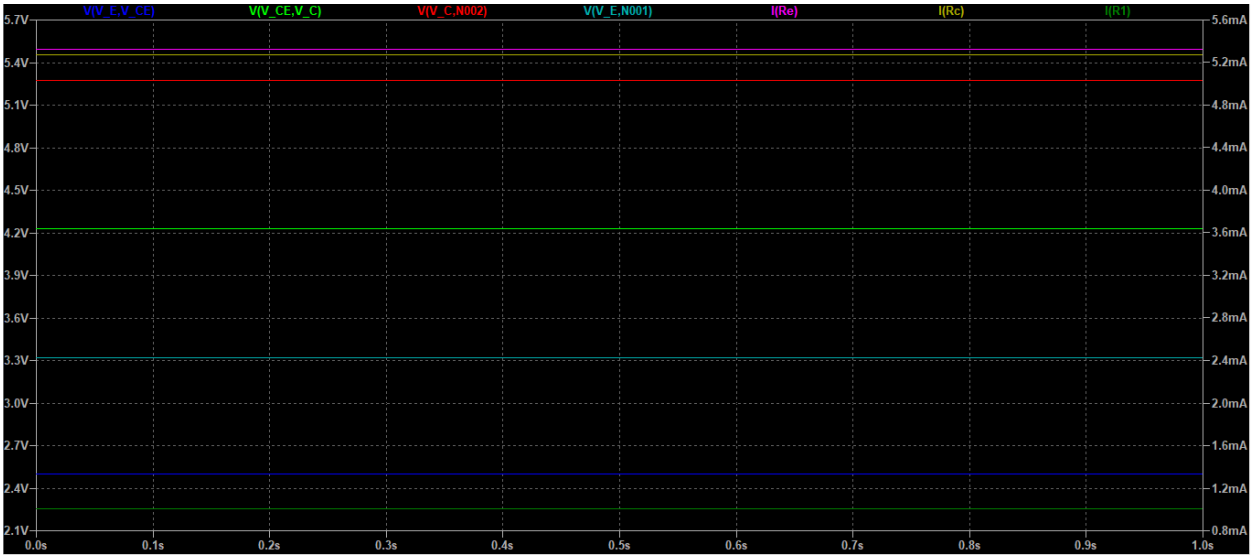


Figure: Simulation results

Task 2

We are provided the following parameters:

$$V_{CE} = 8V, I_c = 8 \times 10^{-3}A, V_{cc} = 20V, \beta = 150, V_E = 4V, R_{Th} = 0.1\beta R_E$$

$$I_E + I_B = I_C$$

$$I_C = \beta I_B => I_B = \frac{I_C}{\beta} = 5.33 \times 10^{-5}A$$

$$I_E = (\beta + 1)I_B = 8.0533 \times 10^{-3}A$$

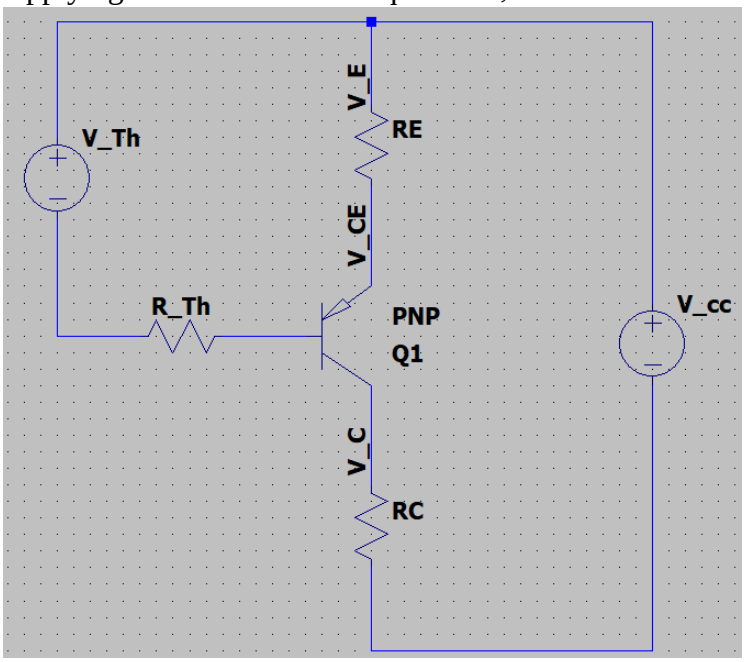
Applying KVL:

$$V_C = V_{CC} - V_{CE} - V_E = 8V$$

$$R_E = \frac{V_E}{I_E} = 496.689\ \Omega$$

$$R_C = \frac{V_C}{I_C} = 1000\ \Omega$$

Applying KVL in Thevenin equivalent, we find:



$$-V_{Th} + V_E + V_{EB} + V_{R_{Th}} = 0$$

$$V_{Th} = 5.097V$$

$$V_{Th} = \frac{R_1 V_{CC}}{R_1 + R_2} => R_2 = 2.924 \cdot R1$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} \rightarrow R_1^2 - 9999R_1 = 0$$

$$R_1 = 0 \; or \; R_1 = 9999\Omega \approx 10k\Omega$$

$$R_2 = 0 \; or \; R_2 = 29235.63\Omega$$

Bias cannot be zero, therefore:

$$R_1 \approx 10k\Omega \; and \; R_2 \approx 29.24k\Omega$$

Figure: Thevenin Equivalent circuit

The final circuit looks as follows:

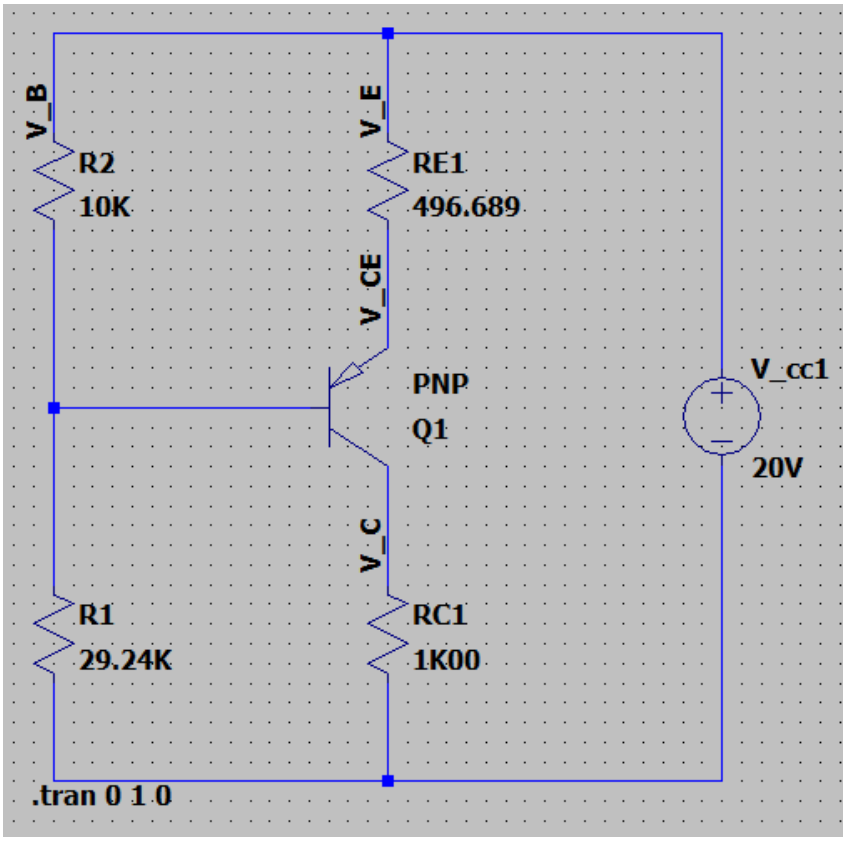


Figure: Transistor circuit for Task 2

Problem 2: Constant Current Source

From Datasheet, we see that V_Z = 4.7V, Iz = 20mA = 0.02A.

The circuit diagram is provided below:

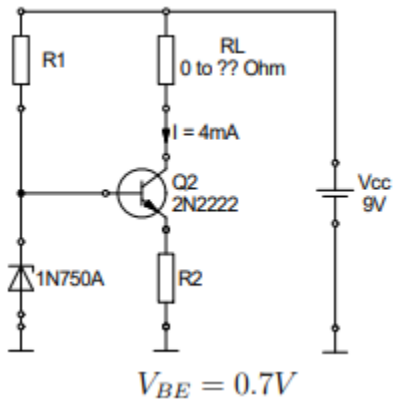


Figure: Transistor circuit with Zener diode

Using KVL around R1:

$$V_{R1} + V_Z = V_{CC}$$

$$V_{R1} = V_{CC} - V_Z = 4.3V$$

We assume that negligible current flows through I_B.

$$R1 = \frac{V_{R1}}{I_Z} = \frac{4.3}{0.02} = 215\Omega$$

Using KVL around R2:

$$-V_Z + V_{BE} + V_{R2} = 0$$

$$V_{R2} = V_Z - V_{BE} = 4V$$

$$I_E \approx I_C = 4mA$$

$$R2 = \frac{V_{R2}}{I_E} = 10^3\Omega = 1k\Omega$$

Task 3

To find the maximum value of R_L, we start with a KVL:

$$-V_{CC} + V_C + V_{CE} + V_E = 0$$

$$V_C = V_{CC} - V_{CE} - V_E$$

$$R_L = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{9 - V_{CE} - 4}{4 \times 10^{-3}} = 250(5 - V_{CE})$$

To ensure active region, V_{BE} must be forward biased and V_{BC} must be reverse biased. We know V_{BE} =0.7V, which is greater than zero. For V_{BC} to be reverse biased, V_{CB} must be greater than or equal to zero.

$$V_{CB} \geq 0 => V_{CE} - V_{BE} \geq 0 => V_{CE} \geq V_{BE} => V_{CE} \geq 0.7V$$

The lowest value for V_{CE} provides us the highest value for R_L.

$$R_L = 250(5 - 0.7) = 1075V$$

Task 4

LTSpice implementation:

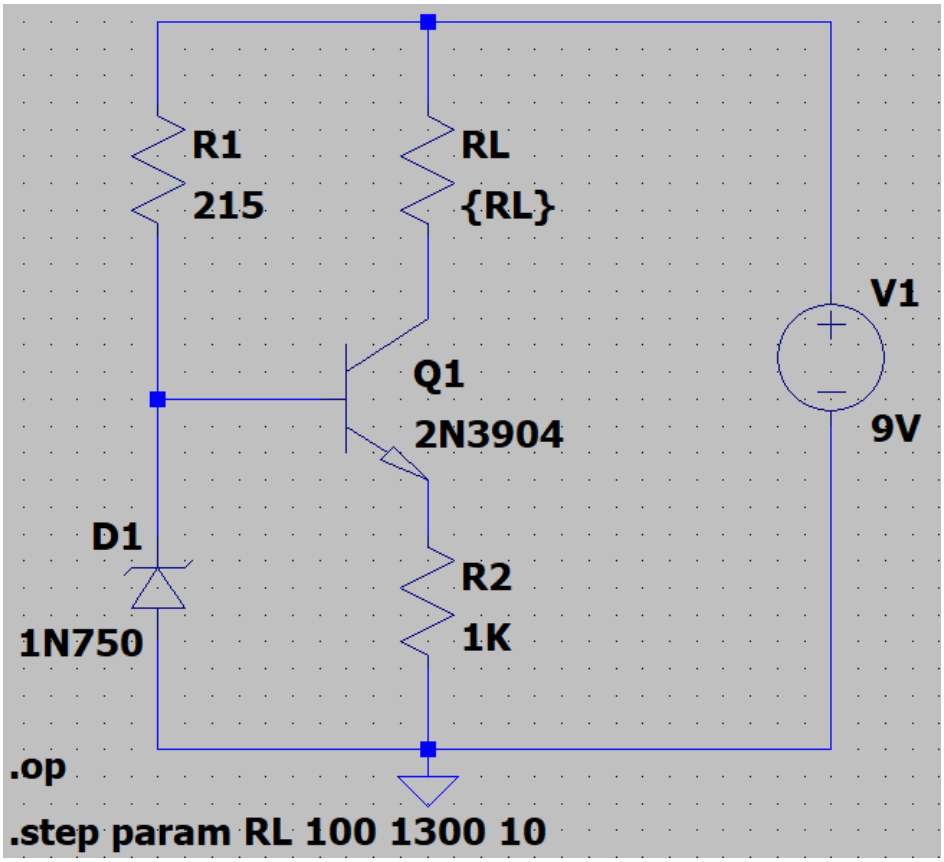


Figure: Transistor circuit simulation with Zener diode for biasing

Simulation results:

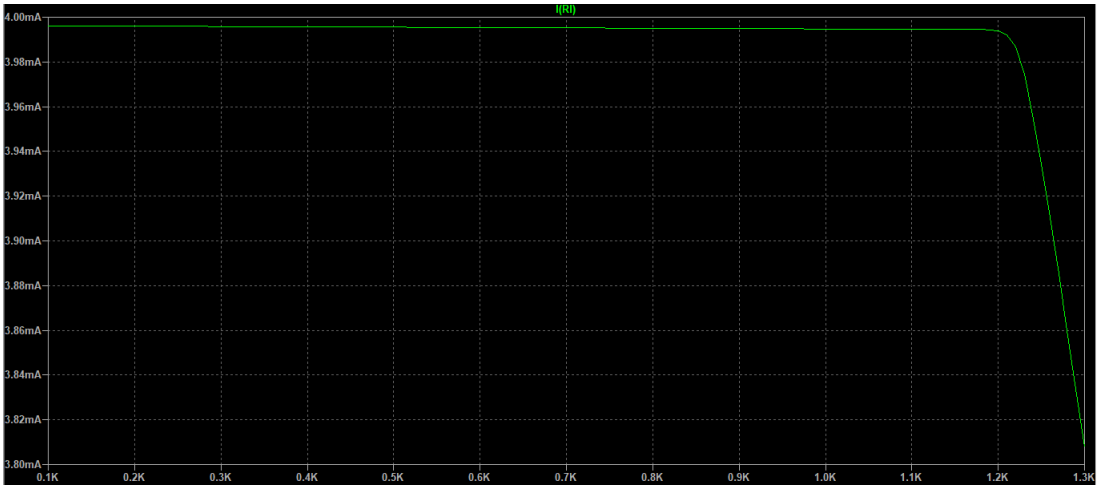


Figure: Simulation results for maximum R_L

R_L measurements at turning points:

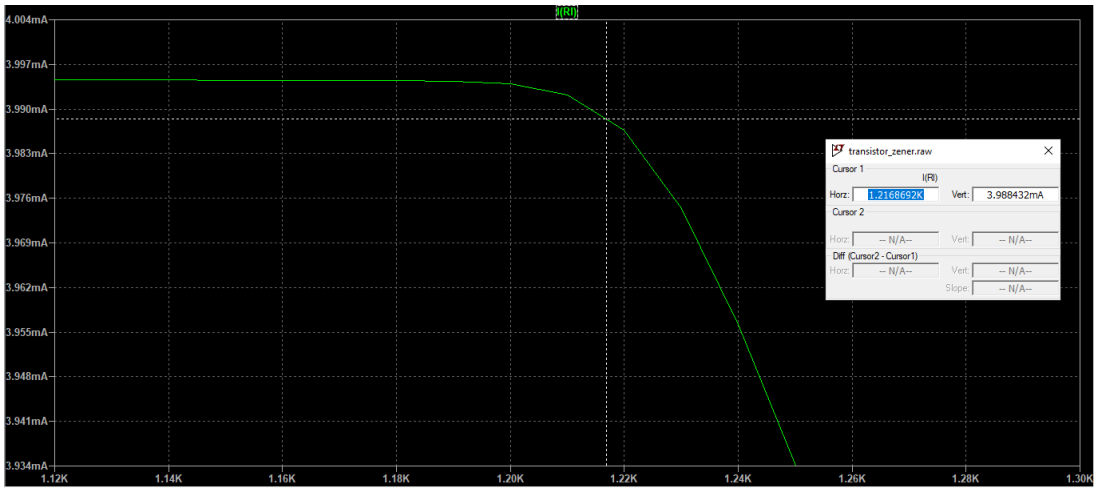


Figure: Measurement for R_L

Based on the simulation, we find that $R_L = 1.217K\Omega$.

According to the datasheet, V_{CE} of 2N2222 transistor is smaller than the value we used for our theoretical calculations. As a result, the value we found for R_L is higher in the simulation.

Task 5

The Zener diode is used as a voltage stabilizer in this circuit. The constant voltage across the Zener diode is 4.7V. As a result, it maintains a constant voltage across R1, which means I_{R1} = constant. Considering V_{BE} remains constant, we can conclude that V_E across R2 also remains constant. Consequently, I_E is also constant, and since I_B is negligible, $I_C = I_E$ = constant for varying R_L as long as we do not cross the threshold.

Problem 3: Amplifier circuit

Task 1

For this task, we are required to build the following circuit on LTSpice:

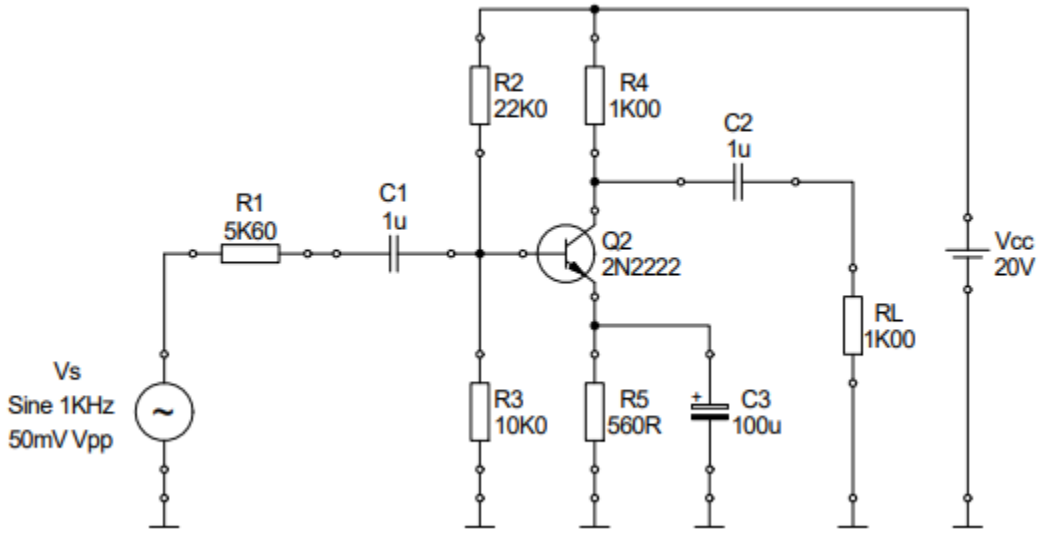


Figure: Amplifier circuit

The implementation is provided below:

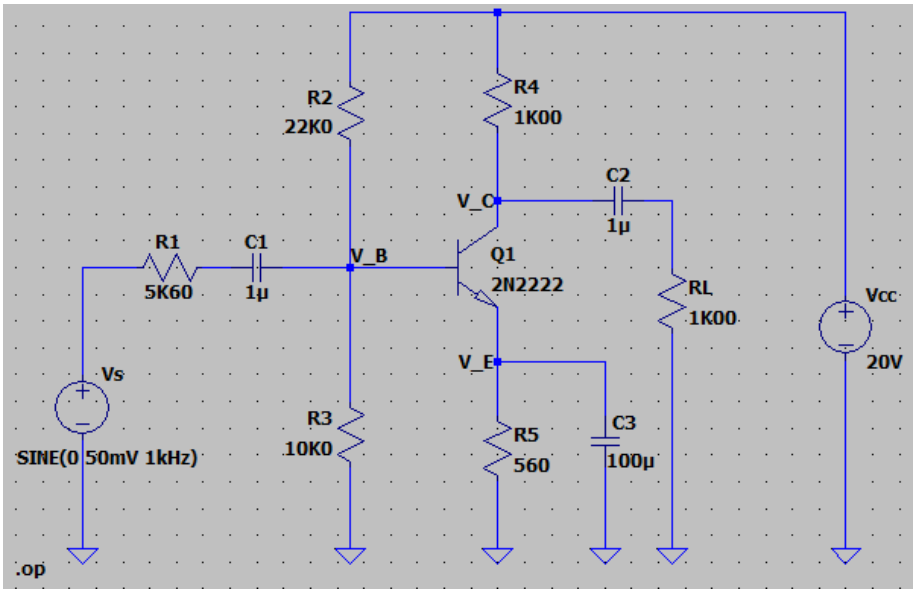
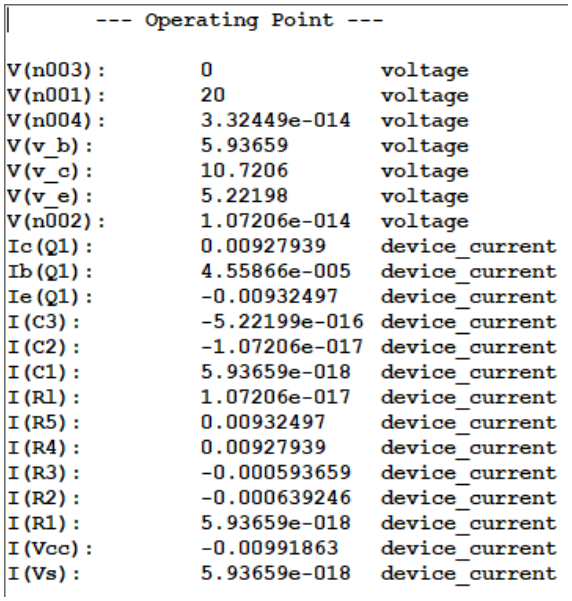


Figure: LTSpice implementation of amplifier circuit

Task 2

The results of DC operation point analysis are provided below:



```
--- Operating Point ---

V(n003):        0              voltage
V(n001):        20             voltage
V(n004):        3.32449e-014   voltage
V(v_b):         5.93659        voltage
V(v_c):         10.7206        voltage
V(v_e):         5.22198        voltage
V(n002):        1.07206e-014   voltage
Ic(Q1):         0.00927939     device_current
Ib(Q1):         4.55866e-005   device_current
Ie(Q1):         -0.00932497    device_current
I(C3):          -5.22199e-016  device_current
I(C2):          -1.07206e-017  device_current
I(C1):          5.93659e-018   device_current
I(Rl):          1.07206e-017   device_current
I(R5):          0.00932497     device_current
I(R4):          0.00927939     device_current
I(R3):          -0.000593659   device_current
I(R2):          -0.000639246   device_current
I(R1):          5.93659e-018   device_current
I(Vcc):         -0.00991863    device_current
I(Vs):          5.93659e-018   device_current
```

Figure: Operating Point Analysis in LTSpice

Based on the results, we know the following:

Parameter	Value
V_B	5.93659V
V_E	5.22198V
V_C	10.7206V
V_{BE}	0.71461V
V_{CE}	5.49862V
I_C	0.00927939A
I_B	$4.559 \times 10^{-5} A$

Task 3

The results of transient analysis are provided below:

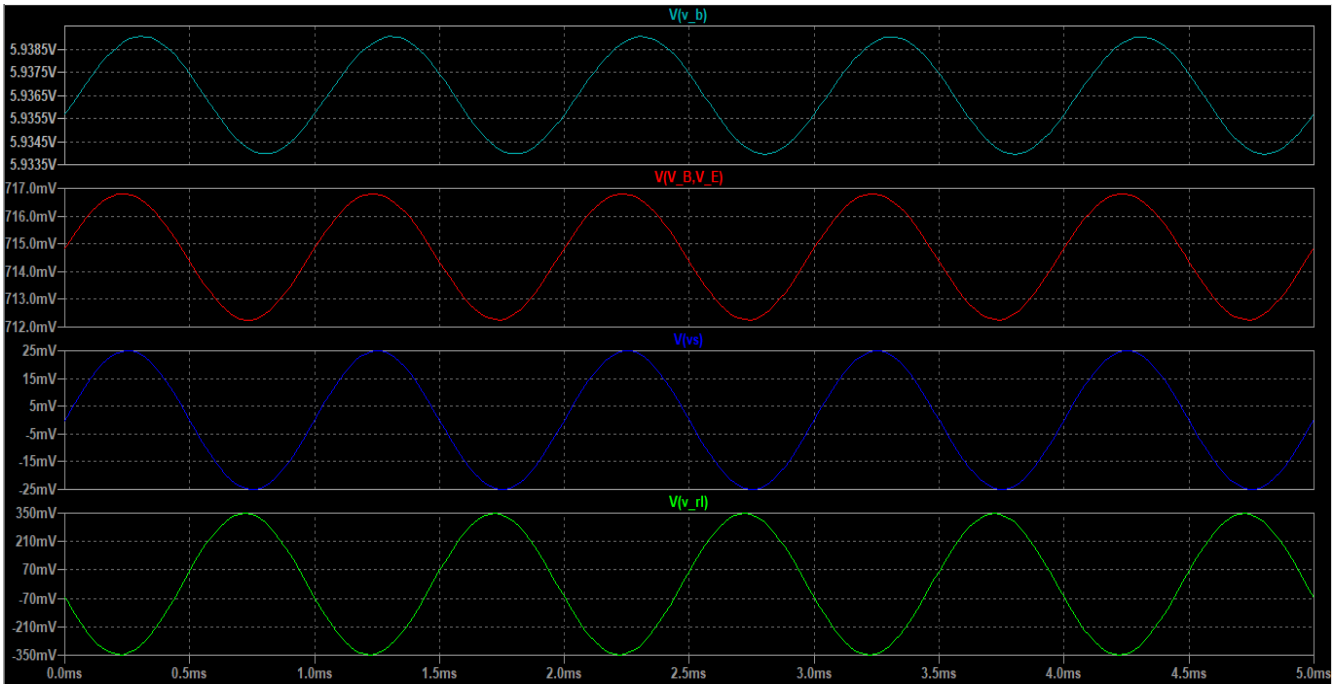


Figure: V_B, V_{BE}, V_S, V_{RL} simulation results

In order to calculate the gain, we use the cursors to obtain the peak-to-peak value of the output, and divide it by the peak-to-peak value of the input.

$$Gain = \frac{V_{RL}}{V_S} = \frac{695.071mV}{50mV} = 13.901$$

Task 4

For this task, we determine the quality of the amplified signal at R_L by using the .step command to vary Vs by 10 mVpp, 20 mVpp, 50mVpp and 200 mVpp.

The results are provided below:

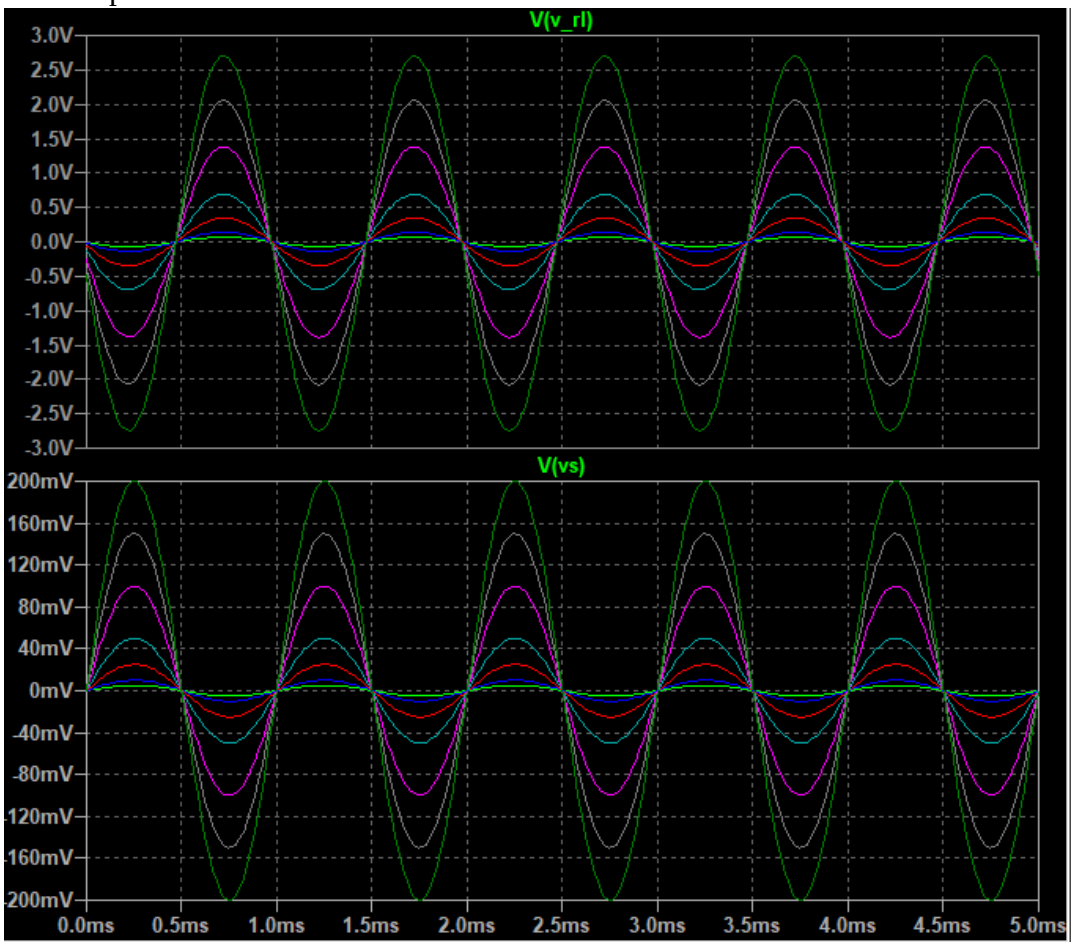


Figure: Input and amplified output

From the plots, we see that the output signal is an amplified version of the input signal with the same frequency and a larger amplitude.

When looked at in the time domain, we do not notice any visible distortions.

Now that we can see the input and output signals, we are ready to analyze their spectrum.

The FFT of the input is provided below:

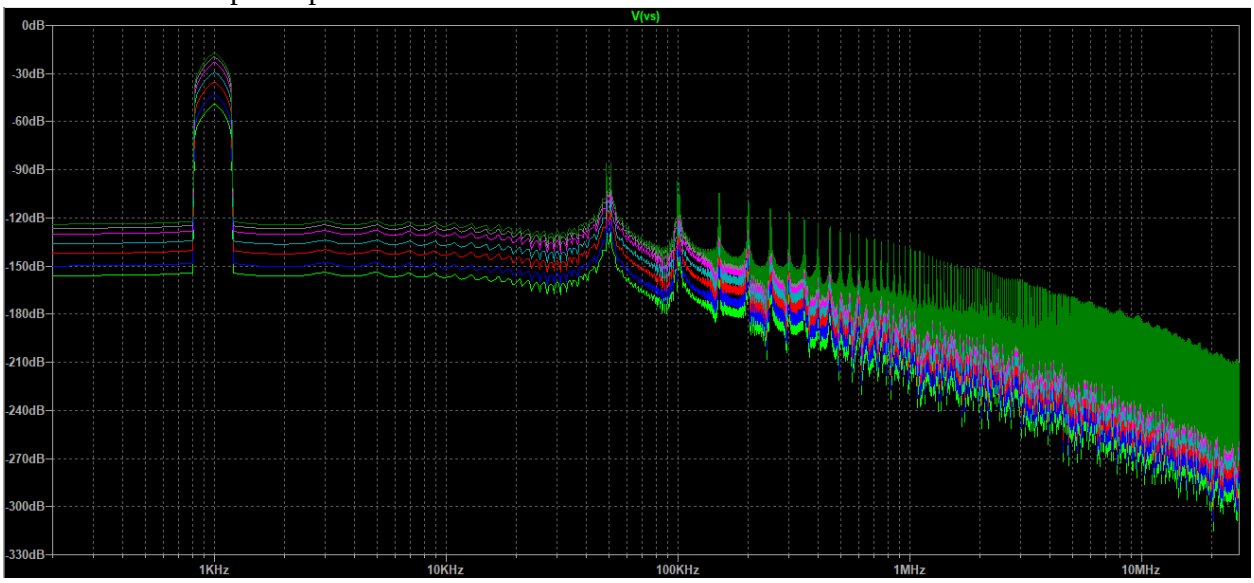


Figure: Spectrum of input signal

The FFT of the output is provided below:

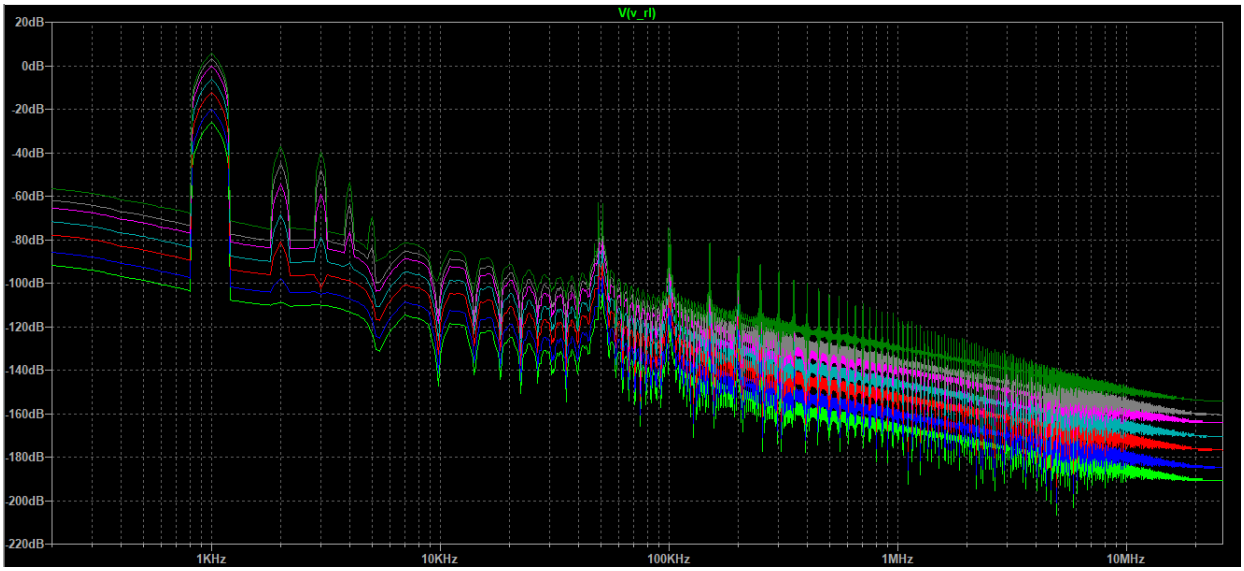


Figure: Spectrum of output signal

When we analyze the input spectra, we can see that they all contain a single peak at 1kHz, which is the frequency of our input signal. However, from the spectra of the output signal, we see that the number of peaks increases with increasing amplitude of the input/output signals, whereas there should be only one amplitude at 1kHz, considering that in the ideal case the output signal is only an amplified version of the input. As the result, the rest of the peaks are proof of distortion.

Task 5

After modifications for this task, the circuit looks as follows:

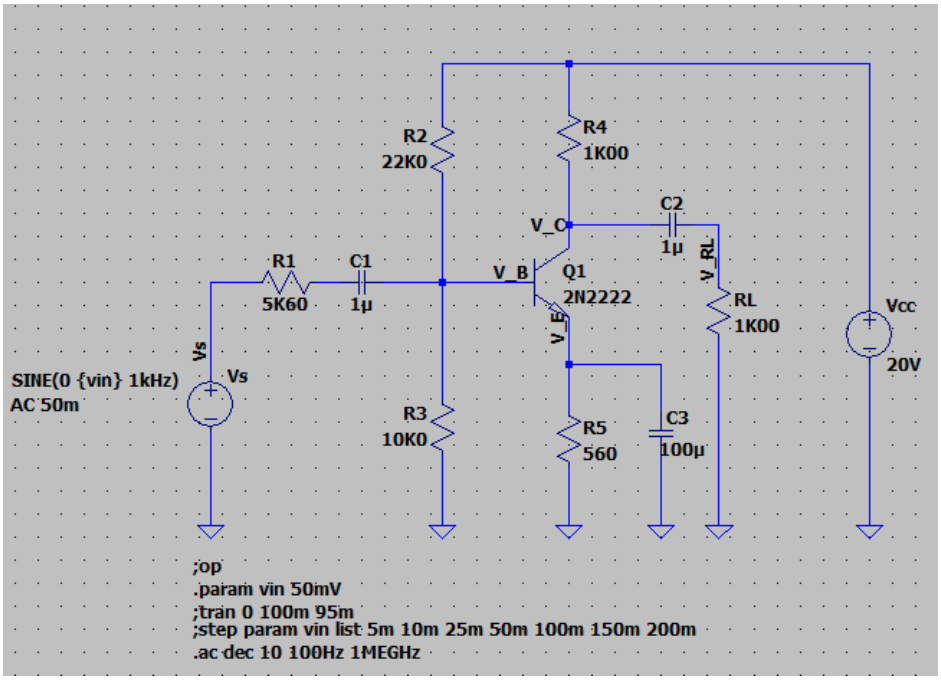


Figure: Transistor circuit for AC Analysis

The simulation is provided below:

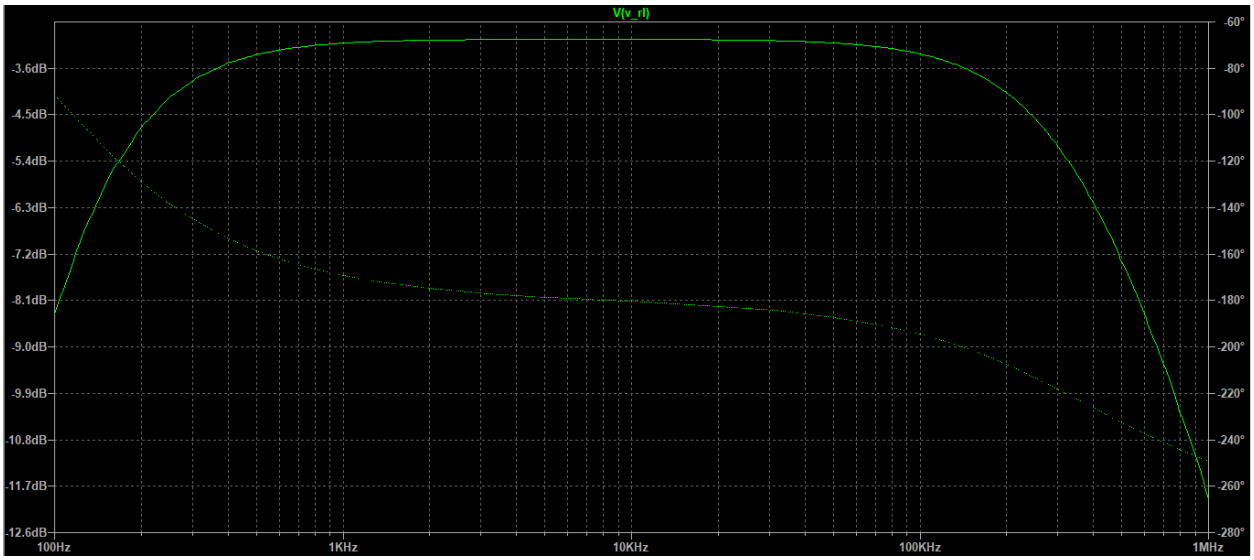


Figure: AC Analysis simulation

Task 6

Using the measure function, we obtain the following results:

SPICE Error Log: C:\Users\hp\Documents\LTspiceXVII\amplifier_circuit.log

```
Circuit: * C:\Users\hp\Documents\LTspiceXVII\amplifier_circuit.asc

Direct Newton iteration for .op point succeeded.

max_val: MAX(mag(v(v_rl)))=(-3.03794dB,0°) FROM 100 TO 1e+006
bw=384725 FROM 145.154 TO 384870


Date: Thu Nov 25 23:19:41 2021
Total elapsed time: 0.044 seconds.

tnom = 27
temp = 27
method = trap
totiter = 4
traniter = 0
tranpoints = 0
accept = 0
rejected = 0
matrix size = 12
fillins = 0
solver = Normal
Matrix Compiler1:      36 opcodes
Matrix Compiler2: 920 bytes object code size
```

Figure: Spice Error Log

From the log, we see that out results are as follows:

$$Lower\ f_{-3dB} = 145.154\ Hz$$

$$Upper\ f_{-3dB} = 384870\ Hz$$

$$B = 384724.846\ Hz$$

Execution: BJT

Problem 1: Determine Type and Pin Assignment of Bipolar Transistors

Using the following procedure, we determined the type of bipolar junction transistor and identify the three terminals of the BJT, based on the bottom view of the transistor:

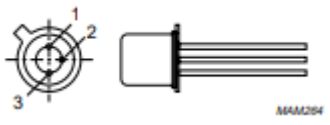


Figure: Bottom view of transistor

Task 1

The first task was to find the base terminal. We set the multimeter to diode testing function and measured and recorded the values between every combination of two terminals. The results are tabulated as follows:

Multimeter Leads connected to BJT		Diode Check value (reading or .0L)
+Terminal	GND terminal	_
1	2	.0L
2	1	0.74
1	3	.0L
3	1	.0L
2	3	0.74
3	2	.0L

Task 2

For this task, we connected the common lead of the multimeter to the base terminal and the positive lead to each one of the other two terminals one by one. Then, we observed the reading. We expected the reading to be either '.0L' or a diode forward voltage drop for both cases. Since we found an overload, we concluded that the transistor is an NPN transistor.

Task 3

In this task, we tried to determine the emitter and collector terminals. We connected the multimeter to the base terminal in a way so that we could see the diode forward voltage drop to each of the other pins. Then, we recorded the voltages we measured between the base and each pin. We expected the lower of the two readings to indicate the base collector junction, and the remaining one to be the base emitter junction. We obtained the following results:

Emitter Terminal	1	higher	0.7422
Collector Terminal	3	lower	0.7400

Based on the data, the transistor type and terminal numbers can be obtained as follows:

Transistor type	NPN
Base Terminal	2
Emitter Terminal	1
Collector Terminal	3

Problem 2: Operating Point of BJTs

In this section, we checked if the BJT is correctly biased to work in the active mode of operation.

Task 1

For this task, we assembled the circuit in the dashed area:

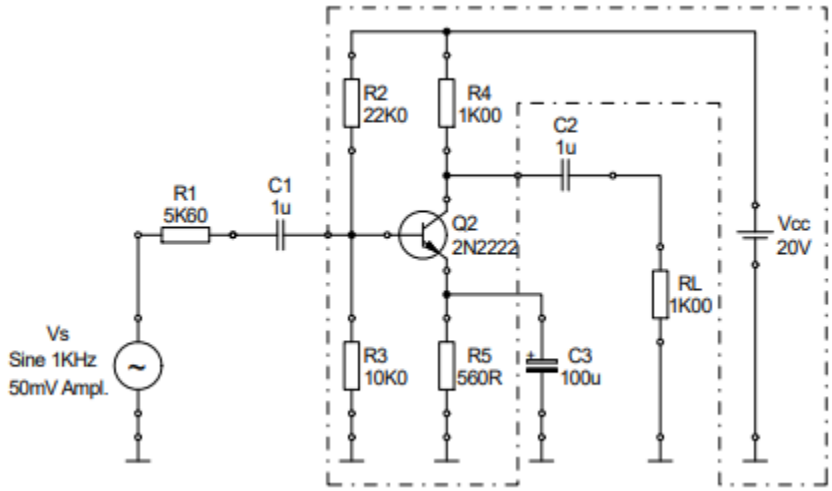


Figure: Amplifier Circuit

Task 2

We then switched on the power supply, and used a multimeter to measure and record the following voltages:

Parameter	Value/V
V_{CC}	20.03
V_B	5.954
V_{BE}	0.6543
V_C	9.413
V_{CE}	5.293
V_E	5.31

Problem 3: Common Emitter Circuit

On this section, we observed the BJT amplification of small signals when it is correctly biased to work in active mode of operation.

Task 1

For this task, we assembled the following circuit completely:

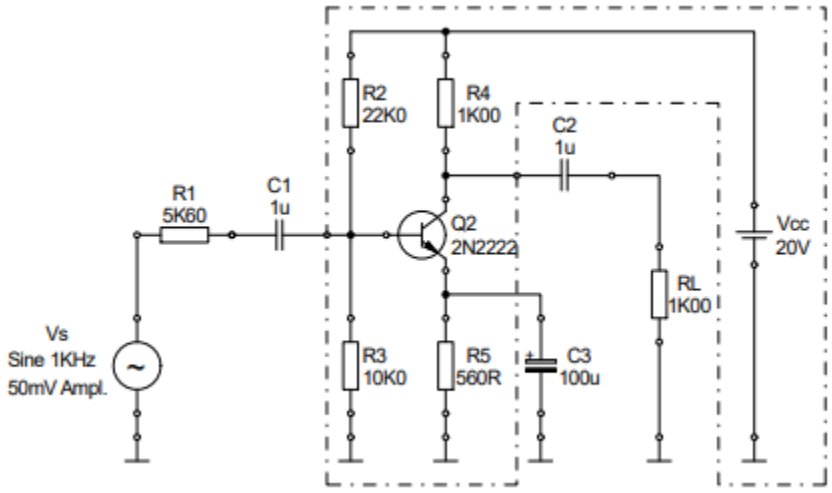


Figure: Amplifier Circuit

We connected the oscilloscope to V_S and over R_L. We started with an input signal of 50mVpp and f = 1 KHz.

Task 2

The results and measurements are provided below:

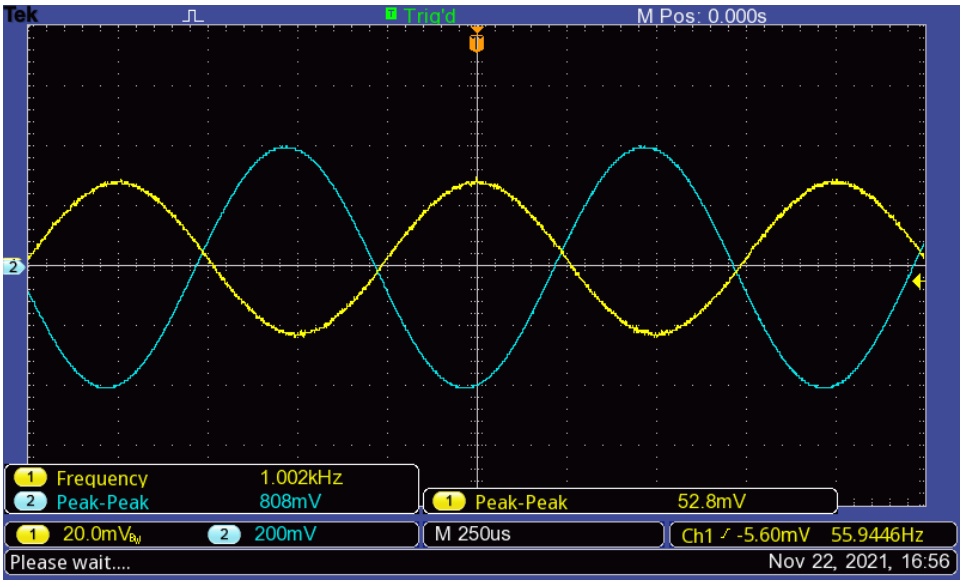


Figure: Common Emitter Circuit input and output signals with measurements. Measurements include V_S, f and V_{RL}.

The spectrum of the above output across V_{RL} is provided below:

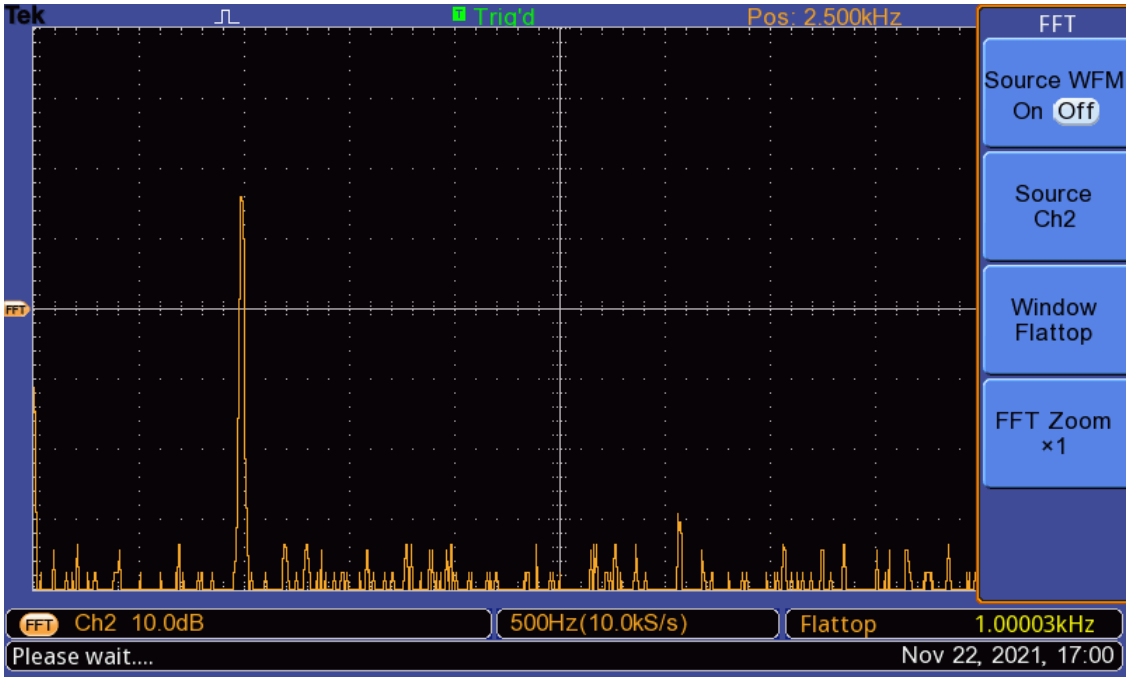


Figure: Spectrum of the output across V_{RL}

Task 3

For this task, we first repeated the measurements with V_S = 100 mVpp. We obtained the following results:

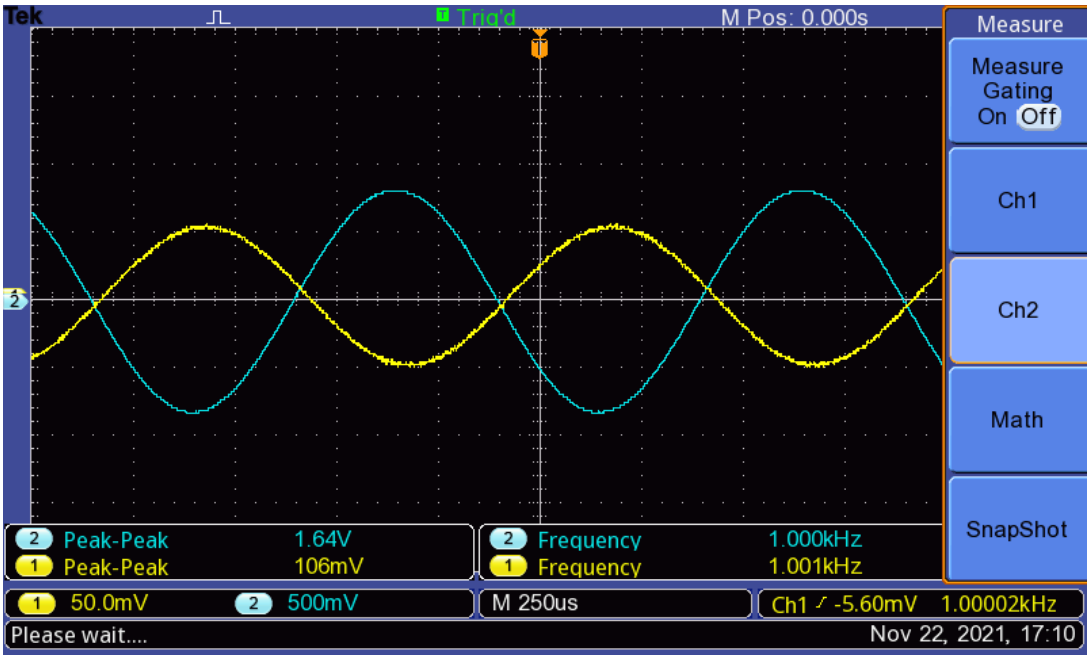


Figure: Common Emitter Circuit input and output signals with measurements. Measurements include V_S, f and V_{RL}.

The spectrum of the above output across V_{RL} is provided below:

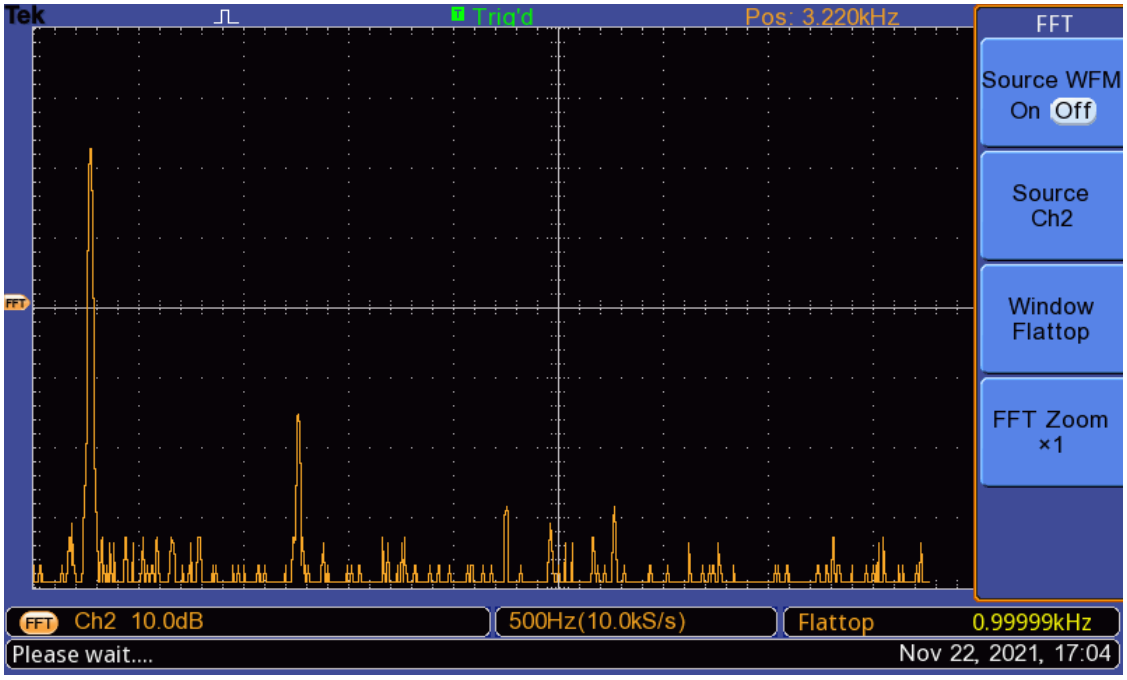


Figure: Spectrum of the output across V_{RL}

We then repeated the same experiment for V_S = 200 mVpp. The results have been provided below:

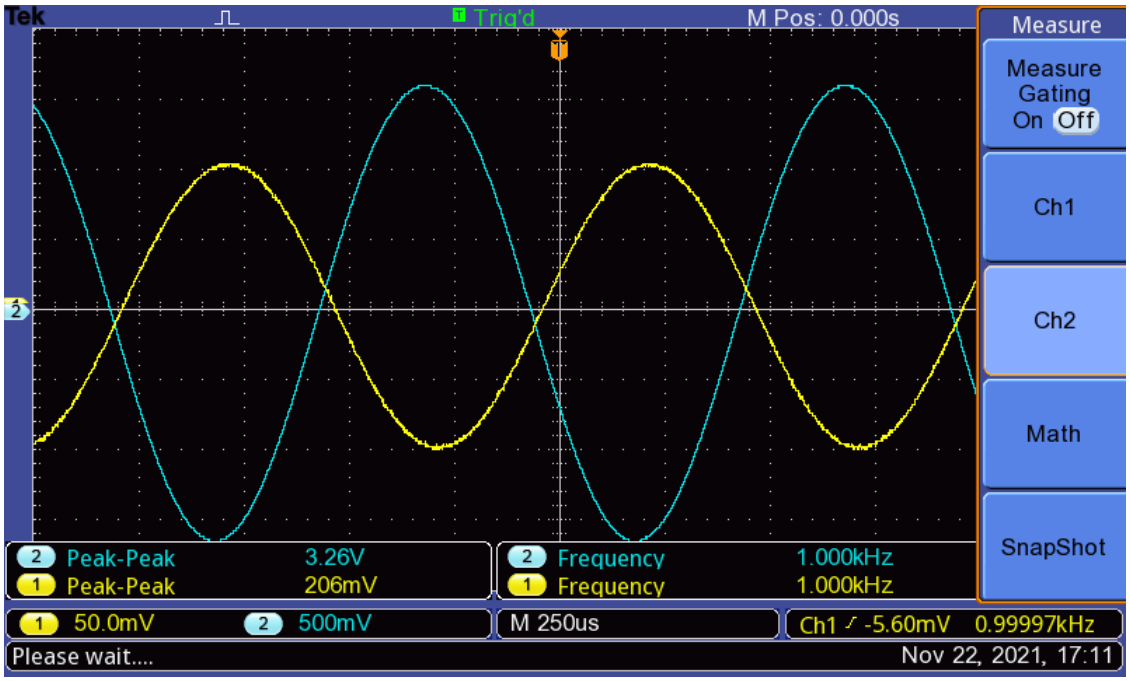


Figure: Common Emitter Circuit input and output signals with measurements. Measurements include V_S, f and V_{RL}.

The spectrum of the above output across V_{RL} is provided below:

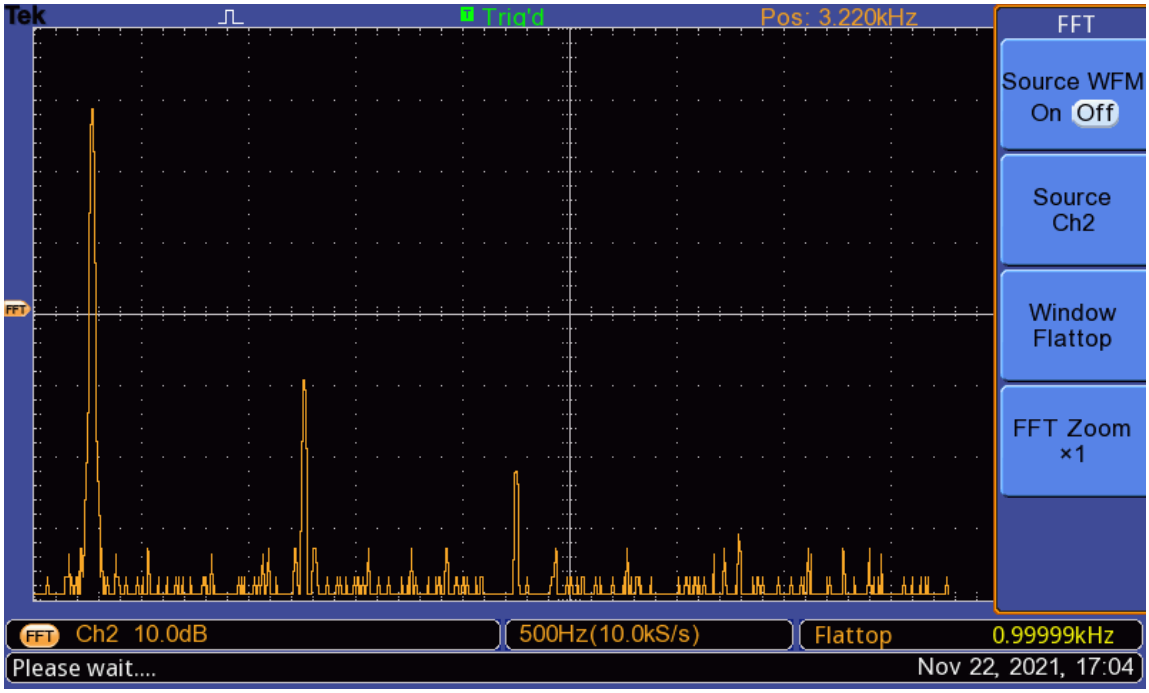


Figure: Spectrum of the output across V_{RL}

Problem 4: Bandwidth of Amplifier Circuit

In this section, we determined the bandwidth of the BJT amplifier circuit and observed how the voltage gain of a BJT is affected with the changing frequency of the input signal.

Task 1

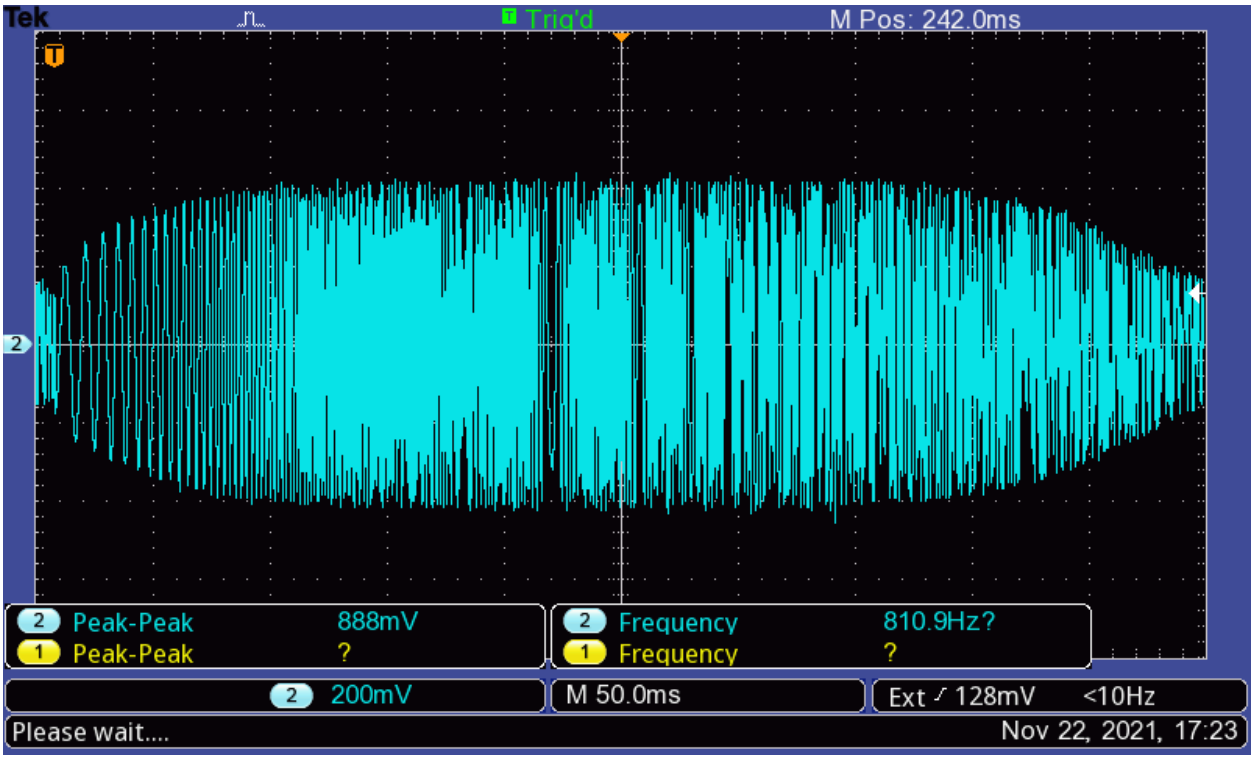
Using V_S = 50mV, we enabled the sweep mode of the function generator for the following settings:

1: START F : 100 Hz
2: STOP F : 1 MHz
3: SWP TIME : 500 ms
4: SWP MODE : logarithmic

We used the SYNC output of the generator as the trigger source of the oscilloscope.

Task 2

We then adjusted the oscilloscope to observe the full sweep of the output signal. The results are provided below:



Task 3

For this task, we disabled the sweep mode of the function generator. Then, without changing the amplitude of V_S, we manually change the frequency of the function generator to obtain the lower and upper -3dB cut-of frequencies. We obtained the following results:

Lower cut-off	150 Hz
Upper cu-toff	410 KHz

Evaluation

Problem 1: Determine Type and Pin Assignment of a Bipolar Transistors

Question 1

When we connected the multimeter to the first and third terminals, we saw a .0L reading, which meant that there was no direct movement of charge carriers between the two pins. Consequently, it could be concluded that the first and the third pin were the emitter and collector terminals of the transistor. By elimination, it could be concluded that the second pin was the base terminal.

Question 2

We determined the type of the transistor by connecting the COM port to the base of the transistor and the positive port to each of the other terminals. We obtained a .0L reading for both, signifying an absence of current flow. Therefore, we were able to conclude that the transistor was an NPN type transistor.

Question 3

The emitter is doped more heavily than the collector. As a result, when we measured the base-terminal voltages, we saw that one was higher than the other. Since the emitter is more heavily doped, we concluded that the higher base-terminal voltage is the base-emitter voltage, and hence the corresponding terminal was the emitter and the other was the collector.

Problem 2: Operating point of BJTs

Question 1

Parameter	Simulated Data	Experimental Data
V_{CC}	20V	20.03V
V_B	5.93659V	5.954V
V_E	5.22198V	5.310V
V_C	10.7206V	9.413V
V_{BE}	0.71461V	0.6543V
V_{CE}	5.49862V	5.293V

The experimental data is very close to the simulated data. The difference can be attributed to a number of reasons. One of them would be the tolerance of the different components we used.For example, transistor itself has a 10% tolerance, and on top of that in lab we used a different transistor from the one used in the simulation. On top of that, there is some error in the supply of the signal generator. Error also arises due to the resolution of the oscilloscope. Values obtained through the cursor have a 10% error, while those obtained through the measure function have a 5% error. All of this error is propagated, and as a result, deviates the final experimental values from those determined from ideal conditions.

Question 2

Using KVL,

$$-V_{CC} + V_{R4} + V_{CE} + V_{R5} = 0$$

$$V_{R4} = V_{CC} - V_{CE} - V_{R5} = V_{CC} - V_{CE} - V_E = 9.427V$$

$$I_C = \frac{V_{R4}}{R4} = 9.427\ mA$$

$$I_E = \frac{V_E}{R5} = \frac{5.310\text{V}}{560\Omega} = 9.482\ mA$$

$$I_E = I_C + I_B$$

$$I_B = 0.055mA$$

$$I_C = \beta I_B$$

$$\beta = \frac{I_C}{I_B} = 171.4$$

Question 3

$$\beta = \frac{I_C}{I_B}$$

Simulated values:

I_C	$9.27939mA$
I_B	$0.04559mA$

Experimental values:

I_C	$9.427\ mA$
I_B	$0.055mA$

$$\Delta I_B = \ 9.41 \times 10^{-3}mA$$

$$\Delta I_C = 0.14761mA$$

$$\Delta\beta = \left|\frac{\partial}{\partial \mathrm{I_C}}\left(\frac{\mathrm{I_C}}{\mathrm{I_B}}\right).\Delta I_C\right| + \left|\frac{\partial}{\partial \mathrm{I_B}}\left(\frac{\mathrm{I_C}}{\mathrm{I_B}}\right).\Delta I_B\right| = \pm 45.25$$

$$\beta_{rel} = \frac{\Delta\beta}{\beta} \times 100 = 26.4\%$$

Without the use of error propagation, we can calculate the relative error as follows:

$$\beta_{sim} = \frac{9.27939mA}{0.04559mA} = 203.54$$

$$\beta_{rel} = \frac{|171.4 - 203.54|}{203.54} = 15.7\%$$

The components used in the circuit, such as the capacitors, resistors, signal generator etc. have a certain amount of tolerance that we do not account for in our calculations. Furthermore, when using measure function of oscilloscope, there is 5% error, and measurements taken using the cursor have about 10% error. Moreover, in our experimentation, we used a transistor that is different from the simulation, which means it has different characteristics from the one used in our simulation. Therefore, the errors due to these parameters propagated to provide us the large error we see in our calculations.

One way to minimize the error would be to use the same transistor as the one used in our simulations. Furthermore, using an oscilloscope with higher resolution can also help.

Problem 3: Common Emitter Circuit

Question 1

The distorted positive amplitude occurs in the saturation region. This occurs when the base current is increased so much that the base-emitter junction is no more forward biased.

The distorted negative amplitude occurs in the cut-off region. Otherwise, the output signal would be a replica of the input with larger gain. Rather, we see an inverted waveform here.

Question 2

From first dataset:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{808mV}{52.8mV} = 15.30$$

From second dataset:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{1.64}{106mV} = 15.47$$

From third dataset:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{3.26V}{206mV} = 15.82$$

The simulation results are provided below:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{695.071mV}{50mV} = 13.901$$

Based on the calculations, we see that the gain calculated from the first dataset is closest to the gain from the simulated data.

It seems that the error in measured data compared to simulated data is about 10%. The reasons for this deviation could be attributed to the same reasons stated in problem 2 question 1.

Question 3

We see from the hard copies that the input and output have a phase difference of 180°, considering that the output signal is inverted. This occurs because, as the input voltage increases, the base current increases, which causes an increase in collector current ($I_C = \beta I_B$). This results in a larger voltage drop over R4. Consequently, the output voltage decreases. Therefore, it can be inferred that the output signal changes in the opposite direction to the input signal. This difference in direction of operation causes the phase shift.

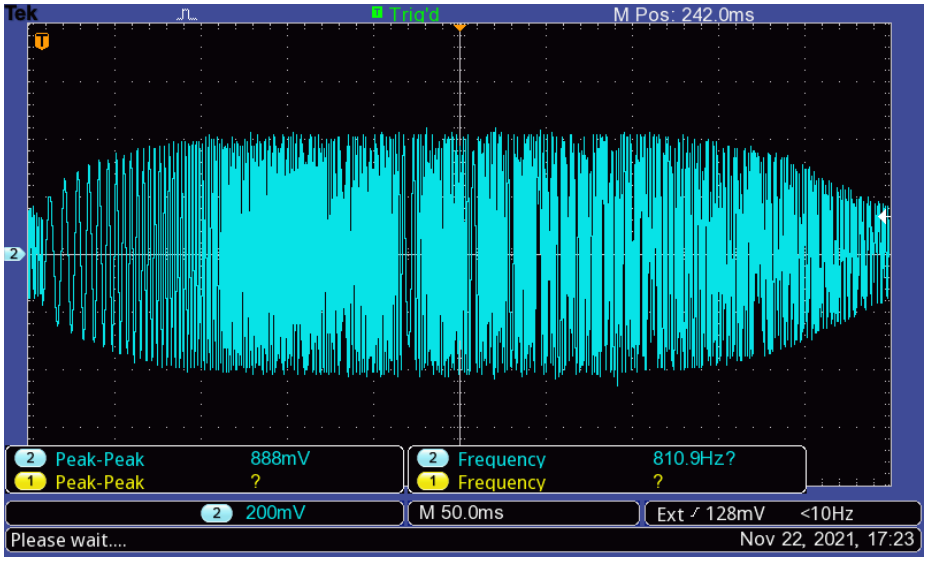
Question 4

In both the simulation and experiment, we saw that the number of peaks increased as the amplitude of the input signal was increased. The FFT of the input signal has only one peak in

both cases because it consists of a pure sinusoidal signal with a frequency of 1KHz. The output, however, is not just an amplified version of the input. It is distorted during the process of amplification, which means the output is a combined version of multiple sinusoidal signals with different frequencies. Therefore, in the FFT Spectrum for output in both experimental and simulated case, we see multiple peaks at different frequencies because the final output is a combined version of multiple sinusoids with different frequencies.

Problem 4: Bandwidth of amplifier circuit

Question 1



On this part, we observed the full sweep of the oscilloscope which results in a Bode Plot representation. We can see that the circuit has low gain at low and high frequencies, which gives the characteristics of a bandpass filter. The suppression at higher frequencies occurs because of the parasitic capacitance of the amplifier, which acts as a limiting factor for the gain. This is called the Miller Effect. On the other hand, the suppression at lower frequencies occurs because the capacitor has high impedance at lower frequencies, and since the capacitor is in parallel to RL in the circuit, a smaller part of the output is distributed to RL due to voltage division.

Question 2

We have the following measurement data:

Lower cut-off	150 Hz
Upper cu-toff	410 KHz

$$B = 410000 - 150 = 409850\ Hz = 409.85\ KHz$$

Question 3

From simulation, we obtained the following results:

$$Lower\ f_{-3dB} = 145.154\ Hz$$

$$Upper\ f_{-3dB} = 384870\ Hz$$

$$B = 384724.846\ Hz = 384.72\ KHz$$

Comparing the experimental results with the simulated results, we see that the experimental bandwidth deviates from the simulated one by about 7%. This could result from the difference in the simulated and experimental cut-off values.

The simulated and experimental cut-off values are different due to a number of reasons. We consider the simulated results as ideal since there are not subject to deviations due to tolerances, resolution error, precision error, equipment error etc.

With regards to the experimental values, difference can be attributed to a number of reasons. One of them would be the tolerance of the different components we used. For example, transistor itself has a 10% tolerance, and on top of that in lab we used a different transistor from the one used in the simulation. Moreover, the signal generator carries 1-2% tolerance. Error also arises due to the resolution of the oscilloscope. Values obtained through the cursor have a 10% error, while those obtained through the measure function have a 5% error. All of these errors are propagated, and as a result, deviates the final experimental values from those determined in ideal conditions.

Conclusion

In this lab, we studied the Bipolar Junction Transistors (BJTs) and their applications. In prelab, we revised our theoretical understanding of the transistor by solving a BJT circuit to extract some parameters. We then simulated the circuit to observe how the theoretical data corresponded to the simulated data. Within the simulation, we then replaced the emitter resistor with a current source, and repeated the steps as before. Then, we built a constant current source using a different circuit formulation which included a Zener diode, and again analyzed the circuit using the datasheet and theoretical constructs to extract certain parameters. Then, we compared the results with simulated data to verify our work. As a result, we understood the behavior of the circuit, realized that it acted as a stabilizer. Next, we simulated an amplifier circuit on LTSpice, and carried out an operating point analysis. We then introduced a variable input to the circuit and observed its output at different terminals. Using the data we obtained, we were able to determine the gain of the circuit. We then simulated a DC Sweep on the circuit. Using the FFT spectrum, we noticed that while the input is a pure sinusoidal signal, the output is a distorted signal made of sinusoids of different frequencies and amplitudes. An increase in the input amplitude resulted in an increase in the number of peaks in the FFT spectrum of the output. Lastly, we performed an AC analysis on the simulated circuit and observed that the result is a Bode Plot, from which we were able to determine the cut-off frequencies and the bandwidth.

In the experimental phase, for the first section, we used the multimeter to determine the collector, emitter and base of the transistor and also the transistor type. We concluded that pin 1 is emitter, pin 2 is base and pin 3 is collector, and the transistor is an NPN type. We then used the transistor to build a transistor circuit on the breadboard, in combination with other components such as a power supply, resistors etc. Using the multimeter, we carried out an operating point analysis on the circuit. Then, we added more components to the circuit to make an amplifier circuit, and supplied 1KHz sin wave inputs of amplitudes 50 mVpp, 100 mVpp and 200 mVpp. We noticed that as the input amplitude was increased, the number of peaks on the FFT spectrum of the output increased, as we observed in the simulation.

Next, we examined the bandwidth of the amplifier circuit experimentally, and observed how the voltage gain of the BJT was affected with changing frequency of the input signal. We enabled the sweep mode of the function generator with a 50mV peak for V_S, starting frequency of 100Hz, a stopping frequency of 1MHz, a logarithmic sweep mode and a sweep time of 500ms. We used the external trigger of the signal generator as the oscilloscope trigger. On the oscilloscope, we oscilloscope, we saw that the output looked like a Bode plot with the signal suppressed at the ends. We concluded that this was due to the capacitance of the capacitor at lower frequencies, which results in high impedance, and the parasitic capacitance of the amplifier at high frequencies as a result of the Milner Effect.

In evaluation part, we compared our experimental data to our simulated data. During evaluation of the experimental data, we found some instances where the experimental data deviated from the simulated data, and we were able to conclude that there were multiple reasons this occurred. Firstly, we used a different transistor in simulation as compared to the one in experiment,

therefore it was inevitable that we'd see some differences in characteristics. Furthermore, the transistor has a tolerance of 10%, the resistor about 1%, the signal generator 1-2% and similarly the other circuit components also have different tolerances. These contribute to the total error of the experimental data. Moreover, the oscilloscope has an error of 5% when using the measure function and an error of 10% when taking measurements using the cursor. All these errors propagate to give us a large final error in our experimental data.

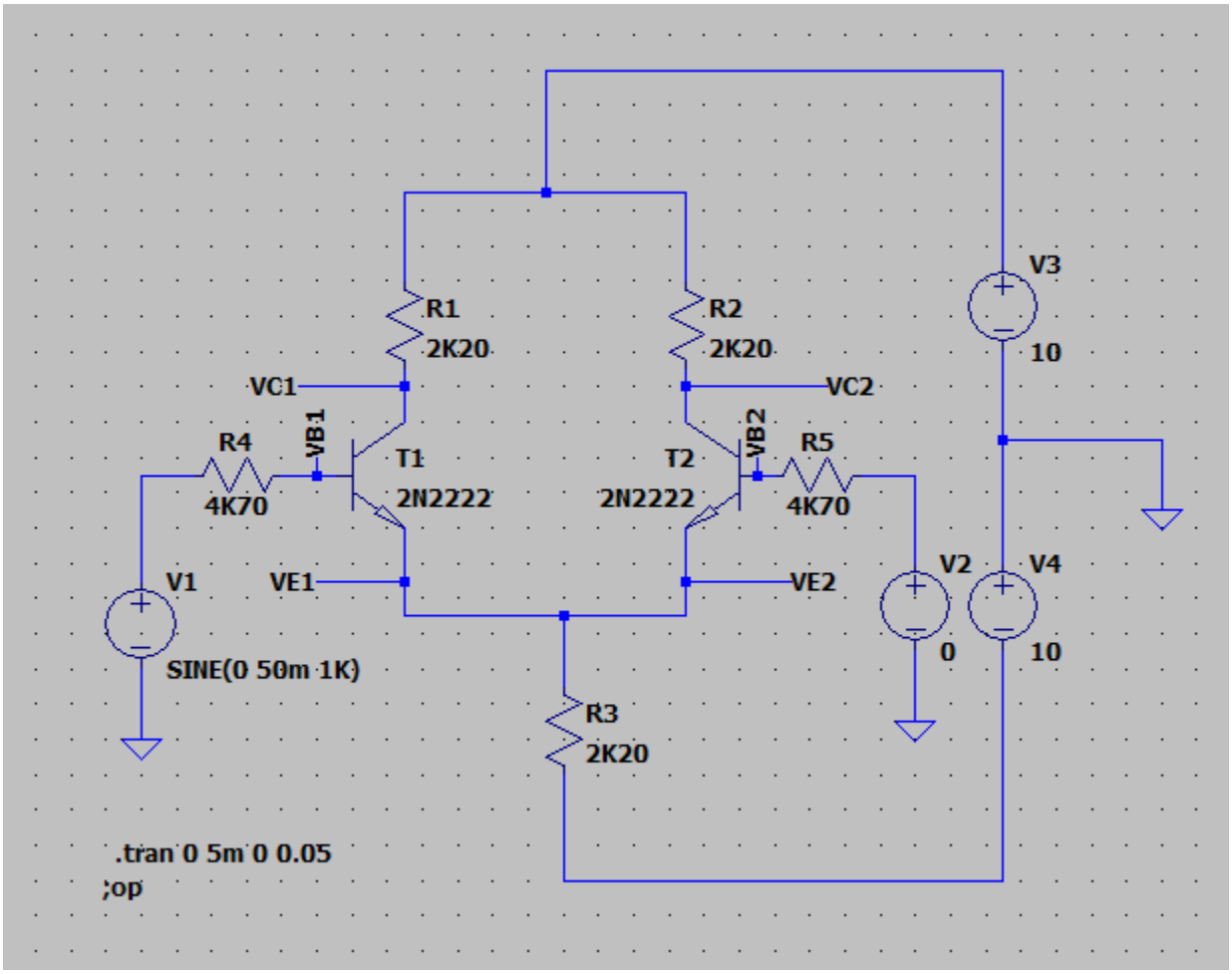
References

- Electronics Lab Manual (Uwe Pagel)
- http://www.faculty.jacobs-university.de/upagel/
- Fundamentals of Microelectronics (Behzad Razavi)

Prelab 4: Operational Amplifier

Problem 1: Simulate a Differential Amplifier

LTSpice Circuit:



Task 1

Perform a dc operation point analysis for the above circuit. Determine the values for VBE(T1, T2), VC(T1, T2) , IC(T1, T2), IE(T1, T2), and IRE. What would happen with the values in the two branches if the transistors are not absolute identical.

	T1	T2
V_{BE}	0.67362V	0.67362V
V_C	5.38824V	5.3824V
I_C	0.002099A	0.002099A
I_E	-0.002109A	-0.002109A
I_{RE}	0.004218A	

Task 2

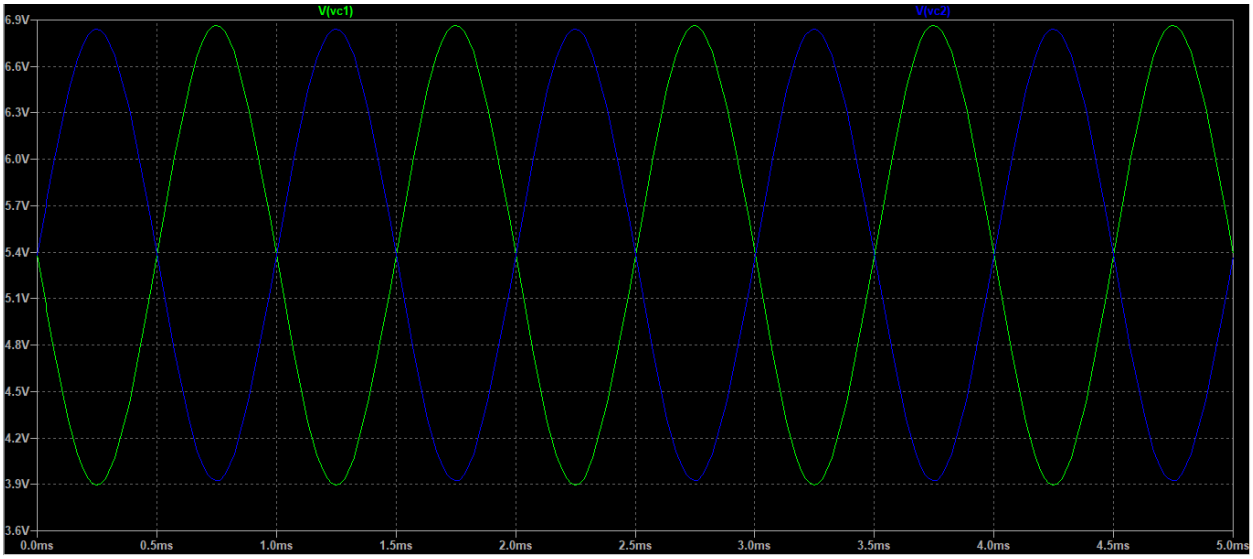


Figure: Collector voltages at output

Using the cursors, we obtain the peak-to-peak difference in V_{out}. Using this value, we can obtain the gain as follows:

$$dBA_{V,diff} = 20\log\left(\frac{2.9371795V}{2\times 50\times 10^{-3}V}\right) = 29.358\ dB$$

Task 3

After making the required changes, we obtain the following results:

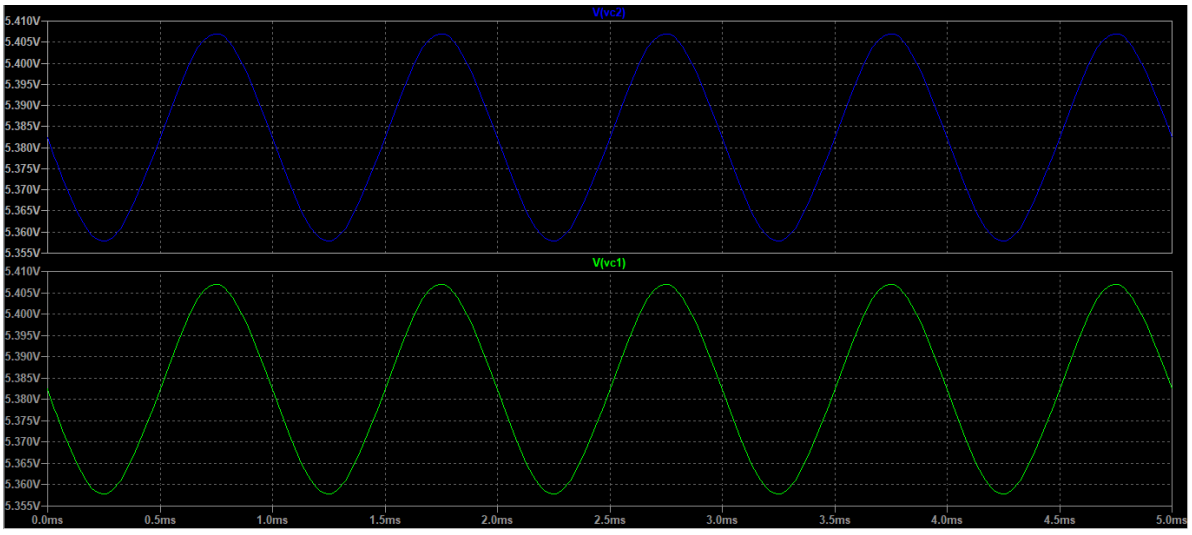


Figure: Output collector voltages

Using the cursors, we find that the difference between the peaks at a point in time. We obtain the following results:

$$dBA_{V,cm} = 20\log\left(\frac{V_{out}}{V_{in}}\right) = 20\log\left(\frac{45.682203\mu V}{2\times 50mV}\right) = -6.805\ dB$$

Task 4

$$CMRR = 20\log\left(\frac{A_{V,diff}}{A_{V,cm}}\right) = 20\log(A_{V,diff}) - 20\log(A_{V,cm}) = 29.358 + 6.805 = 36.163\ dB$$

Task 5

On replacing R_3 with a constant current source, we have the following final set-up:

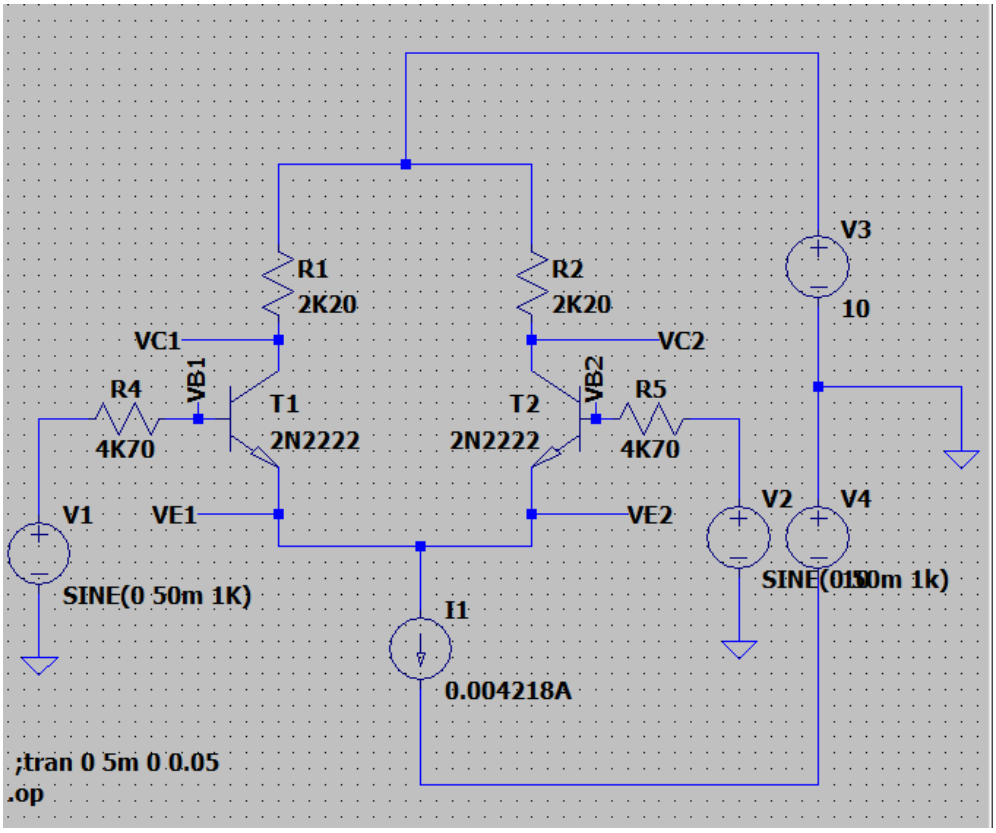


Figure: Differential Amplifier with current source

Sub-task 1

On completing the operation point analysis, we obtain the following values:

	T1	T2
V_C	5.38225V	5.38225V
V_{BE}	0.6736225V	0.6736225V
I_C	0.00209898A	0.00209898A
I_E	-0.002109A	-0.002109A
$I1$	0.004218A	

Sub-task 2

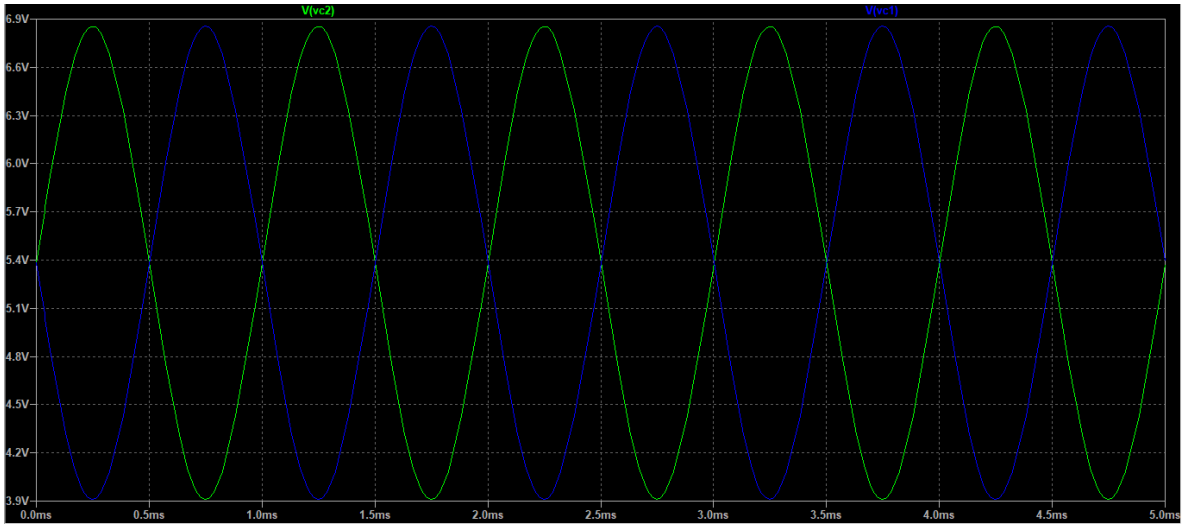


Figure: Collector voltage outputs

Using cursors, we find the difference between the peaks of the output voltage. Using the value, we can make the following calculations:

$$dBA_{V,diff} = 20\log\left(\frac{V_{out}}{V_{in}}\right) = 20\log\left(\frac{2.9424655V}{2\times 50mV}\right) = 29.425dB$$

Sub-task 3

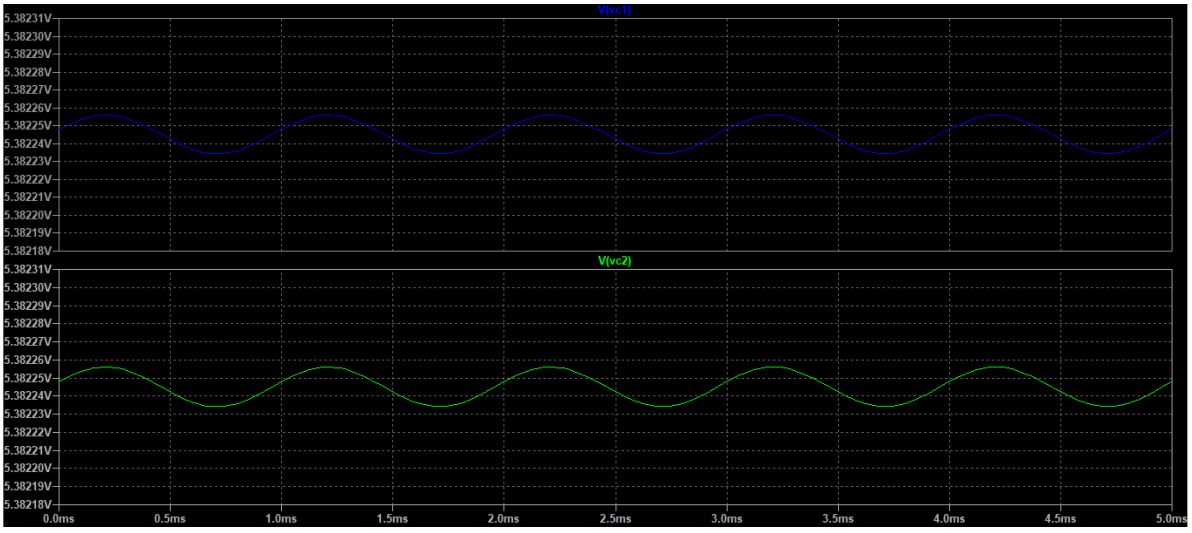


Figure: Common mode simulation results

$$dBA_{V,cm} = 20\log\left(\frac{V_{out}}{V_{in}}\right) = 20\log\left(\frac{64.035565nV}{2\times 50mV}\right) = -123.872\ dB$$

Sub-task 4

$$CMRR = 20\log\left(\frac{A_{V,diff}}{A_{V,cm}}\right) = 20\log(A_{V,diff}) - 20\log(A_{V,cm})$$

$$CMRR = 29.425dB + 123.872\ dB = 153.297\ dB$$

Problem 2: Construct an OP-Amp

For this task, we are required to construct the following circuit:

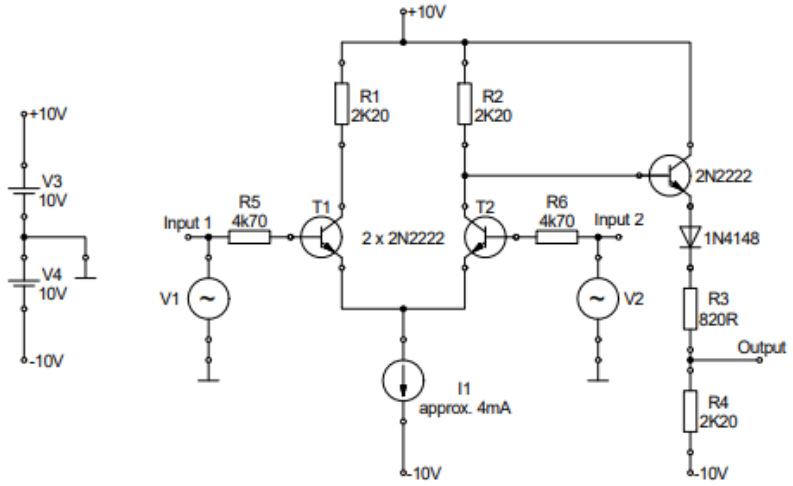


Figure: OP-Amp Circuit

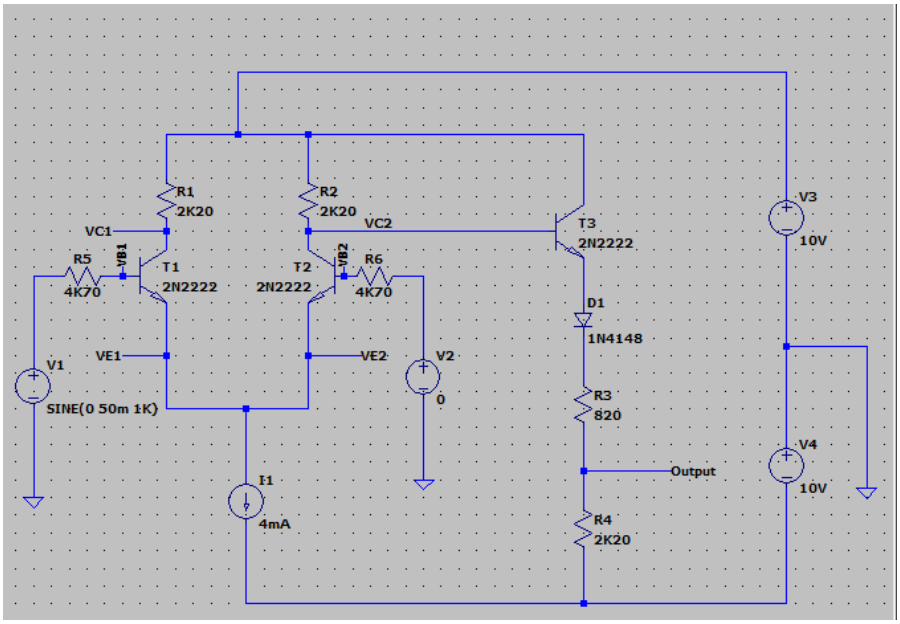


Figure: Op-Amp circuit Implementation

Task 1

Calculate the voltage at the output of the emitter follower when both inputs are connected to ground. Assume β = 200 and UBE = 0.7V. The forward voltage drop of the diode is 0.7V.

$$I_{E2} = I_{C2} = \frac{I_1}{2} = 2mA = 2 \times 10^{-3}A$$

$$V_{R2} = I_{C2}R_2 = \ 4.4V$$

Using KVL:

$$V_{CB} = V_{R2} = 4.4V$$

$$V_{CE} = V_{CB} + V_{BE} = 5.1V$$

$$-10 - 10 + 5.1 + 0.7 + I_{E3}R_3 + I_{E3}R_4 = 0$$

$$I_{E3} = 4.702 \times 10^{-3}A$$

Using KVL about output:

$$V_{out} - (-10V) = 10.344V$$

$$V_{out} = \ 0.344V$$

Task 2

Using the DC Operating Point analysis, we found the following results:

V(vc1):	5.61987	voltage
V(vb1):	-0.0445579	voltage
V(ve2):	-0.71672	voltage
V(vc2):	5.57175	voltage
V(vb2):	-0.044558	voltage
V(n001):	10	voltage
V(n002):	0	voltage
V(n003):	0	voltage
V(n006):	-10	voltage
V(n004):	4.87625	voltage
V(n005):	4.2192	voltage
V(output):	0.358357	voltage
Ic(T3):	0.00468557	device_current
Ib(T3):	2.27702e-005	device_current
Ie(T3):	-0.00470834	device_current
Ic(T2):	0.00199007	device_current
Ib(T2):	9.48043e-006	device_current
Ie(T2):	-0.00199955	device_current
Ic(T1):	0.00199097	device_current
Ib(T1):	9.48041e-006	device_current
Ie(T1):	-0.00200045	device_current
I(D1):	0.00470834	device_current
I(I1):	0.004	device_current
I(R4):	0.00470834	device_current
I(R3):	0.00470834	device_current
I(R6):	9.48043e-006	device_current
I(R5):	-9.48041e-006	device_current
I(R2):	0.00201284	device_current
I(R1):	0.00199097	device_current
I(V2):	-9.48043e-006	device_current
I(V1):	-9.48041e-006	device_current
I(V3):	-0.00868938	device_current
I(V4):	-0.00870834	device_current

As we can see, according to the simulation,

$$V_{out} = 0.358V$$

This value is very close to our calculated value, so the DC Operation Analysis meets our expectations.

Task 3

As in the first problem, we find $A_{V,diff}$ by setting V1 at input 1 to sine, with f = 1KHz and u = 50 mV. Furthermore, V2 is set to GND.

We find the following results:

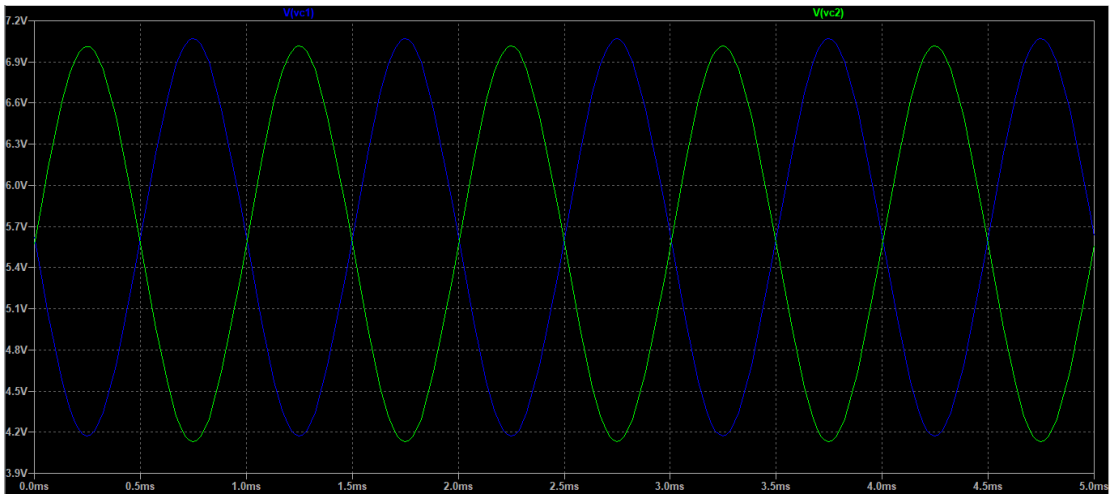


Figure: Collector Output Voltages in Differential Input Mode

$$dBA_{V,diff} = 20\log\left(\frac{2.8376463V}{50mV \times 2}\right) = 29.0592\ dB$$

Setting V2 to be the same as V1 and repeating the simulation, we obtain the following output:

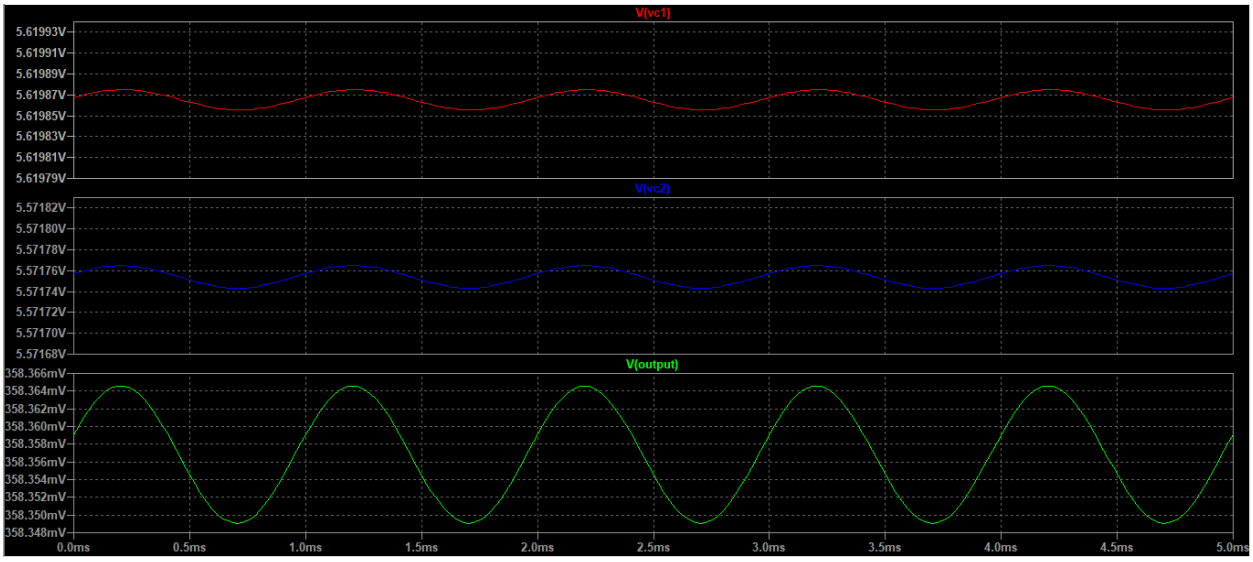
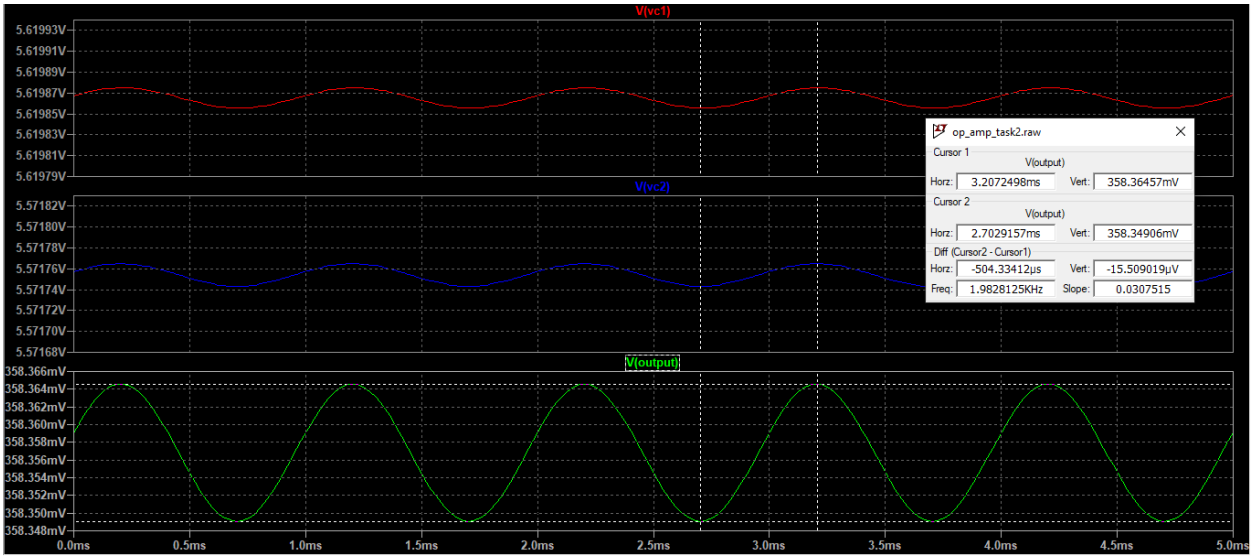


Figure: Collector Output Voltages in Common Input Mode



$$dBA_{v,cm} = 20\log((15.509019\mu V)/(50mV \times 2)) = -76.1883\ dB$$

$$CMRR = dBA_{V,diff} - dBA_{V,cm} = 105.2475\ dB$$

Task 4

To determine the inverting and non-inverting inputs, we first supply a sinusoidal input at V1, set V2 to GND, and observe the output:

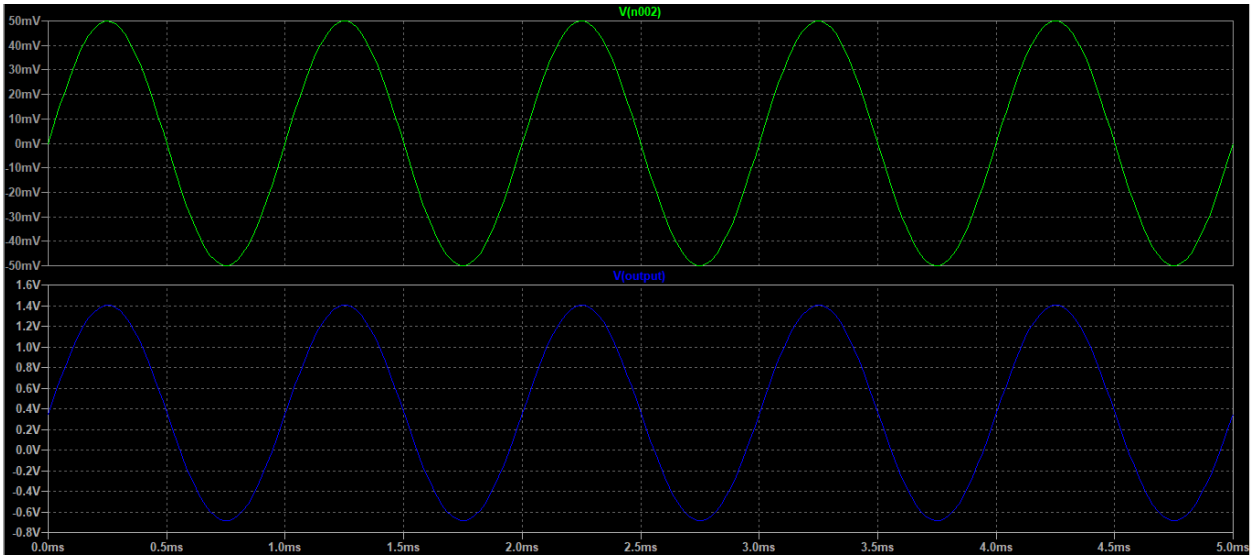


Figure: Output with Sinusoidal Input at V1, V2 set to GND

We see that the output is in phase with the input. Therefore, this is the non-inverting input.

Now, we supply V2 with a sinusoidal input, set V1 to 0 and observe the output:

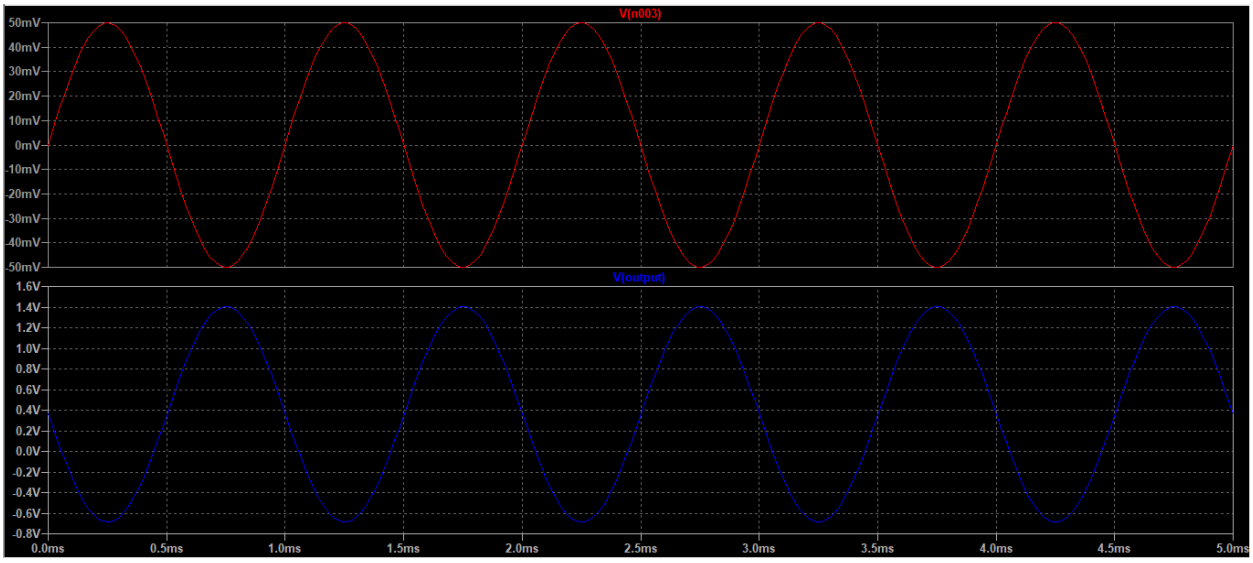


Figure: Output with Sinusoidal Input at V2, V1 set to GND

From the simulation results, we see that the output is inverted for an input at V2.

Therefore, V2 is the inverting input.

Problem 3: Designing a non-inverting amplifier

Task 1

We use the following diagram to make our calculations:

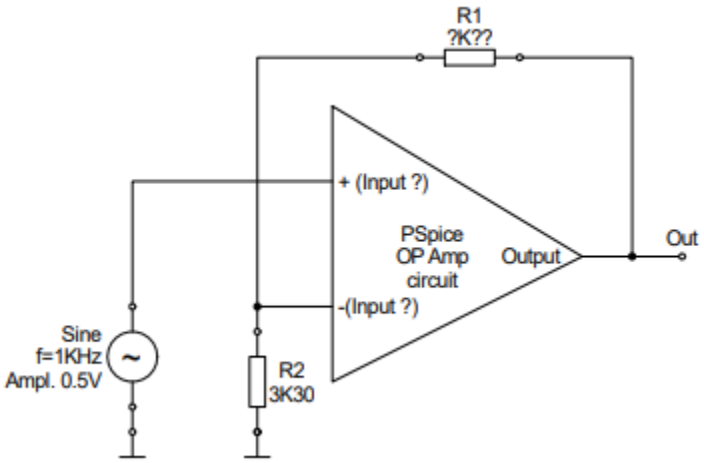


Figure: Op-Amp Circuit

$$\frac{0 - V_S}{3300} = \frac{V_S - V_{out}}{R1}$$

$$-\frac{1}{3300} = \frac{1}{R1} - \frac{1}{R1} \cdot \frac{V_{out}}{V_S}$$

$$-\frac{1}{3300} = \frac{1}{R1} - \frac{3}{R1}$$

$$-\frac{1}{3300} = -\frac{2}{R1}$$

$$R1 = 6600\Omega$$

Task 2

A simulation of the input and output voltages is provided below:

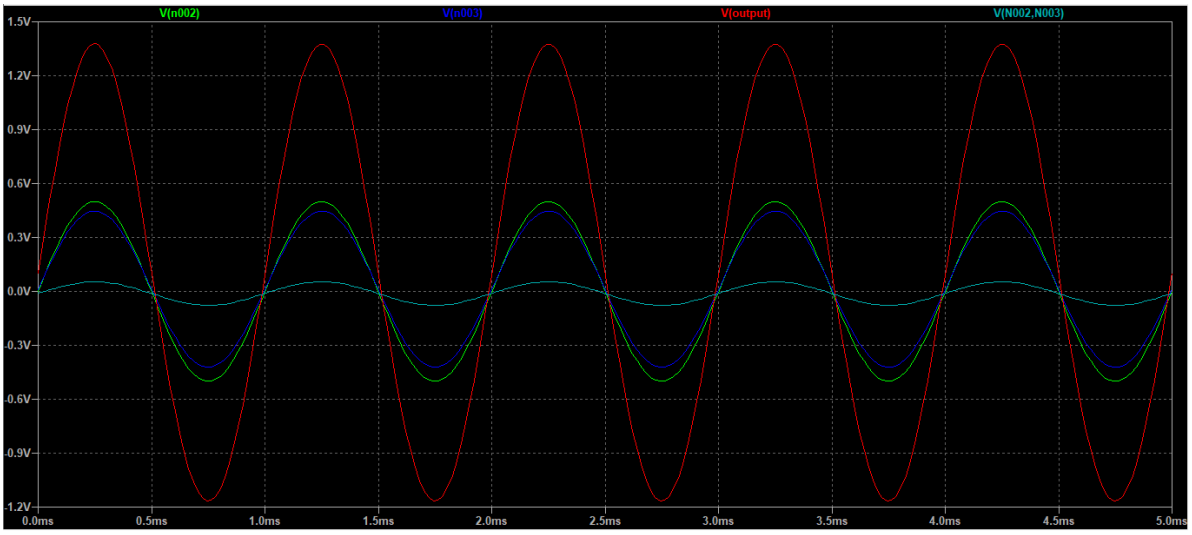


Figure: Input and Output Signals for the Feedback based Op-Amp

Separate plots for input and output signals:

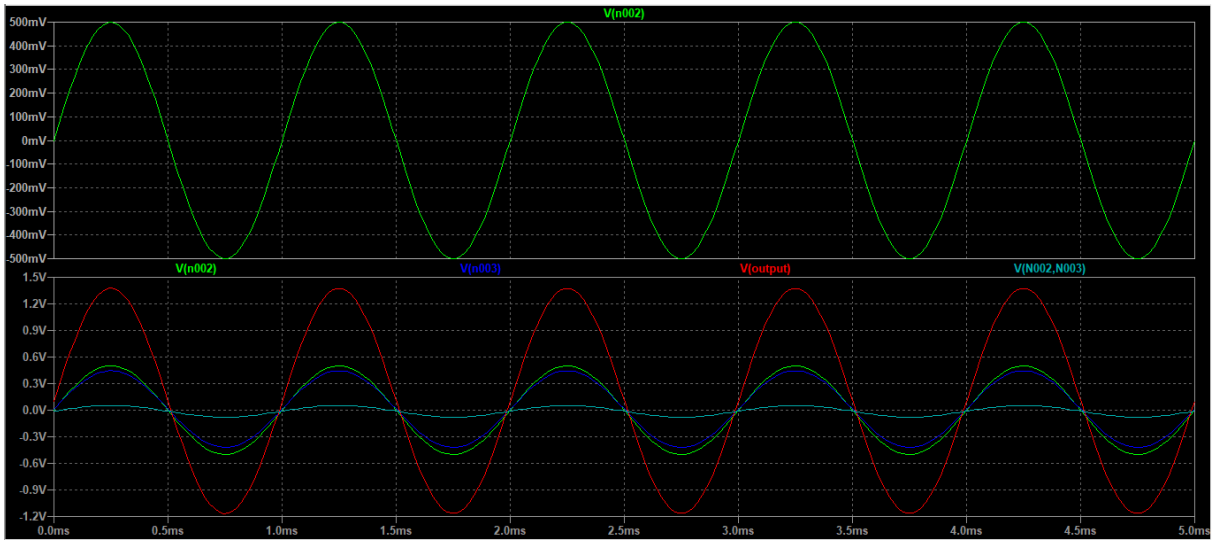


Figure: Input and Output Signals for the Feedback based Op-Amp

Gain calculation:

$$Gain = \frac{V_{out,Vpp}}{V_{in,VPP}} = \frac{2.5407413V}{995.64758mV} = 2.552$$

Task 3

We use the following block diagram to explain the difference between the measured gain and the theoretical gain:

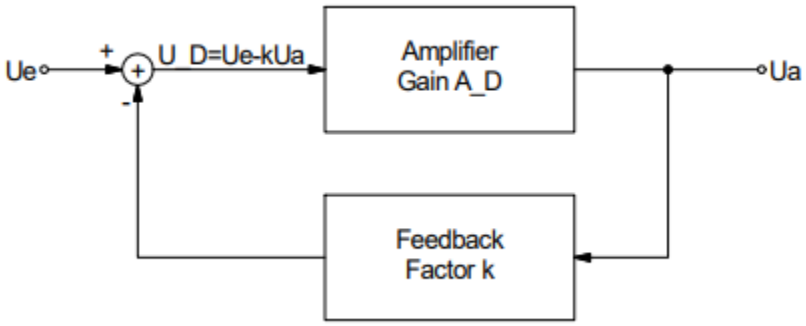


Figure: Block Diagram for a feedback system

$$U_e = V_{in}, \qquad U_a = V_{out}, \qquad A_D = A_v, \qquad K = Feedback\ Factor$$

$$(V_{in} - K \cdot V_{out})A_V = V_{out}$$

$$A_V V_{in} - A_V K V_{out} = V_{out}$$

$$A_V V_{in} = (1 + A_V K)V_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{A_V}{1 + A_V K}$$

As we can see, because of the feedback loop, a weighted version of the output is subtracted from the input during every cycle, which provides us with a new gain, or the closed loop gain, which is lower than the open loop gain.

Using the derivation, we find that the feedback factor in this case is K = 0.0588

Task 4

Input Offset Current = 20nA

Slew Rate = 0.5 V/µs

For the input offset voltage we are going to use the input offset voltage arrangement range.

Parameter	**Datasheet values**
Input bias current	8nA
Input offset voltage	2mV
Voltage gain	200V/mV
CMRR	90dB

Experimental Data and Results

Problem 1: Differential amplifier using a fixed emitter resistor

Task 1

DC Bias Value Measurements

$V_1 = V_2 = 0V$

Parameters	T1	T2
V_C	6.415V	4.308V
V_B	-0.0552V	-0.0535V
V_{BE}	0.637V	0.665V
I_C	0.001666V	0.002603V
I_{RE}	0.004275A	

Task 2

We used single-ended input mode. We set V_2 to 0V DC and V_1 to sine, f = 1 KHz, u = 50mV. The output is provided below:

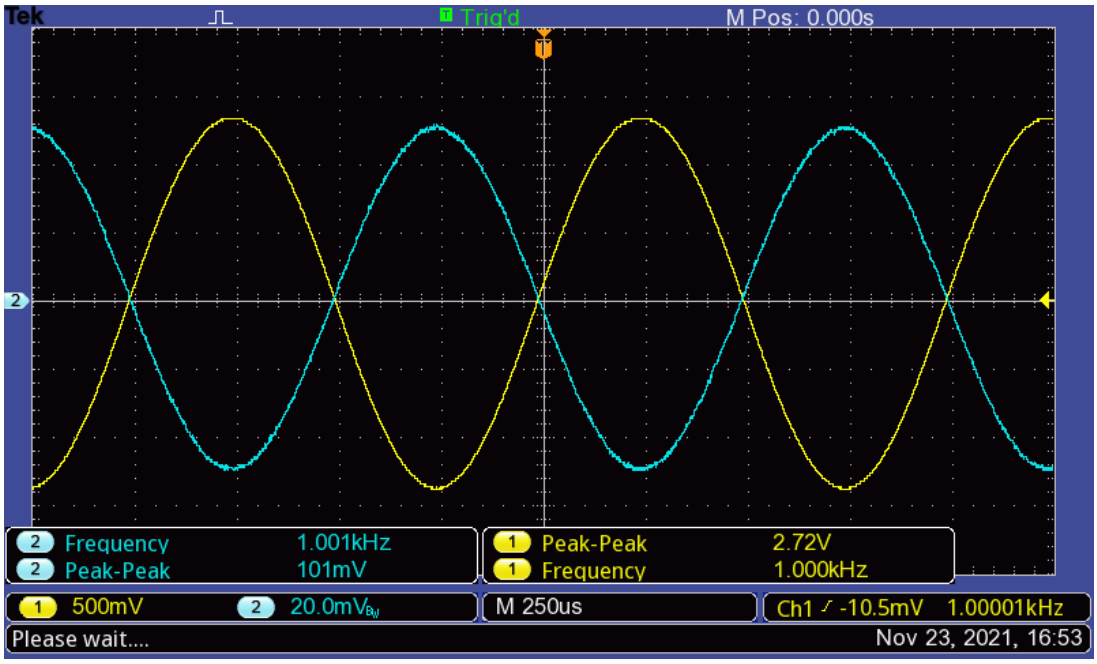


Figure: output for single-ended mode

$$A_{vdm} = \frac{2.72V}{101mV} = 26.931$$

Task 3

We used common input mode. We set V_2 and V_1 to sine, f = 1 KHz, u = 50mV. The output is provided below:

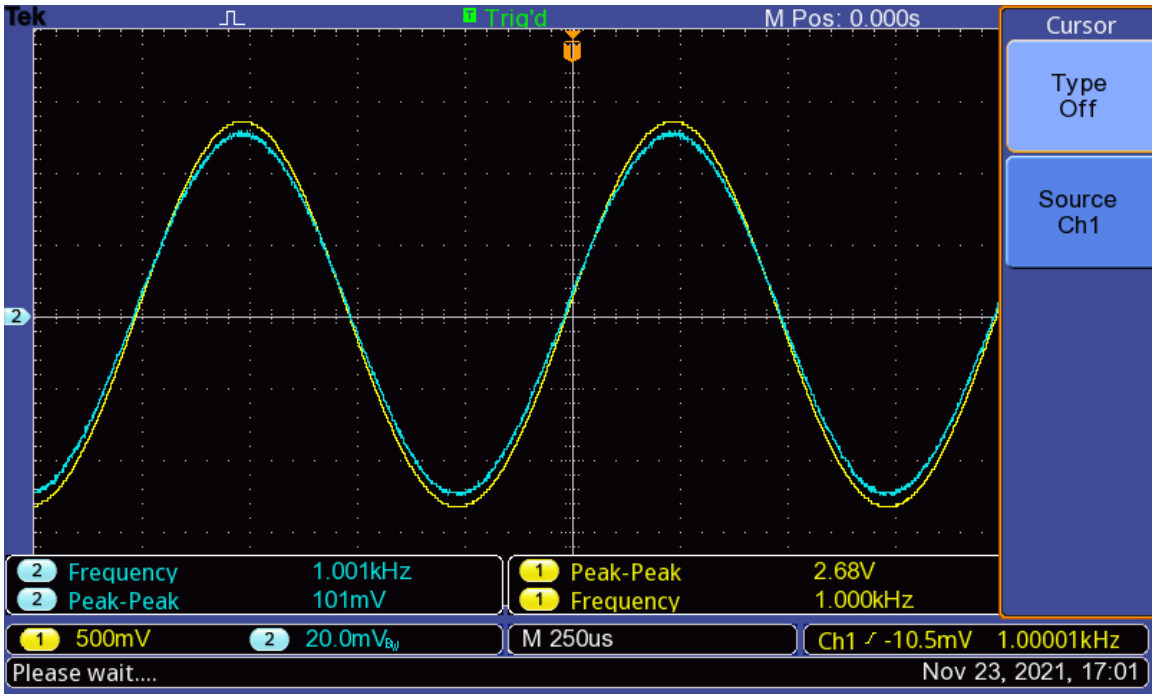


Figure: output for common mode

Problem 2: Implement a Current Source

Task 1

$$R1 = 530\ \Omega$$

$$R2 = 1000\ \Omega$$

Task 3

The circuit is operational.

Problem 3: Differential amplifier using a Current Source

Task 1

Parameters	T1	T2
V_C	6.71V	4.843V
V_B	0.0503V	0.0483V
V_{BE}	0.6339V	0.6362V
I_C	0.001515A	0.002375A
I_{RE}	0.0039267 A	

Task 2

We used single-ended input mode. We set V_2 to 0V DC and V_1 to sine, f = 1 KHz, u = 50mV. The output is provided below:

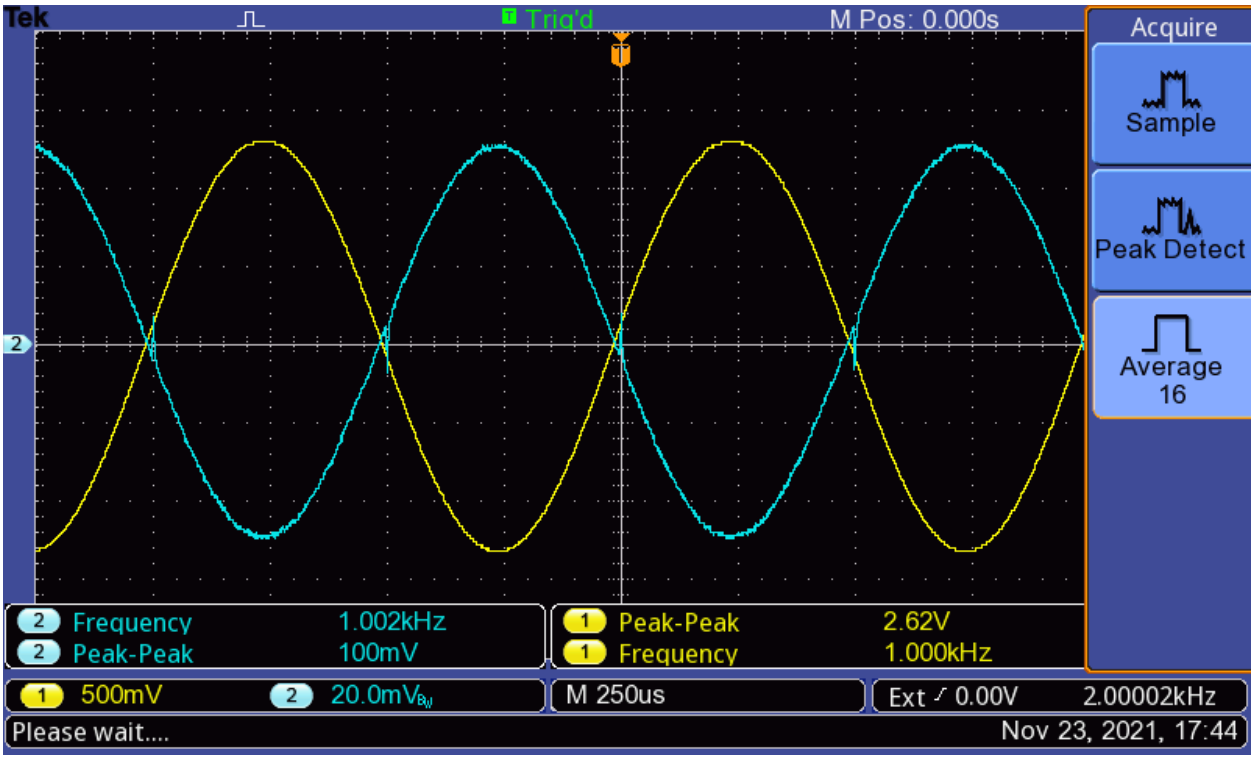


Figure: output for single-ended mode

We used common input mode. We set V_2 and V_1 to sine, f = 1 KHz, u = 50mV. The output is provided below:

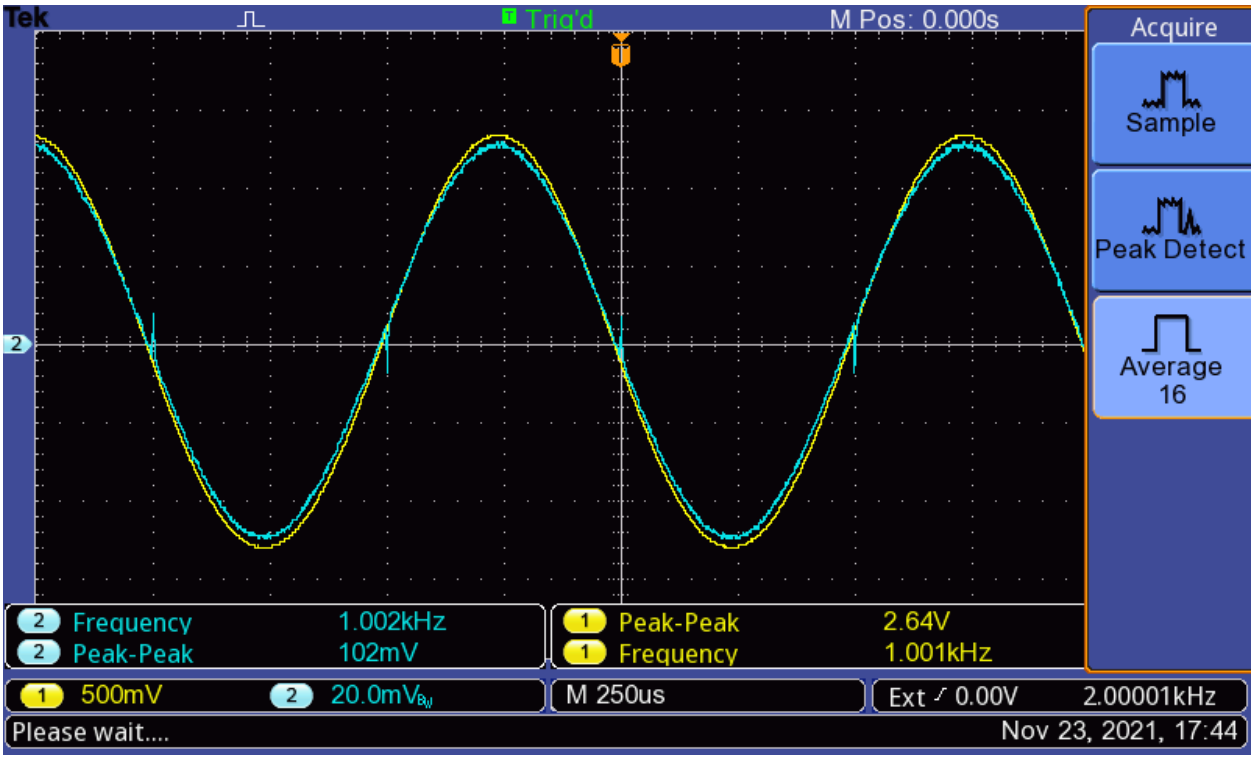


Figure: output for common mode

Further data collected: