Prelab: CMOS Inverters and Logic Gates

Problem 1: Voltage Transfer Characteristic of a CMOS inverter

Task 1

For this task we implement a CMOS inverter on LTSpice:

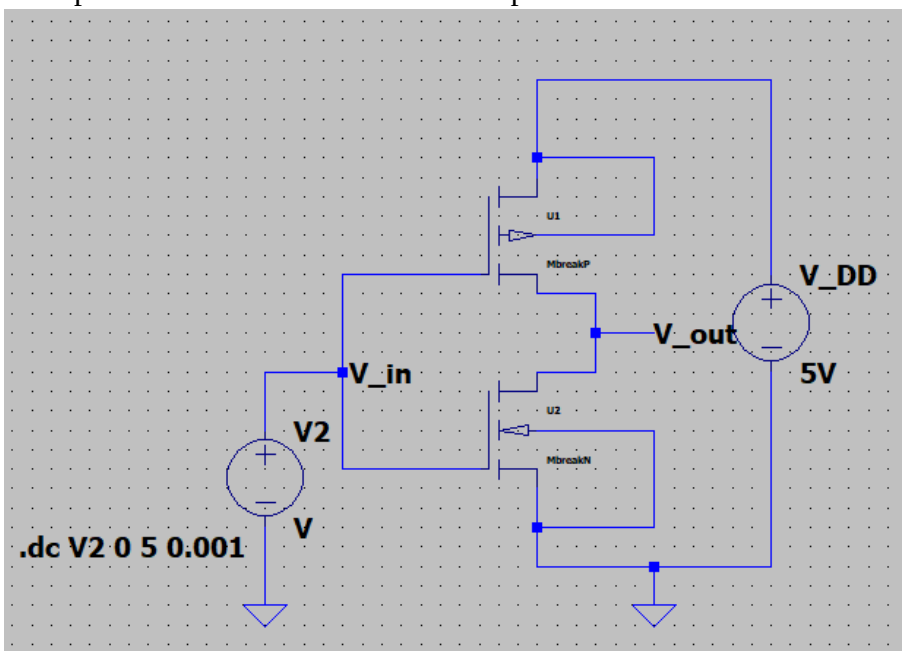


Figure: CMOS inverter

We use a 5V power supply for V_{DD}. Then we simulate the VTC of the CMOS inverter, and use the d() function to obtain the derivative curve. The results are shown as follows:

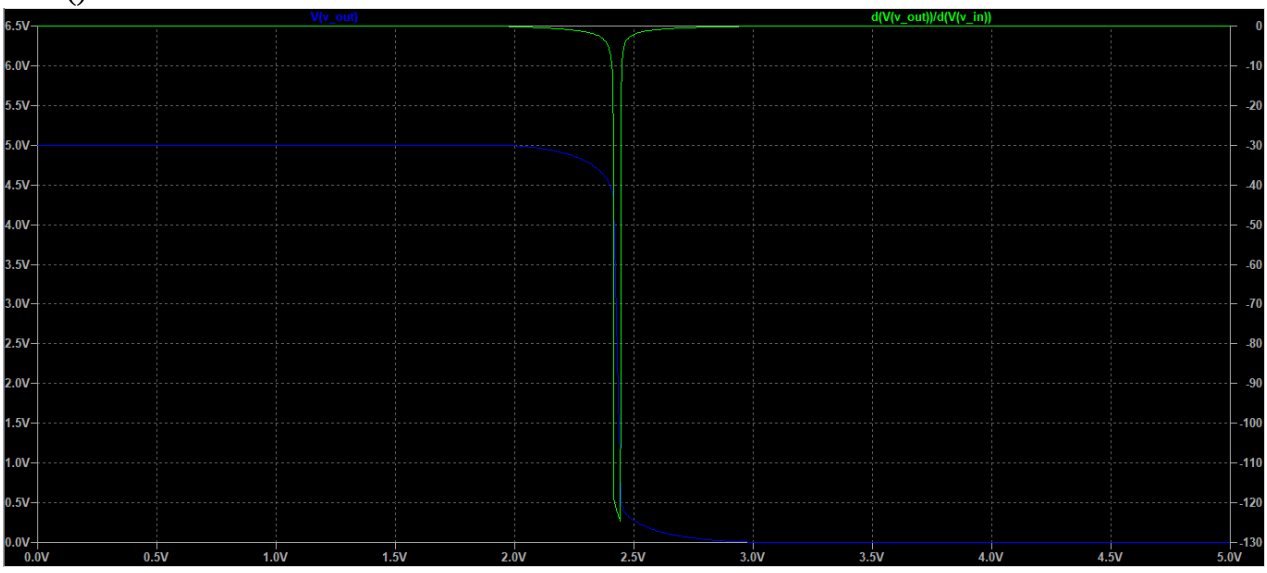


Figure: VTC Simulation results

Then, we extract the following values from the curve:

V_{OH}	4.8669256V
V_{IL}	2.2393162V
V_{OL}	166.89289mV
V_{IH}	2.5726496V
NM_L	133.07445mV
NM_H	166.89285mV

Task 2

Then, we simulate the current flowing through the inverter as a function of the input voltage. The results are provided below:

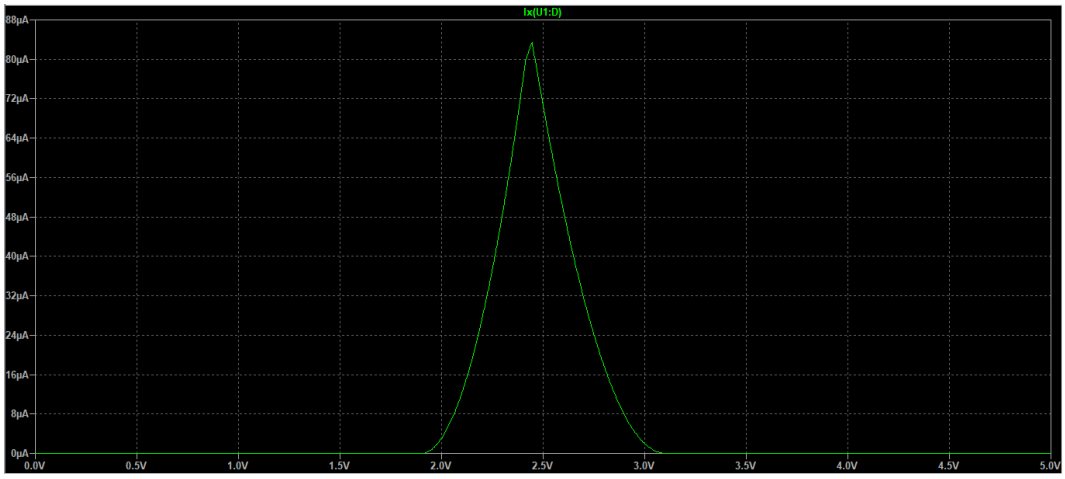
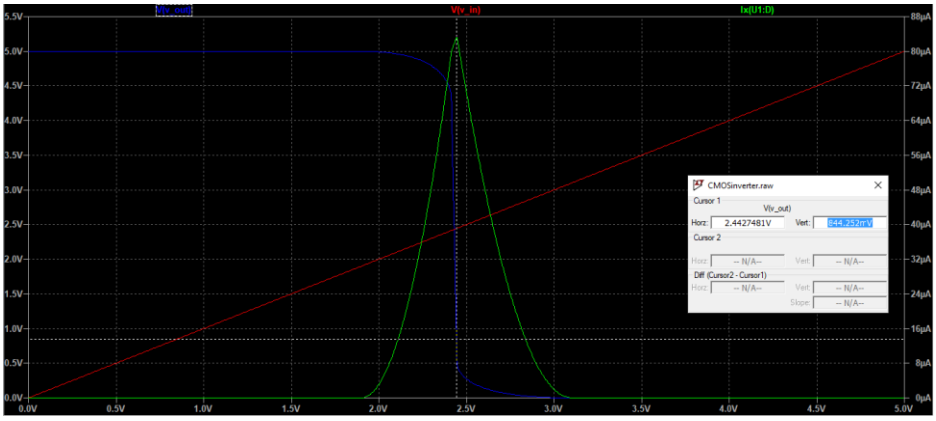


Figure: Inverter current flow simulation

Task 3

Based on the simulation, the maximum is reached when input is 2.4427481V, at which point the current flow is 83.124869µA. At this point the input and output voltages are equal, so both NMOS and PMOS transistors are turned on. As a result, the current reaches its maximum level. We can see a demonstration below:



Problem 2: CMOS Inverter with Capacitive Load

Task 1

We now add a simple load capacitor to the circuit. The circuit looks as follows:

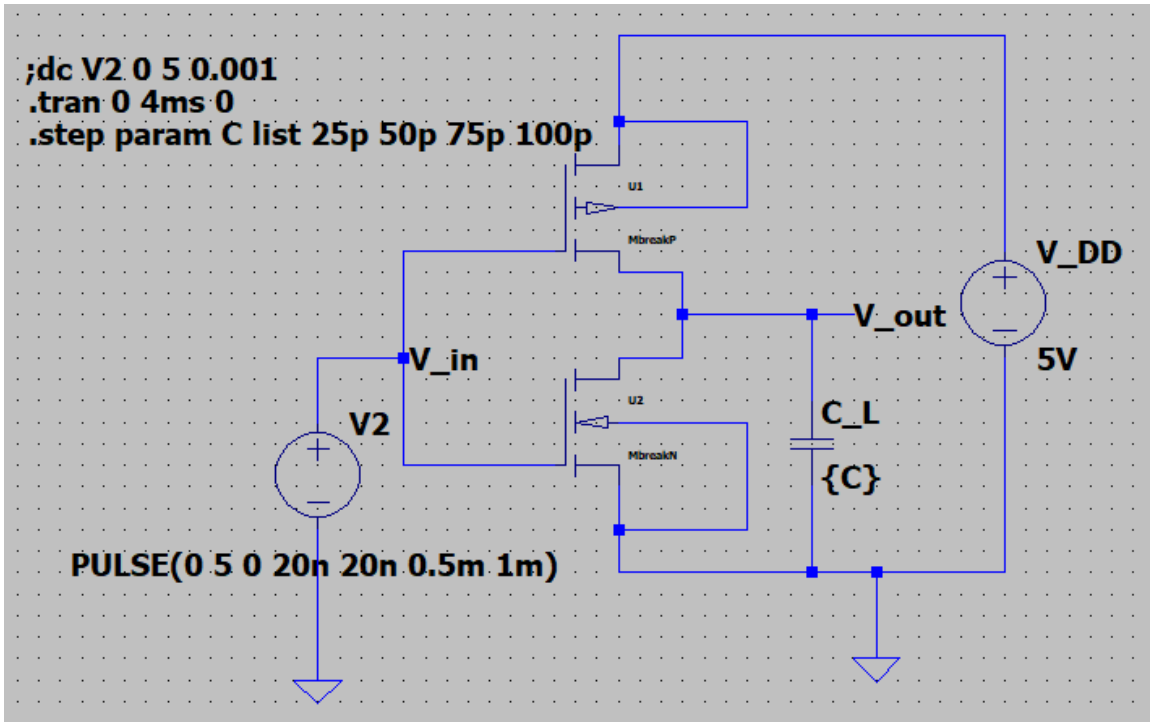


Figure: CMOS inverter

We vary the capacitive load from 25pF to 100pF in 25pF steps for an input signal given by a 1KHz square wave with 20ns rise and fall time and use a 5V power supply for V_DD.

The input and output signal are displayed below:

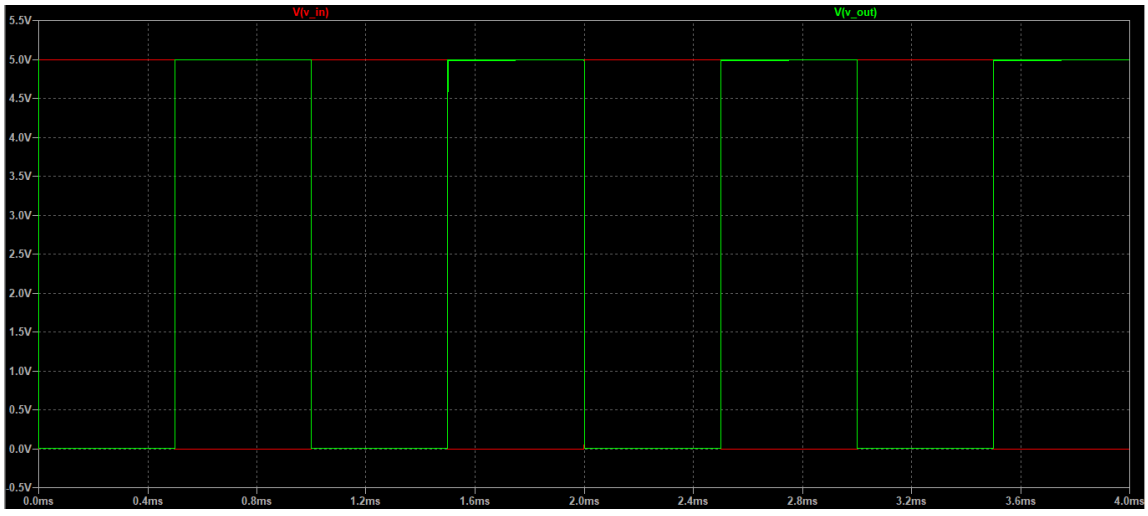


Figure: Input and output

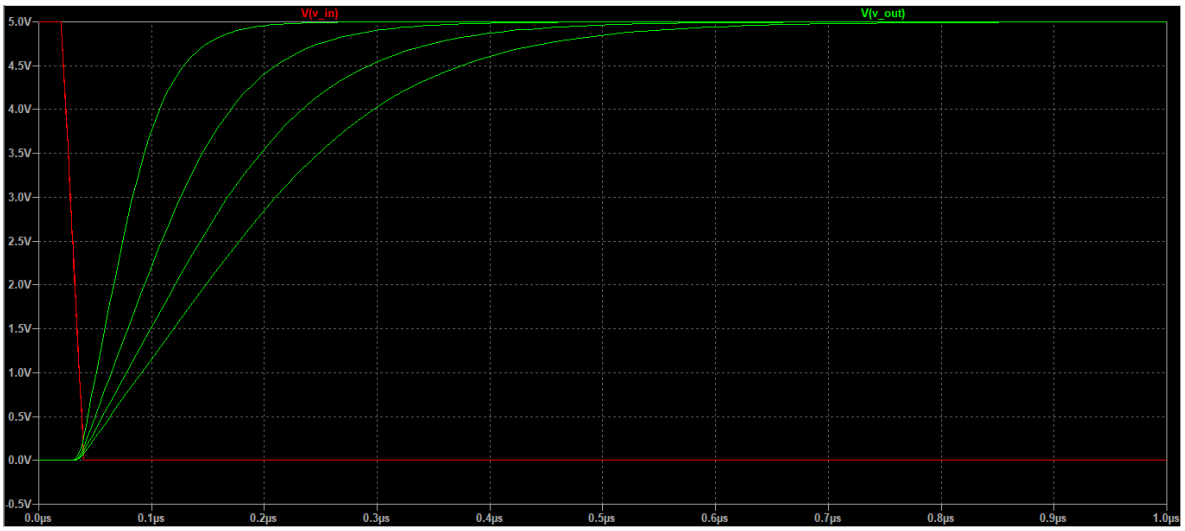


Figure: Examining propagation delay for different capacitances

Capacitance	$t_{PLH} = t_{PHL}$
25 pF	45.141546ns
50pF	76.511094ns
75pF	113.23642ns
100pF	147.66641ns

From the table, we can see that the time delay increases as the capacitance increases.

Task 2

$$P_{D1} = f \times C1 \times V_{DD}^2 = 1000 \times 25 \times 10^{-12} \times 5^2 = 6.25 \times 10^{-7} W = 0.625 \mu W$$
$$P_{D2} = f \times C2 \times V_{DD}^2 = 1000 \times 50 \times 10^{-12} \times 5^2 = 1.25 \times 10^{-6} W = 1.25 \mu W$$
$$P_{D3} = f \times C3 \times V_{DD}^2 = 1000 \times 75 \times 10^{-12} \times 5^2 = 1.875 \times 10^{-6} W = 1.875 \mu W$$
$$P_{D4} = f \times C4 \times V_{DD}^2 = 1000 \times 100 \times 10^{-12} \times 5^2 = 2.5 \times 10^{-6} W = 2.5 \mu W$$

Problem 3: Propagation Delay of an Inverter Stage

For this section, we first implement the following circuit:

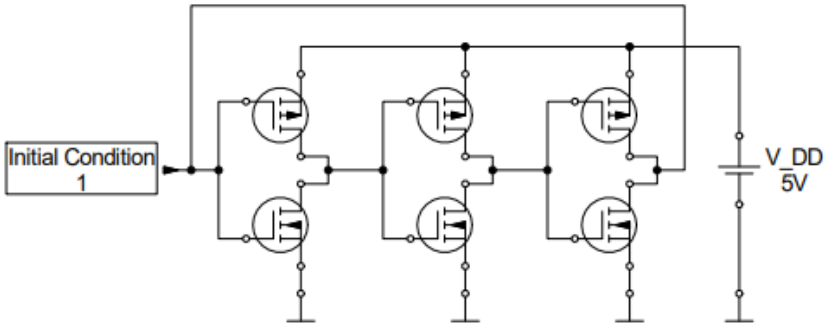


Figure: Inverter Stage

The LTSpice implementation is provided below:

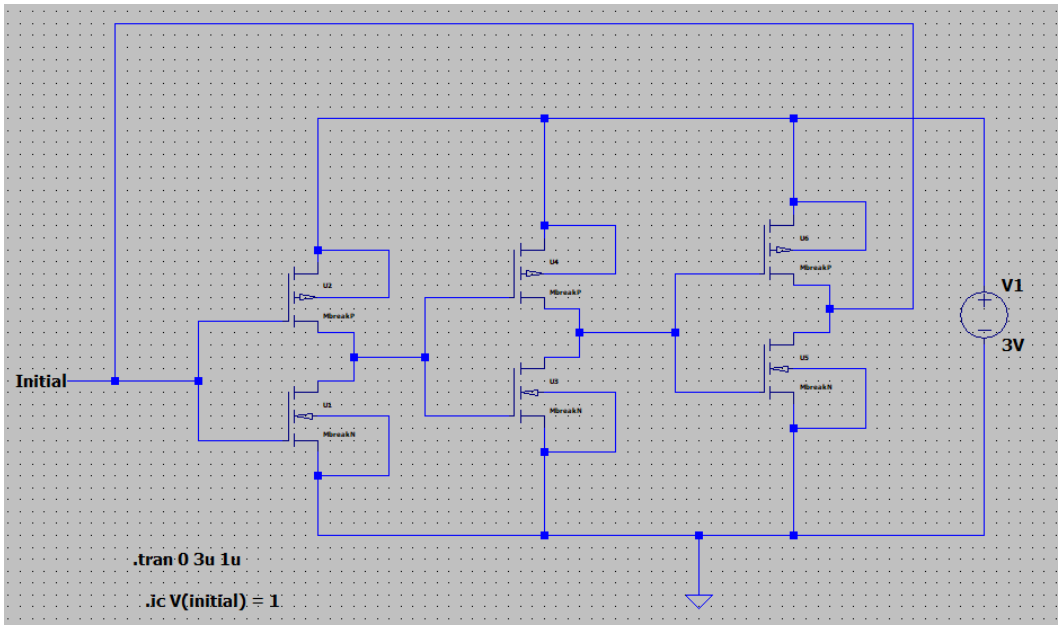


Figure: LTSpice implementation of ring ocsillator

Task 1

We are required to determine the oscillation frequency of the ring oscillator and the propagation delay per inverter stage for supply voltages 3V, 5V, 7V, and 10V.

At V_DD = 3V, we have the following simulation results:

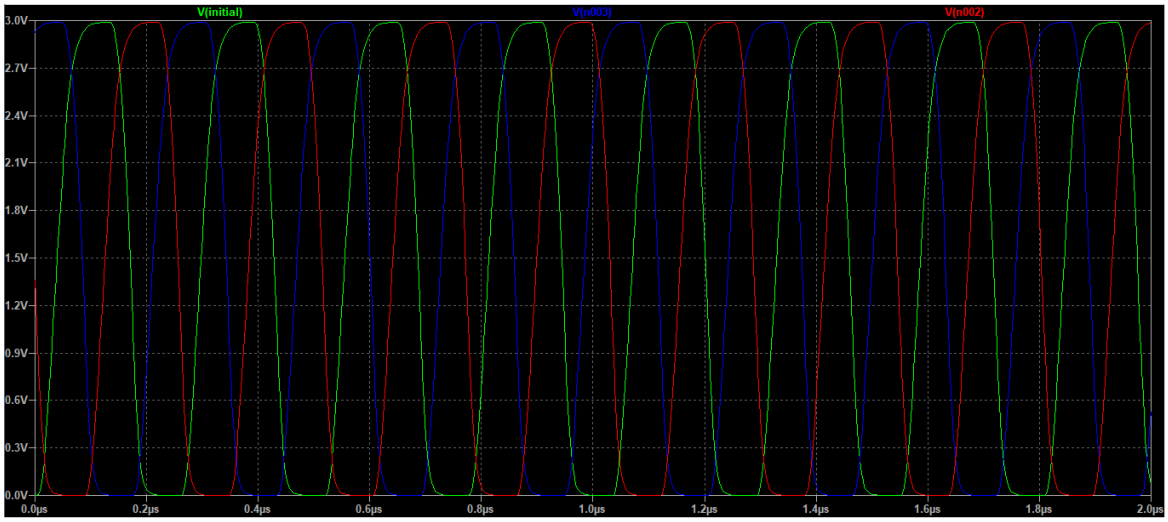


Figure: Simulation for 3V supply

$$f_1 = 3.8786982MHz$$

At V_DD = 5V, we have the following simulation results:

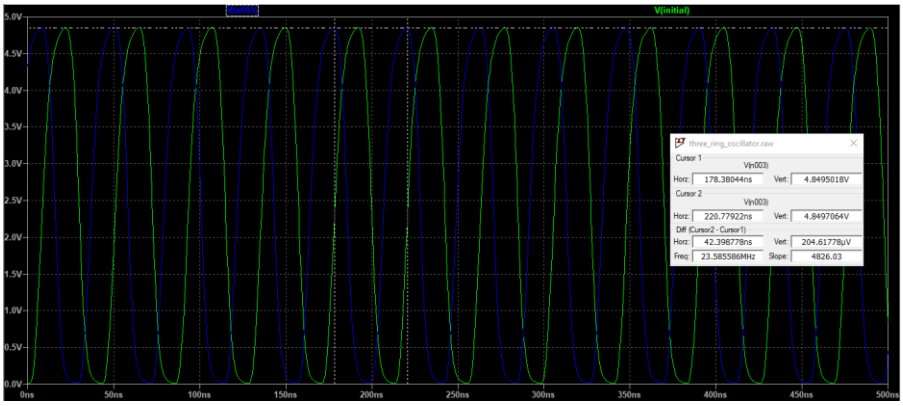


Figure: Simulation for 5V supply

$f_2 = 23.585586MHz$

At V_DD = 7V, we have the following simulation results:

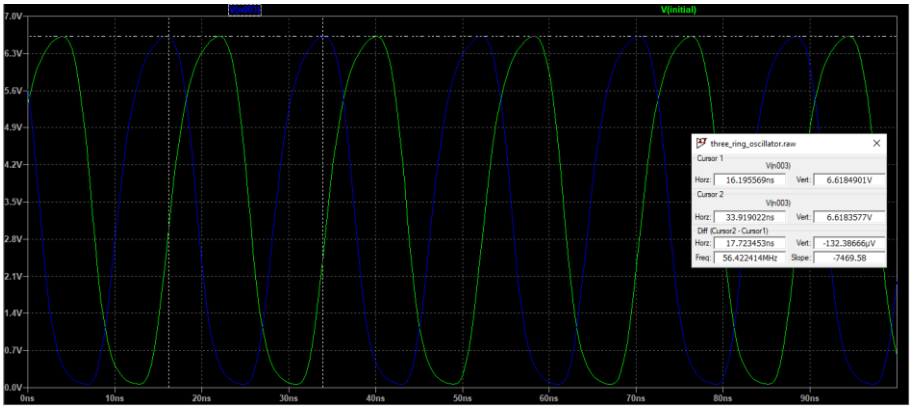


Figure: Simulation for 7V supply

$f_3 = 56.422414MHz$

At V_DD = 10V, we have the following simulation results:

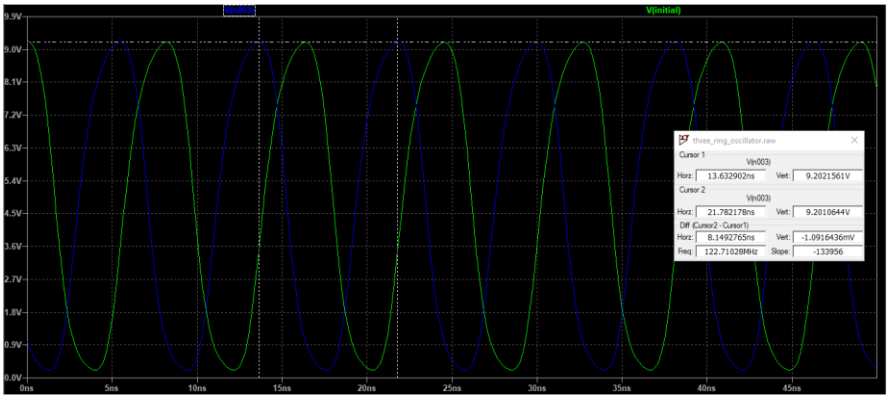


Figure: Simulation for 10V supply

$f_4 = 122.71028MHz$

Propagation delay per inverter stage:

$$t_d = \frac{1}{2 \times N \times f}$$

V_{DD}	Frequency	t_d
3V	$3.8786982MHz$	42.966 ns
5V	$23.585586MHz$	7.0665ns
7V	$56.422414MHz$	2.9539ns
10V	$122.71028MHz$	1.3582ns

Task 2

$$P_D = f \times C \times V_{DD}^2$$

We use C = 5 pF, based on the datasheet.

V_{DD}	Frequency	P_D
3V	$3.8786982MHz$	0.17454 mW
5V	$23.585586MHz$	2.94820 mW
7V	$56.422414MHz$	13.82349 mW
10V	$122.71028MHz$	61.35514 mW

Task 3

For this task, we add a 50 pF load capacitor to each inverter of the 3-stage ring oscillator. We set V_DD = 5V. The final implementation is provided below:

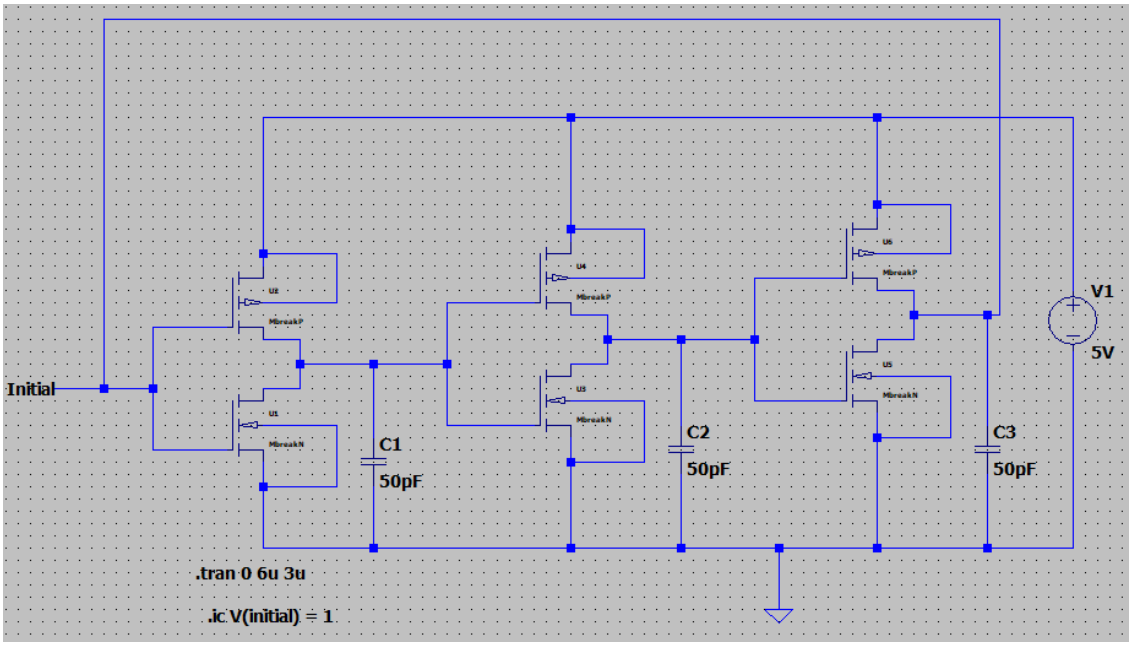


Figure: 3-stage ring oscillator with capacitors

Simulation results are provided below:

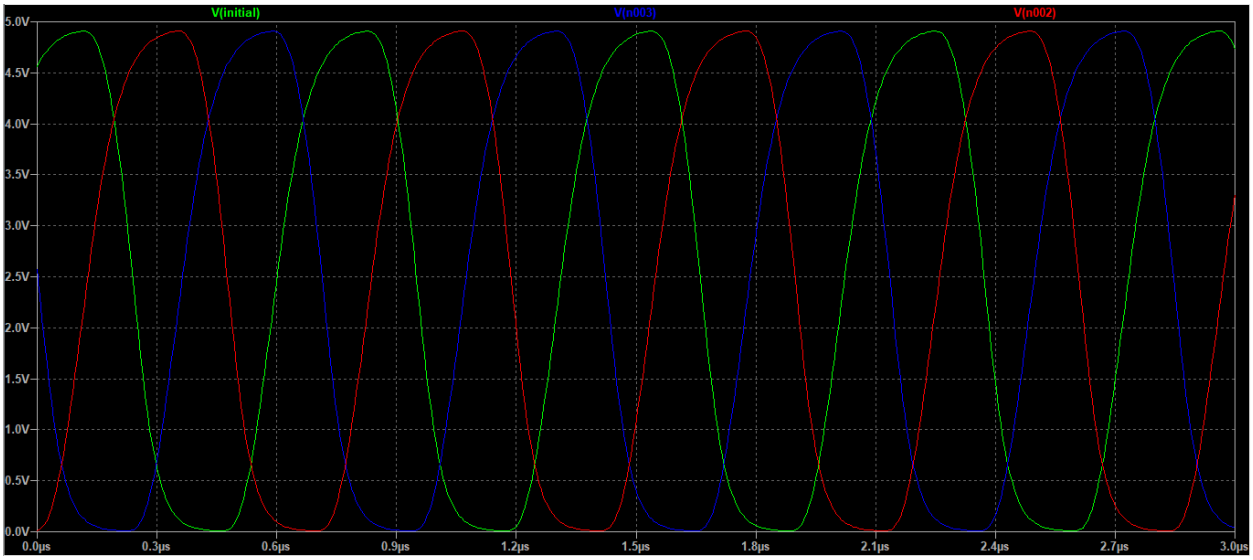


Figure: Simulation results for 3-stage ring oscillator

Determination of the frequency was carried out using the cursors:

$$f = 1.4142395MHz$$

The propagation delay is determined as follows:

$$t_d = \frac{1}{2 \times N \times f} = \frac{1}{2 \times 3 \times 1.4142395MHz} = 1.1784897 \times 10^{-7}s = 117.849\,ns$$

The dynamic power dissipation is determined as follows:

$$P_D = f \times C \times V_{DD}^2 = 1.4142395MHz \times 50 \times 10^{-12} \times 5^2 = 1.768 \times 10^{-3}W = 1.768mW$$

Task 4

Presence of capacitive load results in an increase of propagation delay and decrease of oscillation frequency.

Task 5

We saw that increasing the power supply increases the frequency of the output, and increasing the load capacitance decreases the frequency. Frequency is directly proportional to power dissipation. Therefore, using the load capacitance lowers the power dissipation without any manipulation of the power supply.

Experimental Data and Results

Problem 1: Voltage transfer characteristic of an Inverter

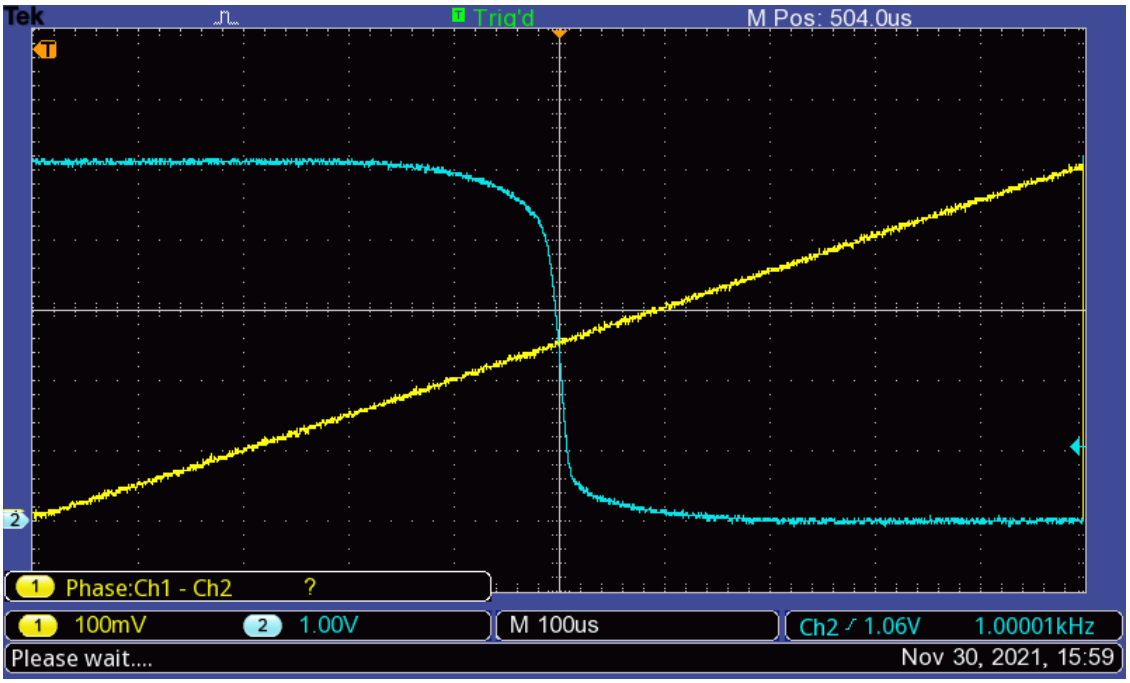
Task 1

Instructions:

To display the VTC we need two steps. In the lab first we measure Vin and Vout for one switch-on event. In the second step in the evaluation MatLab is used to display and measure the VTC parameters.

- Generate a ramp signal with 0 to 5V and f = 1 KHz. Check that the waveform is correct before applying it to the inverter.
- Connect the input of the inverter to Channel 1 and the output to Channel 2. Show one Vin ramp together with Vout on the screen! Use the measure function to determine the properties of the signals.
- Take a hardcopy. Take care that you not only got the picture, but also the complete data set for Ch1 and Ch2 (the *.CSV files)!

Results:



Problem 2: Propagation Delay of an Inverter

Instructions:

Connect the oscilloscope to the input and the corresponding output of the first inverter.

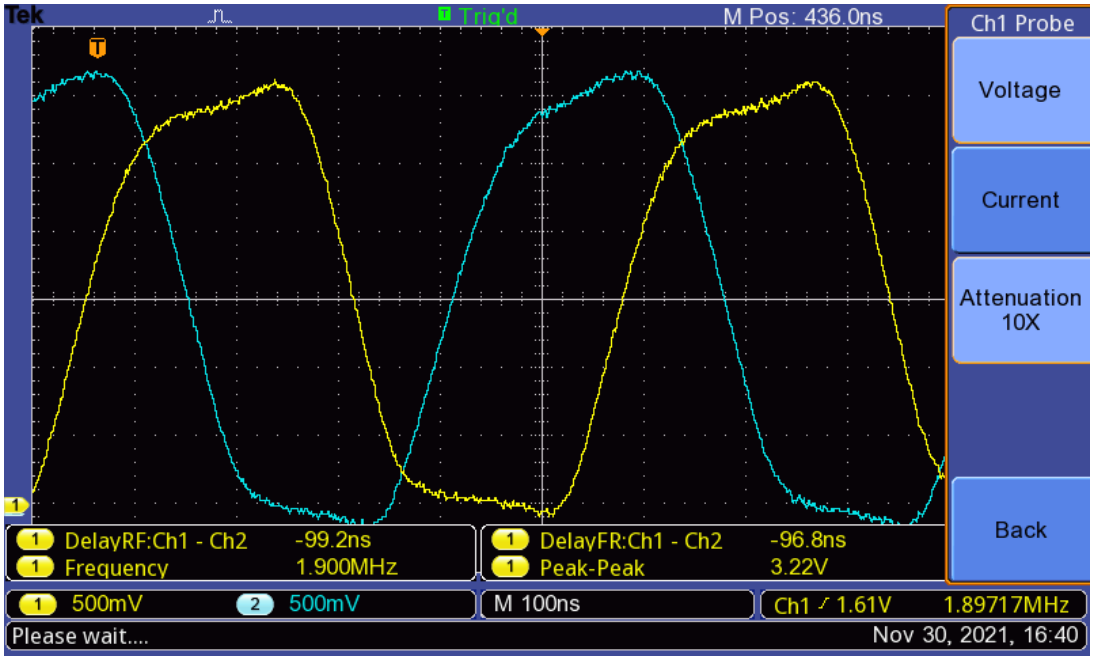
Note: The propagation delay determined by this method is not very accurate, as the probe capacitance has an influence on the measurement. To minimize the effect, the 10x high impedance probe should be used in the measurement.

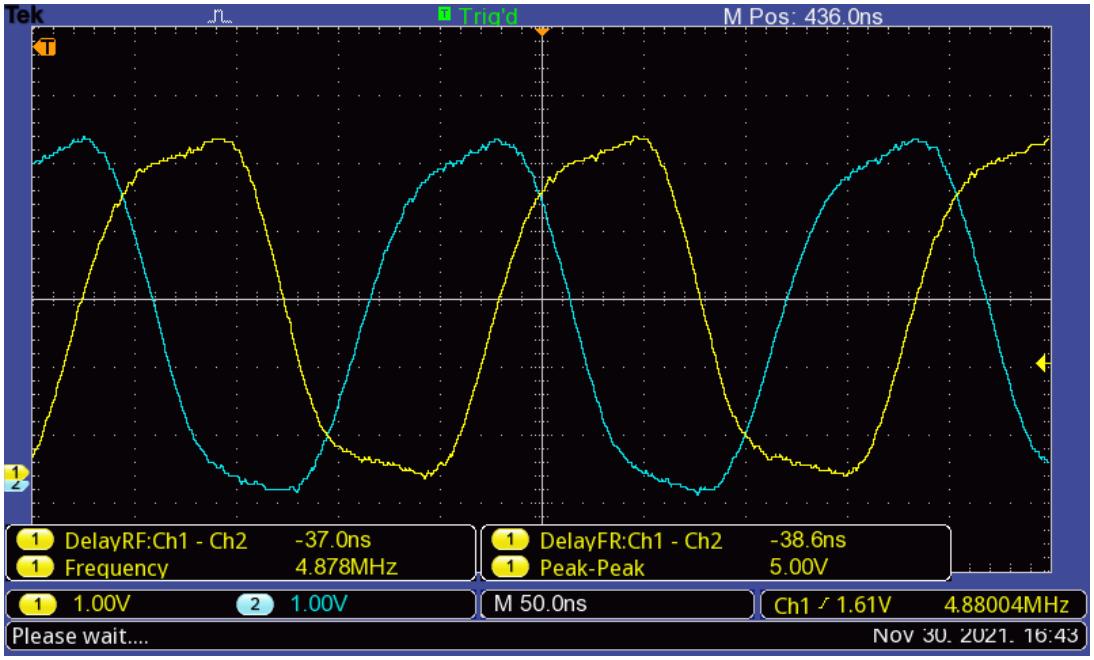
1. Measure the oscillation frequency and propagation delay tP LH and tP HL of the first inverter at 3V, 5V, 7V, and 10V. Take hard copies for the different measurements!

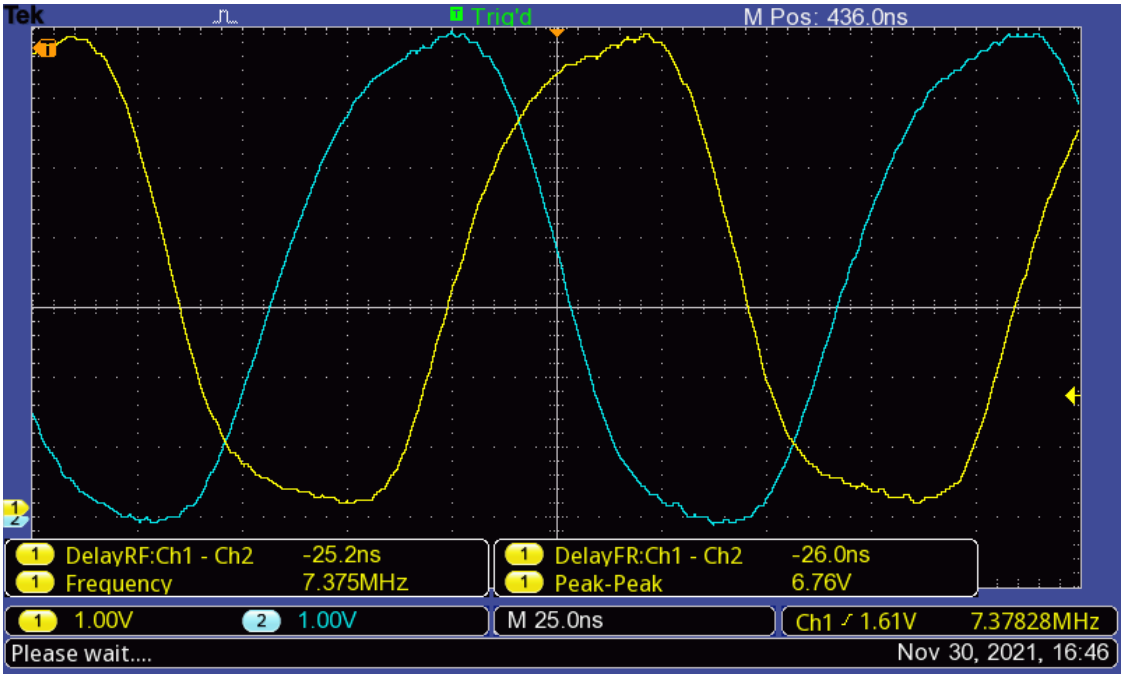
2. Add load capacitors to each of the three output nodes of the 3-stage ring oscillator. The load capacitors should have a capacitance value of 1.5nF.

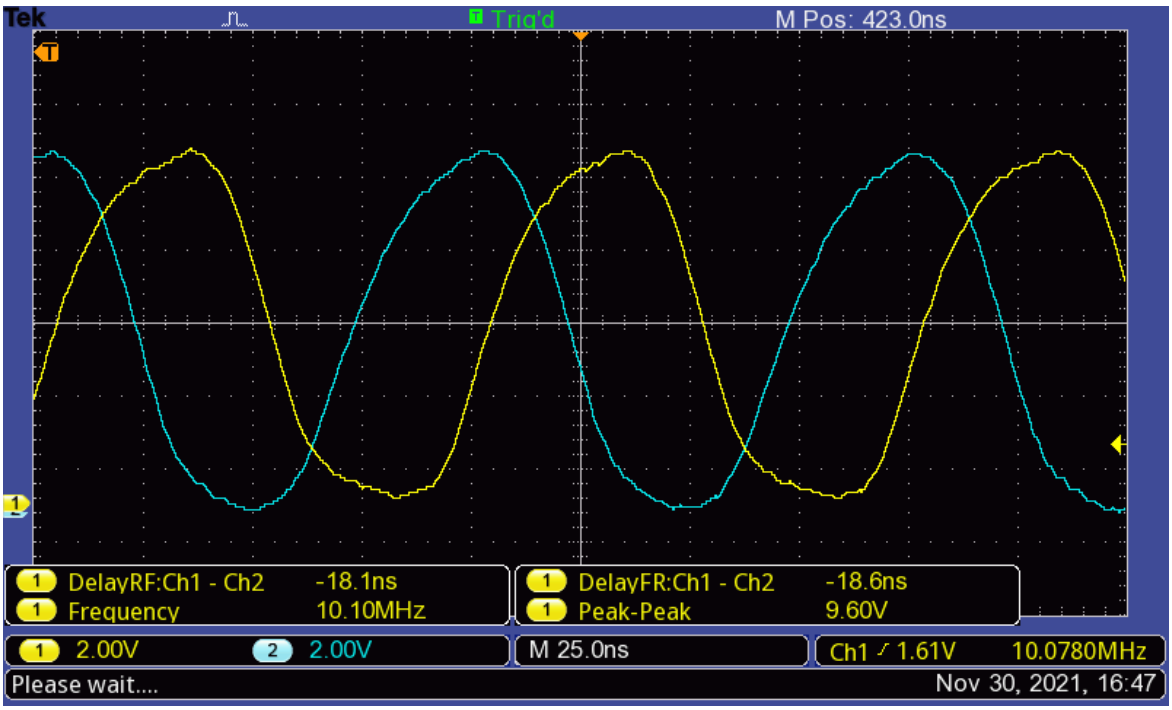
3. Measure the oscillation frequency and the propagation delay tP LH, tP HL for the first inverter at VDD = 5V.

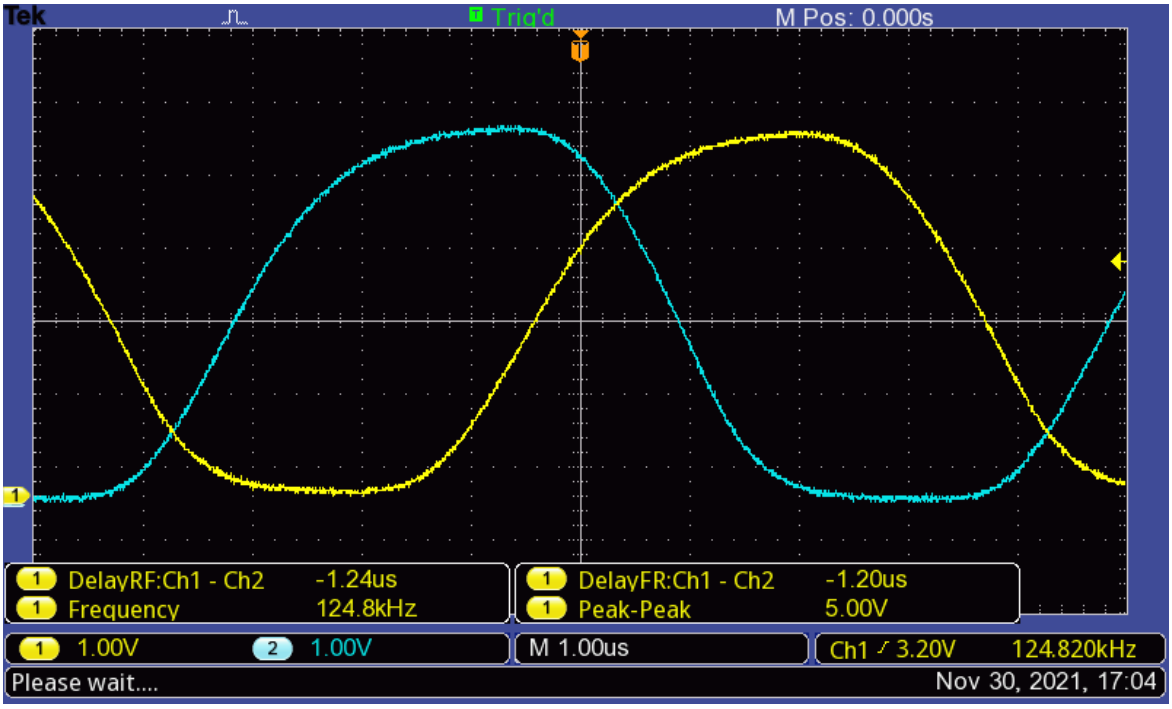
Results:




Tek
Trig'd
M Pos: 436.0ns
DelayRF:Ch1 - Ch2 -37.0ns
Frequency 4.878MHz
DelayFR:Ch1 - Ch2 -38.6ns
Peak-Peak 5.00V
1.00V
1.00V
M 50.0ns
Ch1 ⁄ 1.61V 4.88004MHz
Please wait....
Nov 30. 2021. 16:43


Tek
Trig'd
M Pos: 436.0ns
DelayRF:Ch1 - Ch2 -25.2ns
Frequency 7.375MHz
DelayFR:Ch1 - Ch2 -26.0ns
Peak-Peak 6.76V
1.00V
1.00V
M 25.0ns
Ch1 ⁄ 1.61V 7.37828MHz
Please wait....
Nov 30, 2021, 16:46


Tek
Trig'd
M Pos: 423.0ns
1 DelayRF:Ch1 - Ch2 -18.1ns
1 Frequency 10.10MHz
1 DelayFR:Ch1 - Ch2 -18.6ns
1 Peak-Peak 9.60V
1 2.00V 2 2.00V
M 25.0ns
Ch1 ⟋ 1.61V 10.0780MHz
Please wait....
Nov 30, 2021, 16:47


Tek
Trig'd
M Pos: 0.000s
1 DelayRF:Ch1 - Ch2 -1.24us
1 Frequency 124.8kHz
1 DelayFR:Ch1 - Ch2 -1.20us
1 Peak-Peak 5.00V
1 1.00V 2 1.00V
M 1.00us
Ch1 ⟋ 3.20V 124.820kHz
Please wait....
Nov 30, 2021, 17:04