Report 3 : 93%
Prelab 3 : 95%
Prelab 4 : 99%

Jacobs University Bremen

CO-526-B
Electronics Lab

Fall Semester 2021

Lab Experiment 3 - BJT

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Contents

1 Introduction

1.1 Theory

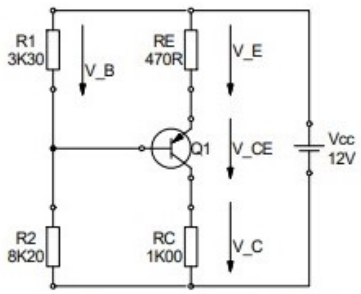
The objective of the experiment is to familiarize with bipolar junction transistors (BJTs). The lab introduces the properties and behaviors of BJTs. The output characteristics of a common-emitter based BJT circuit will be observed. The transistor will be applied as an amplifier and the voltage gain frequency response, and phase relation between the input and output voltages of a common-emitter amplifier will be analyzed.

A BJT is a three terminal semiconductor device. It is widely used in discrete circuits as well as in integrated circuits. The main applications of BJTs are analog circuits. For example, BJTs are used for amplifiers in particular for high-speed amplifiers. There are three operating modes for BJTs, the active mode (amplifying mode), the cut-off mode and the saturation mode. To apply a BJT as an amplifier, the BJT has to operate in the active mode. To apply a BJT as a digital circuit element, the BJT has to operate in the cut-off mode and the saturation mode.

1.2 Prelab BJT

1.2.1 Problem 1 : Biasing of Bipolar Junction Transistors

Considering the following circuit:



$\beta = 100$ and $V_{BE} = -0.7V$

Question 1

Calculating the Thevenin equivalent of the circuit:

$$V_{th} = V_{CC}\frac{R_2}{R_1 + R_2} = 12\frac{8200}{3300 + 8200} = 8.556V$$

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{3300 \times 8200}{3300 + 8200} = 2353\Omega$$

The emitter current is mathematically obtained:

$$I_E = I_C + I_B = \beta \times I_B + I_B = I_E = (1+\beta)I_B$$

Thevenin voltage:

$$V_{th} = V_{CC} - I_{th}R_{th} - I_E R_E - V_{EB} = V_{CC} - I_B R_{th} - (1+\beta)I_B R_E - V_{EB}$$

V_B, V_{BE}, V_C, V_{CE}, V_E, I_B, and I_C can then be determined as follows:

$$\boxed{I_B = \frac{V_{CC} - V_{EB} - V_{th}}{(1+\beta)R_E + R_{th}} = \frac{12 - 0.7 - 8.556}{470 \times 101 + 2353} = 55.075\mu A}$$

$$\boxed{I_C = \beta \times I_B = 100 \times 55.075 \times 10^{-6} = 5.507mA}$$

$$\boxed{I_E = (1+\beta) \times I_B = 101 \times 55.075 \times 10^{-6} = 5.563mA}$$

$$\boxed{V_C = R_C \times I_C = 1000 \times 5.507 \times 10^{-3} = 5.507V}$$

$$\boxed{V_E = R_E \times I_E = 470 \times 5.563 \times 10^{-3} = 2.614V}$$

$$\boxed{V_B = V_{CC} - V_{EB} - V_E = 12 - 0.7 - 2.614 = 8.686V}$$

$$\boxed{V_{CE} = V_{CC} - V_C - V_E = 12 - 5.507 - 2.614 = 3.878V}$$

Question 2

Using the same circuit and defining the parameters to:

$$V_{CE} = 8V \quad I_C = 8mA \quad V_{CC} = 20V \quad \beta = 150 \quad V_E = 4V \quad R_{th} = 0.1\beta \times R_E$$

Obtaining R_C.

$$R_C = \frac{V_C}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20 - 8 - 4}{8 \times 10^{-3}} = 1000\Omega$$

Obtaining R_E.

$$R_E = \frac{V_E}{I_E} = \frac{V_E}{I_C + I_B} = \frac{V_E}{I_C + \frac{I_C}{\beta}} = \frac{4}{8 \times 10^{-3} + \frac{8 \times 10^{-3}}{150}} = 496.689\Omega$$

Obtaining R_1 and R_2.

$$V_{th} = V_{CC} - V_E - V_{EB} - I_B R_{th} = 20 - 4 - 0.7 - 53.333 \times 10^{-6} \times 7450.331 = 14.903V$$

$$V_{th} = V_{CC}\frac{R_2}{R_1 + R_2} \quad \Rightarrow \quad = \frac{V_{th}}{V_{CC}} = \frac{R_2}{R_1 + R_2} = \frac{14.903}{20} = 0.745$$

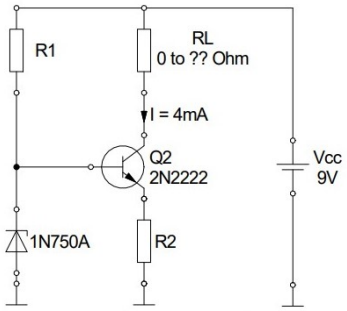
$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = R_1\frac{V_{th}}{V_{CC}} \quad \Rightarrow \quad \boxed{R_1 = \frac{R_{th}}{V_{th}/V_{CC}} = \frac{7450.331}{0.745} = 9998.667\Omega}$$

$$\frac{V_{th}}{V_{CC}} = \frac{R_2}{R_1 + R_2} \quad \Rightarrow \quad \boxed{R_2 = R_1\frac{V_{th}/V_{CC}}{1 - V_{th}/V_{CC}} = 9998.667\frac{0.745}{1 - 0.745} = 29232.168\Omega}$$

1.2.2 Problem 2 : Constant Current Source

Question 1

Considering the following circuit:



$V_{BE} = 0.7V$

Question 2

Applying KVL to the outer loop:

$$V_1 = V_{CC} - V_Z = 9 - 4.7 = 4.3V$$

I_B is negligible compared to I_C and I_E. We also know that $I_E = I_C + I_B$, so we can assume that $I_E = I_C$ or $I_B \approx 0$.

Therefore,

$$I_1 = I_Z - I_B \approx I_Z = 20mA$$

$$\boxed{R_1 = \frac{V_1}{I_1} = \frac{4.3}{20 \times 10^{-3}} = 215\Omega}$$

Applying KVL to the left bottom loop gives:

$$V_E = V_z - V_{BE} = 4.7 - 0.7 = 4V$$

$$I_E \approx I_C = 4mA$$

$$\boxed{R_2 = \frac{V_E}{I_E} = \frac{4}{4 \times 10^{-3}} = 1000\Omega}$$

Question 3

Obtaining R_1 and R_2 to get a constant current of $I_C \approx 4mA$.

$$V_Z = const \quad \Rightarrow \quad V_E = const \quad \Rightarrow \quad I_E = const \quad \Rightarrow \quad I_C = const$$

KVL for the right loop gives the following:

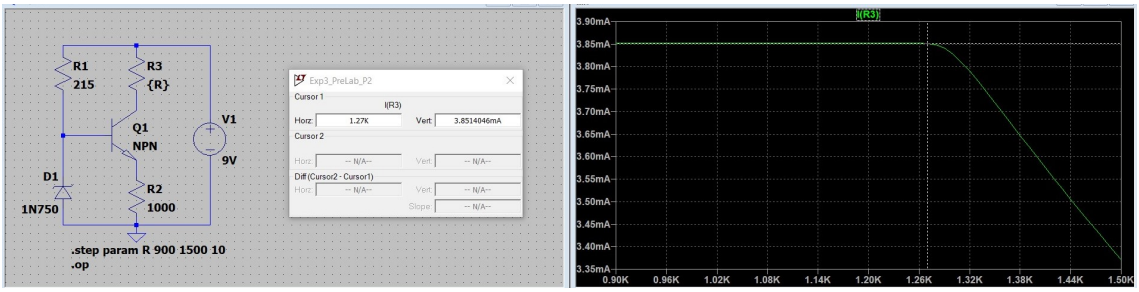
$$V_C = V_{CC} - V_E - V_{CE} = 9 - 4 - 1 = 4V$$

Obtaining maximum value for R_L,

$$\boxed{R_L = \frac{V_C}{I_C} = \frac{4}{4 \times 10^{-3}} = 1000\Omega}$$

Question 4

The experimental value for the maximum load voltage to keep a constant collector current is around 1250Ω. This is due to the fact that the value of V_{CE} used by LT Spice is very small, whereas the one used in our claculations was $1V$.



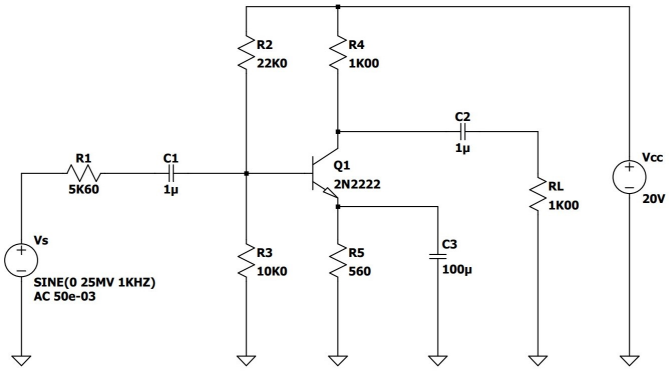
Question 5

In the circuit above, as long as the current flowing through the Zener diode is above the Zener current, the voltage across the diode will remain constant. It is then safe to assume the V_E remains constant given the fact that the base emitter voltage of the transmitter is always $0.7V$. In this case, the emitter and collector currents also remain constant as long as the load resistance stays below the maximum resistance calculated previously.

1.2.3 Problem 3 : Amplifier circuit

Question 1

LTspice was used to implement the following circuit:



LTSpice simulations?

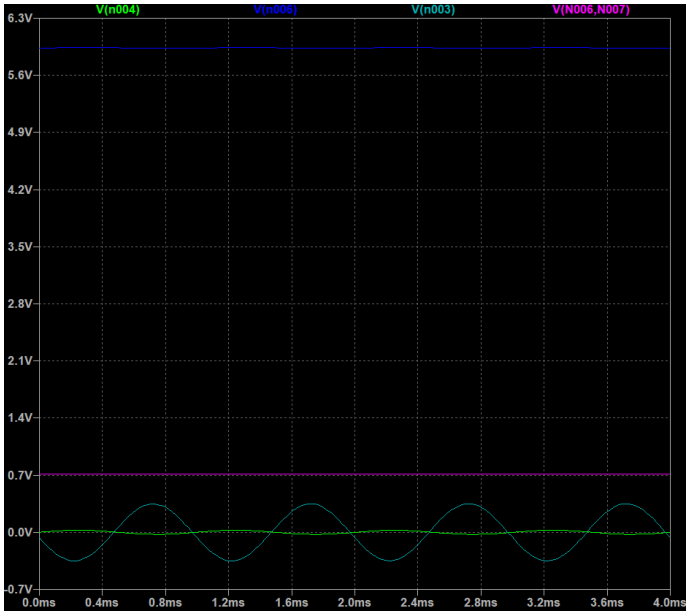
Question 2

A DC operation point simulation was performed to obtain V_B, V_{BE}, V_C, V_{CE}, V_E, I_B, and I_C.

V_B	5.93659 V
V_{BE}	714.57 mV
V_C	10.7206 V
V_{CE}	5.5058 V
V_E	5.22198 V
I_B	45.5586 µA
I_E	9.32497 mA

Question 3

A transient analysis simulation was performed for about 2 cycles of a sinusoidal input signal. Using $V_s = 50mV_{pp}$ input amplitude and $f = 1KHz$. V_S, V_B, V_{BE}, and the voltage across the load resistance R_L are displayed.

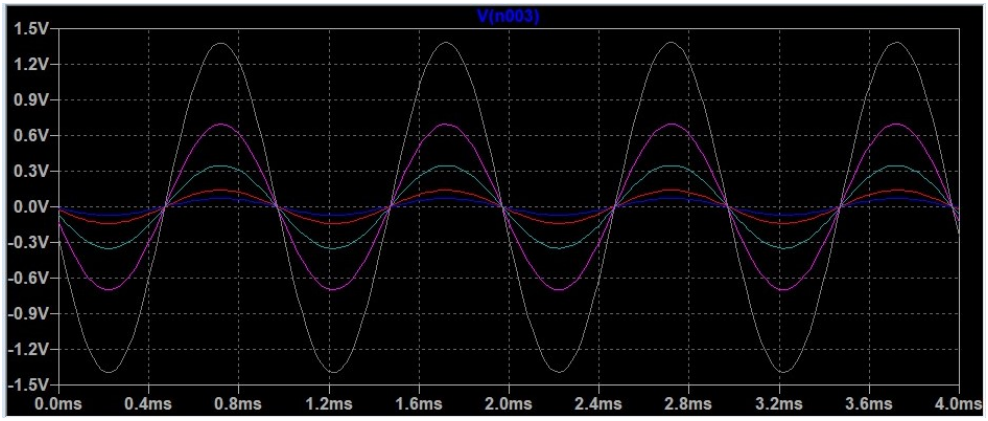


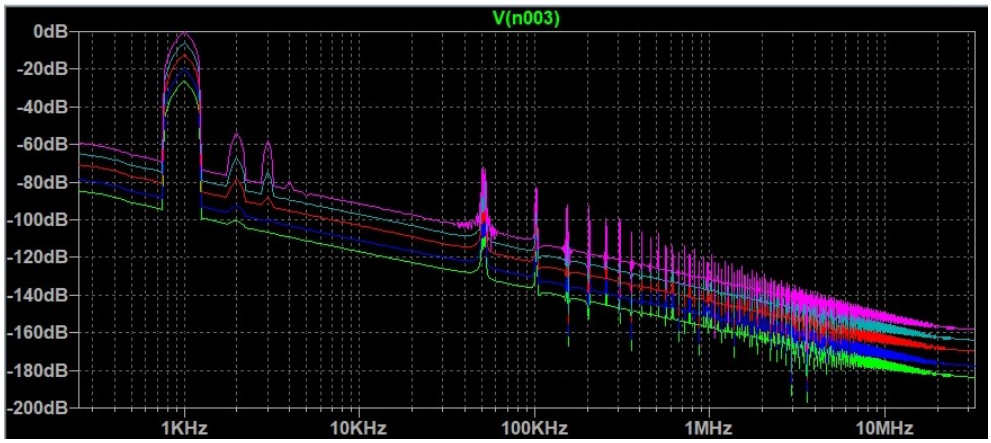
The voltage gain can be determined as follows:

$$\frac{V_{out}}{V_{in}} = \frac{697mV}{50mV} = 13.94$$

Question 4

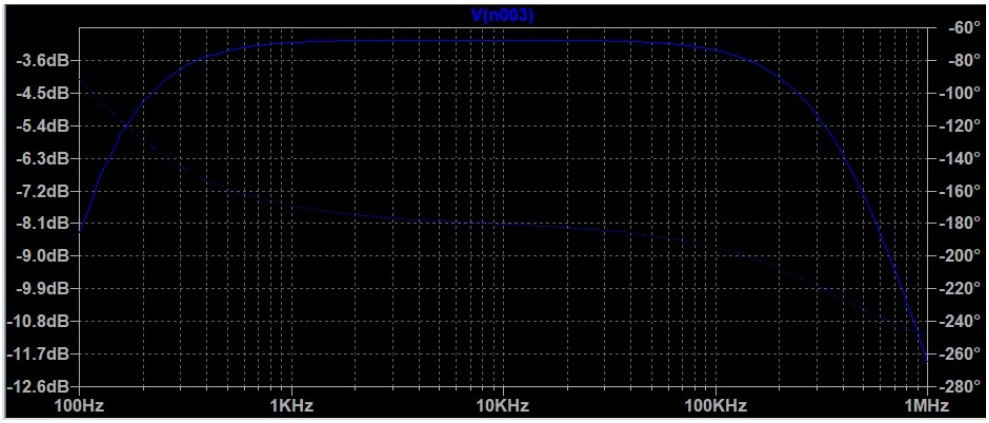
The quality of the amplified signal is determined using the .step command and varying the input voltage by $10mV_{pp}$, $20mV_{pp}$, $50mV_{pp}$, $100mV_{pp}$, and $200mV_{pp}$. The FFT shows the distortion of the signal.





It can be observed that as the amplitude of sinusoidal input signal increases, the voltage over the load decreases, i.e the gain of the amplifier decreases. This distortion however cannot be distinguished from the signal in the time domain.

Question 5



Question 6

The LTSpice .measure command was used to determine the lower and upper $-3dB$ frequencies and the bandwidth.

$$lower f_{-3dB} = 145.154Hz$$

$$upper f_{-3dB} = 384870Hz$$

$$B = 384725Hz$$

2 Experimental Setup and Results

Workbench No 4:

Used tools and instruments:

- AC Voltage Generator
- TENMA multimeter
- Oscilloscope
- BNC-to-Kleps cable
- Voltage probes
- breadboard
- diode
- capacitor
- resistor

2.1 Problem 1 : Determine Type and Pin Assignment of a Bipolar Transistor

2.1.1 Part 1: Setup

A bipolar junction transistor and the TENMA multimeter were used for this part of the experiment.

2.1.2 Part 2: Execution and results

1. Determination of the base using the multimeter in diode test mode.

Multimeter leads connected to BJT		Diode check value
+ Terminal	Gnd Terminal	-
1	2	.0L
2	1	0.7315 V
1	3	.0L
3	1	.0L
2	3	0.7244 V
3	2	.0L

Terminal 2 is the base of the transistor.

2. Determination of the type of BJT by connecting the the COM lead of the multimeter to the base and the positive lead to each of the remaining terminals.

   In our case, both readings showed $.0L$ which means that the transistor provided for the experiment is of type NPN.

3. Determination of the emitter and collector terminals by connecting the positive lead of the multimeter to the base and the COM lead to the remaining terminals.

+ Terminal	Voltage	Type
1	0.7348	Emitter
3	0.7334	Collector

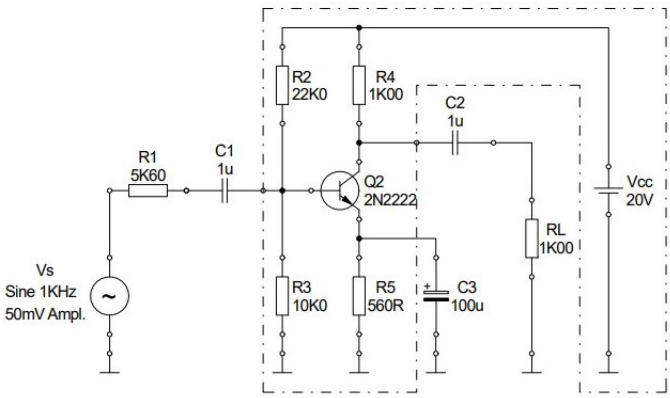
Conclusion:

Transistor type	NPN
Base Terminal	2
Emitter Terminal	1
Collector Terminal	3

2.2 Problem 2 : Operating point of BJTs

2.2.1 Part 1: Setup

The following circuit (dashed area) was assembled on the breadboard.



2.2.2 Part 2: Execution and results

V_{cc}	20.056 V
V_B	6.002 V
V_C	10.518 V
V_E	5.357 V
V_{BE}	0.636 V
V_{CE}	5.131 V

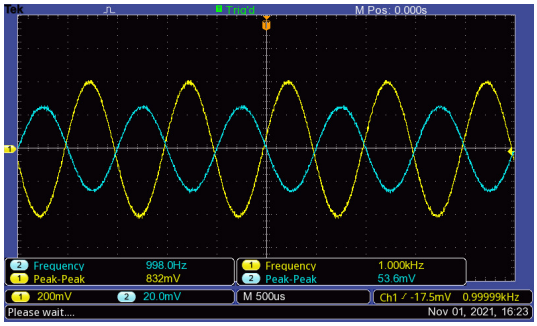
2.3 Problem 3 : Common emitter circuit

2.3.1 Part 1: Setup

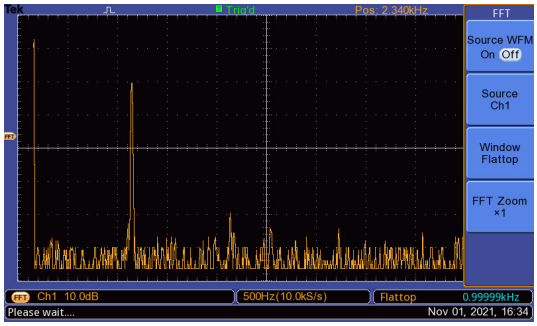
The remaining components of the circuit in Problem 2 were added on the breadboard.

2.3.2 Part 2: Execution and results

The input voltage and the voltage over the load were measured at the oscilloscope. The function generator was initially set to $V_s = 50mV_{pp}$ and $f = 1KHz$, then to $V_s = 100mV_{pp}$, and to $V_s = 200mV_{pp}$.

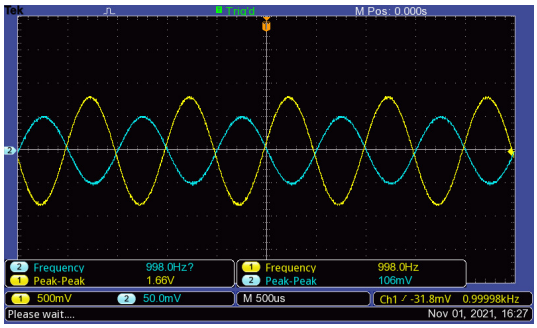


(a) V_s and V_L in the time domain

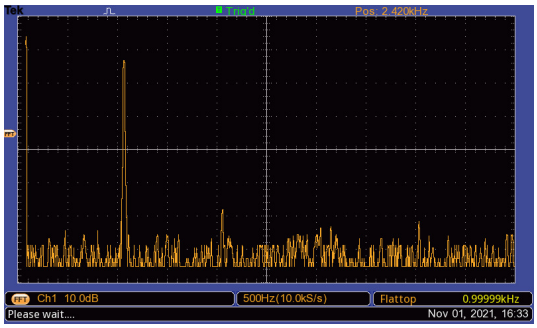


(b) V_L in the frequency domain

Figure 1: $V_s = 50mV_{pp}$

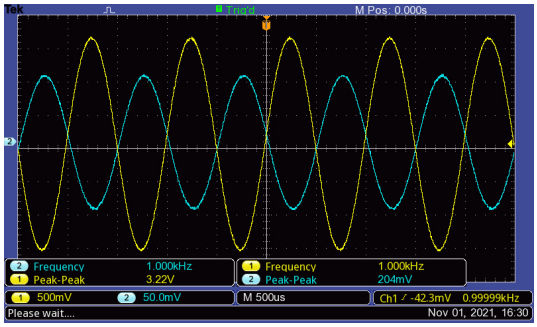


(a) V_s and V_L in the time domain

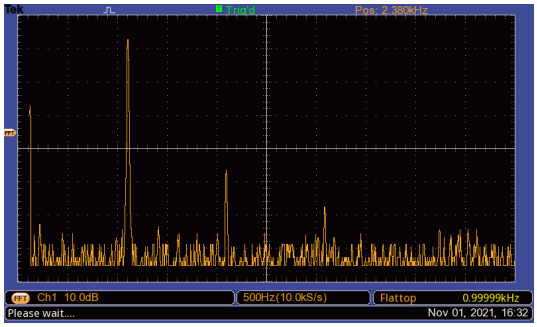


(b) V_L in the frequency domain

Figure 2: $V_s = 100mV_{pp}$



(a) V_s and V_L in the time domain



(b) V_L in the frequency domain

Figure 3: $V_s = 200mV_{pp}$

2.4 Problem 4 : Bandwidth of amplifier circuit

2.4.1 Part 1: Setup

The circuit from Problem 3 was reused and the function generator was set to sweep mode with the following parameters:
START F : 100Hz
STOP F : 1MHz
SWP TIME : 500ms
SWP MODE : logarithmic

2.4.2 Part 2: Execution and results

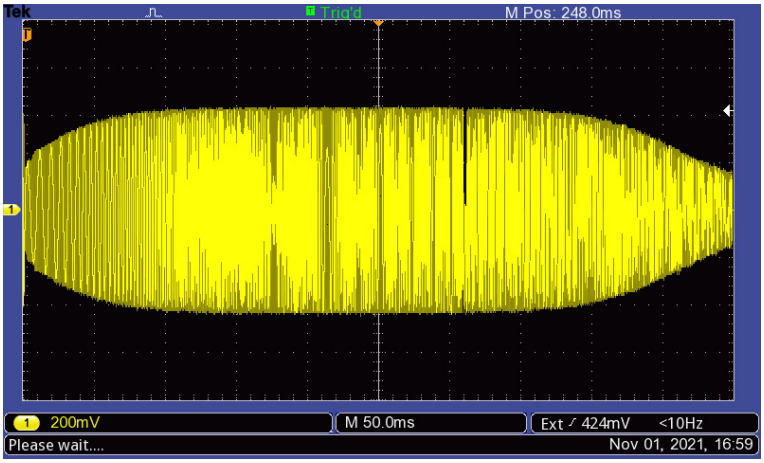


Figure 4: Full sweep of the output signal

The experimental upper and lower $-3dB$ cut-off frequency were as follows:

$$lower f_{-3dB} = 160Hz$$

$$upper f_{-3dB} = 340000Hz$$

3 Evaluation

3.1 Problem 1 : Determine Type and Pin Assignment of a Bipolar Transistor

3.1.1 Question 1

Connecting both leads of the multimeter to the first and third terminals (in both polarities) and getting a $.0L$ reading means that there is no direct movement of charge carriers between the two pins. It is then safe to assume that the first and third pin represent the emitter and collector of the transistor. In this case, the remaining terminal would be the base; i.e the second terminal.

3.1.2 Question 2

The type of the transistor can be determined by connecting the COM lead to the base and the positive lead to the each of the remaining terminals. A $.0L$ reading signifies that the base to emitter and base to collector junctions are reverse biased and the base is represented by an n-type semiconductor whereas the emitter and collector are p-type semidconductors. And vice versa for PNP transistors and voltage drops read at the multimeter.

3.1.3 Question 3

Recording and comparing the base to emitter and base to collector voltage drops helps identifying each terminal because the emitter is more heavily doped than the collector. In this case the voltage drop at the emitter is going to be slightly higher than at the collector.

3.2 Problem 2 : Operating point of BJTs

3.2.1 Question 1

	Experiment	Simulation
V_{cc}	20.056 V	20 V
V_B	6.002 V	5.93659 V
V_C	10.518 V	10.7206 V
V_E	5.357 V	5.22198 V
V_{BE}	0.636 V	0.71457 V
V_{CE}	5.131 V	5.5058 V

We can see from the table above that the experimental and theoretical values are fairly close and confirm each other. why are differences? what are the differences?

3.2.2 Question 2

The current emitter gain can be expressed mathematically as follows:

$$\beta_m = \frac{I_C}{I_B}$$

The base and collector currents can be found using the following formulas:

$$I_B = \frac{V_{TH} - V_E - V_{BE}}{R_{TH}} = \frac{20.056\frac{10\times10^3}{(10+22)\times10^3} - 5.5357 - 0.636}{6875} = 1.39 \times 10^{-5} A$$

$$I_C = \frac{V_C}{R_C} = \frac{10.518}{1000} = 1.0518 \times 10^{-2} A$$

The current emitter gain is:

$$\beta_m = \frac{1.0518 \times 10^{-2}}{1.39 \times 10^{-5}} = 756.69$$

3.2.3 Question 3

To determine the relative error of the emitter current gain, one has to calculate the theoretical gain using the values obtained from the simulation.

$$\beta_t = \frac{I_C}{I_B} = \frac{9.27939mA}{45.5586\mu A} = 203.68$$

$$E_{\%} = \left|\frac{\beta_m - \beta_t}{\beta_t}\right| \times 100 = \frac{756.69 - 203.68}{203.68} \times 100 = 271\%$$

The result relative error is a lot greater than initially expected. The error likely stems from the lack of precision from the measurement devices as to the fact that the base to emitter voltage is measured in mV and a slight change in that value changes the gain completely. It is also possible that the lack of precision from the parameters of the components in the circuit would be an error source.

One way to avoid this error would be to repeat the measurements multiple times to average out the error.

you should have used error propagation using the measured values!!
Then the error is still big but less then yours! ~30%

3.3 Problem 3 : Common emitter circuit

3.3.1 Question 1

When the distorted amplitude is positive, the circuit is in saturation mode. However, if the circuit is in cutoff mode, the distorted amplitude is negative. That can be observed because if the signal was not distorted, the output signal would be a replica of the input but with a bigger gain. It is not the case here, and the output waveform is inverted.

3.3.2 Question 2

The voltage gain can be mathematically expressed as follows:

$$A_v = \frac{1.66}{0.106} = 15.66$$

The error is below 10%. Therefore the simulated and experimental values of the voltage gain can be considered as very similar.

3.3.3 Question 3

It can be deduced from the hardcopies that there is a 180°phase shift between the input and output signals. This is due to the base and collector current relationship.

As one can see in the following equation:

$$V_{cc} = I_c R_c + V_L$$

If the collector current increases due to an increase of the base current and voltage, the load voltage becomes negative.

3.3.4 Question 4

In the experimental results, we can see that as the amplitude increases, additional peaks appear in the FFT. That was expected as the simulation showed similar behavior as the quality of the amplification decreases with the increase of the input amplitude.

reason for harmonics?

3.4 Problem 4 : Bandwidth of amplifier circuit

3.4.1 Question 1

The bandwidth of the amplifier was observed at the oscilloscope (as seen in the hardcopies). It can be observed that the amplifier lowers the gain for low and high frequencies almost behaving like a bandpass filter. The lower cutoff is a consequence of the capacitor rather than the BJT. However, the higher cutoff is due to the fall of gain of

the transistor at high frequencies as a result of the internal capacitance of the BJT. This effect was also observed in the simulation.

3.4.2 Question 2

$$lower f_{-3dB} = 160Hz$$

$$upper f_{-3dB} = 340000Hz$$

$$B = 339840Hz$$

3.4.3 Question 3

The bandwidth obtained via the simulation was around $384725Hz$. the experimental bandwidth is $339849Hz$. The disparity between both results is reasonable given the fact that the determination of the experimental cutoff frequencies at the oscilloscope was rather approximate.

what are the differences?? I think the differences could be explained for all problems in one short paragraph!!

4 Conclusion

The objective of the experiment was to familiarize with bipolar junction transistors (BJTs). The lab introduced the properties and behaviors of BJTs. The output characteristics of a common-emitter based BJT circuit were be observed. The transistor was be applied as an amplifier and the voltage gain frequency response, and phase relation between the input and output voltages of a common-emitter amplifier was analyzed.

The main deductions that were made from the experiments were:

- The transistor terminals and type can be identified using a multimeter in diode check mode. Measuring and recording the values between the combinations of two terminals at the multimeter allows us to determine the base of the transistor. Connecting the COM lead to the identified base and the positive lead to the remaining terminals allows us to determine the type of the transistor. Measuring the base to emitter and base to collector voltage drop allows us to identify the emitter and collector terminals.
- As much as the experimental and simulation results for the operating points of the BJT looked similar. A slight disparity in some of the values resulted in a greater than expected error in the current gain of our circuit.
- There is an inverse relationship between the input and output signals of the circuit analyzed in Problem 3, which is due to the base and collector current relationship.
- It has been established in the simulation and experimentally that the quality of the amplification decreases with the increase of the input amplitude.
- The circuit observed in Problem 4 showed that the circuit exhibits a bandpass behavior.

There were some errors and disparities between the simulation and the experimental results (especially for the current gain). That can be due to the low precision of the measurement devices, or the lack of precision of the parameters of the components used to build the circuits, as well as the resolution of the oscilloscope.

5 References

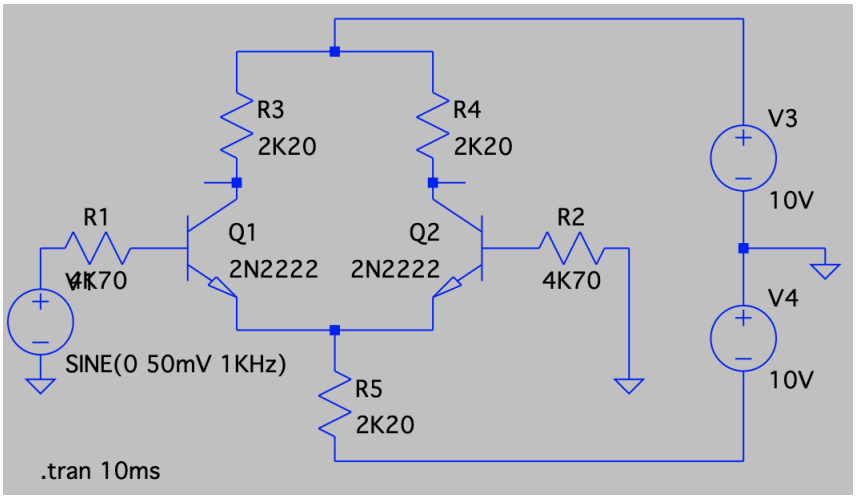
- Electronics Lab Manual (Uwe Pagel)
- http://www.faculty.jacobs-university.de/upagel/

6 Appendix

6.1 Prelab Operational Amplifier

6.1.1 Problem 1 : Simulate a Differential Amplifier

The circuit given in the lab manual was implemented in LTSpice



Question 1

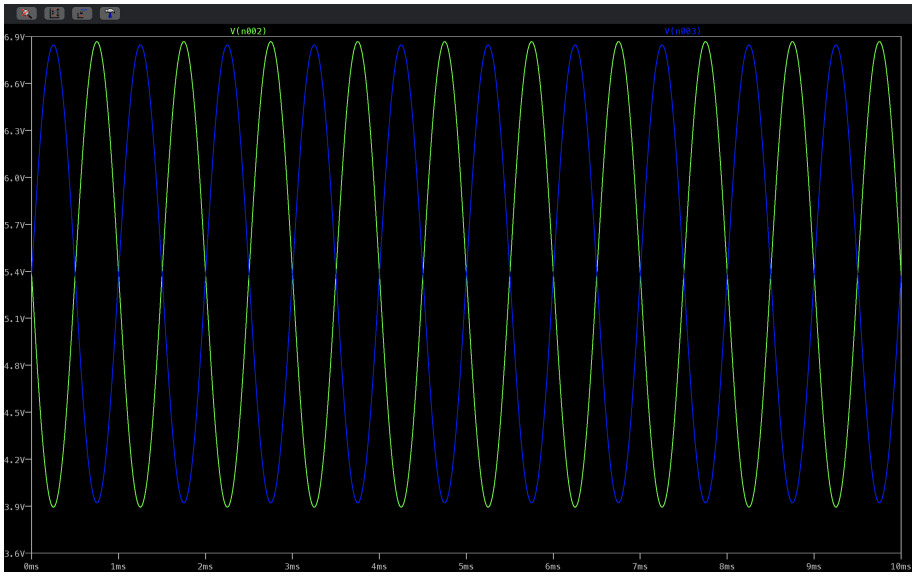
V_1 and V_2 were replaced with grounds. The simulation results were as follows:

	T_1	T_2
V_{BE}	-673.622V	-673.622V
V_C	5.382V	5.382V
I_C	2.099mA	2.099mA
I_E	2.109mA	2.109mA
I_RE	4.218mA	

If the transistors are not absolutely identical, the results from each transistors would be different. In our case, the transistors are identical, so we can see from the table above that values for T_1 and for T_2 are exactly equal.

Question 2

V_1 is set to a sinusoidal signal with $f = 1KHz$ and $V = 50mV$.
The two collector voltages are displayed:



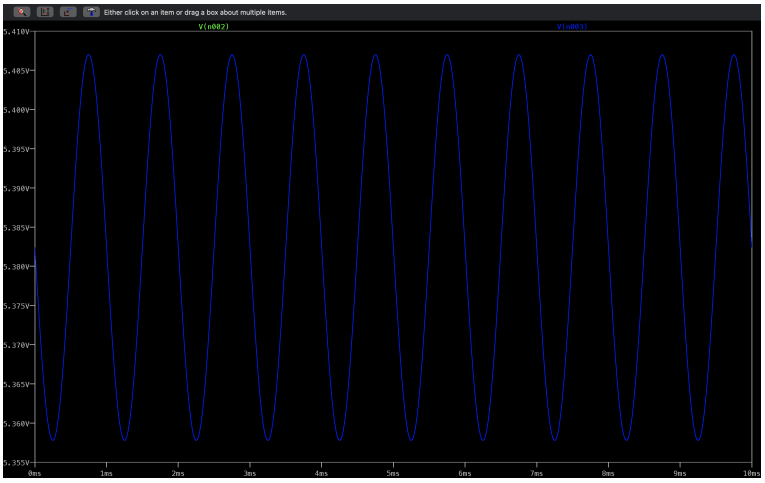
We obtain the following two points using the cursors.

$$(1.251ms, 6.847V) \qquad (1.752ms, 3.920V)$$

$$A_{Vdiff} = 20log\left(\frac{V_{od}}{V_{id}}\right) = 20log\left(\frac{6.847 - 3.920}{0.1}\right) = 29.327dB$$

Question 3

V_2 is also set to a sinusoidal signal with $f = 1KHz$ and $V = 50mV$.
The two collector voltages are displayed:



We obtain the following two points using the cursors.

$$(1.747ms, 5.407V) \qquad (1.249ms, 5.358V)$$

$$A_{Vcm} = 20log\left(\frac{V_{oc}}{V_{ic}}\right) = 20log\left(\frac{5.407V - 5.358V}{0.1}\right) = -6.150dB$$

Question 4

CMRR is often mathematically expressed as follows:

$$CMRR = 20log\left(\frac{A_{Vdiff}}{A_{Vcm}}\right)$$

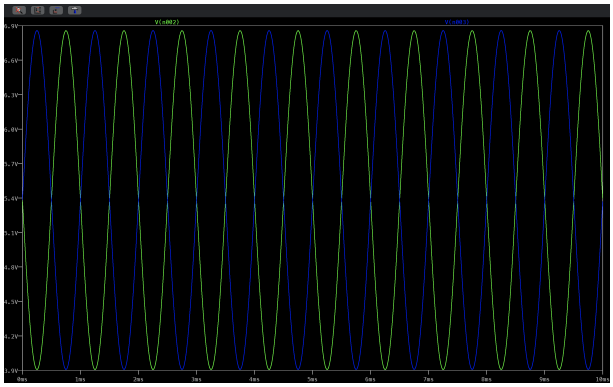
Since both values are already calculated in dB:

$$CMRR = A_{Vdiff} - A_{Vcm} = 29.327 - (-6.150) = 35.477dB$$

Question 5

The resistor R_3 was replaced by a current source and the same process was repeated.

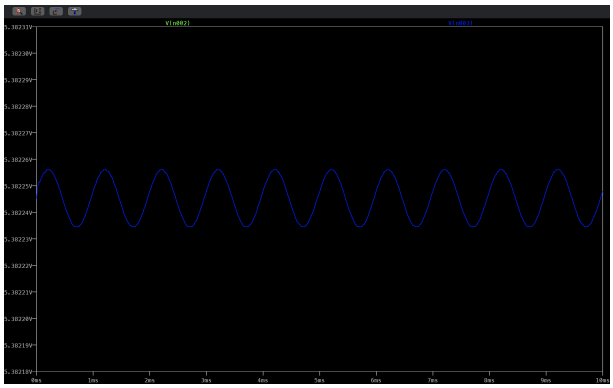
	T_1	T_2
V_{BE}	-673.622V	-673.622V
V_C	5.382V	5.382V
I_C	2.099mA	2.099mA
I_E	2.109mA	2.109mA
I_RE	4.218mA	



We obtain the following two points using the cursors.

$$(1.252ms, 6.858V) \qquad (1.752ms, 3.907V)$$

$$A_{Vdiff} = 20log\left(\frac{V_{od}}{V_{id}}\right) = 20log\left(\frac{6.858 - 3.907}{0.1}\right) = 29.400dB$$



We obtain the following two points using the cursors.

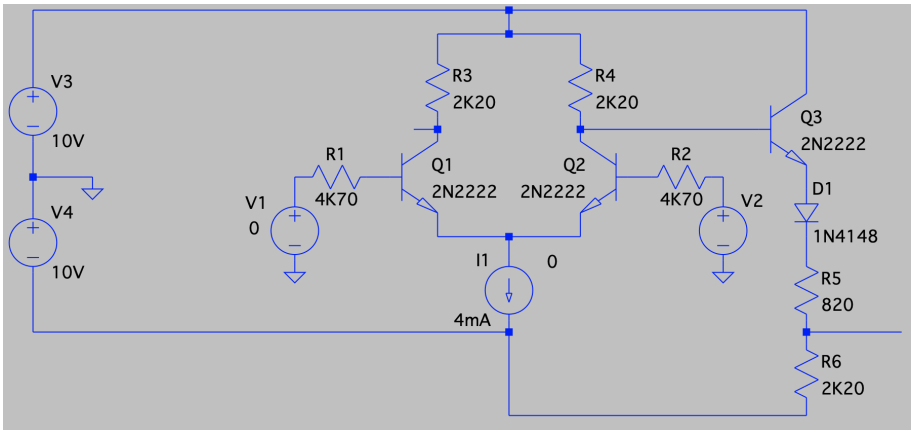
$$(1.213ms, 5.382V) \qquad (1.698ms, 5.382V)$$

$$A_{Vcm} = 20log\left(\frac{V_{oc}}{V_{ic}}\right) = 20log\left(\frac{21.51 \times 10^{-6}}{0.1}\right) = -73.347dB$$

$$CMRR = A_{Vdiff} - A_{Vcm} = 29.400 - (-73.347) = 102.747dB$$

6.1.2 Problem 2 : Construct an OP-Amp

The circuit given in the lab manual was implemented in LTSpice.



Question 1

Both V_1 and V_2 are connected to the ground and output voltage is calculated as follows:

$$I_C(T_2) = I_E(T_2) = \frac{I_1}{2} = \frac{4 \times 10^{-3}}{2} = 2mA$$

Using KVL:

$$V_C(T_2) = V_B(T_3) = V_{CC} - I_C(T_2)R_4 = 10 - 2200 \times 2 \times 10^{-3} = 5.6V$$

For the third transistor:

$$V_E(T_3) = V_B(T_3) - V_{BE}(T_3) = 5.6 - 0.7 = 4.9V$$

$$I_E(T_3) = \frac{V_E(T_3) - V_{diode} - V_{CC}}{R_3 + R_4} = \frac{4.9 - 0.7 - (-10)}{820 + 2200} = 4.702mA$$

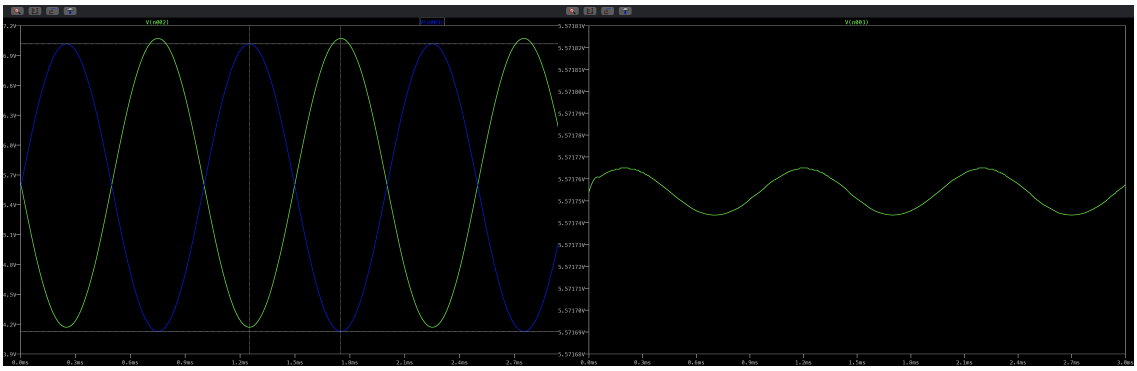
$$\boxed{V_{out} = I_E(T_3)R_6 + V_{CC} = 4.702 \times 10^{-3} \times 2200 + (-10) = 344.371mV}$$

Question 2

A DC operation was performed in LTSpice. An output voltage of $358.357mV$ was obtained. As we can see, it is very close to the calculated one. The difference comes from the diode and the transistors. The components used in LTSpice have slightly different characteristics.

Question 3

As in the previous problem, first the voltage source V_1 was set to a sinusoidal signal with $f = 1KHz$ and $V = 50mV$. The collector voltages were recorded. Then, the second voltage source V_2 was set to the identical signal.



(a) With one voltage source (b) With two voltage sources

Figure 5: Collector voltages

The following numbers are obtained:

$$(1.252ms, 7.018V) \qquad (1.749ms, 4.126V)$$

$$A_{Vdiff} = 20log\left(\frac{V_{od}}{V_{id}}\right) = 20log\left(\frac{7.018V - 4.126V}{0.1}\right) = 29.223dB$$

The following numbers are obtained:

$$(1.201ms, 5.572V) \qquad (1.697ms, 5.572V)$$

$$A_{Vcm} = 20log\left(\frac{V_{oc}}{V_{ic}}\right) = 20log\left(\frac{21.468 \times 10^{-6}}{0.1}\right) = -73.364dB$$

$$CMRR = A_{Vdiff} - A_{Vcm} = 29.223 - (-73.364) = 102.587dB$$

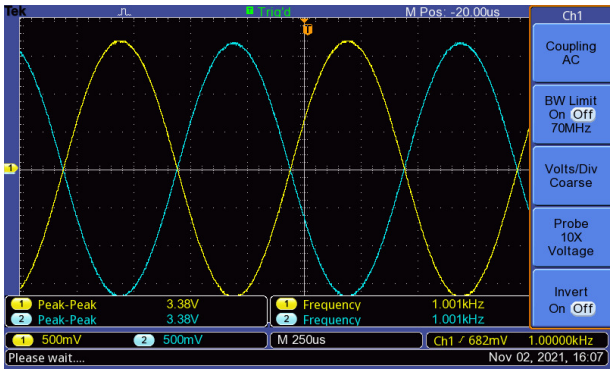
Question 4

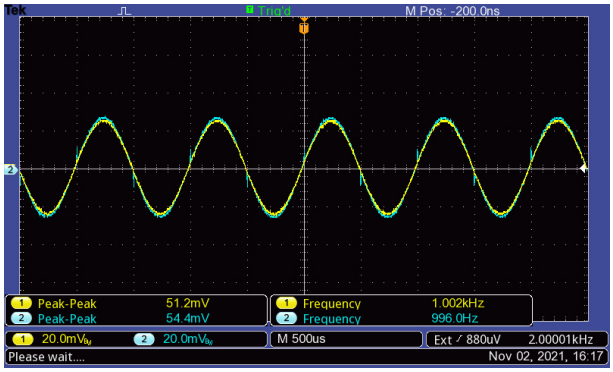
The second input is the inverting input because is has a 180°phase shift with the amplified signal.

6.2 Experiment Data

6.2.1 Problem 1 : Differential amplifier using a fixed emitter resistor

	T_1	T_2
V_C	5.531 V	5.280 V
V_B	-0.0418 V	-0.0412 V
V_{BE}	0.6589 V	0.6345 V
I_C	2.196 mA	2.065 mA
I_{RE}	4.1 mA	





6.2.2 Problem 2 : Implement a Current Source

$$R_1 = 530\Omega \qquad R_2 = 1000\Omega$$

Circuit is operational.

6.2.3 Problem 3 : Differential amplifier using a Current Source