**Prelab: CMOS Inverters and Logic Gates**

**Problem 1: Voltage Transfer Characteristic of a CMOS inverter**

Task 1

For this task we implement a CMOS inverter on LTSpice:

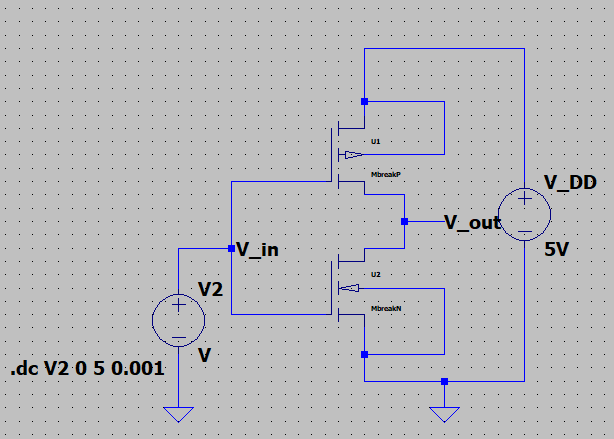


Figure: CMOS inverter

We use a 5V power supply for . Then we simulate the VTC of the CMOS inverter, and use the d() function to obtain the derivative curve. The results are shown as follows:

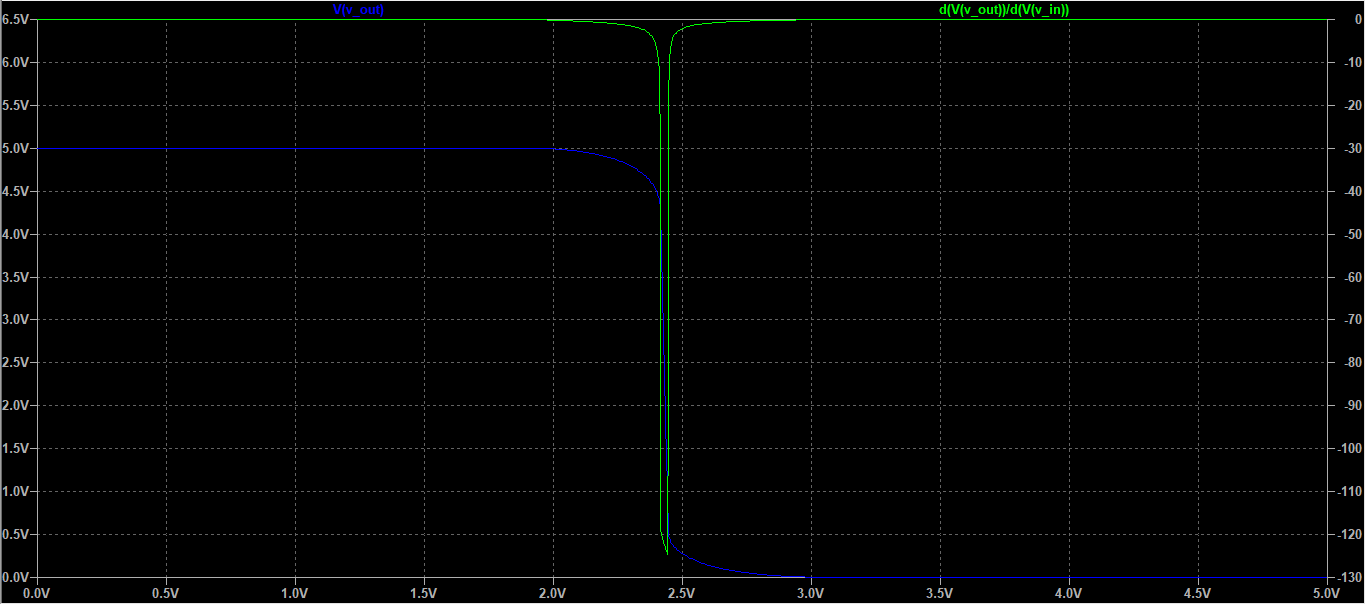


Figure: VTC Simulation results

Then, we extract the following values from the curve:

|  |  |
| --- | --- |
|  | 4.8669256V |
|  | 2.2393162V |
|  | 166.89289mV |
|  | 2.5726496V |
|  | 133.07445mV |
|  | 166.89285mV |

Task 2

Then, we simulate the current flowing through the inverter as a function of the input voltage. The results are provided below:

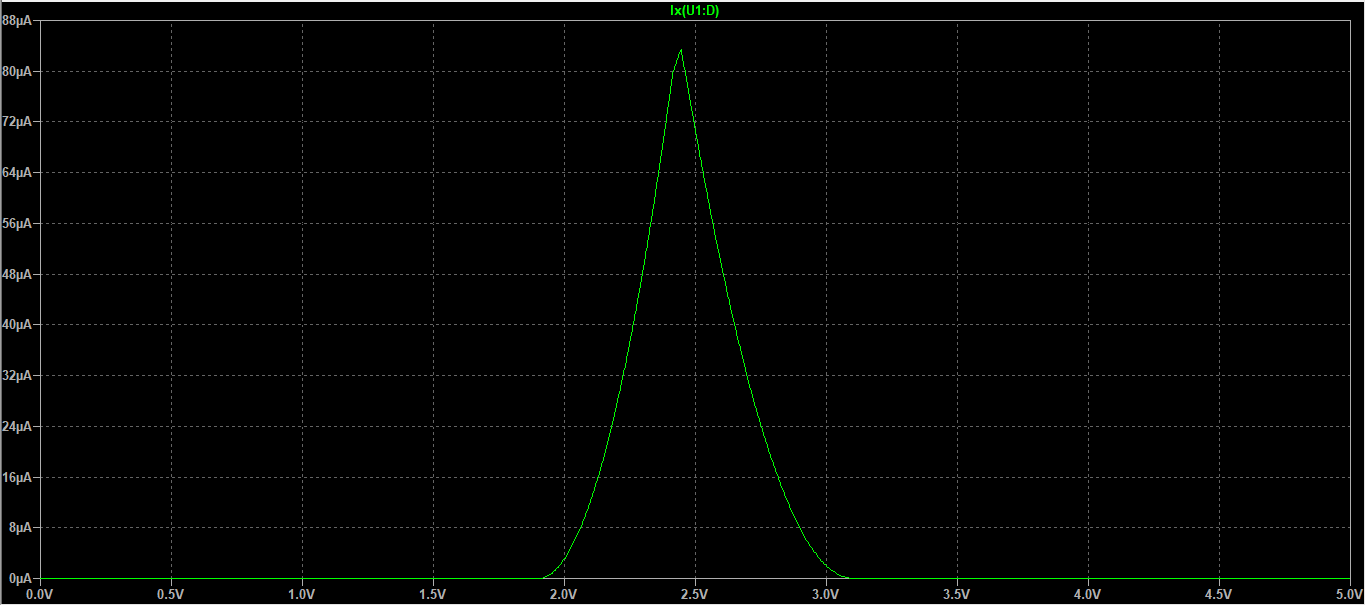
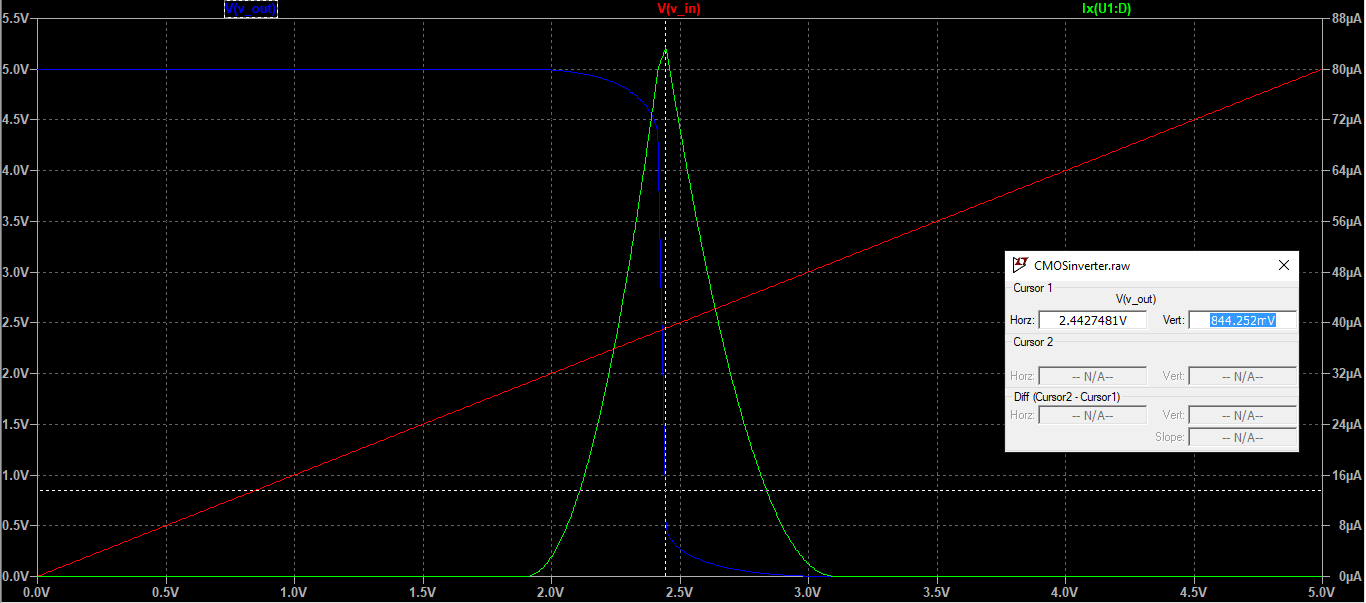


Figure: Inverter current flow simulation

Task 3

Based on the simulation, the maximum is reached when input is 2.4427481V, at which point the current flow is 83.124869µA. At this point the input and output voltages are equal, so both NMOS and PMOS transistors are turned on. As a result, the current reaches its maximum level. We can see a demonstration below:



**Problem 2: CMOS Inverter with Capacitive Load**

Task 1

We now add a simple load capacitor to the circuit. The circuit looks as follows:

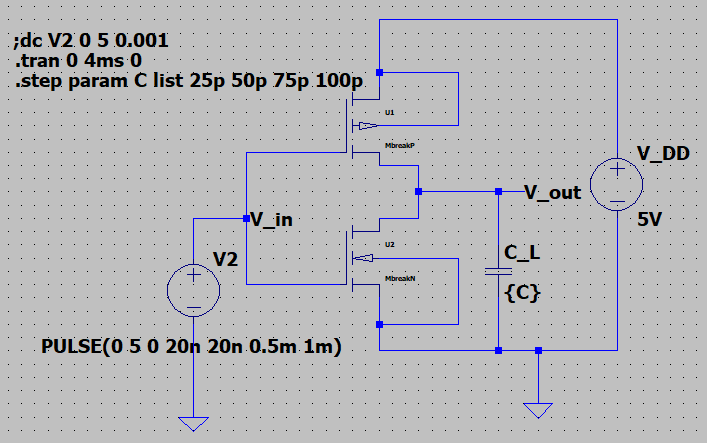


Figure: CMOS inverter

We vary the capacitive load from 25pF to 100pF in 25pF steps for an input signal given by a 1KHz square wave with 20ns rise and fall time and use a 5V power supply for V\_DD.

The input and output signal are displayed below:

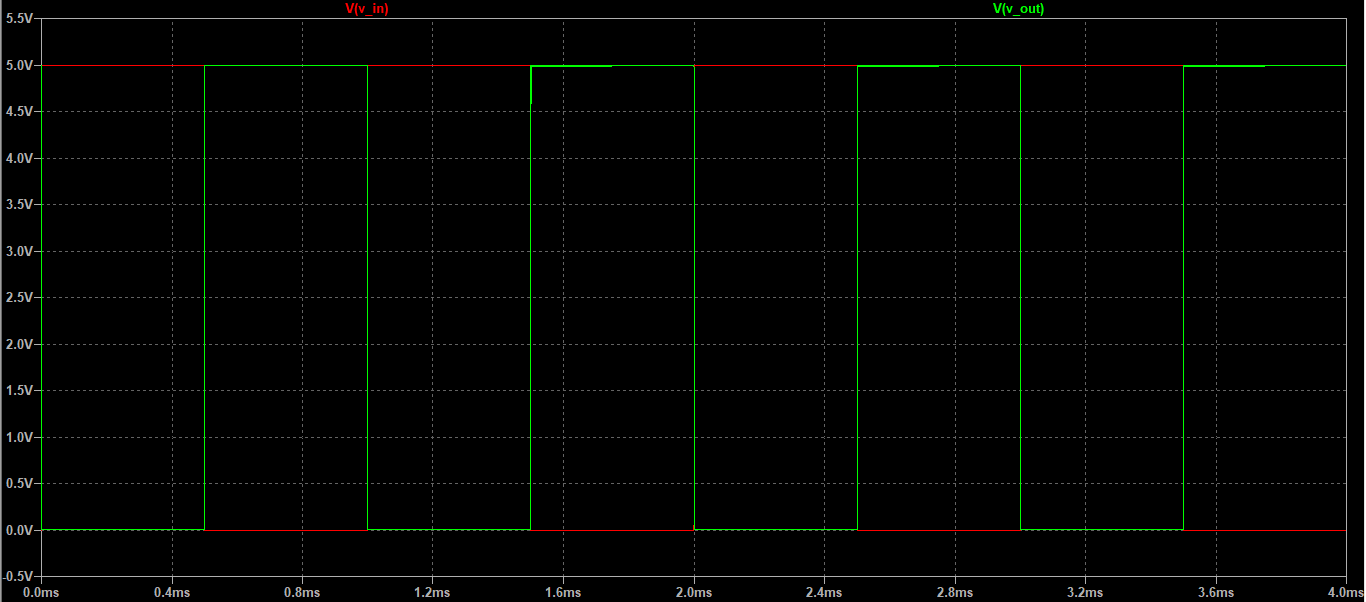


Figure: Input and output

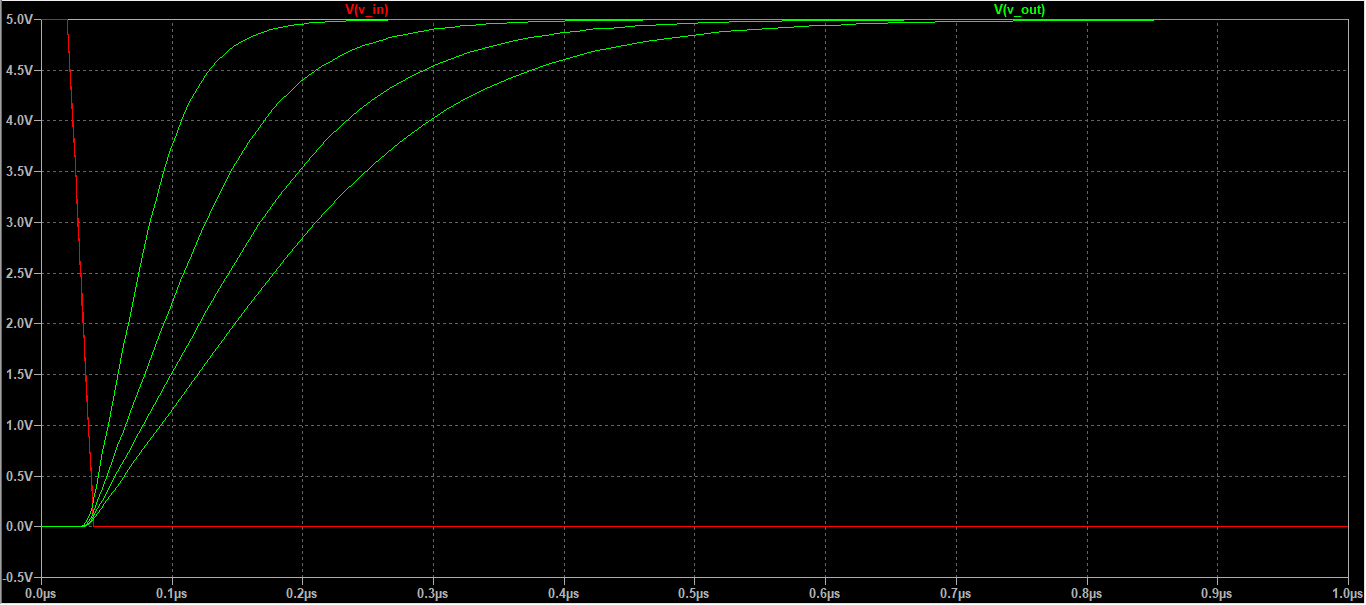


Figure: Examining propagation delay for different capacitances

|  |  |
| --- | --- |
| Capacitance |  |
| 25 pF | 45.141546ns |
| 50pF | 76.511094ns |
| 75pF | 113.23642ns |
| 100pF | 147.66641ns |

From the table, we can see that the time delay increases as the capacitance increases.

Task 2

**Problem 3: Propagation Delay of an Inverter Stage**

For this section, we first implement the following circuit:

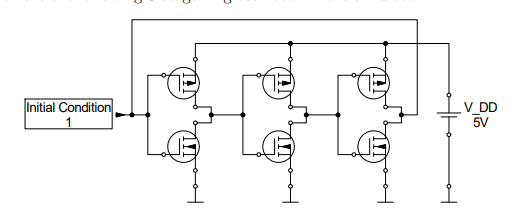


Figure: Inverter Stage

The LTSpice implementation is provided below:

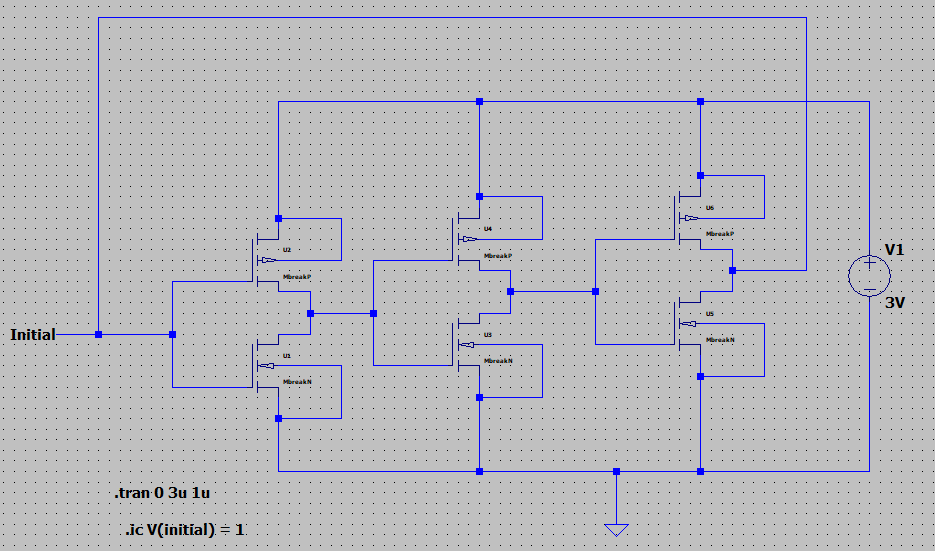


Figure: LTSpice implementation of ring ocsillator

Task 1

We are required to determine the oscillation frequency of the ring oscillator and the propagation delay per inverter stage for supply voltages 3V, 5V, 7V, and 10V.

At V\_DD = 3V, we have the following simulation results:

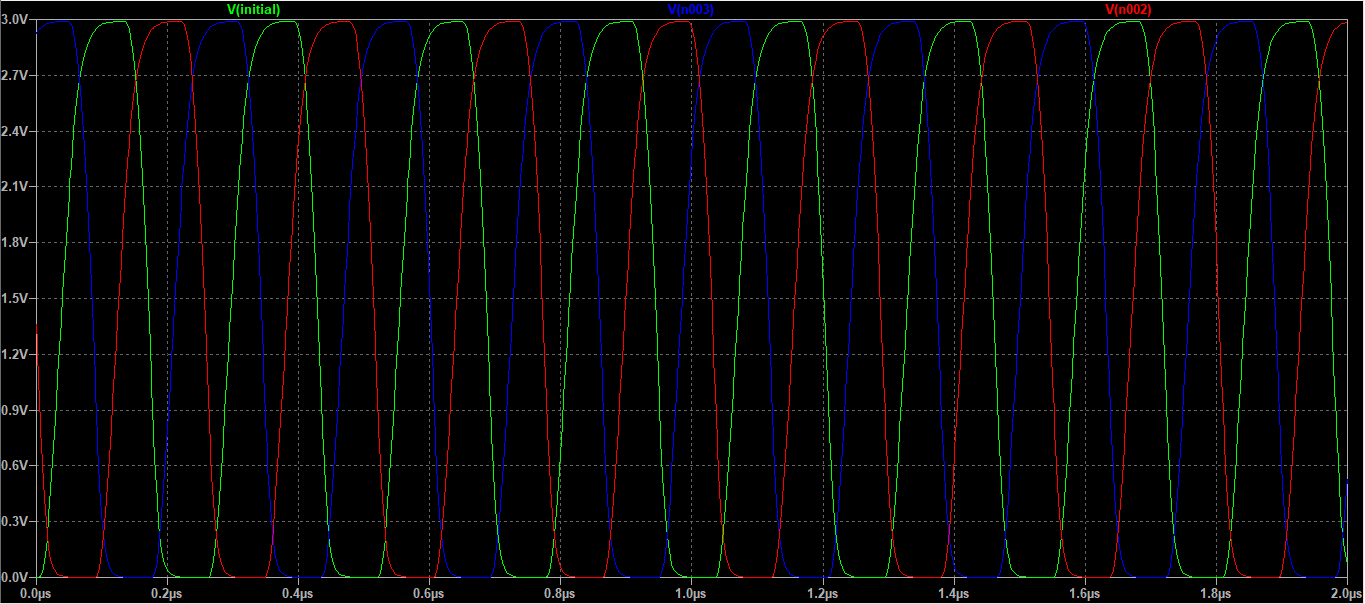


Figure: Simulation for 3V supply

At V\_DD = 5V, we have the following simulation results:

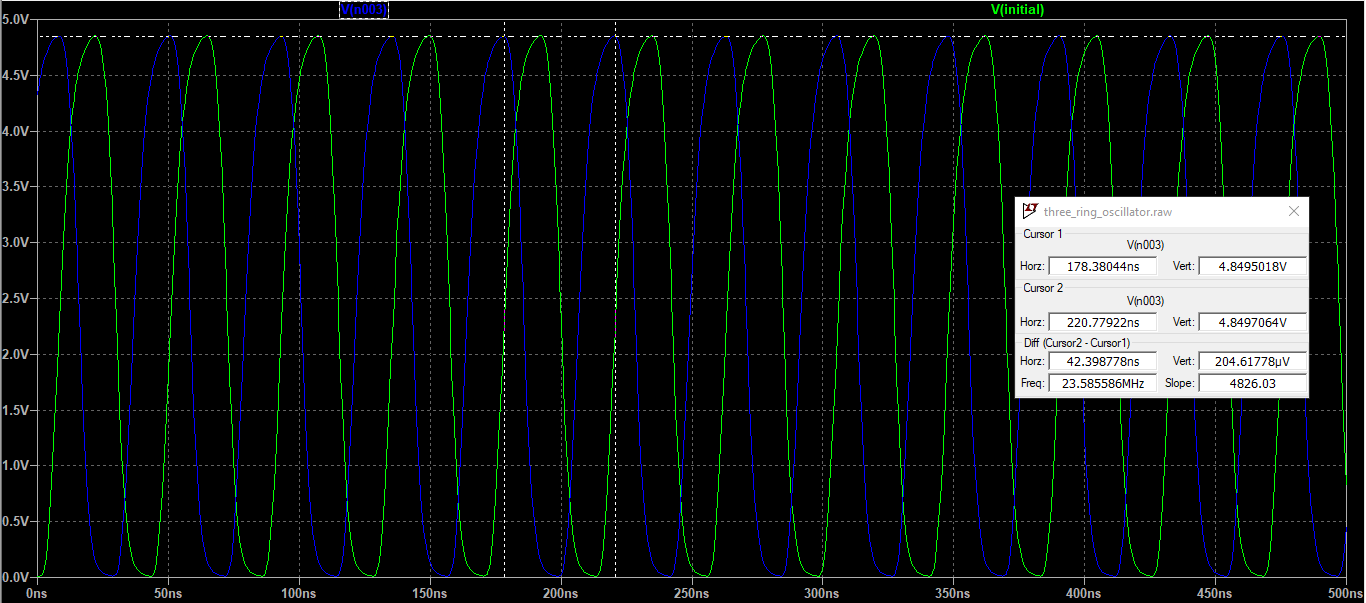


Figure: Simulation for 5V supply

At V\_DD = 7V, we have the following simulation results:

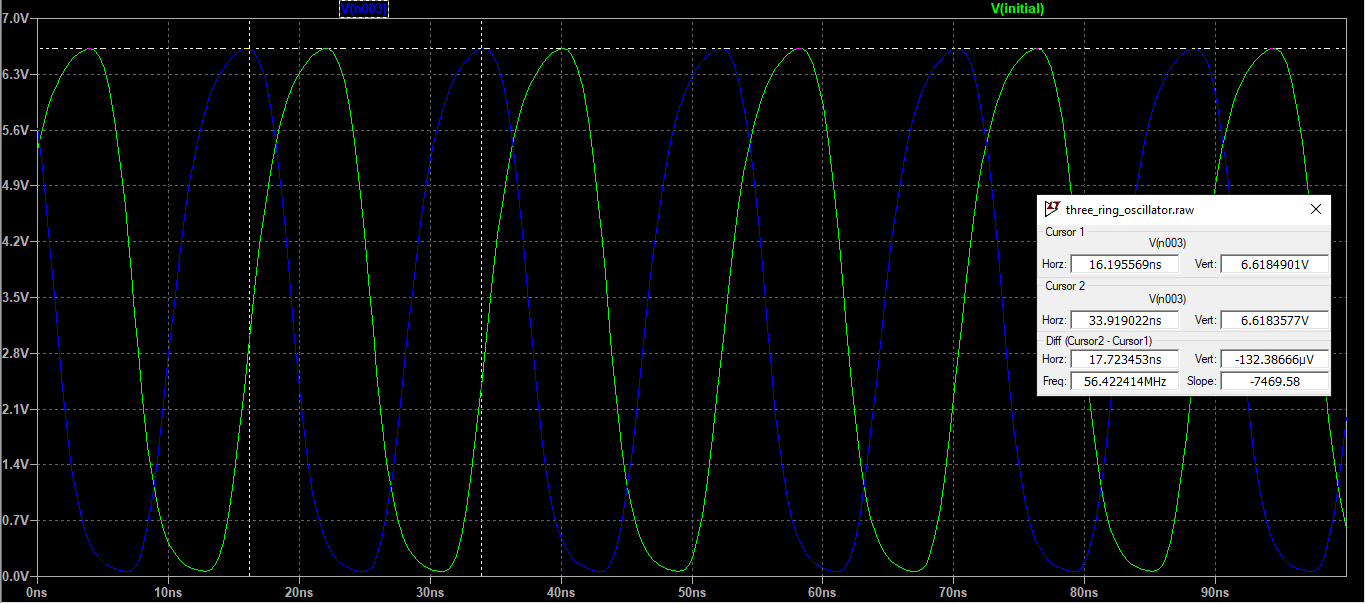


Figure: Simulation for 7V supply

At V\_DD = 10V, we have the following simulation results:

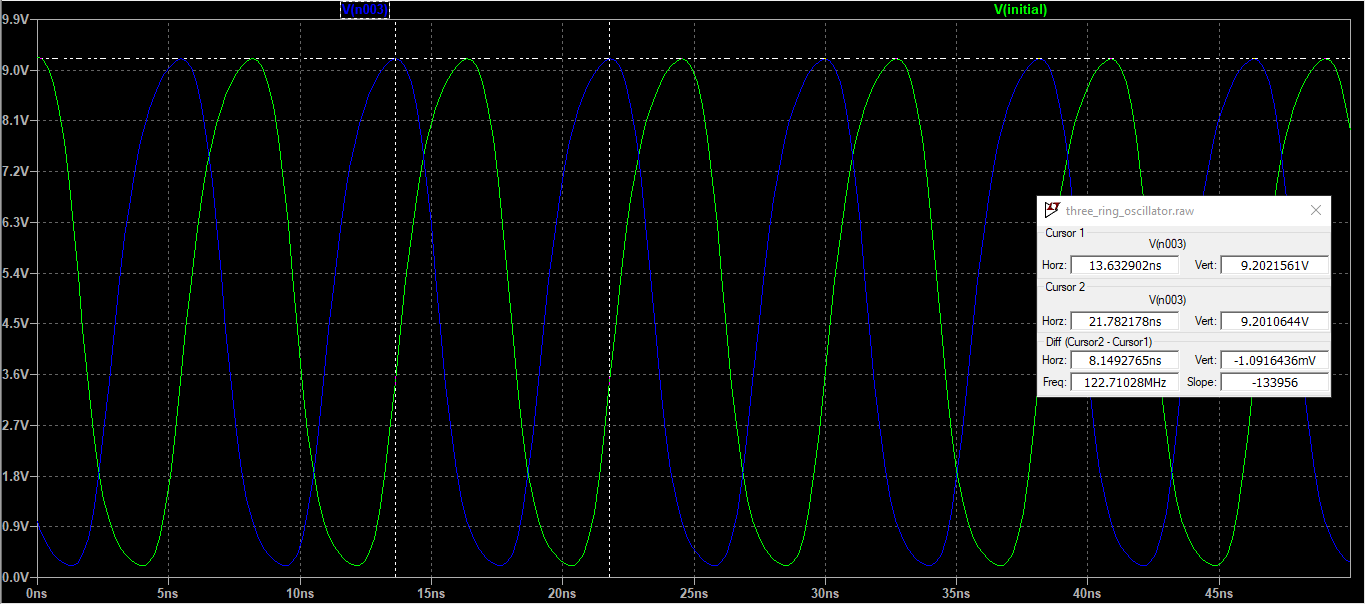


Figure: Simulation for 10V supply

Propagation delay per inverter stage:

|  |  |  |
| --- | --- | --- |
|  | Frequency |  |
| 3V |  | 42.966 ns |
| 5V |  | 7.0665ns |
| 7V |  | 2.9539ns |
| 10V |  | 1.3582ns |

Task 2

We use C = 5 pF, based on the datasheet.

|  |  |  |
| --- | --- | --- |
|  | Frequency |  |
| 3V |  | 0.17454 mW |
| 5V |  | 2.94820 mW |
| 7V |  | 13.82349 mW |
| 10V |  | 61.35514 mW |

Task 3

For this task, we add a 50 pF load capacitor to each inverter of the 3-stage ring oscillator. We set V\_DD = 5V. The final implementation is provided below:

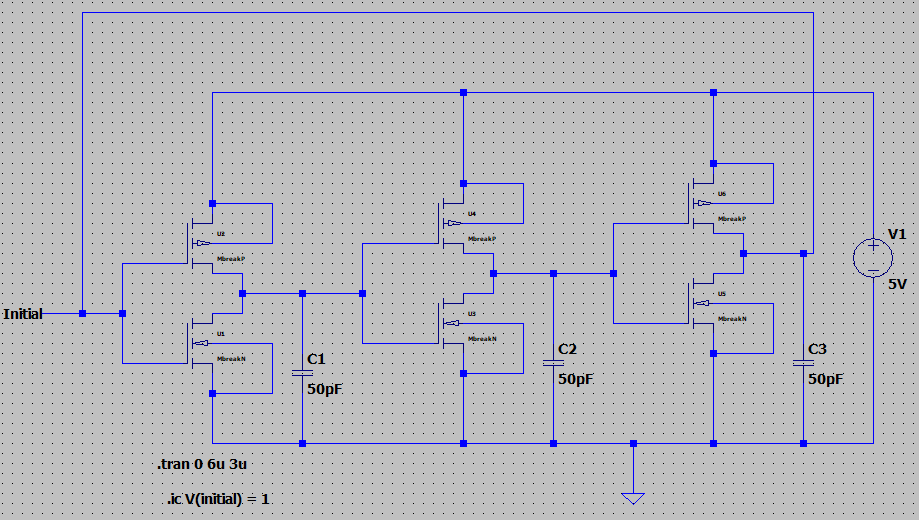


Figure: 3-stage ring oscillator with capacitors

Simulation results are provided below:



Figure: Simulation results for 3-stage ring oscillator

Determination of the frequency was carried out using the cursors:

The propagation delay is determined as follows:

The dynamic power dissipation is determined as follows:

Task 4

Presence of capacitive load results in an increase of propagation delay and decrease of oscillation frequency.

Task 5

We saw that increasing the power supply increases the frequency of the output, and increasing the load capacitance decreases the frequency. Frequency is directly proportional to power dissipation. Therefore, using the load capacitance lowers the power dissipation without any manipulation of the power supply.

**Experimental Data and Results**

**Problem 1: Voltage transfer characteristic of an Inverter**

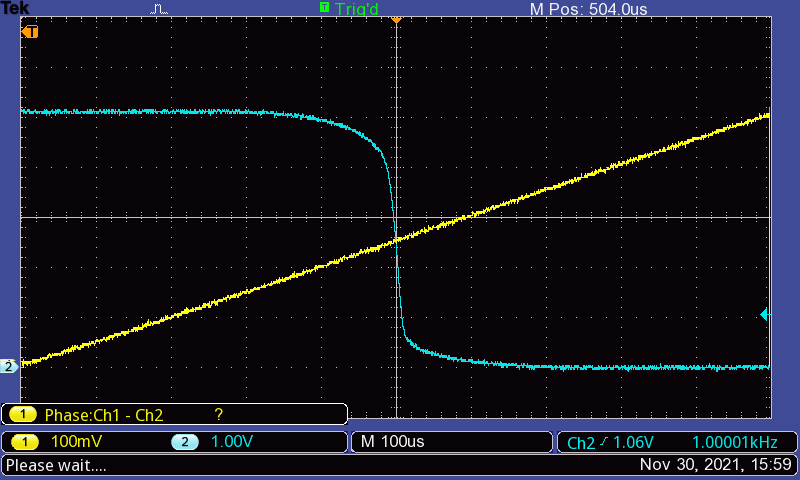
**Task 1**

**Instructions:**

To display the VTC we need two steps. In the lab first we measure Vin and Vout for one switch-on event. In the second step in the evaluation MatLab is used to display and measure the VTC parameters.

* Generate a ramp signal with 0 to 5V and f = 1 KHz. Check that the waveform is correct before applying it to the inverter.
* Connect the input of the inverter to Channel 1 and the output to Channel 2. Show one Vin ramp together with Vout on the screen! Use the measure function to determine the properties of the signals.
* Take a hardcopy. Take care that you not only got the picture, but also the complete data set for Ch1 and Ch2 (the \*.CSV files)!

Results:



**Problem 2: Propagation Delay of an Inverter**

**Instructions:**

Connect the oscilloscope to the input and the corresponding output of the first inverter.

Note: The propagation delay determined by this method is not very accurate, as the probe capacitance has an influence on the measurement. To minimize the effect, the 10x high impedance probe should be used in the measurement.

1. Measure the oscillation frequency and propagation delay tP LH and tP HL of the first inverter at 3V, 5V, 7V, and 10V. Take hard copies for the different measurements!

2. Add load capacitors to each of the three output nodes of the 3-stage ring oscillator. The load capacitors should have a capacitance value of 1.5nF.

3. Measure the oscillation frequency and the propagation delay tP LH, tP HL for the first inverter at VDD = 5V.

Results:

