

AOT240L/AOB240L/AOTF240L 40V N-Channel MOSFET

General Description

The AOT240L & AOB240L & AOTF240L uses Trench MOSFET technology that is uniquely optimized to provide the most efficient high frequency switching performance. Power losses are minimized due to an extremely low combination of $R_{\text{DS(ON)}}$ and Crss.

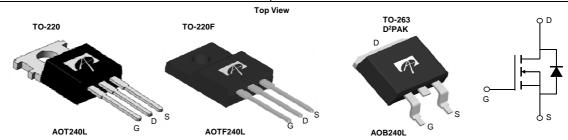
Product Summary

 $\rm V_{DS}$ \$40V\$ $\rm I_{D}$ (at $\rm V_{GS}{=}10V)$ \$105A/85A\$

 $\begin{array}{lll} R_{DS(ON)} \ (at \ V_{GS} = 10 V) & < 2.9 m \Omega & (< 2.6 m \Omega^*) \\ R_{DS(ON)} \ (at \ V_{GS} = 4.5 V) & < 3.7 m \Omega & (< 3.5 m \Omega^*) \end{array}$

100% UIS Tested 100% R_g Tested





Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOT240L	TO-220	Tube	1000
AOB240L	TO-263	Tape & Reel	800
AOTF240L	TO-220F	Tube	1000

Ŀ	Absolute Maximum	Ratings	T _A =25℃	unless	otherwise no	oted

Parameter		Symbol	AOT240L/AOB240L	AOTF240L	Units
Drain-Source Voltage		V _{DS}	40	V	
Gate-Source Voltage		V_{GS}	±20	V	
Continuous Drain	T _C =25℃	1	105	85	
Current ^G	T _C =100℃	'D	82	60	Α
Pulsed Drain Current	t ^C	I _{DM}	400		
Continuous Drain	T _A =25℃	ı	20	А	
Current	T _A =70℃	IDSM	16		
Avalanche Current ^C		I _{AS}	68		A
Avalanche energy L=0.1mH ^C		E _{AS}	231		mJ
	T _C =25℃	D	176	41	W
Power Dissipation ^B	T _C =100℃	$-P_{D}$	88	20]
Power Dissipation A T_{A} =25 $^{\circ}$ T_{A} =70 $^{\circ}$		D	1.9		W
		P _{DSM}	1.2] vv	
Junction and Storage Temperature Range		T_J , T_{STG}	-55 to 175		C

Thermal Characteristics							
Parameter		Symbol	AOT240L/AOB240L	AOTF240L	Units		
Maximum Junction-to-Ambient A	t ≤ 10s	D	15	15	°C/W		
Maximum Junction-to-Ambient AD	Steady-State	$R_{\theta JA}$	65	65	°C/W		
Maximum Junction-to-Case	Steady-State	R _{e.IC}	0.85	3.6	℃/W		

^{*} Surface mount package TO263



Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Тур	Max	Units	
STATIC PARAMETERS								
BV _{DSS}	Drain-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$		40			V	
1	Zero Gate Voltage Drain Current	V_{DS} =40V, V_{GS} =0V	V _{DS} =40V, V _{GS} =0V			1	^	
I _{DSS}	Zero Gate Voltage Drain Current	T _J =55℃				5	μΑ	
I_{GSS}	Gate-Body leakage current	V_{DS} =0V, V_{GS} =±20V				±100	nA	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$		1	1.7	2.2	V	
$I_{D(ON)}$	On state drain current	V _{GS} =10V, V _{DS} =5V		400			Α	
		V_{GS} =10V, I_D =20A	V _{GS} =10V, I _D =20A		2.4	2.9	mΩ	
		TO220/TO220F		3.7	4.7	11152		
		V_{GS} =4.5V, I_D =20A			3	3.7	m()	
D	Static Drain-Source On-Resistance	TO220/TO220F	TO220/TO220F		3	3.7	mΩ	
R _{DS(ON)}	Static Drain-Source On-Resistance	V_{GS} =10V, I_D =20A			2.1	2.6	O	
		TO263			2.1	2.6	mΩ	
		V _{GS} =4.5V, I _D =20A TO263			0.7	3.5	mΩ	
					2.7			
g _{FS}	Forward Transconductance	$V_{DS}=5V$, $I_{D}=20A$			78		S	
V_{SD}	Diode Forward Voltage	I _S =1A,V _{GS} =0V			0.65	1	V	
Is	Maximum Body-Diode Continuous Current ^G					105	Α	
DYNAMIC	PARAMETERS							
C _{iss}	Input Capacitance				3510		pF	
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz			1070		pF	
C _{rss}	Reverse Transfer Capacitance				68		pF	
R_g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		0.5	1	1.5	Ω	
SWITCHI	NG PARAMETERS	•						
Q _g (10V)	Total Gate Charge				49	72	nC	
Q _g (4.5V)	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A			22	32	nC	
Q_{gs}	Gate Source Charge				9		nC	
Q_{gd}	Gate Drain Charge				7		nC	
t _{D(on)}	Turn-On DelayTime	V_{GS} =10V, V_{DS} =20V, R_L =1 Ω , R_{GEN} =3 Ω			11		ns	
t _r	Turn-On Rise Time				10		ns	
t _{D(off)}	Turn-Off DelayTime				38		ns	
t _f	Turn-Off Fall Time				11		ns	
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs			21		ns	
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs	S		58		nC	
A The value	Let of R_{ALL} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}$ C. The						C The	

A. The value of $R_{\theta JA}$ is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

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B. The power dissipation P_D is based on $T_{J(MAX)}$ =175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ =175° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

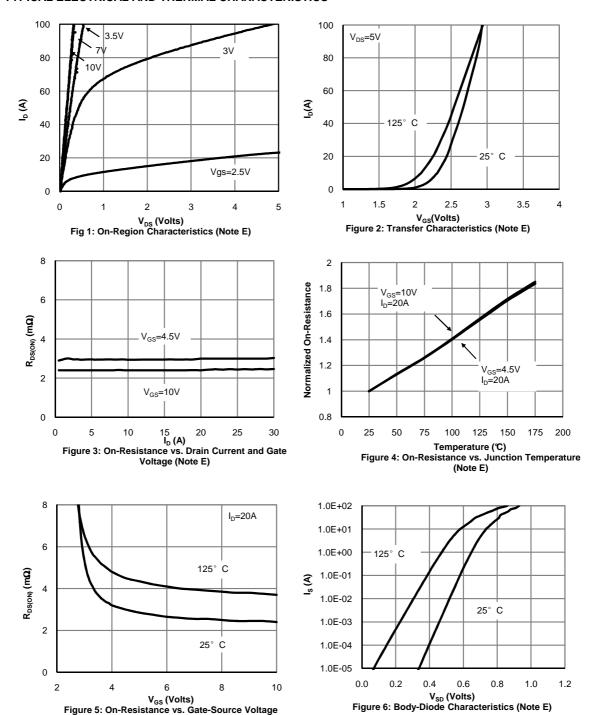
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$ =175° C. The SOA curve provides a single pulse rating.

G. The maximum current limited by package.

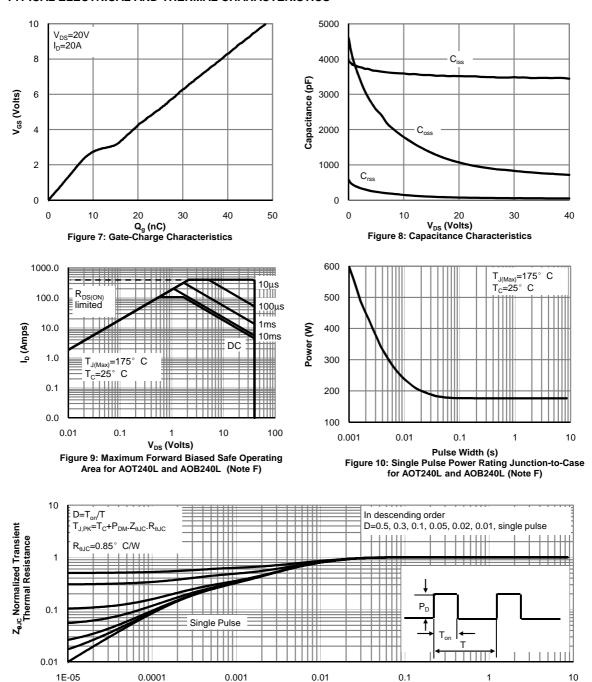
H. These tests are performed with the device mounted on 1 in FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.



(Note E)







Pulse Width (s)
Figure 11: Normalized Maximum Transient Thermal Impedance for AOT240L and AOB240L (Note F)



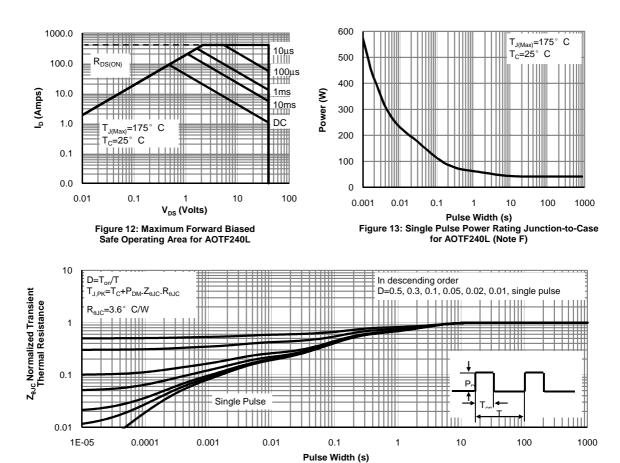
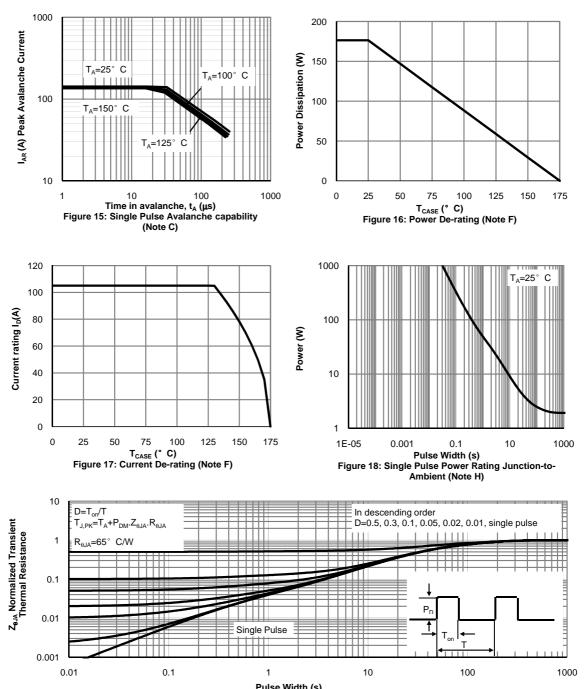


Figure 14: Normalized Maximum Transient Thermal Impedance for AOTF240L (Note F)

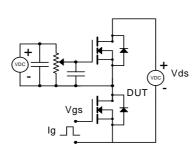


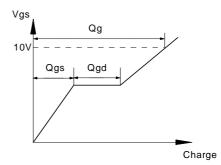


Pulse Width (s)
Figure 19: Normalized Maximum Transient Thermal Impedance (Note H)

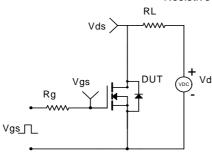


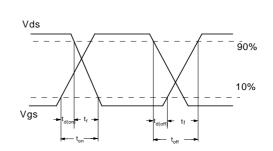
Gate Charge Test Circuit & Waveform



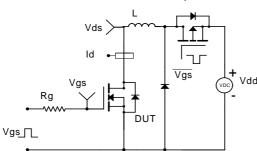


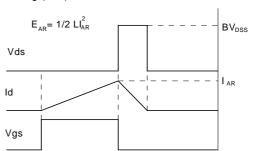
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms

