Pritam Karnnewar

4th B.tech, Electronics and Communication Engineering
B V Raju Institute of Technology, Narsapur.

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CAREER OBJECTIVE:

To work for an organization which provides me the opportunity to improve my skills and knowledge and growth my career.

EDUCATIONAL QUALIFICATIONS:

Program	Institution	Percentage	Year of Pass
B.Tech (ECE)	B V Raju Institute of Technology, Narsapur	9.24 CGPA (Till date)	Pursuing
Intermediate	Narayana Junior College, Dilsukhnagar	98.1%	2016
SSC	Gowtham Model Schools, Adilabad	9.5 GPA	2014

TECHNICAL SKILLS:

- Programming Language: C,Core Java,Angular 6,Spring 5.x,Spring Boot,Bootstrap,Sql.
- Verilog Hardware Programming
- Embedded Systems Programming
- MATLAB (Beginner)

PROJECTS/PRESENTATIONS:

PROJECT 1:

- **Title:** Automatic Manhole System.

- **Description:** Automatic manhole system (AMS) is a novel idea to solve traffic problems and to improve sanitation in our country. The main idea is to prevent accidents due to open manhole along with preventing manhole blockage. AMS works on the sensor data and acts as a manhole only when there is water flow and it also sends the information to the respected authorities in the form of message. This had had shortlisted in IICDC innovation challenge and reached up to quarterfinals.

PROJECT 2:

- **Title:** Automatic railway gate system.

- **Description:** In our day to day dealings man intervention in any work is very crucial but instead of this we are developing and using automated gadgets. The main idea of our project is to decrease the work load, so have

put a foot forward to replace the man work with using present technology. Through which the railway gates are controlled by the action of the Train.

ACADEMIC PROJECT (undergoing):

- **Title**: Shape Recognising Using FPGA.
- **Tools Used:** MATLAB, vivado.
- **Description**: As Most of the real-world situations involve shape recognition (Vehicle Number Plate, Obstacle Detection). Image processing on FPGA is one of the least touched areas in electronics. This project identifies particular shapes in an image (square, rectangle and circle). The processing part is done in MATLAB and then converted to Verilog using HDL code generator, this module is then integrated with other modules in Vivado using IP integration.

ACHIVEMENTS:

- Participated in Automobile Workshop in BVRIT.
- Certified by TEXAS INSTRUMENTATION Online Contest and developed a Project AUTOMATIC MANHOLE SYSTEM.
- Certified by CDAC in digital designing through Verilog.

TRAININGS/INTERNSHIPS:

- C-DAC Workshop on Digital VLSI System Design using HDL
- Participated in SDSOC Zynq Workshop in BVRIT
- Participated in RF EMBEDDED TECHNOLOGIES on a project Automatic Railway Gate System.

PERSONAL DETAILS:

- Father's Name: k.Srinivas.
- Date of Birth : 11-09-1998.
- Languages : Telugu,Hindi and English.
- Hobbies : Watching Movies, Dancing, Photography.
- Address : H.No:3-25, Kajjarla(V),Talamadugu(M),Adilabad(D),Telangana-504308.

Declaration: I hereby declare that all the above information is true and correct to the best of my knowledge.

Pritam Karnnewar.