OmpSan: Static Verification of OpenMP's Data Mapping constructs

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1 Introduction

OpenMP is a widely used directive-based parallel programming model, that now supports offloading computations from hosts to device accelerators. Notable accelerator-related features in OpenMP 4.5 include unstructured data mapping, asynchronous execution, and runtime routines for device memory management.

OMP 4.5 Target offloading and Data mapping OMP 4.5 offers the *omp target* directive for offloading computations to devices and the `omp target data` directive for mapping data across the host and the corresponding device data environment. On heterogeneous systems, managing the movement of data between the host and the device can be challenging, and is often a major source of performance and correctness bugs. In the OpenMP accelerator model, data movement between device and host is supported either explicitly via the use of a `map` clause or, implicitly through default data-mapping rules. The optimal, or even correct, specification of map clauses can be non-trivial and error-prone because it requires users to reason about the complex dataflow analysis.

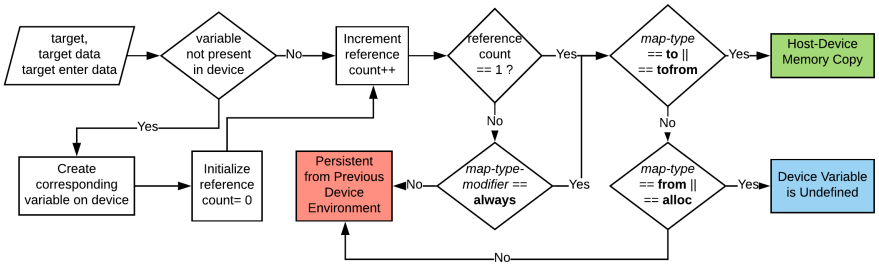
1.1 OpenMP 4.5 Map Semantics

Figure 1 shows a schematic illustration of the complex set of rules used when mapping a host variable to the corresponding list item in the device data environment, as specified in the OpenMP 4.5 standard. For correctness, in this paper we assume the device is a GPU, and mapping a variable from host to device introduces a host-device memory copy, and vice-versa. However, the bugs that we identify reflect errors in the OpenMP code regardless of the target device. The different map types that OpenMP 4.5 supports are,

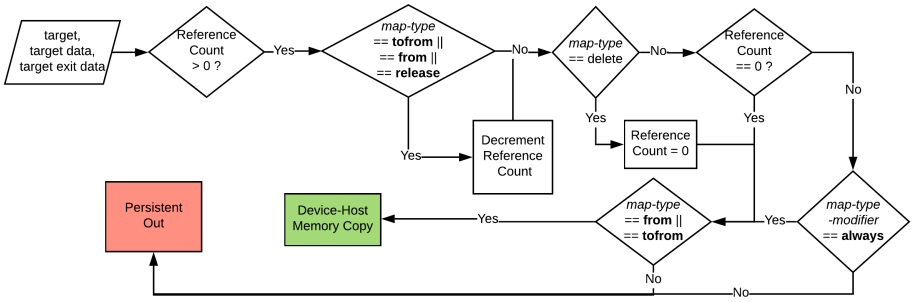
- alloc: allocate on device, uninitialized
- to: map to device before kernel execution, (host-device memory copy)

– from: map from device after kernel execution (device-host memory copy)
– tofrom: copy in and copy out the variable at the entry and exit of the device environment

The default map type for arrays is *tofrom*, while the default for scalars is *first-private*, that is the only copy the value of the scalar at the entry to the device environment. As Figure 1 shows, OpenMP 4.5 specification uses the reference



(a) Flowchart for Enter Device Environment



(b) Flowchart for Exit Device Environment

Fig. 1: Flowcharts to show how to interpret the map clause

count of a variable, to decide when to introduce a device/host memory copy. The host to device memory copy is introduced only when the reference count is incremented from 0 to 1 and the "to" attribute is present. Then the reference count is incremented every time a new device map environment is created. The reference count is decremented on encountering a "from" or "release" attribute, while exiting the data environment.

1.2 Our Solution

To address the complexity of using OpenMP's target and map clauses, we propose the creation of a static analysis tool called OmpSan to perform OpenMP code "sanitization" by using a compile-time approach for static verification of data mapping constructs based on dataflow analysis. "An OpenMP program is expected to yield the same result when enabling or disabling OpenMP constructs". Our approach detects errors by comparing dataflow information (reaching definitions via LLVM's memory SSA representation [5]) between the OpenMP and baseline code. We developed an LLVM-based implementation of our approach and evaluated its effectiveness using several case studies. Our major contributions include the following.

- An algorithm to analyze OpenMP runtime library calls inserted by Clang in the LLVM IR, to infer the host/device memory copies. We expect that this algorithm will have applications beyond our OmpSan tool.
- A static analysis technique to validate if the host/device memory copies respect the original memory def-use relations.
- Diagnostic information to understand how the map clause affects the host and device data environment.

The paper is organized as follows. section 2 provides certain motivating examples, that show common issues and difficulties in usage of OpenMP's *data map* construct. section 3 provides the background information that we use in our analysis. section 4 presents an overview of our approach to validate the usage of data mapping constructs. section 5 presents the LLVM implementation details, and section 6 presents the evaluation and some case studies. subsection 6.3 also lists some of the limitations of our tool, some of them common to any static analysis.

2 Motivating Examples

We discuss potential errors in the user code arising from improper usage of the data mapping constructs, and illustrate how easy it is to incorrectly use the map construct. The accompanying examples motivate the utility and applicability of our proposed analysis and the tool OMPSan.

2.1 Default Scalar Mapping

Our first motivating example is, Listing 2.1. In this example, the definition of "sum" on line 5 does not reach line 6, since the "sum" does not have an explicit mapping and the default map for scalars is "firstprivate". As Listing 2.2 shows, an explicit map clause is essential to specify the copy in and copy out of the scalar "sum" from device.

Listing 2.1: Default scalar map

```
1 int A[N], sum=0, i;
2 #pragma omp target
3 #pragma omp teams distribute parallel for
        reduction(+:sum)
4   for(i=0; i<N; i++)
5     sum += A[i];
6   printf("\n%d",sum);
```

Listing 2.2: Explicit map

```
1 int A[N], sum=0;
2 #pragma omp target map(tofrom:sum)
3 #pragma omp teams distribute parallel for
        reduction(+:sum)
4   for( int i=0; i<N; i++)
5     sum += A[i];
6   printf("\n%d",sum);
```

2.2 Reference Count Issues

Example 1 Listing 2.3 shows an example of data-mapping attributes across different data environments. The array "B", is specified as "alloc" in the first data environment. According to OpenMP 4.5 (Figure 1) exiting a data environment where the variable was mapped as "alloc" does not decrement the reference count, and a variable is mapped back from device to host only if the reference count is decremented to 0. So, we can track the reference count for "B" is as follows.

- Line 5, reference count = 1
- Line 6, enter data environment, reference count = 2
- Line 8, exit data environment "alloc", reference count = 2
- Line 9, exit data environment "from", reference count =1
- Line 12 accesses stale array data for variable "B", since "B" was not mapped back to host from device.

Listing 2.4 shows that replacing "alloc" with "from" on line 6, fixes this issue, and the programmer gets the expected behavior that is "B" is copied out at line 9. (This behavior was actually changed in OpenMP 5.0, and even "alloc" would decrement the reference counter from OpenMP 5.0.)

Listing 2.3: Usage of alloc

```
1  int A[10], B[10];
2  for (int i =0 ; i < 10 ; i++)
3      A[i] = i;
4
5  #pragma omp target enter data map(to:A
       [0:10]) map(alloc:B[0:10])
6  #pragma omp target map(alloc:B[0:10])
7  for (int i = 0 ; i < 10; i++)
8      B[i] = A[i];
9  #pragma omp target exit data map(from:B
       [0:10])
10
11 for (int i = 0 ; i < 10; i++)
12     printf("%d",B[i]);
```

Listing 2.4: Usage of from

```
1  int A[10], B[10];
2  for (int i =0 ; i < 10 ; i++)
3      A[i] = i;
4
5  #pragma omp target enter data map(to:A
       [0:10]) map(alloc:B[0:10])
6  #pragma omp target map(from:B[0:10])
7  for (int i = 0 ; i < 10; i++)
8      B[i] = A[i];
9  #pragma omp target exit data map(from:B
       [0:10])
10
11 for (int i = 0 ; i < 10; i++)
12     printf("%d",B[i]);
```

This example shows the difficulty in interpreting an independent map construct. Especially when we are dealing with the global variables and map clauses across different functions, maybe even in different files, it becomes nearly impossible to understand and identify potential incorrect usages of the map construct. Our static analysis tool can not only error out on such issues, but also the show debug information to help understand how each map construct is interpreted based on its context.

Example 2 Listing 2.5 shows another example, where because of reference count, user might not get the expected behavior. The line, 9 which executes on the host, does not read the value of "A" that was updated on device at line 7. This is again because the "from" clause on line 5, increments the reference count to 2 on entry, and back to 1 on exit, hence after line 7, "A" is not copied out to host. Listing 2.6 shows the usage of "update" to force the copy-out, and read the expected updated "A" on line 11.

Listing 2.5: Reference Count

```
1  define N 100
2  int A[N], sum=0;
3  #pragma omp target data map(from:A[0:N])
4    {
5      #pragma omp target map(from:A[0:N])
6      for(int i=0; i<N; i++)
7        A[i]=i;
8      for(int i=0; i<N; i++)
9        sum += A[i];
10   }
```

Listing 2.6: Update Clause

```
1
2  define N 100
3  int A[N], sum=0;
4  #pragma omp target data map(from:A[0:N])
5    {
6      #pragma omp target map(from:A[0:N])
7      for(int i=0; i<N; i++)
8        A[i]=i;
9      #pragma omp target update from(A[0:N])
10     for(int i=0; i<N; i++)
11       sum += A[i];
12   }
```

3 Background

3.1 Memory SSA

Our analysis is based on the LLVM Memory SSA [5] [7], which is an imprecise implementation of Array SSA[2]. Memory SSA captures the use-def chains for every memory access in the program. We construct the use-def chains for each array variable, based on the Memory SSA. Memory SSA is a virtual IR, where every definition and phi node creates a new version of memory, which are numbered. It has the following nodes,

- $INIT$, a special node to signify uninitialized or live on entry definitions
- $MemoryDef(N)$, corresponds to a memory store instruction, and where N identifies the last write that this definition clobbers
- $MemoryUse(N)$, where N is the reaching definition, that this node uses
- $MemPhi(N_1, N_2, ...)$, where N_i are all the may reaching definitions

We make the following simplifying assumptions,

- Given an array variable we can find all the corresponding load and store instructions.
- A $MemoryDef$ node, clobbers the entire array associated with its store instruction.
- $MemoryPhi$ node are inserted only at the entry of basic blocks, which have more than one $MemoryDef$s that can flow into the basic block.
- We are concerned with only those array variables that are mapped to a target offload region.

3.2 Scalar Evolution Analysis

Scalar Evolution (SCEV) is a very powerful technique that can be used to analyze the change in the value of scalar variables over iterations of a loop. We can use the SCEV analysis to represent the loop induction variables as chain of recurrences. Then it can be used to symbolically evaluate the minimum and maximum value of every array index expression. section 5 has details of how we implement the analysis and handle different cases.

4 Our Approach

In this work, we assume that variables that have corresponding list items across host and device boundary or across different data environment boundaries on the device need to be updated at the edge of such boundaries. Typically this assumption reflects the practical use-case of the variables. For example, in Listing 2.3, a user would expect the updated value of "B" after the second data environment on line 12. Having said that, a skilled ninja programmer may very well expect "B" to remain stale, because of his knowledge and understanding of the complexities of data mapping rules. Our analysis and error/warning reports from this work are intended only for the former case.

Here we first outline the key steps of our approach with the algorithm and exemplify it with two concrete examples to illustrate the algorithm in action.

4.1 Algorithm

The Algorithm 1 shows the overall algorithm for the data map analysis. Firstly we collect all the array variables used in the various map clauses in the entire module. Then line 5, calls the function `ConstructArraySSA`, which constructs the array ssa for each of the mapped Array varaibles. Then, we call the function, `InterpretTargetClauses`, which modifies the Array SSA graph, as per the map semantics. Then finally `ValidateDataMap` checks the reachability on the final graph, to validate the map clauses, and generates a diagnostic report with the warnings and errors.

Example 1 Let us consider the first example Figure 2a to illustrate our approach for analysis of data mapping clauses. As per Algorithm 1, Figure 2b shows the memory SSA for arrays "A" and "C". Figure 2c shows the resulting graph after disconnecting the nodes belonging to host and device. Figure 2d connects $L1$ with $S2$ with a host-device memory copy for the enter data map pragma with `to`: $A[o:N]$ on line 5. Also, we connect $INIT$ node with $L2$, to account for the `alloc`:$C[0:N]$, which means an uninitialized reaching definition. Now, we can conclude our analysis with the following report

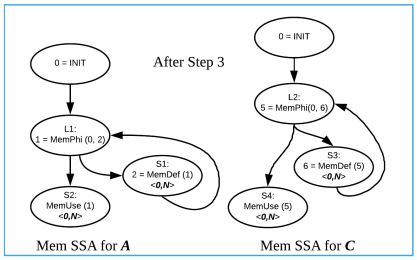
– Error, Node $S4$:$MemUse(5)$ is not connected with its reaching definition from $L2:5 = MemPhi(0,6)$

Algorithm 1 Overview of Data Mapping Analysis

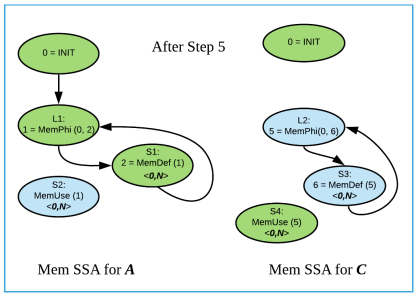
```
1: function DataMapAnalysis(Module)
2:     MappedArrayVars = φ
3:     for ArrayVar ∈ MapClauses do
4:         MappedArrayVars = MappedArrayVars ∪ ArrayVar
5:     ConstructArraySSA(Module, MappedArrayVars)
6:     InterpretTargetClauses(Module, MappedArrayVars)
7:     ValidateDataMap(MappedArrayVars)
8: function ConstructArraySSA(Module, MappedArrayVars)
9:     for MemoryAccess ∈ Module do
10:        ArrayVar = getArrayVar(MemoryAccess)
11:        if ArrayVar ∈ MappedArrayVars then
12:            if MemoryAccess ∈ OMP_targetOffload_Region then
13:                targetNode = true                ▷ If Memory Access on device
14:            else
15:                targetNode = false               ▷ If Memory Access on host
16:            Range = SCEVGetMinMax(MemoryAccess)
17:            underConstruction= GetArraySSA(ArrayVar)
18:                                                 ▷ could be null or incomplete
19:            InsertNodeArraySSA(underConstruction,MemoryAccess, targetNode, range
    )
20:                                  ▷ Incrementally construct, by adding this access
21: function InterpretTargetClauses(Module, MappedArrayVars)
22:     for ArrayVar ∈ MappedArrayVars do
23:        ArraySSA = GetArraySSA(ArrayVar)
24:        for edge, (node, Successornode) ∈ (ArraySSA) do
25:            nodeIsTarget = isTargetOffload(node)
26:            succIsTarget = isTargetOffload(Successornode)
27:            if nodeIsTarget ! = succIsTarget then
28:                RemoveArraySSAEdge( node, Successornode )
29:    for dataMap ∈ dataMapClauses do
30:        hostNode = getHostNode(dataMap)
31:        deviceNode = getDeviceNode(dataMap)
32:        mapType = getMapClauseType(dataMap)
33:                              ▷ alloc/copyIn/copyOut/persistentIn/persistentOut
34:        InsertDataMapEdge(hostNode, deviceNode, mapType)
35: function ValidateDataMap(MappedArrayVars)
36:     for ArrayVar ∈ MappedArrayVars do
37:        ArraySSA = GetArraySSA(ArrayVar)
38:        for memUse ∈ getMemoryUseNodes(ArraySSA) do
39:            useRange = getReadRange(memUse)
40:            clobberingAccess = getClobberingAccess(ArraySSA, memUse)
41:            if isPartiallyReachable(ArraySSA, clobberingAccess, memUse, useRange)
    then
42:                Report WARNING
43:            else if isNotReachable(ArraySSA, clobberingAccess, memUse) then
44:                Report ERROR
```

```
1
2  L1: for ( i =0 ; i < 100 ; i++) {
3          S1: A[i] = 0;
4      }
5  #pragma omp target enter data map(to:A[0:N],
       alloc:C[0:N])
6  #pragma omp target
7  L2: for (i=0; i < 100; i++ ) {
8          S2: t = A[i] ;
9          S3 C[i] = t;
10     }
11 #pragma omp target exit data map( release:C[0:N])
12 L3: for (i=0; i < 100; i++) {
13         S4: print(C[i])
14     }
```

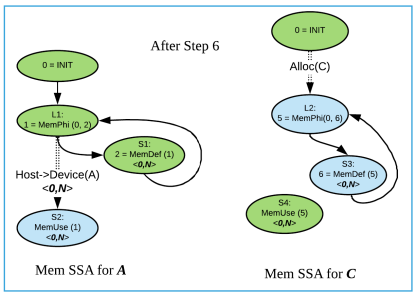
(a) Example 1, user Code



(b) Memory SSA



(c) Classify Host/Device Regions



(d) Host/Device Memory Copies

Fig. 2: Data Map Analysis Example 1

Example 2 For our next example, We modify the Figure 2a, with the following map clauses,

```
#pragma omp target enter data map(to:A[0:50], alloc:C[0:100])
#pragma omp target exit data map(from:C[0:100])
```

Figure 3 shows the SSA graphs for the array "A" and "C" and the final graph after interpreting the map clauses. We report the following warning, after our analysis,

– Warning, Node $S2{:}MemUse(1)$ uses, $< 0, 100 >$, which is not a subset of $< 0, 50 >$

5 Implementation

We have implemented our framework in LLVM 7.0, which has the OpenMP 4.5 implementation. The OpenMP constructs are lowered to runtime calls in Clang, so in the LLVM IR we only see calls to the OpenMP runtime. There are several disadvantages of this approach especially with respect to our analysis. Firstly the region of code that needs to be offloaded to a device, is opaque since it is moved to separate functions. These functions are in turn called from the OpenMP runtime library. As a result, its difficult to perform a global data flow analysis for the

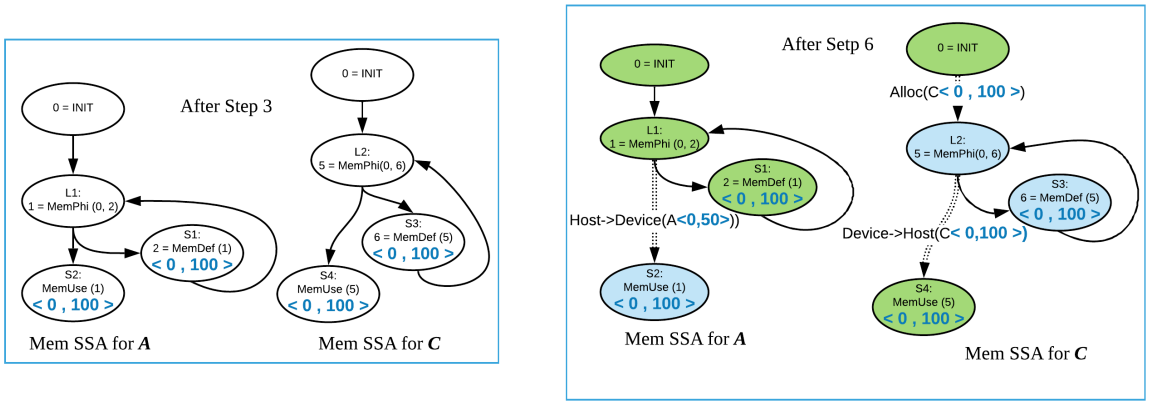


Fig. 3: Data Map Analysis Example 2

memory use-def information of the offloaded region. To simplify the analysis, we implemented a two-pass approach. Firstly we compile the OpenMP program with the flag that enables parsing the OpenMP constructs, and then again without the flag, such that Clang ignores the OpenMP constructs and generates the baseline LLVM IR. During the OpenMP compilation pass, Clang calls our analysis pass, that parses the runtime library calls and generates a csv file that records all the user specified "target map" clauses, as explained in subsection 5.1. During the second pass, we perform the whole program context and flow sensitive data flow analysis, to construct the Memory use-def chains, subsection 5.2. Then this pass validates if the "target map" information generated by the previous pass, respects all the Memory use def relations.

5.1 Interpreting OpenMP pragmas

The offload mechanism used by clang is to generate calls to a runtime library(RTL) whenever "target" directives are encountered. The offload library implements the routines shown in Table 1. In the LLVM IR, whenever we encounter a call to one of these RTL routines, we parse the arguments of the functions, and extract the relevant information from them.

Listing 5.1: Example map clause

```
1 #pragma omp target
2     map(tofrom:A[0:10])
3     for (i = 0 ; i < 10; i++)
4       A[i] = i;
```

Listing 5.2: Pseudocode for LLVM IR with RTL calls

```
1 void **ArgsBase = {&A}
2 void **Args = {&A}
3 int64_t* ArgsSize = {400}
4 void **ArgsMapType = { OMP_TGT_MAPTYPE_TO
        | OMP_TGT_MAPTYPE_FROM }
5 call @__tgt_target
6 (-1, HostAdr, 1, ArgsBase,
7 Args, ArgsSize, ArgsMapType)
```

Listing 5.1 shows a very simple user program, with the target data map clause. Listing 5.2 shows the corresponding LLVM IR in pseudocode, after clang

Table 1: Target Runtime Library Routines

RTL Routines	Arguments

__tgt_target_data_begin :: Initiate a device data environment	`int64_t device_id, int32_t num_args`
	`void** args_base, void** args,`
	`int64_t *args_size, int64_t *args_maptype`

__tgt_target_data_end :: Close a device data environment	`int64_t device_id, int32_t num_args`
	`void** args_base, void** args,`
	`int64_t *args_size, int64_t *args_maptype`

__tgt_target_data_update :: Make a set of values consistent between host and device	`int64_t device_id, int32_t num_args`
	`void** args_base, void** args,`
	`int64_t *args_size, int64_t *args_maptype`

__tgt_target :: Begin data environment, launch target region execution and end device environment	`int64_t device_id, void *host_addr,`
	`int32_t num_args`
	`void** args_base, void** args,`
	`int64_t *args_size, int64_t *args_maptype`

__tgt_target_teams :: Same as above, also specify number of teams and threads	`int64_t device_id, void *host_addr,`
	`int32_t num_args, void** args_base,`
	`void** args, int64_t *args_size,`
	`int64_t *args_maptype,`
	`int32_t num_teams, int32_t thread_limit`

introduces the runtime calls. Line 5 is one of the RTLs from the Table 1, and we parse the arguments of this call to interpret the map construct. For example, the 3rd argument to the call at line Listing 5.2 is 1, that means there is only item in the map clause. Line 1, that is the value loaded into *ArgsBase* is used to get the memory variable that is being mapped. Line 3, *ArgsSize* gives the end of the corresponding array section, starting from *ArgsBase*. Line 4, *ArgsMapType*, gives the map attribute used by the programmer, that is "tofrom".

We wrote an LLVM pass that analyzes every such RTL call, and tracks the value of each of its arguments, as explained above. Once we have this information, we use the algorithm of Figure 1 to interpret the data mapping semantics of each clause. The data mapping semantics can be classified into following categories,

- Copy In: A memory copy is introduced from the host to the corresponding list item in the device environment.
- Copy Out: A memory copy is introduced from the device to the host environment.
- Persistent Out: A device memory variable is not deleted, it is persistent on the device, and available to the subsequent device data environment.
- Persistent In: The memory variable is available on entry to the device data environment, from the last device invocation.

subsection 6.2 shows some examples, to illustrate the above classification.

5.2 Baseline Memory Use Def Analysis

Once we have the information regarding the memory copies introduced by the map clause we construct the Memory SSA of the program. We also perform inlining of all user functions to enable a context-sensitive analysis.

Memory SSA LLVM has an analysis called the MemorySSA[5]. It is a relatively cheap analysis that provides an SSA based form for memory use-def and def-use chains. LLVM MemorySSA is a virtual IR, which maps "Instructions" to "MemoryAccesses", which is one of three kinds, "MemoryPhi", "MemoryUse", "MemoryDef". [5] has more details about the implementation. Listing 5.3 shows an example, with Figure 4 as the simplified MemorySSA.

Listing 5.3: Example of MemorySSA

```
1  int main(){
2    int A[10], B[10];
3    for (int i =0 ; i < 10 ; i++) {
4      // %arrayidx = getelementptr %A, 0, %idxprom
5      // store %i.0, %arrayidx,
6      A[i] = i;
7    }
8  #pragma omp target enter data map(to:A[0:5])
9            map(alloc:B[0:10])
10 #pragma omp target
11   for (int i = 0 ; i < 10; i++) {
12     // %arrayidx7 = getelementptr %A, 0, %idxprom6
13     // %2 = load %arrayidx7
14     int t =  A[i];
15     // %arrayidx9 = getelementptr %B, 0, %idxprom8
16     // store %2, %arrayidx9
17     B[i] = t
18   }
19
20   for (int i = 0 ; i < 10; i++) {
21     //arrayidx19 = getelementptr %B, 0, %idxprom18
22     //%3 = load %arrayidx19
23     printf("%d",B[i]);
24   }
25
26     return 0;
27 }
```

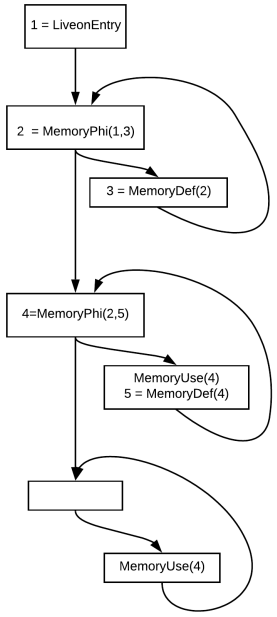


Fig. 4: MemorySSA

We have simplified this example, to make it relevant to our context. *LiveonEntry* is a special "MemoryDef" that dominates every "MemoryAccess" within a function, and implies that the memory is either undefined or defined before the function begins.

The $3 = MemoryDef(2)$ node, notes that there is a store instruction which clobbers the heap version 2, and generates heap 3, which represents the line 8 of the source code. Each for loop can be represented by a $MemoryPhi$ node. For example, $2 = MemoryPhi(1, 3)$ corresponds to the for loop on line 3. There are two versions of the heap reaching this node, the heap 1, $1 = LiveonEntry$ and from the back edge, heap 3, $3 = MemoryDef(2)$. The load of memory A on line

7, corresponds to the $MemoryUse(4)$, that notes that the last instruction that could clobber this read is MemoryAccess 4.

Now, given this MemorySSA, we can extract the Array use-def chains, if we can disambiguate the memory variable that the load/store instruction refers to. So, for any store instruction, for example line 19, we can analyze the LLVM IR, and trace the value that the store instruction refers to. In this example, line 18, refers to memory variable B, and hence clearly, the $5 = MemoryDef(4)$ does not clobber memory variable A.

We perform an analysis on the LLVM IR, which tracks the set of memory variables that each LLVM load/store instruction refers to. It is a context-sensitive and flow-sensitive iterative data flow analysis that associates each MemoryDef/MemoryUse with a set of memory variables. The result of this analysis is an array SSA, for each array variable, that tracks its use-def chain.

5.3 Scalar Evolution Analysis, Array Sections

For our analysis, we need the range of a memory index expression. That is the minimum and maximum values, of the index expression of any memory address. The SCEV analysis can be queried to get the maximum number of iterations of a loop. This value can be used to evaluate the maximum value of the SCEV expression. We have implemented an algorithm in our analysis pass, that given a load/store, computes the minimum and maximum values of the corresponding index into the memory access. This minimum and maximum can be an expression in terms of program variables. We use this analysis to extract the array sections accessed by any memory load/store.

There are three main cases for the result of SCEV analysis

1. The upper and lower bounds are compile time constants
2. The upper and lower bounds are expressions of program variables
3. SCEV is an unknown or cannot be evaluated

For our analysis, we approximate the case 2 and 3, with the maximum size of an array. If the memory load/store is from a static array, then the bounds of the array are compile time constants. Otherwise we parse the arguments of the call to memory alloc (malloc), to get the bounds of the corresponding memory variable.

So, the Array Sections analysis works only if the range of a memory access can be evaluated to compile time integer constants.

Finally we use the algorithm from Algorithm 1 to warn the user if incorrect array sections are used in the memory map clause. The warning can be of the following types

- Array section accessed on the device environment is larger than the array section mapped onto the device, that is out of bounds access on the device
- Array section mapped out of the device environment to the host, is smaller/subset of what the host environment accesses.

6 Evaluation and Case Studies

Listing 6.1: DRACC File 22

```
15 int init(){
16     for(int i=0; i<C; i++){
17         for(int j=0; j<C; j++){
18             b[j+i*C]=1;
19         }
20         a[i]=1;
21         c[i]=0;
22     }
23         return 0;
24 }
25
26
27 int Mult(){
28
29     #pragma omp target map(to:a[0:C]) map(
       tofrom:c[0:C]) map(alloc:b[0:C*C]) device
       (0)
30     {
31         #pragma omp teams
                   distribute parallel for
32         for(int i=0; i<C; i++){
33             for(int j=0; j<C; j++){
34                 c[i]+=b[j+i*C]*a[j];
```

Listing 6.2: DRACC File 26

```
29     #pragma omp target
               enter data map(to:a[0:C],b[0:C*C
                    ],c[0:C]) device(0)
30     #pragma omp target device(0)
31     {
32         #pragma omp teams
                       distribute parallel for
33         for(int i=0; i<C; i++){
34             for(int j=0; j<C; j++){
35                 c[i]+=b[j+i*C]*a[j];
36             }
37         }
38     }
39     #pragma omp target exit
               data map(release:c[0:C])
               map(release:a[0:C],b[0:C*C])
                    device(0)
40     return 0;
41 }
42
43 int check(){
44     bool test = false;
45     for(int i=0; i<C; i++){
46         if(c[i]!=C){
```

Listing 6.3: DRACC File 23

```
28 int Mult(){
29
30     #pragma omp target map(to:a[0:C],b[0:C])
       map(tofrom:c[0:C]) device(0)
31     {
32         #pragma omp teams
                       distribute parallel for
33         for(int i=0; i<C; i++){
34             for(int j=0; j<C; j++){
35                 c[i]+=b[j+i*C]*a[j];
36             }
37         }
38     }
```

Listing 6.4: DRACC File 30

```
19 int init(){
20     for(int i=0; i<C; i++){
21         for(int j=0; j<C; j++){
22             b[j+i*C]=1;
23         }
24         a[i]=1;
25         c[i]=0;
26     }
~
31 int Mult(){
32
33     #pragma omp target
           map(to:a[0:C],b[0:C*C]) map(from:c[0:
                C*C]) device(0)
34     {
35         #pragma omp teams
                       distribute parallel for
36         for(int i=0; i<C; i++){
37             for(int j=0; j<C; j++){
38                 c[i]+=b[j+i*C]*a[j];
```

We use the the DRACC benchmark [1] from Aachen University to evaluate our tool. Table 2 shows some distinct errors found by our tool in the benchmark. We were able to find all the data mapping errors in the benchmark. For example in file number 22,Listing 6.1 the map clause on line 29 is using the *alloc* attribute while line 34 is actually reading the array b, that was defined on line 18, so our tool points out the error message that the "to" clause is mssing. For Listing 6.2 "c" is updated on the device at line 34, but it is not mapped back, and our error points out that the "from/update" clause is missing. For Listing 6.4, "c" is initialized on line 25, but the host variable is not mapped to the device, when creating the device environment at line 33. For Listing 6.3, only "C" elements of "b" are mapped to the device, while the actual size of "b" is "C*C". Our tool is able to track the malloc call to flag this usage as a warning.

The last 3 rows of the table shows the errors pointed out by our tool, for the examples from the motivation section. The errors were explained in section 2

Table 2: Errors found in the DRACC Benchmark

File Name	Error/Warning
DRACC File 22 Listing 6.1	ERROR Definition of :b on Line:18 is not reachable to Line:34, Missing Clause:to:Line:32
DRACC File 26 Listing 6.2	ERROR Definition of :c on Line:35 is not reachable to Line:46 Missing Clause:from/update:Line:44
DRACC File 30 Listing 6.4	ERROR Definition of :c on Line:25 is not reachable to Line:38 Missing Clause:to:Line:36
DRACC File 23 Listing 6.3	WARNING Line:30 maps partial data of :b smaller than its total size
Motivation Ex Listing 2.1	ERROR Definition of :sum on Line:5 is not reachable to Line:6 Missing Clause:from/update:Line:6
Motivation Ex Listing 2.3	ERROR Definition of :B on Line:8 is not reachable to Line:12 Missing Clause:from/update:Line:10
Motivation Ex Listing 2.5	ERROR Definition of :A on Line:7 is not reachable to Line:9 Missing Clause:from/update:8

6.1 Time to Compile

Table 3 shows the time to run OmpSan, on few SPEC ACCEL and NAS parallel benchmarks. We compare it with the time to compile the programs with "-O3" flag. Due to the context and flow sensitive data flow analysis implemented in OmpSan, its runtime is significant, and almost as much as the time to compile the entire program.

Table 3: Time to Run OmpSan

Benchmark Name	-O3 Compilation Time (sec)	OmpSan Runtime (sec)
SPEC 504.polbm	17	16
SPEC 503.postencil	3	3
SPEC 552.pep	7	4
SPEC 554.pcg	15	9
NAS FT	32	15
NAS MG	34	31

6.2 Diagnostic Information

Another major use case for our tool, is to help understand the data mapping behavior of an existing source code. For example, Listing 6.5 shows a code fragment from the benchmark "FT" of "NAS" suite. We argue that it is very difficult to read this openmp target code, as line 311 explicitly maps every array variable with the "alloc" map type. Since, these are global variables, the semantics of this `target map` depend on the previous occurrences of the mapping clause. Our tool can generate the following information, which shows the current state of the data mapping clause.

- *__tgt_target_teams*, from::"ft.c:311" to "ft.c:331"
- Alloc: $u0\_imag[0:8421376], u0\_real[0:8421376]$
- Persistent In :: $twiddle[0:8421376], u1\_imag[0:8421376], u1\_real[0:8421376]$
- Persistent Out :: $twiddle[0:8421376], u0\_imag[0:8421376], u0\_real[0:8421376], u1\_imag[0:8421376], u1\_real[0:8421376]$
- Copy In:: *Null*, Copy Out:: *Null*

Similarly, the data mapping for the function $cffts3\_pos$ Listing 6.6, is as shown below,

- *__tgt_target_teams*, from::"ft.c:1180" to "ft.c:1276"
- Persistent In :: $gty1\_imag[0:16777216], gty1\_real[0:16777216], gty2\_imag[0:16777216], gty2\_real[0:16777216], logd3[0:0], u0\_imag[0:8421376], u0\_real[0:8421376], u1\_imag[0:8421376], u1\_real[0:8421376], u\_imag[0:257], u\_real[0:257]$
- Persistent Out: $u1\_imag[0:8421376], u1\_real[0:8421376], u\_imag[0:257], u\_real[0:257]$
- Copy Out: $gty1\_imag[0:16777216], gty1\_real[0:16777216], gty2\_imag[0:16777216], gty2\_real[0:16777216], u0\_imag[0:8421376], u0\_real[0:8421376]$

Listing 6.5: *evolve* from NAS/ft.c

```
 307 static void evolve(int d1, int d2, int d3)
308 {
309   int i, j, k;
310 // ...
311 #pragma omp target map (alloc: u0_real,
      u0_imag,u1_real,u1_imag,twiddle)
312   {
313 #pragma omp teams distribute
314     for (k = 0; k < d3; k++) {
315 #pragma omp parallel for
316       for (j = 0; j < d2; j++) {
317 #pragma omp simd
318         for (i = 0; i < d1; i++) {
319           u0_real[k*d2*(d1+1) + j*(d1+1) + i
      ] = u0_real[k*d2*(d1+1) + j*(d1+1) + i]
320
      *twiddle[k*d2*(d1+1) + j*(d1+1) + i];
321           u0_imag[k*d2*(d1+1) + j*(d1+1) + i
      ] = u0_imag[k*d2*(d1+1) + j*(d1+1) + i]
322
      *twiddle[k*d2*(d1+1) + j*(d1+1) + i];
```

Listing 6.6: *cffts3_pos* from NAS/ft.c

```
 1153 static void cffts3_pos(int is, int d1, int
       d2, int d3)
1154 {
1155   int logd3;
1156   int i, j, k, ii;
1157   int l, j1, i1, k1;
1158   int n1, li, lj, lk, ku, i11, i12, i21, i22
      ;
1159   double uu1_real, x11_real, x21_real;
1160   double uu1_imag, x11_imag, x21_imag;
1161   double uu2_real, x12_real, x22_real;
1162   double uu2_imag, x12_imag, x22_imag;
1163   double temp_real, temp2_real;
1164   double temp_imag, temp2_imag;
1165
1166   logd3 = ilog2(d3);
~
1180 #pragma omp target teams distribute collapse
      (2)
1181     for (j = 0; j < d2; j++) {
1182 //#pragma acc loop vector independent
1183 //#pragma omp simd
1184       for (i = 0; i < d1; i ++) {
1185 #pragma omp parallel for
1186         for (k = 0; k < d3; k++) {
1187           gty1_real[j][k][i] = u1_real[k*d2
      *(d1+1) + j*(d1+1) + i];
1188           gty1_imag[j][k][i] = u1_imag[k*d2
      *(d1+1) + j*(d1+1) + i];
1189         }
1190
```

6.3 Limitations

Since our analysis is a static analysis tool, there are a few limitations as listed below

- We can only deal with Array variables, and we cannot handle dynamic data structures like linked lists. This is an inherent limitation of static analysis

- Our implementation cannot handle target regions inside recursive functions, since we are inlining every function. This can be fixed by improving our context sensitive analysis
- Our implementation can only handle compile time constant array sections, and constant loop bounds. Our tool can be extended to handle runtime expressions, if we can compare the equivalence of two symbolic expressions.
- We donot handle "declare target", since in LLVM IR, the "declare" region is moved to a separate region, this can also be fixed if we can analyze the modules together.

7 Related Work and Conclusion

Managing data transfers to and from GPUs has always been an important problem for GPU programming. Several solutions have been proposed to help the programmer in managing the data movement. The OpenMPC compiler [4] also proposed a static analysis to insert data transfers automatically. Seyong et. al proposed a directive based approach, that combined compile-time/runtime method to verify the correctness of CPU-GPU memory transfer and even optimize it in [3]. Pai et. al [8] proposed a compiler analysis to detect potential stale accesses and uses a runtime to initiate transfers as necessary, for the X10 compiler. [9] also proposed a static analysis technique to optimize the data transfers for the X10. [6] has also worked on automatically inferring the OpenMP mapping clauses using some static analysis.

In this paper, we have developed a static analysis technique to interpret the semantics of the openmp map clause, and deduce the data transfers introduced by the clause.

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