ECE 4623/5623
Computer Hardware Design
Fall 2017

TIME: TR 6:00 - 7:20 PM

PLACE: CEC 438

INSTRUCTOR:

Dr. Nick Mould
Office: DEH 305
Phone: (405) 488-5252
Office Hours: TR 5:00 PM - 6:00 PM
Email: nick.mould@gmail.com

TEACHING ASSISTANT:

TBD
Office:
Office Hours:
Email:

REFERENCES:

1. *Basys3 ^{TM} Evaluation Board Tutorial*, Digilent Incorporated, 2015.
2. *Basys3 ^{TM} FPGA Board Reference Manual*, Digilent Incorporated, August 12, 2014.
3. *Basys3 ^{TM} Evaluation Board Schematic*, Digilent Incorporated, May 21, 2014.
4. *VHDL Language Reference Manual*, IEEE Standard 1076, 2008.

COURSE WEBSITE:

We will use the OU Desire to Learn website for everything in this course.

PREREQUISITE:

ECE 3223

COURSE DESCRIPTION:

In this course we will learn the fundamentals of digital circuit design with FPGAs (Field Programmable Gate Arrays). We will be programming circuits into low-cost FPGA evaluation boards using VHDL. The topics covered in this course include: register transfer structures, arithmetic logic units (ALUs), state machines, data acquisition and filtering, and universal asynchronous receive/transmit (UART). Additionally, we will study several different CLBs (complex logic blocks) used in FPGAs to realize digital circuits.

COURSE OUTLINE:

1. **8/22/2017:** First Day Quiz, Explain Homework 1

2. **8/24/2017:** Lecture: Decoders, Encoders, Latches, and Flip-Flops
3. **8/29/2017:** Lecture: VHDL Basics, Xilinx Software Install
4. **8/31/2017:** Xilinx Workshop (New Project, Constraint File, Program Board)
5. **9/5/2017:** Xilinx Workshop (Binary to BCD)
6. **9/7/2017:** Xilinx Workshop (7-Segment Display)
7. **9/12/2017: Homework 1 Due**, Lecture: State Machine Design
8. **9/14/2017:** No Class, Career Fair
9. **9/19/2017:** Xilinx Workshop (Sequence Detection)
10. **9/21/2017:** Lecture: IO Circuits
11. **9/26/2017:** Xilinx Workshop (Register File)
12. **9/28/2017:** Xilinx Workshop (Adder)
13. **10/3/2017: Homework 2 Due**
14. **10/5/2017:** Xilinx Workshop (Array Multiplier)
15. **10/10/2017:** Lecture: Counters and Clock Division Methods
16. **10/12/2017:** Excel Workshop (Clock Division and Waveform Synthesis)
17. **10/17/2017: Homework 3 Due**, Lecture: UART, LaTeX
18. **10/19/2017:** Homework Help Day
19. **10/24/2017:** Xilinx Workshop (UART Receive)
20. **10/26/2017:** Xilinx Workshop (UART Transmit)
21. **10/31/2017:** Xilinx Workshop (FIFO)
22. **11/2/2017:** Xilinx Workshop (UART, FIFO, RISC Computer)
23. **11/7/2017:** Lecture: SPI, I^2C, Ethernet
24. **11/9/2017:** Xilinx Workshop (A/D Converter)
25. **11/14/2017:** Xilinx Workshop (A/D Converter, FIFO, Filter)
26. **11/16/2017: Homework 4 Due**
27. **11/21/2017:** No Class, Thanksgiving
28. **11/23/2017:** No Class, Thanksgiving
29. **11/28/2017:** Review for Final Exam
30. **11/30/2017:** Final Exam

HOMEWORK PROJECTS:

There will be a total of 4 homework assignments composed of 1 review/orientation assignment and 3 projects. Each of the homework assignments will be be worth 20% of the final grade. All of the homework assignments will require the Basys3 ^{TM} Evaluation Board (approximately $100). Late homework assignments will not receive full credit. The grade on late homework assignments will be reduced by 10% for each business day that the homework is late.

It is very important that you do your own work. You are encouraged to work together, but your work should be your own. A good way to do this is to work together on diagrams of the

circuit design and then each person implement their own VHDL project. I will read the code that you submit. Please do not cheat. Please do not cheat and then attempt to camouflage the cheating by obscuring unimportant features of the code and then hope that I will be too lazy to detect this behavior. Don't cheat, I will turn you in to the Academic Misconduct Office.

TESTS:

The final exam will be worth 20% of the final grade.

GRADING:

Item	Value
HW #1	20%
HW #2	20%
HW #3	20%
HW #4	20%
Final Exam	20%

REASONABLE ACCOMMODATION FOR STUDENTS WITH DISABILITIES:

Any student in this course who has a disability that may prevent the full demonstration of his or her abilities should contact me personally as soon as possible so we can discuss accommodations necessary to ensure full participation and facilitate your educational opportunities.

ADJUSTMENTS FOR PREGNANCY/CHILDBIRTH RELATED ISSUES:

Should you need modifications or adjustments to your course requirements because of documented pregnancy-related or childbirth-related issues, please contact me as soon as possible to discuss. Generally, modifications will be made where medically necessary and similar in scope to accommodations based on temporary disability. Please see
http:www.ou.edu/content/eoo/faqs/pregnancy-faqs.html for frequently asked questions.

TITLE IX RESOURCES:

For any concerns regarding gender-based discrimination, sexual harassment, sexual misconduct, stalking, or intimate partner violence, the University offers a variety of resources, including advocates on-call 24.7, counseling services, mutual no contact orders, scheduling adjustments and disciplinary sanctions against the perpetrator. Please contact the Sexual Misconduct Office 405-325-2215 (8-5, M-F) or the Sexual Assault Response Team 405-615-0013 (24.7) to learn more or to report an incident.

ACADEMIC MISCONDUCT:

The College of Engineering enforces the requirements of the OU Academic Misconduct Code. You should be fully aware of, and familiar with, OUs policy on plagiarism and academic misconduct. OU policy will apply in cases of (1) cheating, plagiarism, falsification of records, unauthorized possession of exams, intimidation, and any and all other actions that may improperly affect the evaluation of a student's academic performance or achievement; (2) assisting others in any such act; or (3) attempts to engage in such acts. Unfamiliarity with OU policy will not be accepted as an adequate excuse in cases of academic misconduct. More information is available on-line at http://integrity.ou.edu.

REGISTRATION & WITHDRAWAL:

You are responsible for ensuring that all University paperwork required for enrollment and/or withdrawal is done correctly and submitted consistent with deadlines. Your grade will be calculated with missed grades entered as zero if you stop attending the course and doing the course work unless you complete the appropriate University form, obtain the required signatures, and turn the form in before the deadline. This could result in receiving a grade of F in the course. Deadlines are shown in the Academic Calendar, which is available from the Office of Admissions and Records or online at http://www.ou.edu/admissions.