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Diagram illustrating the proposed 1T1R device structure. The structure consists of a p-type substrate (P-TS) at the bottom, a 1T1R layer in the middle, and a p-type layer (P-TS) at the top. The 1T1R layer is divided into two regions: a 'ferro' region on the left and a 'qma' region on the right. A 'GND' label is at the top left, and a 'pH' label is at the top right.

2G5	2A
2GT	
GND	

46

$\frac{1}{2}$

The diagram illustrates a 16-bit bus system. It features two 8-bit data buses, labeled 'DATA' and 'DATA', and a 16-bit address bus, labeled 'ADDRESS'. The address bus is connected to a memory block labeled 'MEM'. The data buses are connected to a memory block labeled 'MEM'. The address bus is also connected to a memory block labeled 'MEM'. The diagram shows the internal structure of the bus system, including the address and data buses, and the memory blocks.

The Available Pins
Are Labeled

[illegible]

IN-
IN+

☐ - TUO
 775
☐ + TUO
 777

Two V5

noqmo3