Virtual Impedance Loop for Droop-Controlled Single-Phase Parallel Inverters Using a Second-Order General-Integrator Scheme

José Matas, Miguel Castilla, Luis García de Vicuña, Jaume Miret, *Member, IEEE*, and Juan Carlos Vasquez

***Abstract*—This paper explores the impact of the output impedance on the active and reactive power flows between parallelized inverters operating with the droop method. In these systems, a virtual output impedance is usually added to the control loop of each inverter to improve the reactive power sharing, regardless of line-impedance unbalances and the sharing of nonlinear loads. The virtual impedance is usually implemented as the time derivative of the inverter output current, which makes the system highly sensitive to the output current noise and to nonlinear loads with high slew rate. To solve this, a second-order general-integrator (SOGI) scheme is proposed to implement the virtual impedance, which is less sensitive to the output current noise, avoids to perform the time derivative function, achieves better output-voltage total harmonic distortion, and enhances the sharing of nonlinear loads. Experimental results with two 2-kVA inverter systems under linear and nonlinear loads are provided to validate this approach.**

***Index Terms*—Distributed generation (DG), droop control method, nonlinear loads, parallel inverters, second-order general integrators (SOGIs), virtual output impedance.**

I. Introduction

ENERGY distribution in a system formed by several inverters operating in parallel can be performed today with different methods, either with or without communication between the power elements. In such systems, it is very important to minimize the circulating current that can flow among the power units in order to have equal load sharing and deliver high-quality power. Several control strategies have been adopted to achieve this goal, such as the concentrated control technique [1], the master-slave control method [2]–[4], the power-deviation control method [5], [6], the control area network communication [7], and the frequency and voltage droop method [8]–[13]. In these last parallel systems, the controller is only based on inverter local-measured information, it does not rely on intercommunication signals between the inverters, and constitutes a truly distributed and redundant system.

In order to achieve good power sharing, the droop method makes tight adjustments over the output-voltage frequency and amplitude of the inverter, as a power-dependent function, to compensate the active and reactive power unbalances [12], [13]. However, the transient and steady-state behaviors of the droop method are highly dependent on the system mismatches, that can affect the inverter output impedance accuracy, and the line impedance of the wires used to perform the inverters connection [14], [15].

Usually, the line impedance and the output impedance of the inverters are considered to be mainly inductive, due to a large output-inductor value or by long distances between the units. However, this is not always true since the inverter output impedance also depends on the adopted inverter control strategy and on the system parameters [16]–[20]. Improved droop methods have been proposed and successfully applied to the case of inductive [19], [20], resistive [21], and complex impedances [22]. In these works, virtual inductive, resistive, and complex impedances are proposed to fix the output impedance of the inverter and to ensure power-sharing stability. In the case of virtual inductor, this impedance is implemented by drooping the output-voltage reference proportionally to the time derivative of the inverter output current. In addition, in [19] the proposed virtual inductor includes a soft start operation for grid connection and considers the time derivative of higher harmonics to reduce and share current distortion among the inverters of a microgrid. As a consequence, the inverter can be affected by the output-current inherent noise and distorted by any kind of nonlinear load with a strong slew rate. For this reason, a low-pass filter (LPF) is normally used in conjunction with the virtual inductor to limit the amount of distortion introduced into the system.

The second-order general integrator (SOGI) algorithm is normally used, in cooperation with a Frequency Locked Loop (FLL), for grid voltage and frequency synchronization, due to its effectiveness when the grid is unbalanced and distorted. Additionally, it is easy to implement and it can filter the input signal without delay due to its natural resonance at the fundamental frequency [23]–[29]. The SOGI algorithm is essentially an effective way to provide an orthogonal signal system that it is insensitive to the input signal noise.

In this paper, the SOGI scheme is proposed to reduce the distortion that nonlinear loads produce on a paralleled system

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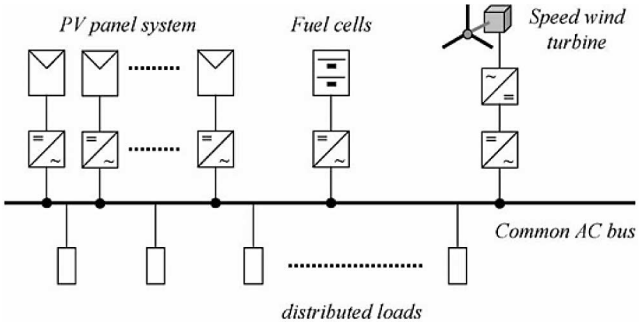


Fig. 1. DG units connected in parallel to a common ac bus.

due to the virtual-inductor impedance implementation. To perform this, an analysis of the SOGI algorithm applied to linear and nonlinear loads is presented that leads to a new scheme design for the virtual impedance implementation using the SOGI algorithm. This virtual impedance can be resistive, inductive, or complex. This scheme has the property that it only operates with the fundamental component of the output current and it is not sensitive to noise, therefore, it reduces the amount of distortion produced by nonlinear loads in the inverter output voltage. Moreover, the virtual inductance implementation avoids the time derivative operation of the output current, which reduces the computational time charge of the algorithm. Experimental results are provided for a system formed by two 2-kVA inverters in parallel using a virtual-inductor impedance. The obtained results show that the SOGI virtual impedance approach achieves less distortion on the output voltage, so better THD is achieved for the proposed system.

This paper is organized as follows. In Section II, the droop-method scheme with virtual impedance is briefly reviewed. The effect of linear and nonlinear loads on a virtual-inductor impedance is examined. Section III explains the SOGI-filter structure, describes its orthogonal characteristics in detail, and depicts its time responses to linear and nonlinear loads. In this section, an SOGI alternative structure for virtual impedance that can be resistive, inductive, or complex, and its benefits over the classical approach is presented. In Section IV, experimental results of two 2-kVA paralleled inverters with virtual-inductor impedance are presented. This section shows the effect of the SOGI virtual impedance on the system, and how the SOGI approach reduces the distortion in the system output voltage, achieving better THD in the case of nonlinear loads. Section V is devoted to the conclusion.

II. Review of Droop Control and Virtual Impedance Concepts

Fig. 1 shows a distributed generation (DG) system made up of different kind of resources, such as solar panels, fuel cells, and speed wind turbines. Every resource needs an electric power interface to transfer energy to the common bus, and can be modeled as an inverter connected to the common bus through decoupling impedance, as shown in Fig. 2.

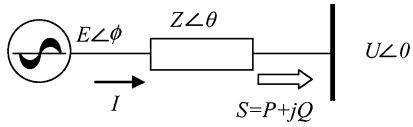


Fig. 2. Equivalent circuit of an inverter connected to a common bus.

From Fig. 2, the expression of the output current is

$$I = \frac{E\angle\phi - U\angle 0}{Z\angle\theta} = \frac{E}{Z}\angle(\phi-\theta) - \frac{U}{Z}\angle(-\theta) \tag{1}$$

where $E\angle\phi$ is the inverter open circuit voltage, I is the inverter output current, $U\angle 0$ is the common bus voltage, and $Z\angle\theta = R + jX$ is the inverter to the common bus impedance, which considers the inverter output impedance and the line impedance of the connection wires. The apparent power injected by an inverter to the ac common bus is

$$S = P + jQ \tag{2}$$

where P is the active power, and Q is the reactive power. By using (1) and (2), the active and reactive powers can be deduced as follows:

$$P = \frac{U}{Z}\left[(E\cos\phi - U)\cos\theta + E\sin\theta\sin\phi\right] \tag{3}$$

$$Q = \frac{U}{Z}\left[(E\cos\phi - U)\sin\theta - E\cos\theta\sin\phi\right]. \tag{4}$$

These expressions can be simplified if we consider that the phase difference ϕ between the inverters output voltages and the common bus voltage are very small, which is true because the inverters are first accurately synchronized to the common bus voltage before the connection to the bus. Therefore, considering ϕ to be very small, (3) and (4) can be simplified to

$$P \cong \frac{U}{Z}\left[(E-U)\cos\theta + E\phi\sin\theta\right] \tag{5}$$

$$Q \cong \frac{U}{Z}\left[(E-U)\sin\theta - E\phi\cos\theta\right]. \tag{6}$$

With these last terms, it can be seen that P and Q depend simultaneously on the difference between the inverter output voltage and the common bus voltage $(E-U)$, and on the system impedance angle θ [22]. The active and reactive powers can then be particularized to three kinds of possible system impedances: mainly inductive, mainly resistive, and complex impedance. For DG systems, where the impedance is usually mainly inductive, $X \gg R$ and $Z\angle\theta \cong X\angle 90$, (5) and (6) can be further simplified to

$$P \cong \frac{UE\phi}{X} \tag{7}$$

$$Q \cong \frac{U(E-U)}{X} \tag{8}$$

where X is the output reactance of an inverter. In these relations, it can be seen that the inverter amplitude appears in both, (7) and (8), but the angle ϕ appears only in (7). Hence, the angle ϕ and

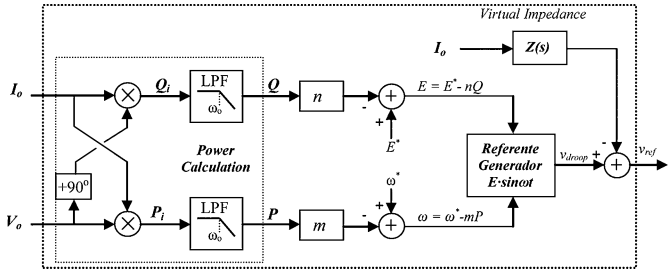


Fig. 3. Block diagram of the droop method with virtual output impedance.

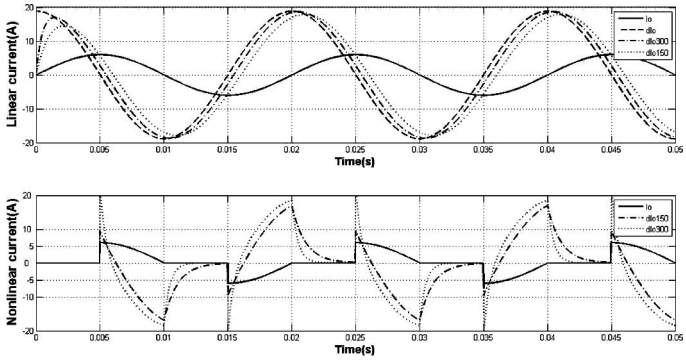


Fig. 4. Output response of the virtual inductor of (12) for different LPF cut-off frequencies: $dI_o(150)$ and $dI_o(300)$ for 150 and 300 Hz, cut-off frequencies, respectively; dI_o is the response without LPF. Upper plots: Responses to a linear current of 6 A. Bottom plots: Responses to a thyristor-type nonlinear current of 6 A.

the voltage difference between the inverter and the common bus $E - U$, are used to regulate the amount of active and reactive powers injected to the system, respectively. Consequently, most of the wireless controllers used in parallel inverters employ the conventional droop method, which introduces the following droops in the amplitude E and frequency ω of the inverter output voltage

$$\omega = \omega^* - mP \tag{9}$$

$$E = E^* - nQ \tag{10}$$

ω^* and E^* being the nominal frequency and amplitude output voltage at no load, and *m* and *n* the frequency and amplitude droop coefficients, respectively.

It is well known that if droop coefficients are increased, then good power sharing is achieved at the expense of degrading the voltage regulation [16], which can be acceptable if, for instance, the frequency and amplitude deviations are mostly at 2% and 5%, respectively [30]. The inherent trade-off of this scheme restricts the mentioned coefficients, which can be a serious limitation in terms of transient response, power-sharing accuracy, and system stability [21].

On the other hand, to carry out the droop functions expressed at (9) and (10), it is necessary to calculate the average value over one line cycle of the instantaneous active and reactive output powers. This is usually done by the means of LPFs with a cut-off frequency lower than the bandwidth of the closed-loop inverter. Therefore, the power calculation filters and droop coefficients determine, to a large extent, the stability and dynamics of the DG system [21].

In order to increase the stability of the system, reduce the impact of circulating currents, and to share linear and nonlinear loads, some approaches introduce a virtual impedance into the system by an additional control loop [11], [20], [21], of the form

$$v_{\rm ref} = v_{\rm droop} - z_v(s) i_o \tag{11}$$

where $v_{\rm droop}$ is the voltage reference delivered by the droop method and $z_v(s)$ is the virtual output impedance. Fig. 3 shows the bock diagram of the system control by the droop method and with the virtual impedance.

In [20], a virtual inductive output impedance ($z_v(s) = sL_v$, where L_v is the inductor value and *s* is the Laplace operator) is implemented by drooping the reference output voltage proportionally to the time derivative of the inverter output current. This loop increases the total inverter output inductive impedance, increasing thus the impedance between the inverter and the common bus line, and reducing the circulating current in the system. However, the virtual impedance is implemented by the time derivative of the inverter output current that can amplify the noise that is normally present in this current. As a result, a LPF is introduced into this loop to avoid the introduction of excessive noise into the system. This approach works well for linear loads, and also, for nonlinear loads with smooth current waveforms. However, the virtual-inductor value should be small in the case of nonlinear loads with a high slew rate, or a sharp current waveform, to prevent the system to be affected by excessive distortion. This effect can be noticed in Fig. 4 that shows the time response of the following virtual-inductor impedance

$$z_v(s) = sL_v \frac{\omega_C}{s + \omega_C} \tag{12}$$

where, ω_C is the LPF cut-off frequency. Fig. 4 shows the output response of (12) to linear and nonlinear currents considering different cut-off frequencies and for a virtual inductor of 10 mH. In the upper plots, it is shown the linear input current as I_o, the output response without LPF as dI_o, and the output responses with LPF and cut-off frequencies of 150 and 300 Hz, as $dI_o(150)$ and $dI_o(300)$, respectively. In the bottom plots are shown, in the same way, the output responses for a thyristor-type nonlinear input current. As it can be seen, for linear currents, it is desirable to have higher cut-off frequencies in order to achieve an output behavior with less delay as possible, but this fact would lead to an increase of the harmonic content of the system. On the other hand, for a nonlinear current, a higher cut-off frequency produces higher output spikes that can generate strong output-voltage distortions, because the output impedance response is directly related to the inverter voltage reference, see Fig. 3.

III. Proposed Virtual Output Impedance Based on the SOGI Algorithm

The SOGI scheme is based on a frequency-adjustable resonator, which can be implemented by two cascaded integrators working in a closed loop [21], see Fig. 5. This structure is usually used with an FLL algorithm for grid characterization to

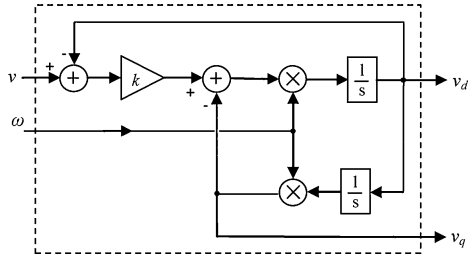


Fig. 5. Block diagram of SOGI structure.

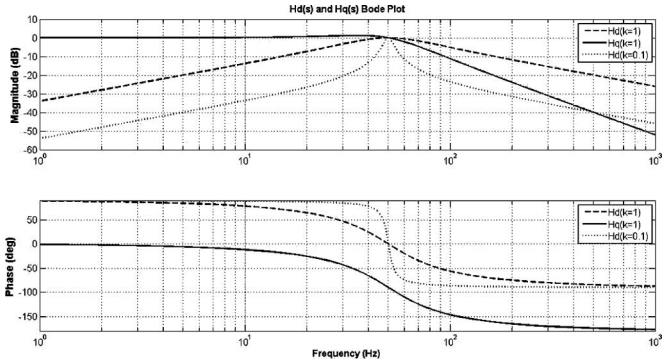


Fig. 6. Bode plot of $H_d(s)$ and $H_q(s)$ transfer functions.

provide precise grid magnitude and phasors in three-phase systems [26]–[28]. In addition, it can be easily implemented and has the advantages of fast and accurate signal-tracking capabilities with good rejection to the input signal noise.

As shown in Fig. 5, it requires a signal *v* and a frequency value ω as inputs, and generates two orthogonal sine waves as outputs (v_d and v_q), which have the same magnitude as the input v, but with a phase shift of 90° with respect to each other. Furthermore, the output v_d is in phase with the fundamental component of the input signal v. The SOGI closed-loop transfer functions are

$$H_d(s) = \frac{v_d}{v}(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{13}$$

$$H_q(s) = \frac{v_q}{v}(s) = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{14}$$

where *k* is the gain of the closed-loop system. The Bode diagrams of these transfer functions are represented in Fig. 6 for $\omega = 2\pi 50\,\mathrm{rad/s}$ and $k = 1$. From this figure, it can be seen that $H_d(s)$ behaves as a bandpass filter, with a bandwidth determined by k, while $H_q(s)$ behaves as a LPF.

The SOGI bandpass behavior is more selective for lower values of *k*. On the other hand, in Fig. 7, it can be seen that the value of *k* also determines the transient response of the filter: a lower value of *k* implies long transient responses, while a higher value of *k* implies short transient responses.

Fig. 8 shows the SOGI time response to a linear current with a peak value of 6 A and distorted by high-frequency noise. It is clear that the v_d and v_q outputs are unaffected by the

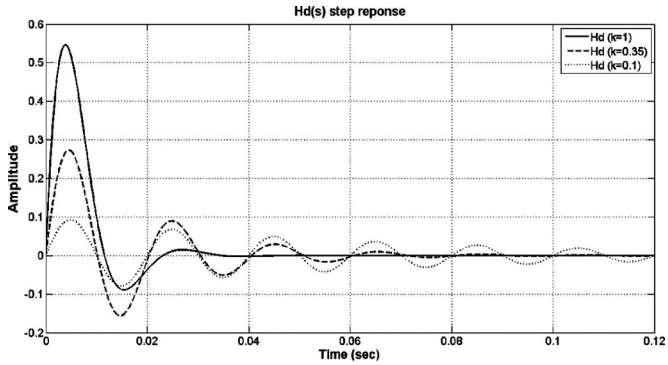


Fig. 7. Step response of the close-loop transfer function (H_d) for different values of k.

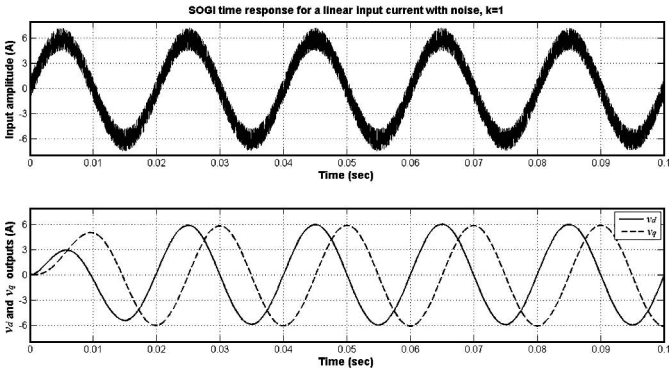


Fig. 8. SOGI time response for a linear input current of 6 A with noise and for $k = 1$.

input noise, v_d is in phase with the input, and v_q is 90° lagged respect to v_d. Likewise, Fig 9 shows the SOGI time response to a nonlinear load for $k = 1$ and $k = 0.1$, respectively. It is obvious that the transient response is shorter for $k = 1$ than for $k = 0.1$. However, it is important to note that, for $k = 1$, the v_d output is not a pure sinusoid due the bandwidth of $H_d(s)$. This output is distorted by the nonlinear input current waveform, meanwhile v_q is nearly sinusoidal and less distorted than v_d. On the other hand, it is clear that the SOGI v_d output, for $k = 1$, has a fast transient response, but it cannot be used to perform an inductive virtual impedance, because is not quite the fundamental component of the input current and a time derivative of it is going to amplify the v_d signal harmonics. For this reason and to operate only with the fundamental component, it is necessary to use lower *k* values, like $k = 0.1$, or $k = 0.35$, but at the expense of longer dynamic responses, see Fig. 9.

Another approach can be adopted to implement a virtual inductor ($z_v(s) = sL_v$) taking the benefits of the SOGI orthogonal features. Looking to Fig. 9, for $k = 0.1$, it can be seen that the v_q signal, plotted with a dashed line, is nearly sinusoidal and 90° lagged respect of v_d. Note that this behavior is because v_q is obtained through an integrator in the block scheme of Fig. 5 ($v_q(s)/v_d(s) = \omega/s$). Thus, assuming that the output v_d is going to be the fundamental component of the input v, we can state

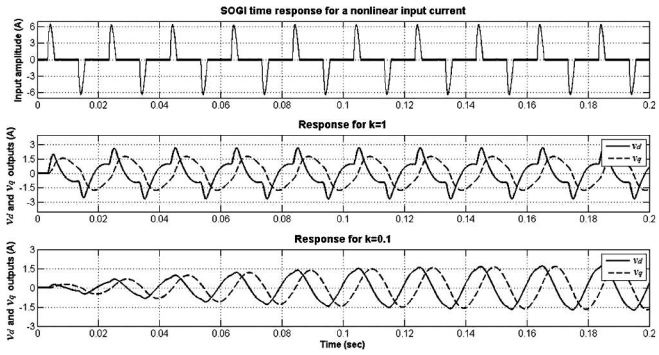


Fig. 9. SOGI time response for a nonlinear input current of 6 A and for $k = 1$ and for $k = 0.1$.

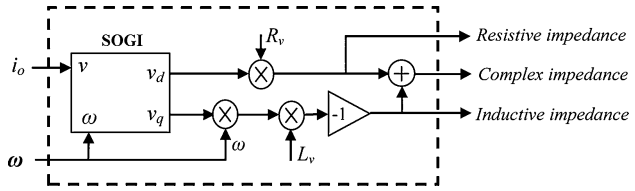


Fig. 10. Virtual impedance implementation by SOGI approach that can be inductive, resistive, or complex.

that

$$v_d(t) = A\sin(\omega t) \tag{15}$$

$$v_q(t) = -A\cos(\omega t) \tag{16}$$

where A and ω are the amplitude and frequency of the input signal, respectively. Considering (15), the virtual impedance is

$$z_v(t) = L_v \frac{dv_d(t)}{dt} = \omega L_v A\cos(\omega t). \tag{17}$$

Then, using (16) and (17), the virtual impedance can be obtained by simply multiplying v_q by $-\omega$ and by the inductance desired value, i.e.,

$$z_v(t) = -\omega L_v v_q(t) \tag{18}$$

Now, by using v_q instead of v_d, we avoid to perform the time derivative of (17). Moreover, its realization by using v_q is less affected by input harmonics, as it is shown in Fig. 9, for $k = 1$ and 0.1, than using v_d.

In the same way, if a virtual resistor is needed, in the case of systems with only resistive lines, it can be simply implemented by using the SOGI v_d output as follows:

$$z_v(t) = R_v v_d(t) \tag{19}$$

where R_v is the virtual resistor value. Fig. 10 depicts the final block diagram of the virtual impedance with the SOGI-filter approach that can be inductive, resistive, or complex. Take into account that in this proposed SOGI scheme the frequency input corresponds to the frequency delivered by the droop method in (9).

IV. Effects of the Virtual Impedance in a Parallel Inverter's System

In a parallel system, it is interesting to increase the inverter output impedance in order to achieve less circulating current between the inverters, which it is usually done by adding a virtual impedance into the system as an additional control loop, see Fig. 3. This loop usually consists of a virtual inductor implemented by a time derivative of the output current and an LPF. This section shows the limitations of this approach and proposes a new implementation for the virtual impedance with the SOGI algorithm. With this new approach, the increase in the inverter impedance is achieved only around the frequency of operation of the droop method (around 50 Hz). Thus, the virtual impedance effects are also constrained around this frequency achieving, at the end, less distortion, so better THD, on the output voltage of the line bus shared by the inverters.

Fig. 11 illustrates the block diagram of the controller used to regulate the inverters in a paralleled system sharing a common load. The controller includes an output-voltage loop and a current compensation loop that ensures good steady state and dynamic performance [22]. In this figure, k_p and k_i are the proportional and integral coefficients of a PI control voltage loop, k_c is a current loop gain, VDC is the inverter DC bus voltage, H is the amplitude of the inverter pulse width modulation (PWM), kPWM = 1/H is the PWM gain, L is the inductance of the output filter, r is the inductor parasitic resistance, C is the capacitance of the output filter, and $Z_{\rm Load}$ is the inverter load.

The dynamic behavior of the closed-loop output voltage is obtained from the control block diagram in Fig. 11 as follows:

$$v_o(s) = \frac{k_c(k_p s + k_i)}{LCs^3 + C(r + k_c)s^2 + k_p k_c s + k_i k_c} v_{\rm ref}(s) - \frac{Ls^2 + rs}{LCs^3 + C(r + k_c)s^2 + k_p k_c s + k_i k_c} i_o(s) \tag{20}$$

From (20), it can be seen that the inverter can be modeled as a two-terminal Thevenin equivalent circuit, [20]–[22], of the form

$$v_o(s) = g(s)v_{\rm ref}(s) - z_o(s)i_o(s) \tag{21}$$

where $g(s)$ is the inverter reference-to-output-voltage transfer function, and $z_o(s)$ is the closed-loop output impedance transfer function. Looking at (21) it is clear that the output impedance of the closed-loop inverter affects the power-sharing accuracy and also determines the droop-control strategy [20]. To impose a desired output impedance, the output-voltage reference can be drooped as a function of the output current by

$$v_{\rm ref}(s) = v_{\rm droop}(s) - z_v(s)i_o(s) \tag{22}$$

where $v_{\rm droop}$ is the inverter voltage reference delivered by the droop method, see Fig. 3. With (22), the inverter output impedance can be fixed in terms of magnitude and phase to ensure a proper behavior in the paralleled system. Introducing (22) into (21), the closed-loop dynamic behavior of the inverter can be reformulated as follows:

$$v_o(s) = g(s)v_{\rm droop}(s) - \left[z_o(s) + g(s)z_v(s)\right] i_o(s) \tag{23}$$

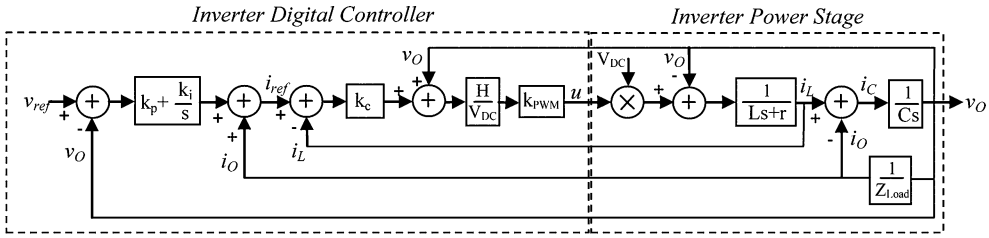


Fig. 11. Block diagram of the controller that regulates an inverter of the paralleled system.

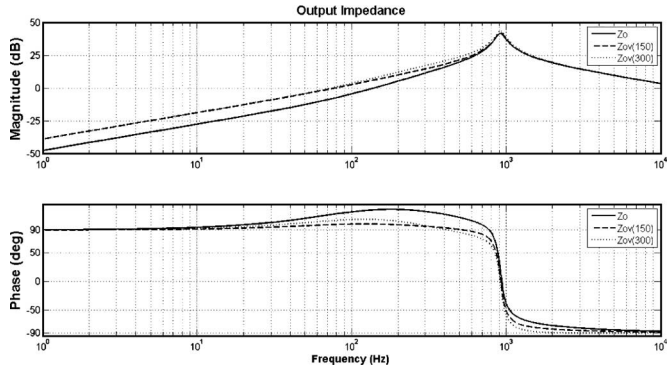


Fig. 12. Bode plot of the inverter output impedance considering the virtual-inductor impedance of (12). Z_o is the original inverter's output impedance. $Z_{ov}(150)$ and $Z_{ov}(300)$ considers the effect of a virtual inductor $L_v = 4\,\mathrm{mH}$ with 150 Hz and 300 Hz cut-off frequencies, respectively.

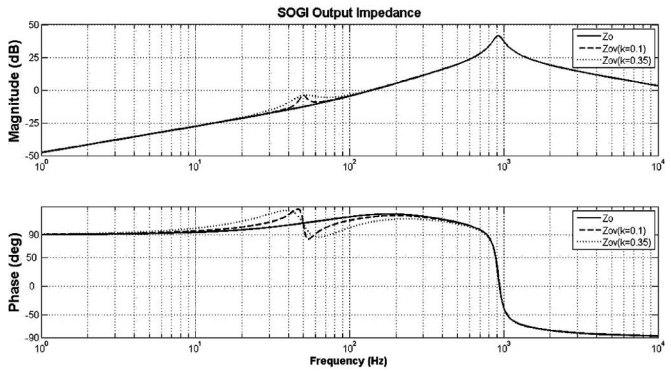


Fig. 13. Bode plot of the inverter output impedance considering the SOGI virtual-inductor-impedance approach. Z_o is the original inverter's output impedance. $Z_{ov}(k = 0.1)$ and $Z_{ov}(k = 0.35)$ considers the effect of a virtual inductor $L_v = 4\,\mathrm{mH}$ and a SOGI filter with gains $k = 0.1$ and $k = 0.35$, respectively.

where $z_o(s) + g(s)z_v(s) = z_{ov}(s)$ is defined as the inverter total output impedance transfer function.

To see the effect of the virtual impedance in the system, a comparison between the original output impedance $z_o(s)$, and the total output impedance achieved considering the virtual impedance of (12) $z_{ov}(s)$, is shown in the Bode plot of Fig. 12 ($z_o(s)$ is depicted by a solid line and $z_{ov}(s)$ by a dot and dashed lines for different values of ω_C). The expression of $z_{ov}(s)$ considering (12) is shown in (24), at the bottom of the next page. This Bode plot has been obtained for the following parameters: $v_o = 220\,\mathrm{V_{rms}}, L = 1.36\,\mathrm{mH}, L_v = 4\,\mathrm{mH}, r = 0.8\,\Omega, C = 11\,\mu\mathrm{F}, \omega = 2\pi 50\,\mathrm{rad/s}, k_p = 0.15, k_i = 350,$ and $k_c = 3.5$.

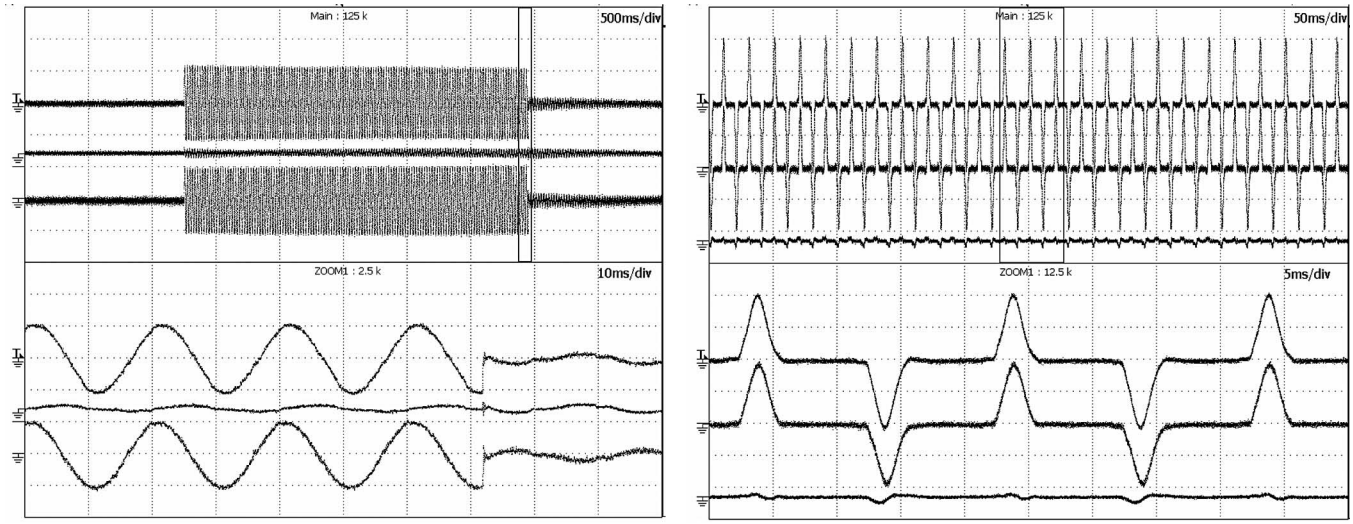
In Fig. 12, it can be seen that the inverter impedance is inductive around the output-voltage frequency (50 Hz), and how the LPF of the virtual impedance modifies the output impedance. In this figure, it can be seen that the value of the virtual inductance, L_v, has a direct effect on the entire Bode gain. Hence, an increase of L_v implies directly an increase on the harmonics gain. As a contrast, in Fig. 13, the frequency effect of a virtual inductor implemented by the SOGI-filter approach of (18) that is constrained only around the fundamental frequency is shown. In Fig. 13, Z_o is the Bode plot of the original inverter output impedance and $Z_{ov}(k = 0.1)$ and $Z_{ov}(k = 0.35)$ are the inverter output impedances considering the SOGI virtual inductor of 4 mH and the SOGI gains $k = 0.1$ and, respectively. The expression of $z_{ov}(s)$, considering (18), is shown in (25), at the bottom of the next page.

TABLE I
INVERTER AND CONTROLLER PARAMETERS OF DROOP METHOD WITH CLASSICAL VIRTUAL IMPEDANCE AND THE SOGI PROPOSED ONE

Symbol	*Parameter*	*Inverter #1*	*Inverter #2*
E^*	*Nominal output voltage*	220Vrms	220Vrms
ω^*	*Nominal frequency*	2π50rad/s	2π50rad/s
m	*Frequency Droop Coefficient*	3×10^{-5}Hz/W	3×10^{-5}Hz/W
n	*Amplitude Droop Coefficient*	8×10^{-5}V/VAr	8×10^{-5}V/VAr
L_v	*Virtual inductor value*	4mH	4mH
ω_c	*Cut-off frequency*	2π300rad/s	2π300rad/s
k	*SOGI gain*	0.35	0.35
V_{DC}	*DC bus voltage*	364 V	368 V
L	*Inductance of output filter*	1.36 mH	1.34 mH
C	*Capacitance of output filter*	11 µF	11 µF
r	*Inductance parasitive resistance*	0.8Ω	0.75 Ω
k_p	*PI proportional gain*	0.15	0.15
k_i	*PI integral gain*	350	350
k_c	*Current loop gain*	3.5	3.5
f_s	*Switching frequency*	25kHz	25kHz

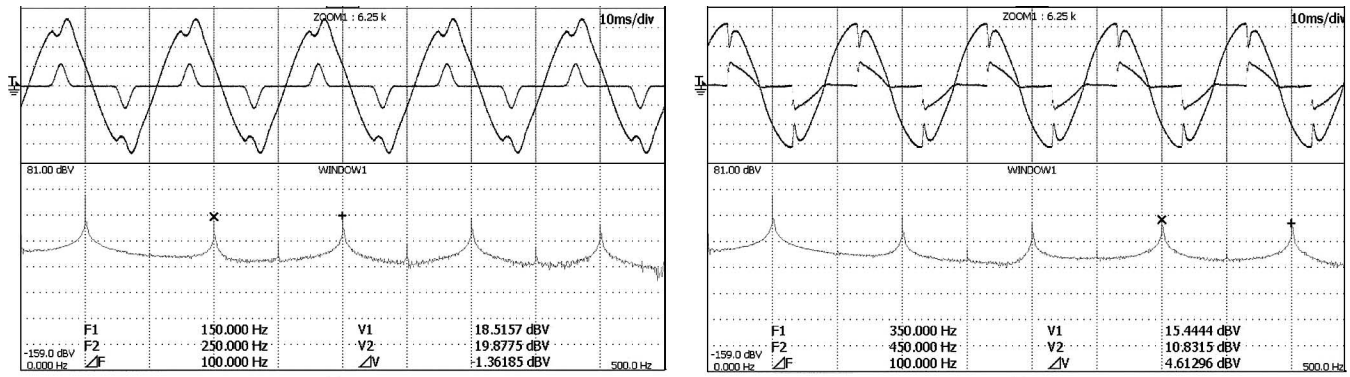
V. EXPERIMENTAL RESULTS

Experimental results were obtained considering the droop method, and both the classical virtual impedance of (12) and the proposed SOGI virtual impedance of (18) for a system formed by two 2-kVA inverters sharing a common load. Each inverted consisted of a single-phase IGBT full bridge with a switching frequency of 25 kHz and an *LC* output filter, using the parameters listed in Table I. The inverter controllers were implemented on a



(a) (b)

Fig. 14. Experimental results of the parallel inverters with the droop method and using a SOGI virtual inductor of 4 mH: (a) A linear load is connected and disconnected. Top and bottom: inverter's current. Middle: circulating current. (*X*-axis: top 500 ms/div, bottom: 10 ms/div; *Y*-axis: 2 A/div). (b) A rectifier-type nonlinear load. Top and middle: inverter's current. Bottom: circulating current. (*X*-axis: top 50 ms/div, bottom: 5 ms/div; *Y*-axis: 2 A/div).



(a) (b)

Fig. 15. Experimental results of two parallel inverters with droop method and using the LPF classical approach with $L_v = 4\,\mathrm{mH}$ and 300 Hz cut-off frequency, and FFT analysis of the output voltage: (a) Output voltage and output current when sharing a rectifier-type nonlinear load ($\mathrm{THD}(v_o) = 9.33\%$). (b) Output voltage and output current when sharing a thyristor-type nonlinear load ($\mathrm{THD}(v_o) = 7.74\%$). (*X*-axis: top 200 ms/div, middle: 10 ms/div, bottom: 50 Hz/div; *Y*-axis: 100 V/div, 5 A/div, bottom: 30 dBV/div).

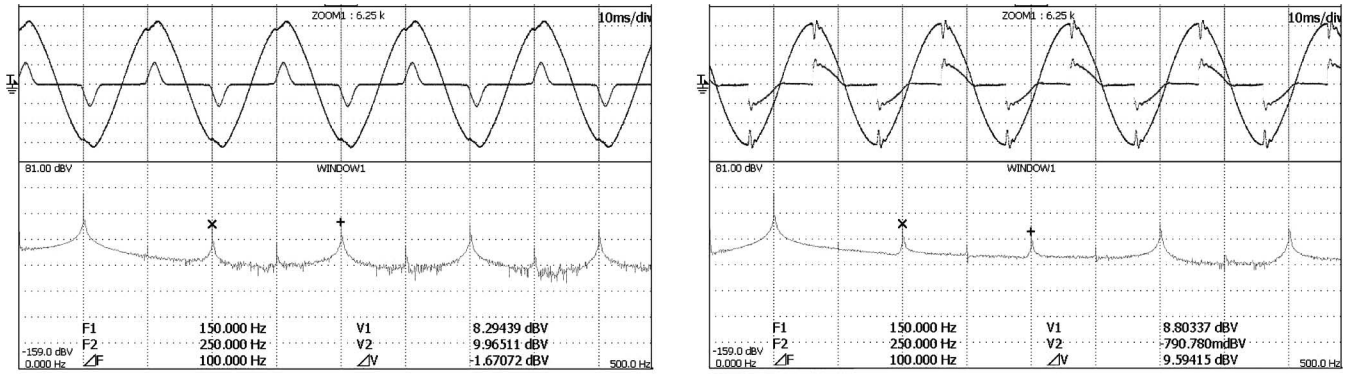
TMS320F2811 DSP, fixed-point digital signal processor (DSP) from Texas Instruments. The gain *k* of the SOGI filter has been chosen to 0.35 has a compromise between the time response and the bandwidth of the filter. Lower values of *k* achieve small improvements on the output voltage THD at expenses of much larger transient responses to step changes in the shared load.

Fig. 14 shows the experimental results of two inverters paralleled with the droop method and using the SOGI virtual inductor proposed in (18). Fig. 14(a) shows the current of each inverter and the circulating current when the system shares a linear load. Fig. 14(b) shows the same kind of results for a shared rectifier-type nonlinear load with a crest factor of 2.6. Note that the linear and the rectifier-type loads are properly shared between two inverters, given that the circulating current is small.

The SOGI virtual impedance approach achieves less distortion on the output voltage than the classical LPF virtual

$$z_{ov}(s) = \frac{Ls^3 + (\omega L + r + \omega L_v k_p k_c)s^2 + (\omega r + \omega L_v k_i k_c)s}{LCs^4 + C(\omega L + r + k_c)s^3 + (k_p k_c + \omega C(r + k_c))s^2 + k_c(k_i + \omega k_p)s + \omega k_i k_c} \tag{24}$$

$$z_{vo}(s) = \frac{Ls^4 + (r + \omega k(L + L_v k_c k_p))s^3 + (k\omega r + \omega^2 L + L_v k \omega k_i)s^2 + \omega^2 rs}{LCs^5 + C(k\omega L + r + k_c)s^4 + (k_p k_c + \omega C(\omega L + k(r + k_c)))s^3 + (k_c(k\omega k_p + k_i) + \omega^2 C(r + k_c))s^2 + k_c\omega(kk_i + \omega k_p)s + \omega^2 k_i k_c} \tag{25}$$



(a) (b)

Fig. 16. Experimental results of two parallel inverters with droop method and using the SOGI proposed approach with $L_v = 4\,\mathrm{mH}$, and FFT analysis of the output voltage: (a) Output voltage and output current when sharing a rectifier-type nonlinear load ($\mathrm{THD}(v_o) = 3.1\%$). (b) Output voltage and output current when sharing a thyristor-type nonlinear load (THD(v_o) = 2.54%). (*X*-axis: top 200 ms/div, middle: 10 ms/div, bottom: 50 Hz/div; *Y*-axis: 100 V/div, 5 A/div, bottom: 30 dBV/div).

TABLE II
OUTPUT-VOLTAGE HARMONICS AND THD(v_o).

Virtual impedance approach	Nonlinear load type	3rddB	5thdB	7thdB	9thdB	THD(v_o)
L_v=4mH with LPF	rectifier-type	-25.43	-24.02	-27.55	-35.35	9.33%
L_v=4mH with SOGI	rectifier-type	-35,49	-33.82	-36.68	-42.59	3.1%
L_v=4mH with LPF	thiristor-type	-24.31	-31.87	-28.28	-32.89	7.74%
L_v=4mH with SOGI	thiristor-type	-34.99	-44.57	-36.34	-40.78	2.24%

impedance approach. Experimental results have been obtained to corroborate this statement. Fig. 15(a) and (b) shows the experimental results for the parallel system sharing rectifier-type and thyristor-type nonlinear loads, both obtained with the classical virtual-inductor approach, respectively. In these figures, a fast Fourier transform (FFT) is illustrated to see the output-voltage harmonic content achieved in each case. The experimental results shown in Fig. 16 were obtained for the SOGI virtual-inductor approach with the same nonlinear loads. From Figs. 15 and 16, it can be clearly seen that the SOGI virtual-inductor approach achieves less distortion, so better THD, on the system output voltage. The THD of Fig. 15(a) and (b) are 9.33% and 7.44%, respectively, while of Fig. 16(a) and (b) is reduced to 3.1% and 2.54%, respectively. This proves that the proposed SOGI virtual impedance approach achieves better THD, distorting less the output voltage of the paralleled system when sharing nonlinear loads, because it operates mainly with the fundamental components of the inverter output currents. Table II shows the harmonic content of the output voltage till the ninth harmonic and the total achieved THD. These values are given in decibels and referred to the first harmonic value.

The SOGI-filter approach adopted in this paper attenuates the distortion that certain types of nonlinear loads produce in the system due to the time derivative action usually used to perform a virtual inductance. This work, however, can be improved by adding a series of SOGI filters in the higher harmonics component of the output current that would help to distribute the load distortion properly among inverters. The effect and improvements of this series of SOGI filters on the system is going to be explored by Authors in the future. The proper current distribution between several inverters inside a microgrid and the sharing of harmonics produced by nonlinear loads should also be investigated to ensure the stability of the whole system.

VI. CONCLUSION

This paper presented a novel virtual impedance implementation with a SOGI algorithm to be used in a parallel inverter system with no intercommunication signals. The proposed SOGI virtual impedance approach has been applied and validated in a parallel system formed by two UPS inverters of 2 kVA. The virtual impedance impact in the system performance has been analyzed. The obtained experimental results show how this approach achieves less output-voltage distortion than the conventional virtual impedance approach when operating with nonlinear loads, since the SOGI approach operates mainly with the fundamental component of the inverter output current. With this controller, the parallel inverters are capable to deliver high-quality power even in presence of nonlinear loads with high slew rates like a rectifier-type and thyristor-type loads. The presented controller provides good steady-state performance and fast transient response when sharing common loads. The paper, finally, proposes future lines of research to improve the results and the system stability.

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