Parallel Control Strategy of Single-Phase Inverter Based on Virtual Impedance

Shungang Xu[1 2], Jianping Xu[2]
[1] College of Physics and Electronic Engineering, Chongqing Normal University, Chongqing, China
[2] School of Electrical Engineering, Southwest Jiaotong University, Chengdu, Sichuan, China
Shungang_xu@163.com, jpxu-swjtu@163.com

Abstract — **In the conventional single-phase inverter parallel system, because of the inconsistent line impedance and frequency characteristic of the inverter output equivalent impedance, the load harmonic power can not be well-distributed by the inverters in the system. By analyzing the equivalent impedance of the single-phase inverter, this paper proposed a virtual impedance design method in the dual close loop feedback control inverter. This method can improve the frequency response performance of the inverter impedance and the equivalent output impedance appears as pure resistance on a large scale. Therefore, the inverter parallel system adopted this control method can share the harmonic power symmetrically, and lead to better load-sharing performance. The parallel system model based on the control method is built, and the experiment platform is constructed. Finally, experimental results show the effectiveness and the engineering practicability of the method.**

I. INTRODUCTION

INVERTER parallel operation is an efficient way to expand the capacity and to enhance the reliability of inverter system. *N+X* parallel inverter structure features with redundancy, expansibility and reliability.[1,2]

Nowadays, for parallel connect inverter, droop control is widely used[3-5]. Droop control need no interconnection and droop the voltage and phase of the inverter output. Thus the parallel system is of high reliability and of easy installation [10-14]. But the conventional droop-control strategy assumes that the output impedance of inverter is purely inductive by neglecting the influence of its resistance. However, as the output impedance is not purely inductive and power sharing is influenced by the output impedance of the inverter, this inverter parallel technique can not share current well under nonlinear load condition [13, 14]. In [15], a new droop-control scheme is presented, in which all inverters share the same synchronous signal. This method can improve phase synchronization precision, but the problem caused by output impedance still exists. Furthermore, the reliability of the parallel inverter system is affected as all inverters use the same synchronous signal.

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In this paper, a virtual impedance design method is proposed. The method can improve the frequency response performance of the inverter impedance and the equivalent output impedance appears as pure resistance on a large scale. Therefore, the inverter parallel system adopted this control method can share the harmonic power symmetrically, and lead to better load-sharing performance.

II. ANALYSIS OF SINGLE PHASE INVERTER

For the control of the single phase inverter, two-loop feedback control scheme is usually adopted. Fig.1 shows a two-loop feedback control scheme with inductor current inner loop and capacitor voltage outer loop. The capacitor voltage outer loop adopts proportion-integral control to stabilize the output voltage, and the inductor current inner loop uses proportion control to enhance the performance of the transient response of the inverter.

In Fig.1, r_L comprises the ESR of the inductor, the on-resistance of the switch and the resistance of the connection line. According to nonlinear control and feedback linearization theory, the open-loop averaged output voltage can be characterized by

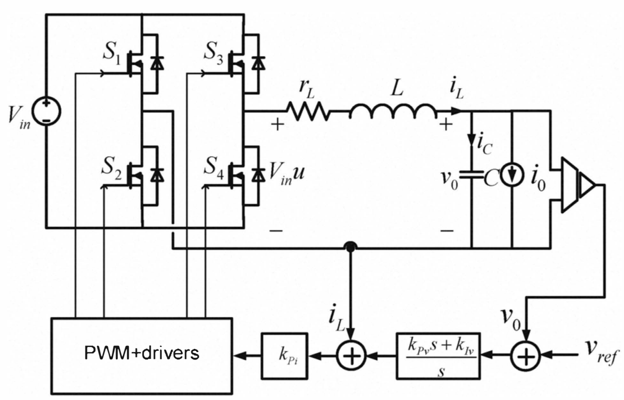


Fig.1 Single phase inverter with two-loop feedback control.

$$LC\frac{d^2\langle v_0\rangle}{dt^2}+r_L C\frac{d\langle v_0\rangle}{dt}+\langle v_0\rangle+L\frac{d\langle i_0\rangle}{dt}+r_L\langle i_0\rangle=\langle V_{in}u\rangle \quad (1)$$

where $\langle\ \rangle$ means the average value over one switching cycle and u is the control variable, which can take the values 1, 0, or -1, depending on the state of switches S_1, S_2, S_3 and S_4.

For the two-loop feedback control inverter shown in Fig.1, the controller can be characterized by

$$\langle V_{in}u\rangle = \left(\frac{k_{Pv}s+k_{Iv}}{s}\left(v_{ref}-\langle v_0\rangle\right)-\left(\langle i_0\rangle - Cs\langle v_0\rangle\right)\right)k_{Pi} \quad (2)$$

From (1) and (2), we can get the dynamic characteristics of closed-loop output voltage as

$$\begin{aligned} v_0 = & \frac{k_{Pv}k_{Pi}s+k_{Pi}k_{Iv}}{LCs^3+\left(r_LC+k_{Pi}C\right)s^2+\left(1+k_{Pv}k_{Pi}\right)s+k_{Pi}k_{Iv}}v_{ref} \\ & -\frac{Ls^2+\left(r_L+k_{Pi}\right)s}{LCs^3+\left(r_LC+k_{Pi}C\right)s^2+\left(1+k_{Pv}k_{Pi}\right)s+k_{Pi}k_{Iv}}i_0 \end{aligned} \quad (3)$$

where s is Laplace operator.

From (3) we can know that the inverter can be modeled by two terminal equivalent circuits as shown in Fig.2, with

$$v_0 = G(s)\times v_{ref} - Z(s)\times i_0 \quad (4)$$

$$G(s) = \frac{k_{Pv}k_{Pi}s+k_{Pi}k_{Iv}}{LCs^3+\left(r_LC+k_{Pi}C\right)s^2+\left(1+k_{Pv}k_{Pi}\right)s+k_{Pi}k_{Iv}} \quad (5)$$

$$Z(s) = \frac{Ls^2+\left(r_L+k_{Pi}\right)s}{LCs^3+\left(r_LC+k_{Pi}C\right)s^2+\left(1+k_{Pv}k_{Pi}\right)s+k_{Pi}k_{Iv}} \quad (6)$$

where $G(s)$ is the voltage gain and $Z(s)$ is the output impedance of inverter.

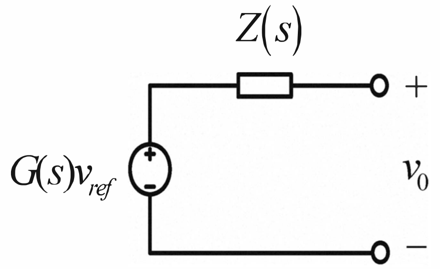


Fig.2 Equivalent circuit of the two-loop feedback control single phase inverter.

From (6) we can know that the output impedance of the inverter relies heavily on the parameters of the output filter and the control parameters of the feedback loop, and the output impedance is usually a complex value. When $L=500uH$, $C=10uF$, $k_{Pv}=5$, $k_{Iv}=100$, $k_{Pi}=1$, and $r_L=0.1\Omega, 0.2\Omega, 0.3\Omega$ respectively, the bode diagram of the output impedance of the inverter can be get as Fig. 3.

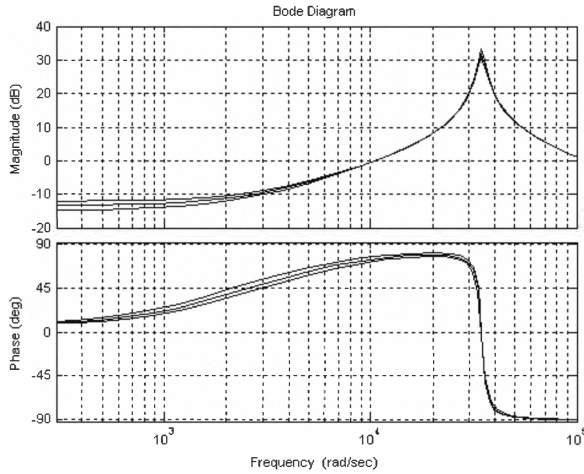


Fig.3 Bode diagram of the output impedance.

From Fig.3, the output impedance appears as resistance at 50Hz, but the inductive component rapidly increases with the frequency. At the same time, the r_L is smaller, the increasing of the inductive component is more quickly. In the conventional droop control strategy, the output impedance is looked as constant and the current-sharing is aimed at the fundamental component of the output current. But under the nonlinear load condition, the current-sharing effect of inverter parallel system is poor.[10]

III. Virtual Impedance Design of Single Phase Inverter

In a inverter parallel system, the output impedance characteristic of close-loop control inverter is close related to the current-sharing precision, and decides the droop control strategy of the parallel system. The right design of the output impedance can also decrease the asymmetrical current caused by the difference line impedance.[11]

So, the virtual impedance is design as shown in Fig.4, and the expression is

$$v_{ref} = v_{ref}^* + R_D(s)i_0 \quad (7)$$

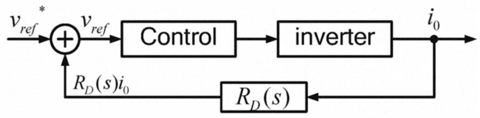


Fig.4 The virtual impedance control loop design.

The virtual impedance design is $R_D(s)=\frac{Ls}{K_{Pv}K_{Pi}}$, and v^*_{ref} is the reference signal. From the expression (3) and (7), the output voltage of inverter including the virtual impedance can be expressed as

$$v_0 = G(s)\times v_{ref}^* - Z_0(s)\times i_0 \quad (8)$$

In the expression, $Z_0(s)$ is the inverter equivalent output impedance including the virtual impedance.

$$Z_0(s)=\frac{\left(r_L+k_{Pi}-\dfrac{k_{Iv}}{k_{Pv}}L\right)s}{LCs^3+\left(r_LC+k_{Pi}C\right)s^2+\left(1+k_{Pv}k_{Pi}\right)s+k_{Pi}k_{Iv}} \tag{9}$$

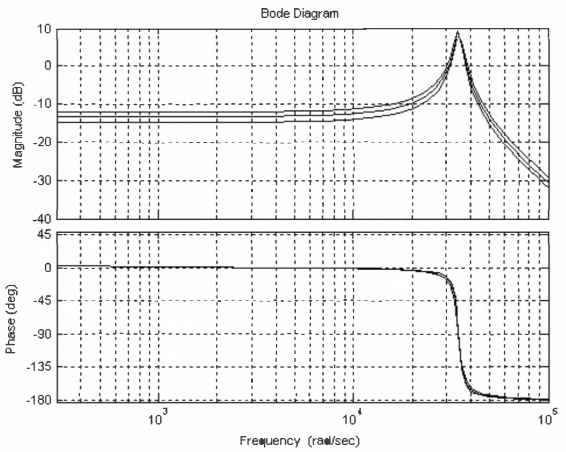


Fig.5 Bode diagram of output equivalent impedance after introduced virtual impedance control loop. ($r_L = 0.1\Omega$, 0.2Ω , 0.3Ω)

Bode diagram of output equivalent impedance after introduced the virtual impedance control loop is shown as Fig.5. The impedance appears as pure resistance at fundamental component and harmonics components of the output frequency. The resistance increases with r_L of the inverter output filter. Therefore, the equivalent output impedance of the inverter after introduced virtual impedance control loop can be regard as resistor with fixed resistance.

IV. Analysis of Double Loop Control Inverter Parallel Operation

Based on the above analysis, the equivalent circuit with two dual close-loop feedback control single-phase inverter after introduced virtual impedance can be shown as Fig.6.

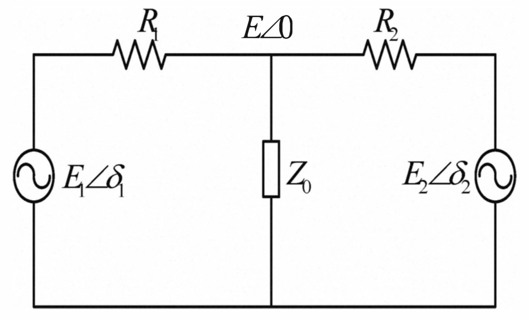


Fig.6 Equivalent circuit of inverter parallel operation.

In the Fig.6, $E_1\angle\delta_1 = G_1(s)v_{ref1}^*$, and $E_2\angle\delta_2 = G_2(s)v_{ref2}^*$. And $G_1(s)$, R_1 , v_{ref1}^* are the voltage gain, output impedance and reference signal of the inverter1, respectively, and $G_2(s)$, R_2 , v_{ref2}^* are the voltage gain, output impedance and reference signal of the inverter1, respectively.

The output active power and reactive power of the inverter i in the parallel system can be expressed as

$$\begin{cases} P_i = \dfrac{EE_i}{R_i}\cos\delta_i - \dfrac{E^2}{R_i} \\ Q_i = -\dfrac{EE_i}{R_i}\sin\delta_i \end{cases} \tag{10}$$

The output apparent power ($S = P + jQ$) of the inverter i in the parallel system in polar coordinate system can be expressed as

$$S_i = -\frac{E^2}{R_i} + \frac{EE_i}{R_i}e^{-j\delta_i} \tag{11}$$

From the polar coordinate diagram shown as Fig.7, the apparent power S_i is related not only to output voltage amplitude E_i but also to output voltage phase δ_i . δ_i is positive when the load is inductive and δ_i is negative when the load is capacitive. In the first and fourth quadrant, the inverter can work normally, so, $E_i > E$.

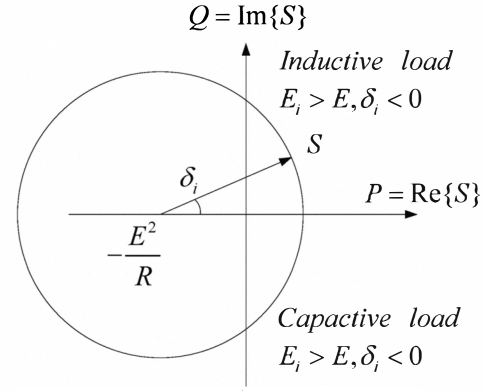


Fig.7 The apparent power polar coordinate diagram of inverter.

V. Control Circuit Design

Due to small difference of output phase voltage between individual inverter, we can assume that $\sin\delta_i \approx \delta_i$ and $\cos\delta_i \approx 1$ .Therefore, the output active power and output reactive power of the inverter i in the parallel system can be simplified as

$$\begin{cases} P_i = \dfrac{EE_i}{R_i} - \dfrac{E^2}{R_i} \\ Q_i = -\dfrac{EE_i}{R_i}\delta_i \end{cases} \tag{12}$$

So, increasing amplitude of output voltage can increase output active power of the inverter in the parallel system. By the same reason, increasing phase of output voltage can decrease output reactive power. Therefore, the following control strategy can be introduced to control the amplitude and phase droop of the inverter.

$$\begin{cases} E = E^* - nP - n_d\dfrac{dP}{dt} \\ \omega = \omega^* + mQ + m_d\dfrac{dQ}{dt} \end{cases} \tag{13}$$

where m, m_d are the proportion coefficient and integral coefficient of reactive power droop control, n, n_d are the proportion coefficient and integral coefficient of active power droop control, respectively. The reference signal of a inverter generation diagram is shown as Fig.8.

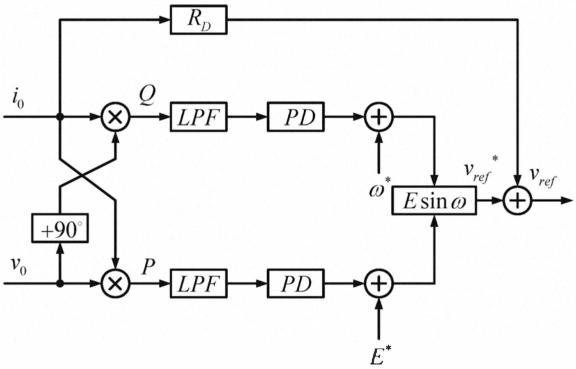
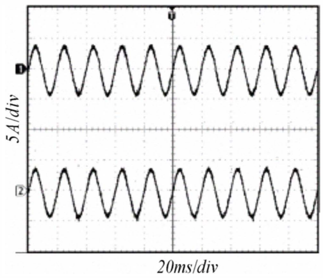


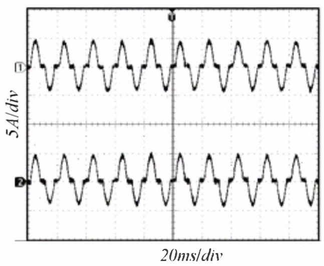
Fig.8 The reference signal of inverter generation diagram.

VI. EXPERIMENT RESULTS

Based on the above analysis and design, a parallel inverter system with two 2KVA inverters is designed, with 500uH output filter inductance and 10uF output filter capacitance for the individual inverter. The input DC voltage is 200V and the output AC voltage is 110V with 50Hz. The closed-loop control, droop arithmetic, power computation and the SPWM control signal are processed by TMS320F2812 digital signal processor.



(a) Current wave under linear load.



(b)Current wave under nonlinear load.

Fig.9 Experiment wave of parallel inverter.

Experiment results for the parallel inverter are shown in Fig. 9. Two inverters can share the load current very well under linear load condition, and excellent load sharing is achieved between two inverters under nonlinear load condition.

VII. CONCLUSION

In this paper, a virtual impedance design method is proposed. The method can improve the frequency response performance of the inverter impedance and the equivalent output impedance appears as pure resistance on a large scale. Therefore, the inverter parallel system adopted this control method can share the harmonic power symmetrically, and lead to better load-sharing performance. Experimental results show the effectiveness and the engineering practicability of the method.

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