Design and Analysis of the Droop Control Method for Parallel Inverters Considering the Impact of the Complex Impedance on the Power Sharing

Wei Yao, Min Chen, José Matas, Josep M. Guerrero, *Senior Member, IEEE*, and Zhao-Ming Qian, *Senior Member, IEEE*

***Abstract*—This paper investigates the characteristics of the active and reactive power sharing in a parallel inverters system under different system impedance conditions. The analyses conclude that the conventional droop method cannot achieve efficient power sharing for the case of a system with complex impedance condition. To achieve the proper power balance and minimize the circulating current in the different impedance situations, a novel droop controller that considers the impact of complex impedance is proposed in this paper. This controller can simplify the coupled active and reactive power relationships, which are caused by the complex impedance in the parallel system. In addition, a virtual complex impedance loop is included in the proposed controller to minimize the fundamental and harmonic circulating current that flows in the parallel system. Compared to the other methods, the proposed controller can achieve accurate power sharing, offers efficient dynamic performance, and is more adaptive to different line impedance situations. Simulation and experimental results are presented to prove the validity and the improvements achieved by the proposed controller.**

***Index Terms*—Circulating current, droop method, impedance, parallel inverters.**

I. Introduction

POWER ENERGY distribution in a system that is formed by several uninterruptible power supplies (UPS) that operate in parallel can now be performed with different methods, either with or without communication between the power elements. In such systems, it is very important to minimize the circulating current that can flow among the power units to have equal load sharing and deliver high-quality power. Several control strategies have been adopted to achieve this goal, such as the concentrated control technique [1], the master–slave control method [2]–[4], the power deviation control method [5], [6], and the frequency and voltage droop method [7]–[10]. In those parallel systems, the droop control method is very interesting, because it is only based on inverter locally measured information, does not rely on intercommunication signals between the inverters, and constitutes a truly distributed and redundant system.

To achieve efficient power sharing, the droop method makes tight adjustments over the output voltage frequency and amplitude of the inverter, as a power-dependent function, to compensate for the active and reactive power unbalances [11], [12]. However, the transient and steady-state behaviors of the droop method highly depend on the system mismatches that can affect the inverter output impedance accuracy and the line impedance of the wires for UPS connection [13], [14].

Usually, the line impedance and the output impedance of the inverters are considered to be mainly inductive due to the large output-inductor value or by the long distances between the units. However, this case is not always true, because the inverter output impedance also depends on the adopted inverter control strategy and on the system parameters [15]–[17]. Improved droop methods have been proposed and successfully applied to the case of pure inductive [18] and pure resistive impedances [19], but few papers study such a case where the system impedance is complex. In fact, in many practical applications, different UPS units are located a little far from each other and are paralleled through different wires, which present nonnegligible inductive and resistive line impedance [20]. Furthermore, it is normal to find that the inverter output impedance is, in fact, complex due to the multiple feedback design possibilities [21]. For these systems, the performance of the conventional droop method is very poor, and it cannot achieve efficient power sharing due to the coupled active and reactive power characteristic of the system [22]–[24].

In this paper, the characteristics of the active and reactive power sharing for the parallel inverters under the situations of pure inductive, pure resistive, and complex impedances are thoroughly analyzed. This paper shows that the conventional droop method cannot achieve efficient power sharing in the case of complex system impedance. To overcome this obstacle and minimize the circulating current under all situations, a novel droop controller that considers the impact of complex impedance is proposed in this paper. This controller simplifies the coupled active and reactive power relationships under the

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W. Yao, M. Chen, and Z.-M. Qian are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: yw@zju.edu.cn; calim@zju.edu.cn; qian@zju.edu.cn).

J. Matas is with the Department of Electronic Engineering, Technical University of Catalonia, Barcelona 08800, Spain (e-mail: matas@eel.upc.edu).

J. M. Guerrero is with the Department of Automatic Control Systems and Computer Engineering, Technical University of Catalonia, Barcelona 08036, Spain (e-mail: josep.m.guerrero@upc.edu).

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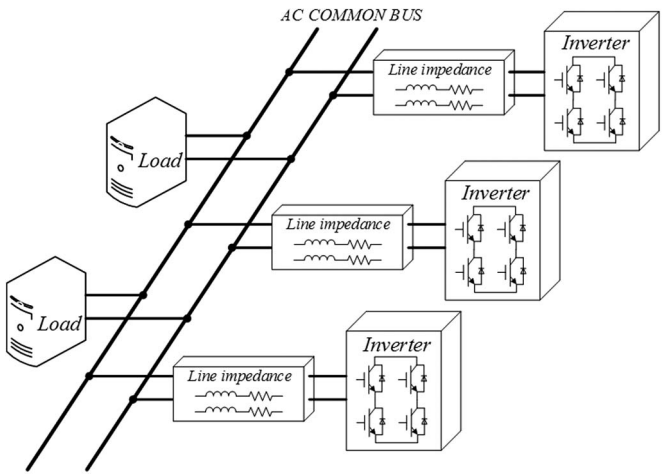


Fig. 1. Power supply system with the parallel inverters.

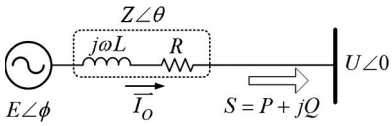


Fig. 2. Equivalent circuit of a parallel inverter.

complex impedance condition. In addition, an instantaneous virtual complex impedance loop is introduced to ensure efficient steady-state and transient performances when sharing the loads. It is also shown that the proposed control method can allow efficient power sharing with low sensitivity to unbalances in the line impedance, including inductive, resistive, or complex situations. Finally, the performance of the proposed control strategy and its experimental evaluation with two single-phase parallel inverters are discussed and reported in this paper.

II. Theoretical Analysis of Power Sharing

Fig. 1 depicts a power supply system with several single-phase UPS connected in parallel and with load sharing through an ac common bus. Fig. 2 depicts the equivalent circuit of one single-phase inverter derived from Thévenin's theorem [18]. In this figure, $E\angle\phi$ is the inverter open-circuit voltage, $\overline{I_O}$ is the inverter output current, $U\angle 0^\circ$ is the common ac bus voltage, $R + j\omega L$ is the impedance of the inverter system, which includes the output impedance and the line impedance, and Z and θ are its magnitude and phase values, respectively.

According to the equivalent circuit of a parallel inverter in Fig. 2, the output current expression can be derived as

$$\overline{I_O} = \frac{E\angle\phi - U\angle 0}{Z\angle\theta} = \frac{E}{Z}\angle(\phi-\theta) - \frac{U}{Z}\angle(-\theta) \quad \overline{Z} = R + jX. \tag{1}$$

In addition, the apparent power injected by an inverter to the ac common bus is

$$S = \overline{U} \cdot \overline{I_O}^{\,*} = P + jQ \tag{2}$$

TABLE I
Active and Reactive Power of Parallel Inverters With Different System Impedances

System Impedance	Pure Inductive $\theta = 90^\circ$, $\overline{Z} = jX$	Pure Resistive $\theta = 0^\circ$, $\overline{Z} = R$	Complex Impedance θ, $\overline{Z} = R + jX$
Active Power	$P \cong \frac{UE\phi}{Z}$	$P \cong \frac{U(E-U)}{Z}$	$P \cong \frac{U}{Z}[(E-U)\cos\theta + E\phi\sin\theta]$
Reactive Power	$Q \cong \frac{U(E-U)}{Z}$	$Q \cong \frac{-UE\phi}{Z}$	$Q \cong \frac{U}{Z}[(E-U)\sin\theta - E\phi\cos\theta]$

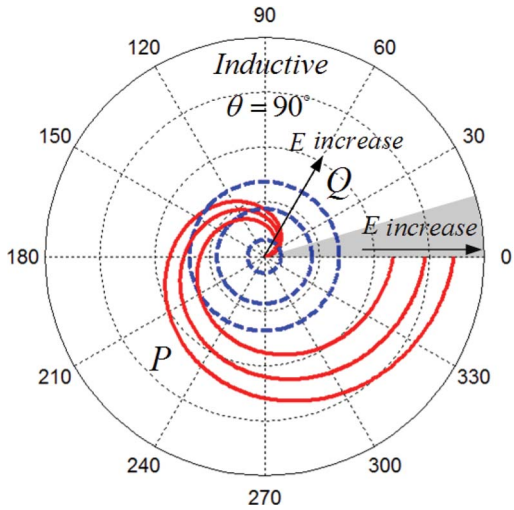


Fig. 3. Polar plot of the P/Q behaviors of parallel inverter with pure inductive impedance. Solid line: P. Dashed line: Q.

where $\overline{I_O}^{\,*}$ is the conjugate of $\overline{I_O}$. Using (1) and (2), the active and reactive powers are

$$P = \frac{U}{Z}\left[(E\cos\phi - U)\cos\theta + E\sin\theta\sin\phi\right] \tag{3}$$

$$Q = \frac{U}{Z}\left[(E\cos\phi - U)\sin\theta - E\cos\theta\sin\phi\right]. \tag{4}$$

Assuming that the phase differences ϕ between the inverter output voltage and the common bus voltage is very small, because the inverters are first synchronized by using the phase-locked loop (PLL) module, then (3) and (4) can be simplified to

$$P \cong \frac{U}{Z}\left[(E-U)\cos\theta + E\phi\sin\theta\right] \tag{5}$$

$$Q \cong \frac{U}{Z}\left[(E-U)\sin\theta - E\phi\cos\theta\right]. \tag{6}$$

Now, by using (5) and (6), it is shown that the relationships between the output voltage and the delivered power are determined by the system impedance angle θ [25]. Table I shows the active and reactive power expressions according to the value of θ.

To clarify the relationship between the system impedance and the power sharing, the output active and reactive power behaviors with different impedances are illustrated by polar coordinates, as shown in Figs. 3–5. The polar radii here denote the values of the active power and the reactive power, whereas

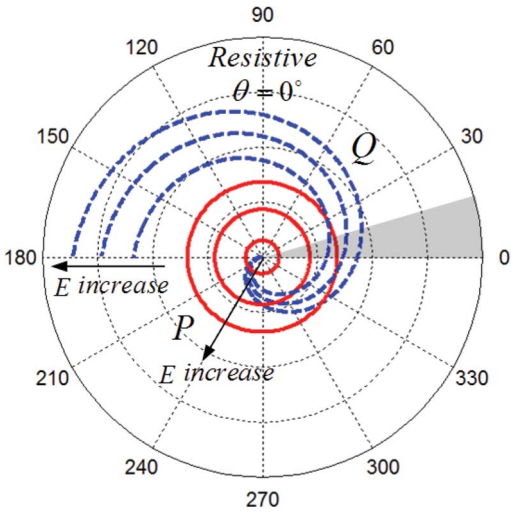


Fig. 4. Polar plot of the P/Q behaviors of parallel inverter with pure resistive impedance Solid line: P. Dashed line: Q.

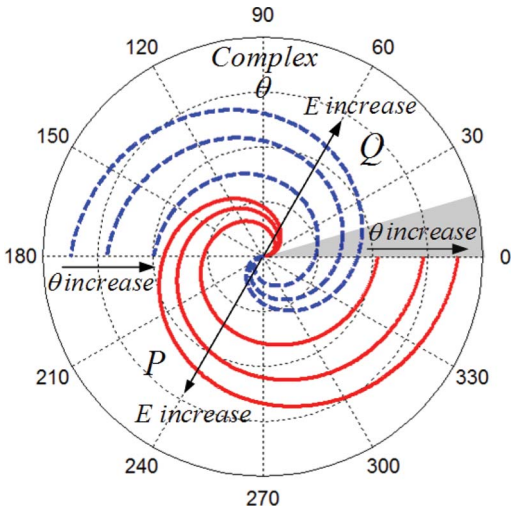


Fig. 5. Polar plot of the P/Q behaviors of parallel inverter with complex impedance Solid line: P. Dashed line: Q.

the polar angles denote the power angle ϕ between the inverter output voltage and the ac common bus voltage. Note that only the shaded parts are valid in a real system, because the power angle ϕ of each inverter is always very small.

A. Pure Inductive Impedance

Fig. 3 illustrates the behaviors of the active and reactive powers when using inductive output impedance. In this figure, it is shown that the active and reactive powers that an inverter delivered increase as the amplitude of the output voltage E increases. Notice that the polar radius of the reactive power here is constant with any variation of the power angle ϕ; however the polar radius of the active power increases when the power angle ϕ increases.

B. Pure Resistive Impedance

For the case of pure resistive impedance, the active and reactive powers behaviors are inverse to the previous one shown

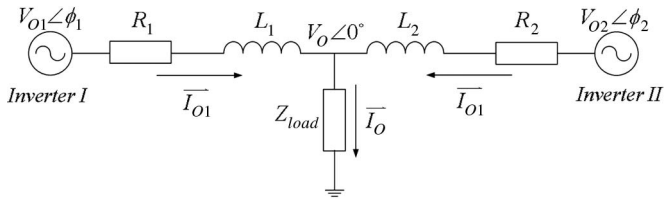


Fig. 6. Equivalent circuit of two inverters connected in parallel.

for inductive impedances (see Fig. 4). Note that the delivered active and reactive powers of the inverter still increase with the increase of E, but here, the polar radius of the reactive power increases with the power angle ϕ, whereas the polar radius of the active power remains constant with ϕ variations.

C. Complex Impedance

Usually, impedance analyses are made under a pure inductive assumption, and few papers such as [25] deal with pure resistive output impedance. However, these assumptions are not applicable in the case where the inverter output impedance depends on the adopted control strategy and on the power stage parameters, which are responsible for presenting complex impedance at the fundamental frequency. Meanwhile, in several practical applications, the line impedance is also complex.

For this case, according to Fig. 5, both the active and the reactive powers increase their polar radius when the power angle ϕ increases. The active power increases in a counterclockwise direction when ϕ varies, whereas the reactive power increases in a counterclockwise direction. The more inductive behavior of the complex impedance is emphasized to increase the amount of active power but decrease the reactive power. In contrast, the more resistive behavior of the complex impedance is emphasized to increase the amount of reactive power but decrease the active power. In view of this case, it can be concluded that the output power behavior of parallel inverters system with complex impedance is completely different from the other two conventional situations. The ubiquities of the complex impedance in practical parallel inverters system significantly change the active and the reactive power sharing behaviors, and this issue has not been properly treated in the conventional techniques.

III. Circulating Current Characteristic Analysis

A circulating current between two inverters exists due to the small differences between the inverter output voltages, which is mainly a consequence of parameter mismatch. For this reason, the circulating current can be very large. It may result in overcurrent damage to the inverter and can further undermine the parallel operations. Fig. 6 depicts a classical setup of two single-phase inverters that are connected in parallel with a load. In this figure, $\overline{V_{O1}}$ and $\overline{V_{O2}}$ are the open-circuit voltages of the inverters, $\overline{V_O}$ is the load voltage, and $R_i + j\omega L_i$ $(i = 1, 2)$ are the equivalent system impedances, i.e., the line impedance and the output impedance of the inverter. ϕ_i and θ_i $(i = 1, 2)$ are the voltage angle and the system impedance angle, respectively. $\overline{I_{Oi}}$ $(i = 1, 2)$ are the output currents of both inverters, and $\overline{I_O}$ is the load current. Fig. 7 depicts a vector diagram

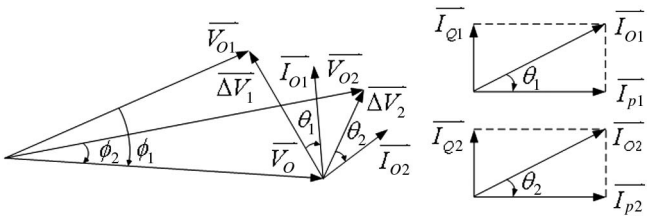


Fig. 7. Vector diagram of equivalent circuit.

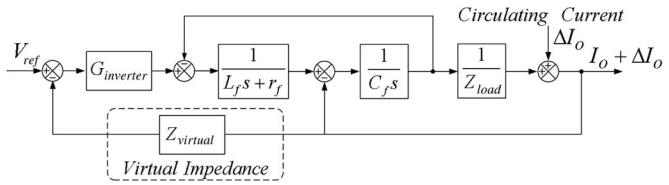


Fig. 8. Block diagram of an inverter with the circulating current.

that illustrates the circulating current behavior between the paralleled inverters. In this figure, $\overline{I_{Pi}}$ and $\overline{I_{Qi}}$ $(i = 1, 2)$ are the active current and the reactive current components, respectively, of the output current for each inverter.

In these figures, the active and the reactive parts of the circulating current are determined by the angle of the system impedance θ_i $(i = 1, 2)$. The expressions of the active and reactive circulating currents in a parallel system can be derived as

$$\begin{aligned}\overline{\Delta I_P} &= \frac{\overline{I_{P1}} - \overline{I_{P2}}}{2} \\ &= \frac{1}{2}\left[\frac{V_{O1}R_1\cos\phi_1 + V_{O1}\omega L_1\sin\phi_1 - V_O R_1}{R_1^2 + (\omega L_1)^2}\right. \\ &\qquad \left. - \frac{V_{O2}R_2\cos\phi_2 + V_{O2}\omega L_2\sin\phi_2 - V_O R_2}{R_2^2 + (\omega L_2)^2}\right]\end{aligned} \tag{7}$$

$$\begin{aligned}\overline{\Delta I_Q} &= \frac{\overline{I_{Q1}} - \overline{I_{Q2}}}{2} \\ &= \frac{1}{2}\left[\frac{V_{O1}R_1\sin\phi_1 - V_{O1}\omega L_1\cos\phi_1 + V_O\omega L_1}{R_1^2 + (\omega L_1)^2}\right. \\ &\qquad \left. - \frac{V_{O2}R_2\sin\phi_2 - V_{O2}\omega L_2\cos\phi_2 + V_O\omega L_2}{R_2^2 + (\omega L_2)^2}\right]\end{aligned} \tag{8}$$

where $\overline{\Delta I_P}$ and $\overline{\Delta I_Q}$ are the active current and reactive current components of the circulating current. Note that the power angle ϕ_i $(i = 1, 2)$ is always very small due to the synchronization achieved by the PLL modules $(\sin\phi \approx \phi, \cos\phi \approx 1)$. Assuming that there are no phase errors $(\phi_i \approx 0)$ and the impedance are almost the same $(R_1 \approx R_2, L_1 \approx L_2)$, (7) and (8) can be simplified to

$$\overline{\Delta I_P} \approx \frac{1}{2}\frac{R_i(V_{O1} - V_{O2})}{R_i^2 + (\omega L_i)^2} \tag{9}$$

$$\overline{\Delta I_Q} \approx \frac{1}{2}\frac{\omega L_i(V_{O2} - V_{O1})}{R_i^2 + (\omega L_i)^2}. \tag{10}$$

Based on these expressions, it is shown that, when the phases are the same, both the active and reactive circulating currents do not only depend on the output voltage difference of the inverter. The active circulating current also depends on the resistance of the system impedance, whereas the reactive circulating current also depends on the inductance of the system impedance. Furthermore, the output frequency ω, which is determined by the droop controller, will also affect the circulating current.

A frequency domain analysis of the circulating current in a parallel system is also carried out in this section. Based on the equivalent circuit in Fig. 6, the circulating current is shown as an output disturbance to the inverter controller. Then, Fig. 8 depicts the block diagram of an inverter module considering the circulating current as an external perturbation.

In this figure, L_f and C_f are the inductance and the capacitance of inverter output filter, and r_f is the inductor parasitic resistance. Z_{load} is the sharing load, ΔI_O is the circulating current injected by one inverter, Z_{virtual} is the virtual impedance, and G_{inverter} is the gain of the internal controller.

The virtual impedance is used for modifying the output impedance of the inverter, which can be implemented by a fast control loop. Take into account that a virtual inductor can be implemented by drooping the output voltage reference proportional to the time derivative of the output current and a virtual resistor can be implemented by subtracting the output voltage reference proportional to the output current. Notice that the relationship between the output voltage and the circulation current shows the sensibility of the inverter to the circulating current, as in (11), shown at the bottom of the page.

Usually, the output impedance of the inverter is considered inductive because of the inductor of the filter and the inductor current feedback controller [18], [19]. Consequently, a virtual inductive impedance loop is added in some applications to decrease the circulating current [10], [12], [22]. Fig. 9 shows a Bode plot comparison for the situations that use and do not use a virtual inductor.

The virtual resistive impedance is also adopted in some works, which provides the following advantages: 1) system damping; 2) automatic harmonic current sharing; and 3) active power sharing that is barely affected by phase errors [21], [25]. Fig. 10 shows the comparison between the situations with and without the virtual resistor.

In this paper, a virtual complex impedance method is proposed, which is composed of both the virtual inductor and the

$$\frac{V_O(s)}{\Delta i_O(s)} = \frac{L_f s + Z_{\text{virtual}}G_{\text{inverter}} + r_f}{L_f C_f s^2 + (L/Z_{\text{load}} + r_L C_f)s + (Z_{\text{virtual}}G_{\text{inverter}} + r_f)/Z_{\text{load}} + 1} \tag{11}$$

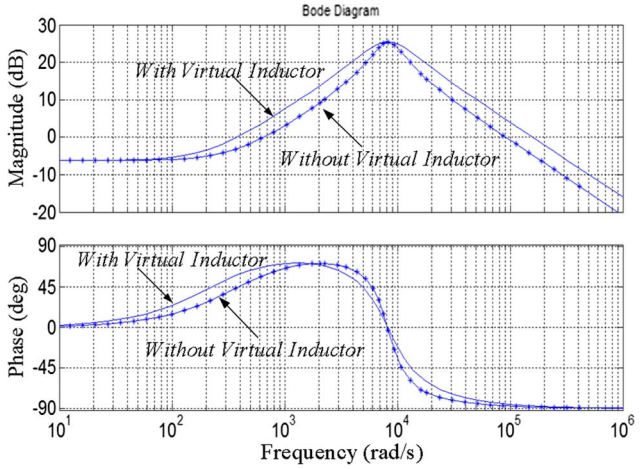


Fig. 9. Bode plot of the sensibility of the inverter to the circulating current with (solid line) and without (dotted line) the virtual inductor.

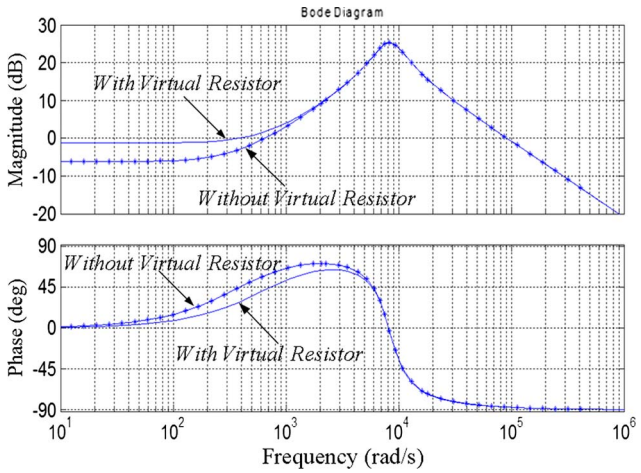


Fig. 10. Bode plot of the sensibility of the inverter to the circulating current with (solid line) and without (dots line) the virtual resistor.

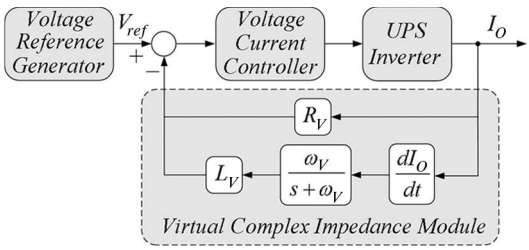


Fig. 11. Block diagram of the proposed virtual complex impedance controller.

virtual resistor and can be expressed as follows:

$$Z_{\text{virtual}} = R_v + \frac{\omega_v}{s+\omega_v} sL_v \tag{12}$$

where a low-pass filter with a cutoff frequency of ω_v is used to avoid high-frequency noise, which is amplified by the time derivative of the output current, R_v is the value of the virtual resistive part, and L_v is the value of the virtual inductive part. Fig. 11 depicts the block diagram of the proposed virtual complex impedance controller. The virtual complex impedance can be implemented by drooping the output voltage related to the output current as shown in Fig. 11.

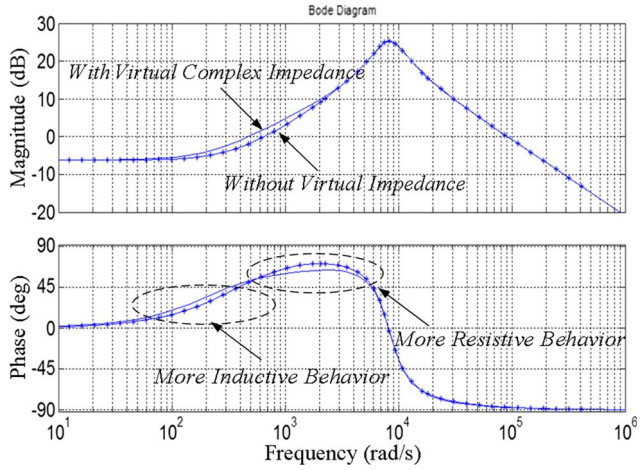


Fig. 12. Bode plot of the sensibility of the inverter to the circulating current with (solid line) and without (dots line) the proposed virtual impedance.

Compared with the conventional virtual inductive and resistive impedance methods, the proposed virtual complex impedance offers the following advantages.

1) It can reduce the circulating current, because the output impedance combines more inductive behavior around the output voltage frequency and more resistive behavior in the case of the high-order harmonic circulating current, as shown in Fig. 12.
2) Its implementation can reduce the drop of the output voltage, which is caused only by virtual resistor impedance.
3) In the range of high frequency, the harmonic circulating current of the loads can automatically be shared by the inverters without any extra control, because the virtual resistive impedance can make the controller more damped.
4) It can also improve the controller to be less sensitive to line impedance unbalance or parameter mismatching, particularly in the case of complex impedance systems.
5) Based on the accurate design for virtual complex impedance, it can be adopted to properly change the impedance angle θ, as described in Section II, decoupling the active and reactive relationship more easily (which will be introduced in the next section).

IV. Design and Implementation of Proposed Droop Controller

In this section, a novel P/Q droop control strategy, which is based on the proper design of the proposed virtual complex impedance, is proposed. The controller can be adaptive to achieve efficient power sharing under the resistive or the inductive line impedances and also for the case of complex line impedance. Furthermore, it minimizes the circulating current and reduces the influence of unbalance in the line impedance, providing proper active and reactive power sharing capability with both steady-state and dynamic response performance.

A. Proposed Controller With Virtual Complex Impedance

The first step in the design is to examine the inherent output impedance of the inverter. Fig. 13 illustrates the feedback

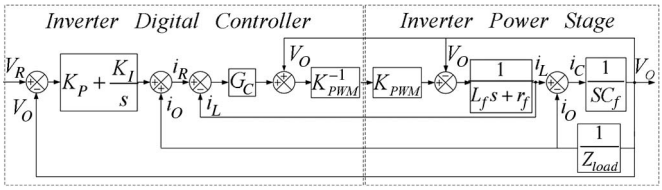


Fig. 13. Block diagram of the multiple-loop controlled inverter.

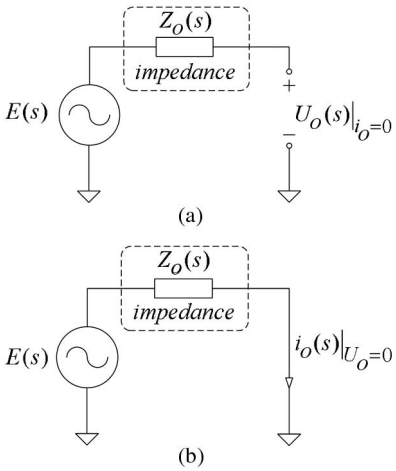


Fig. 14. Thevenin equivalent circuit of the inverter (a) open-circuit voltage and (b) short-circuit current.

controller configuration used in this paper, and this configuration regulates the output voltage of each inverter. The controller includes an output voltage loop and an output current compensation loop, which can ensure the efficient steady-state and dynamic performance.

In Fig. 13, K_P and K_I are, respectively, the proportional and integral coefficients of the proportional–integral (PI) control voltage loop, which have been designed using root locus methods that lead to the following gains: $K_P = 0.5$, $K_I = 350$, G_C is the gain of the current loop with the value of 6.5, and K_{PWM} is the equivalent gain of sinusoidal pulsewidth modulation (SPWM). For the output LC filter stage, an inductor value of $L_f = 1.36$ mH, $r_f = 0.3\ \Omega$, and a capacitor value of $C_f = 11\ \mu$F are used. The output impedance of the inverter is derived from the open-circuit voltage and the short circuit current by using Thévenin's theorem (see Fig. 14), and its expression in the frequency domain is

$$Z_O(s) = \frac{V_O(s)}{i_O(s)} = \frac{L_f s^2 + r_L s}{L_f C_f s^3 + (G_C C_f + r_L C_f)s^2 + K_P G_C s + K_I G_C}. \quad (13)$$

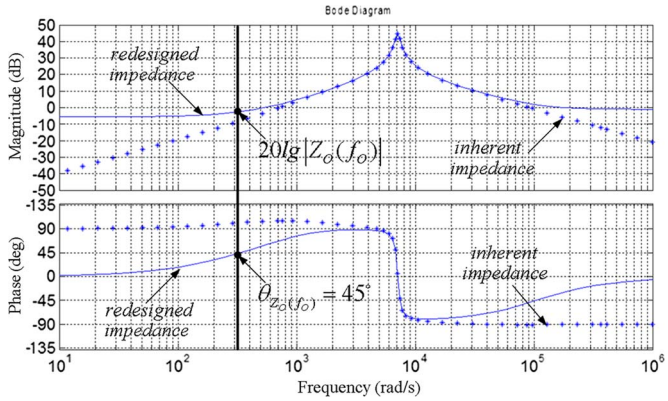


Fig. 15. Bode diagram of the output impedance of the inverter. Dotted line: inherent. Solid line: redesigned.

As previously stated, the output impedances will strongly affect the power-sharing behavior of the parallel inverters. It can be observed that the relationship between P/Q and $\frac{E}{\phi}$ are completely changed with the complex impedance compared to the traditional droop methods. To effectively achieve P/Q droop control and minimize the circulating current, the output impedance can be redesigned by adding virtual complex impedance, as proposed in Section III. The redesigned output impedance can be expressed as in (14), shown at the bottom of the page.

Fig. 15 shows the frequency-domain behavior of the output impedance. In this figure, the original output impedance that the inverter controller achieved is depicted by a dotted line, and the output impedance that the virtual complex impedance achieved is depicted by a solid line. As shown in Fig. 15, apart from its inherent inductive or resistive nature, the phase of the output impedance is very sensitive to the parasitic resistance of the system. Consequently, the power-sharing accuracy can be affected, because the output impedance is not fixed and is very small. The virtual complex impedance, which can fix this output impedance, is added by the controller, considering the inherent output impedance of the inverters. Notice that, in most cases where the UPS are paralleled with low-voltage cabling, the virtual output impedance will be dominant compared to the system line impedance, given a proper choice. As a consequence, the system impedance can be near constant.

As shown in Fig. 15 (solid line), the angle of the new output impedance has been redesigned to near $\pi/4$ by adding the virtual complex impedance to the inherent output impedance. The values of virtual impedance adopted here are $R_v = 0.19\ \Omega$ and $L_v = 535\ \mu$H based on the power-sharing relationships in Section II. Now, the coupled P/Q sharing relationship, as shown in (5) and (6), can be decoupled and simplified by using the virtual complex impedance module. Note that both P and

$$Z_{\text{redesigned}}(s) = \frac{L_f(R_v + \omega_v L_v)s^3 + (R_v r_L + \omega_v L_v r_L + L_v R_v + \omega_v L_v R_v)s^2 + (R_v r_L + \omega_v R_v r_L)s}{L_f C_f s^4 + (G_C C_f + r_L C_f + \omega_v L_f C_f)s^3 + (K_P G_C + \omega_v G_C C_f + \omega_v r_L C_f)s^2 + (K_I G_C + \omega_v K_P G_C)s + \omega_v K_I G_C} \quad (14)$$

TABLE II
PARAMETERS OF PROPOSED CONTROLLER

Parameters	Symbol	Value
Impedance magnitude	Z	0.25
Impedance angle	θ	46.1°
Amplitude of output voltage	E	310.5 V
Initial phase error	Φ	0.8°
Amplitude droop coefficient	m	3×10^{-5}
Frequency droop coefficient	n	8×10^{-5}
Load voltage	U	309 V
Cut-off frequency of power calculation	ω_f	62.8 rad/s
Cut-off frequency of virtual inductor	ω_V	$350\times2\pi$ rad/s
Value of Virtual resistor	R_V	0.19Ω
Value of Virtual inductor	L_V	535μH

Q depend simultaneously on the output-voltage parameters ω (i.e., $\omega = d\phi/dt$) and E. Therefore, the novel droop controller based on the proper design of the virtual complex impedance can be expressed as follows:

$$\omega = \omega_0 - m(P - Q) \tag{15}$$

$$E = E_0 - n(P + Q) \tag{16}$$

where m and n are the droop coefficients of the frequency and amplitude, respectively, and ω_0 and E_0 are the initial frequency and amplitude of the inverter output voltage, respectively.

B. Design of Droop Coefficients

It is well known that, if the droop coefficients are increased, then efficient power sharing can be achieved, at the expense of degrading the voltage regulation. Therefore, the droop coefficients must be set with a compromise between the power-sharing precision and the voltage-regulating precision. This feature is inherent in the droop method [11], [18].

According to the proposed frequency and amplitude droop scheme, as shown in (15) and (16), and considering that, in the system, there is some voltage bias and some system errors due to parameter mismatch, the initial frequency and amplitude cannot exactly be equal in different inverters. Therefore, the maximum droop coefficient of the frequency is determined by the maximum allowed frequency deviation $\Delta\omega_{\max}$ and the maximum allowed apparent power $S_{\max}$, i.e.,

$$m_{\max} = \frac{\Delta\omega_{\max}}{|S_{\max}|}. \tag{17}$$

In the case of the Q–E droop, the design is different from the P–ω droop, because the voltage amplitude droop should also take the virtual impedance into account [24]. To satisfy the voltage regulation specification, the maximum droop coefficient for the Q–E droop is determinate by the maximum allowed deviation of tracked voltage reference $\Delta E_{\max}$, and it can be expressed as

$$n_{\max} = \frac{\Delta E_{\max} - I_{O\max}|Z_{\text{virtual}}(j\omega_O)|}{|P_{\max} + Q_{\max}|} \tag{18}$$

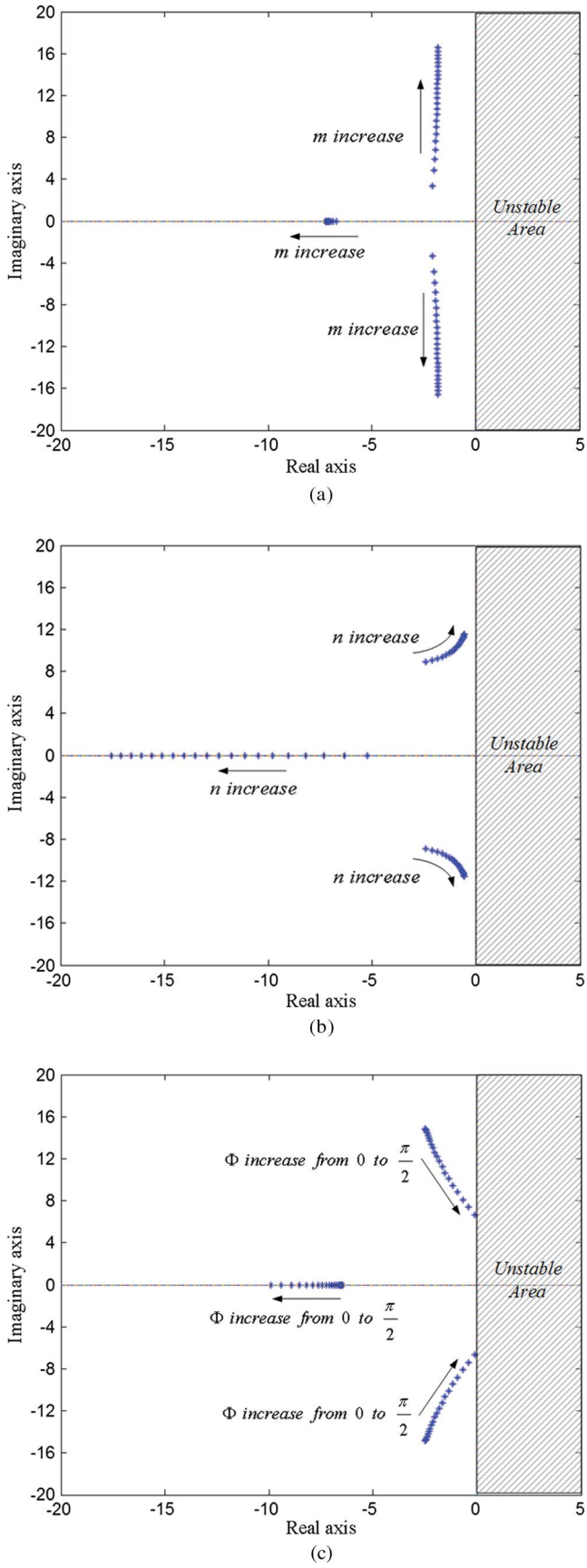


Fig. 16. Root locus diagram for the small signal model. (a) $1\times10^{-6} \le m \le 1\times10^{-3}, n = 8\times10^{-5}$. (b) $1\times10^{-6} \le n \le 1\times10^{-3}, m = 3\times10^{-5}$. (c) $0 \le \Phi \le \pi/2, m = 3\times10^{-5}, n = 8\times10^{-5}$.

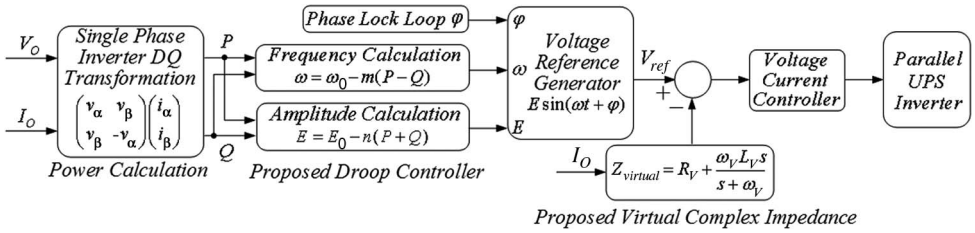


Fig. 17. Implementation of the proposed power-sharing controller.

where $I_{O\max}$ is the output current at full load, and $Z_{\text{virtual}}(j\omega_O)$ is the virtual output impedance around the fundamental frequency.

C. Modeling and Implementation of Proposed Controller

To investigate the stability and the transient response of the system, a small signal model of the system is presented. The small signal dynamics of the active and reactive power can be obtained by linearizing (5) and (6), considering that $\theta \approx \pi/4$, as

$$\hat{p} = \frac{\sqrt{2}}{2}\frac{\omega_f U}{(s+\omega_f)Z}\left[(1+\Phi)\hat{e} + E\hat{\phi}\right] \tag{19}$$

$$\hat{q} = \frac{\sqrt{2}}{2}\frac{\omega_f U}{(s+\omega_f)Z}\left[(1-\Phi)\hat{e} - E\hat{\phi}\right] \tag{20}$$

where ω_f is the cutoff frequency of the power calculation module, $\hat{}$ denotes perturbed values, and capital letters mean equilibrium point values. Now, considering the small disturbances around the state of equilibrium point, (15) and (16) can be linearized as

$$\hat{\omega} = -m(\hat{p} - \hat{q}) \tag{21}$$

$$\hat{e} = -n(\hat{p} + \hat{q}). \tag{22}$$

For simplicity, the high-frequency impedance components are not considered here, because they have little effect on the system dynamics. By substituting (19) and (20) into (21) and (22) and taking $\hat{\omega}$ as $s\hat{\phi}$, the small signal dynamics of parallel system with respect to $\hat{\phi}$ can be obtained as

$$s^3\hat{\phi} + As^2\hat{\phi} + Bs\hat{\phi} + C\hat{\phi} = 0 \tag{23}$$

where

$$A = \frac{2\omega_f Z + \sqrt{2}n\omega_f U\cos\Phi}{Z}$$

$$B = \frac{\omega_f^2 Z + \sqrt{2}m\omega_f EU\cos\Phi + \sqrt{2}n\omega_f^2 U\cos\Phi}{Z}$$

$$C = \frac{2mn\omega_f^2 EU^2 + \sqrt{2}m\omega_f^2 EUZ\cos\Phi}{Z^2}.$$

According to (23), the dynamics and stability of the proposed controller can be evaluated through the root locus plots with the parameters listed in Table II. Fig. 16(a) and (b) shows the root locus plot for the system, considering the variation of the droop coefficients m and n from 1×10^{-6} to 1×10^{-3} and from 1×10^{-6} to 1×10^{-3}, respectively. Note that the system has two conjugated roots and one real root. The arrows indicate the evolution of the corresponding poles when the coefficients change. It can be observed that the poles can be adjusted to achieve certain dynamic behaviors and that the system is stable.

TABLE III
PARAMETERS OF PARALLEL INVERTERS

Items	*Inverter #1*	*Inverter #2*
DC Bus Voltage	363 V	367 V
Output Voltage (Rms)	219.5 V	221.0 V
Inductance of LC Filter	1.36 mH	1.29 mH
Capacitance of LC Filter	11 μF	11 μF
Initial Frequency f_O	50 Hz	50 Hz
Frequency Droop Coefficient m	3×10^{-5}	3×10^{-5}
Amplitude Droop Coefficient n	8×10^{-5}	8×10^{-5}
Values of Virtual resistor	0.19Ω	0.19Ω
Values of Virtual inductor	535μH	535μH

As shown in Fig. 16(a), with the increase in m from 1×10^{-6} to 1×10^{-3} and with n fixed at 8×10^{-5}, the conjugated poles tend to go far away from the real axis, making the system faster but less damped. Fig. 16(b) shows that, when m is fixed at 3×10^{-5} but n is increased from 1×10^{-6} to 1×10^{-3}, the complex poles make the system faster like a second-order behavior. In both cases, the poles remain in the left half plane; therefore, the system is stable with the coefficients. Fig. 16(c) illustrates the root locus, considering a variation in the initial phase error Φ, which allows us to identify stable and unstable behaviors. With the selected coefficient, there is a range of Φ from 0 to $\pi/2$, in which the system remains stable. Out of this range, the system becomes unstable, as shown in the shadowed area. In view of this result, it can be learned that the phase error should carefully be examined and the coefficient should also be well chosen to compromise between the dynamic response and the system stability based on the practical system.

The block diagram of the proposed power-sharing controller is depicted in Fig. 17. The voltage reference for the inverter output voltage tracking is obtained with the outputs of the droop controller and with the synchronization of a PLL. Based on the proper design of virtual complex impedance loop, the proposed decoupled active and reactive power sharing controller is adopted, as shown in Fig. 17.

V. SIMULATION AND EXPERIMENTAL RESULTS

To compare the proposed controller with the conventional droop method, both the simulations and experiments were

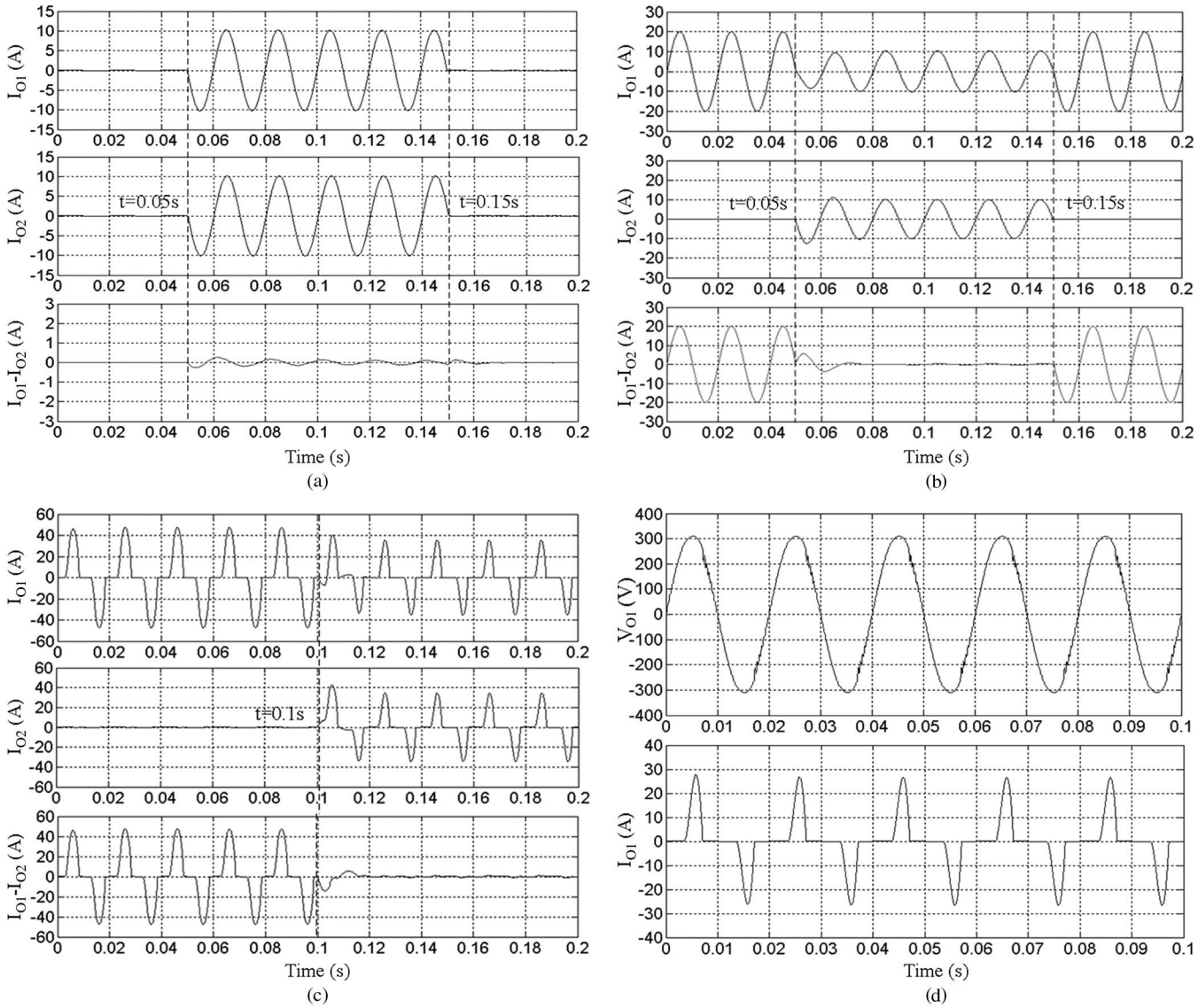


Fig. 18. Simulation results of the parallel inverters using the proposed controller. (a) Linear load connected ($t = 0.05$ s) and disconnected ($t = 0.15$ s). (b) One inverter added to ($t = 0.05$ s) and then removed ($t = 0.15$ s) from the parallel system. (c) One inverter added to the parallel system ($t = 0.1$ s) with a rectifier-type load. (d) Output voltage and current when sharing a rectifier-type load.

implemented and tested. All the parameters are listed in Table III.

Fig. 18 shows the simulation results with the proposed control scheme using the MATLAB/Simulink software. Fig. 18(a) and (b) depicts the dynamic responses of two parallel inverters at the system startup and to sudden linear load step perturbations. In contrast, Fig. 18(c) depicts the same dynamic responses for a rectifier-type load sharing. Fig. 18(d) depicts a more detailed waveform of the output current and output voltage when sharing a rectifier-type load. Table IV illustrates the simulated steady-state current sharing error between the conventional method and the proposed scheme with different line impedances. The conventional method was adopted, which is only based on the following droops in the amplitude $E = E_0 - nQ$ and the frequency $\omega = \omega_0 - mP$ of the inverter output voltage. The deviations of the frequency and amplitude between the conventional scheme and the proposed scheme are selected to be the same.

TABLE IV
SIMULATED RESULTS OF STEADY-STATE CURRENT-SHARING ERROR IN PARALLEL INVERTERS SYSTEM

Line impedance (Z_{L1}, Z_{L2})	*Circulating current (Peak) Linear load, R=15 Ω Load current:20A (Peak)*		*Circulating current (Peak) RCD load, R=14 Ω, C=2500uF, Load current:50A (Peak)*	
	Conventional Scheme	*Proposed Scheme*	*Conventional Scheme*	*Proposed Scheme*
Inductive Z_{L1}=800 μH, Z_{L2}=600 μH	0.85 A	0. 60 A	1.80 A	1.10 A
Resistive Z_{L1}=0.25 Ω, Z_{L2}=0.2 Ω	0.55 A	0.30 A	1.30 A	0.90 A
Complex Z_{L1}=0.08+j0.05 Ω, Z_{L2}=0.01+j0.01 Ω	1.50 A	0.80 A	2.50 A	1.20 A

These results confirm that the proposed controller achieves better sharing performance than the performance obtained from the classical method. It is also shown that the proposed

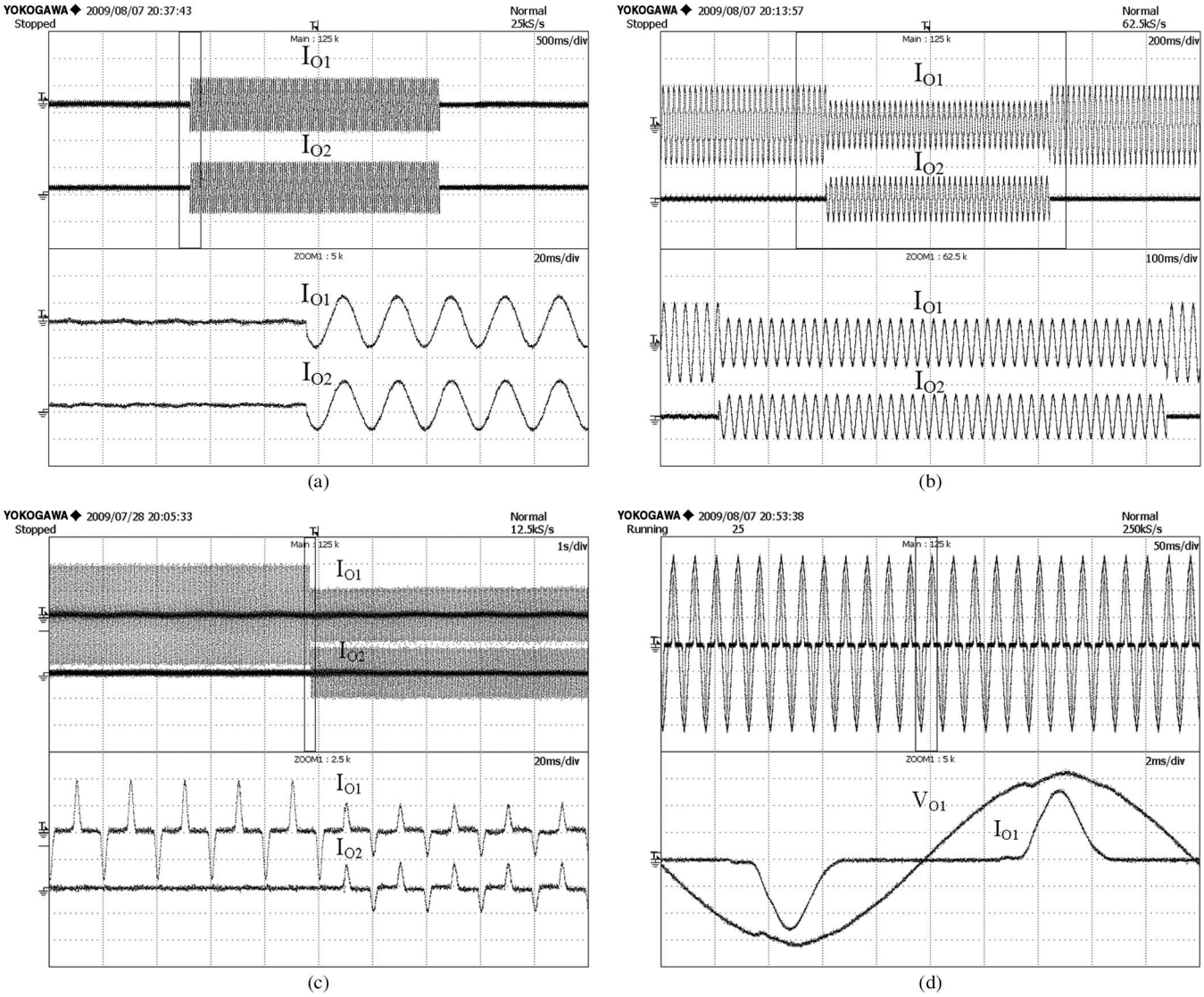


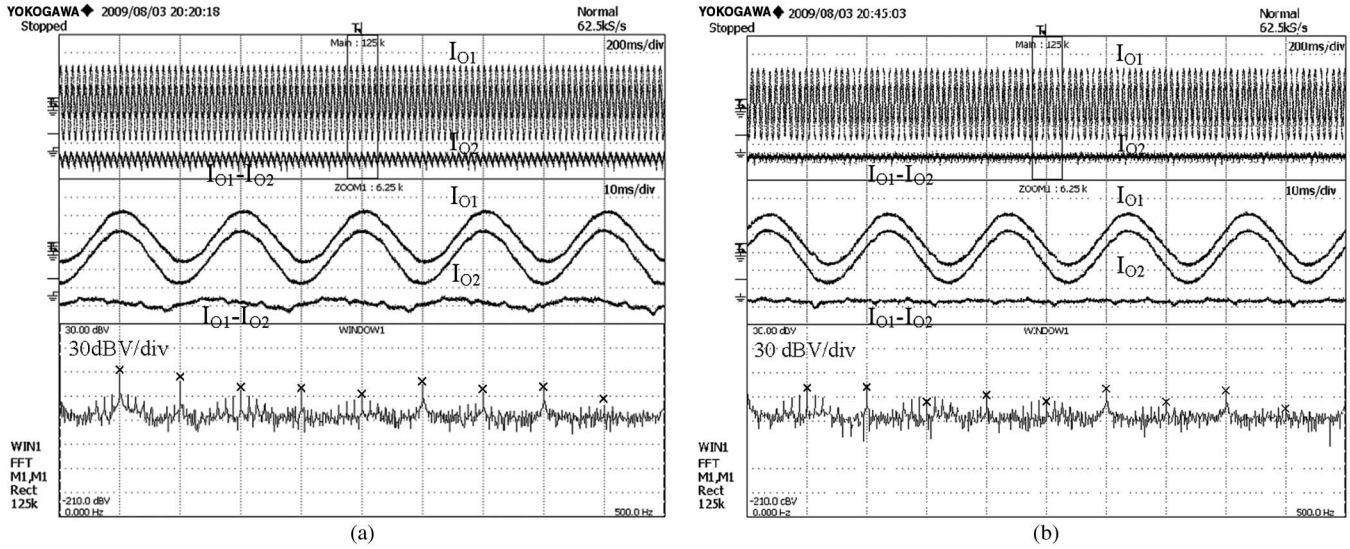
Fig. 19. Experimental results of the parallel inverters using the proposed controller. (a) Linear load connected and disconnected [x-axis: 500 ms/div (top), 20 ms/div (bottom); y-axis: 10 A/div]. (b) One inverter added to and then removed from the parallel system [x-axis: 200 ms/div (top), 100 ms/div (bottom); y-axis: 10 A/div]. (c) One inverter add to the parallel system when supplying a rectifier-type load [x-axis: 1 s/div (top), 20 ms/div (bottom); y-axis: 10 A/div]. (d) Output voltage and output current when sharing a rectifier-type load [x-axis: 50 ms/div (top), 2 ms/div (bottom); y-axis: 10 A/div, 100 V/div].

controller can allow efficient power sharing with lower sensitivity to the unbalances of line impedance, including inductive, resistive, and complex impedance situations.

A system with two 2-kVA UPS inverters was built and tested. Each inverter is formed by a single-phase stage, and the parameters are shown in Table III. The line impedances in the practical system, i.e., $Z_{L1} = 0.08 + j0.05\ \Omega$, $Z_{L2} = 0.01 + j0.01\ \Omega$, were intentionally unbalanced similar to the simulation. The controllers of these inverters were implemented on a TMS320F2811, 32-b fixed-point 150-MHz digital signal processor (DSP) from Texas Instruments. The controller also includes the PLL, which is constituted by a second-order generalized integrator (SOGI) and the frequency-locked loop (FLL) [26], to synchronize the inverter with the common ac bus at the beginning and can work for hot swap. The PLL will quit as soon as the inverter is connected to the ac common bus.

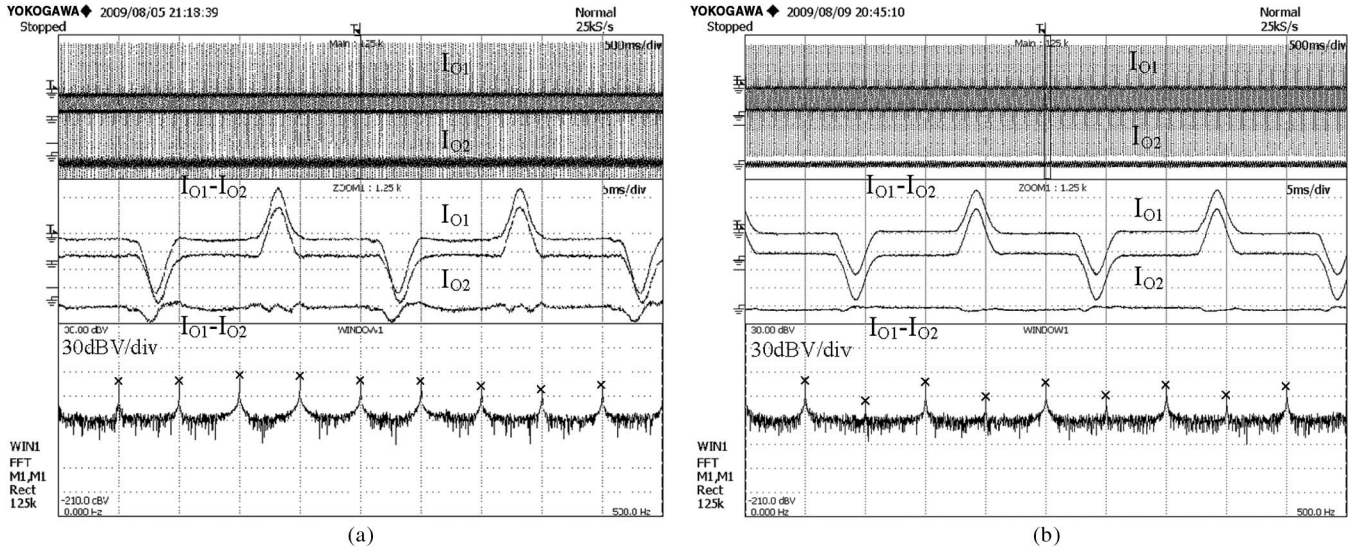
Fig. 19(a) depicts the output current of the inverter, showing the time response to a connection and disconnection of a linear load ($R = 15\ \Omega$). Fig. 19(b) depicts the time response of the inverter output currents for the case in which one of the inverters is connected and disconnected from the parallel system. Fig. 19(c) shows a detail of the time response of the inverter output current when one inverter feeds a rectifier-type load (CF $=$ 2.6) and a second inverter is connected to the system to share this load. Note that the rectifier-type load is precisely shared between the two inverters. Fig. 19(d) shows the output voltage and output current waveforms in detail when the inverters share a rectifier-type load. The measured total harmonic distortion (THD) of the voltage in the shared load was about 2.95%. It is shown that the inverter smoothly synchronizes, whereas the currents stabilize after a transient time to almost-perfect current sharing. These experimental results demonstrate that the proposed controller achieves efficient sharing and dynamic behaviors under both linear and rectifier-type loads.

Figs. 20 and 21 depict the comparisons of the circulating current between the conventional and the proposed droop



(a) (b)

Fig. 20. Comparisons of the current sharing under a linear load and FFT analysis of the circulating current in the parallel system [x-axis: 200 ms/div (top), 10 ms/div (middle), 50 Hz/div (bottom); y-axis: 10 A/div, 30 dBV/div (bottom)]. (a) Conventional droop method. (b) Proposed droop method.



(a) (b)

Fig. 21. Comparisons of the current sharing under a rectifier-type load and FFT analysis of the circulating current in the parallel system [x-axis: 500 ms/div (top), 5 ms/div (middle), 50 Hz/div (bottom); y-axis: 10 A/div, 30 dBV/div (bottom)]. (a) Conventional droop method. (b) Proposed droop method.

methods. The fast Fourier transform (FFT) results are also illustrated, which can help in identifying the harmonic content of the circulating current. Fig. 20(a) depicts the case in which the two UPS inverters supply a linear load with the conventional droop method. Fig. 20(b) depicts the same case but with the proposed control scheme. In these figures, it is shown that the circulating current that flows between the parallel inverters has been reduced and that the system harmonic content has been also reduced compared to the conventional method.

Fig. 21 depicts the behavior of the inverter output currents that feed a rectifier-type load $(\mathrm{CF} = 2.6)$ with the conventional droop method [see Fig. 21(a)] and with the proposed control method [see Fig. 21(b)]. As shown at the bottom of Fig. 21(a) and (b), better sharing with less harmonic circulating current has been obtained with the proposed controller. It is also proven that the virtual complex impedance can minimize both the fundamental and harmonic components of the circulating current.

VI. Conclusion

This paper has presented a novel control scheme for parallel inverters with no intercommunication signals, considering the impact of the complex impedance on power sharing. Applying the proposed controller, the parallel UPS inverters can deliver high-quality power, even in the presence of the rectifier-type load with unbalanced line impedances. The analyses clarify the relationship between the impact of the impedance and the power sharing in a parallel system. The virtual complex impedance module has also been proposed and well researched in this paper. The presented controller provides steady-state performance and efficient dynamic response when sharing common loads.

A series of simulations and experiments were carried out to test the performance of the proposed controller. The obtained results validate the proposed control approach and show that it can minimize the fundamental and harmonic circulating current. More accurate power sharing can be obtained for different line impedance situations through the proposed droop controller. Simulation and experimental results confirm the improvement of the proposed control scheme.

REFERENCES

[1] M. C. Chandorkar, D. M. Divan, and R. Adapa, "Control of parallel connected inverters in standalone ac supply systems," *IEEE Trans. Ind. Appl.*, vol. 29, no. 1, pp. 136–143, Jan./Feb. 1993.

[2] J. Holtz and K.-H. Werner, "Multi-inverter UPS system with redundant load sharing control," *IEEE Trans. Ind. Electron.*, vol. 37, no. 6, pp. 506–513, Dec. 1990.

[3] J.-F. Chen and C.-L. Chu, "Combination voltage controlled and current-controlled PWM inverters for UPS parallel operation," *IEEE Trans. Power Electron.*, vol. 10, no. 5, pp. 547–558, Sep. 1995.

[4] H. Van Der Broeck and U. Boeke, "A simple method for parallel operation of inverters," in *Proc. IEEE INTELEC*, 1998, pp. 143–150.

[5] T. Kawabata and S. Higashino, "Parallel operation of voltage source inverters," *IEEE Trans. Ind. Appl.*, vol. 24, no. 2, pp. 281–287, Mar./Apr. 1988.

[6] H. Hanaoka, "Development of a novel parallel redundant UPS," in *Proc. IEEE INTELEC*, 2003, pp. 493–498.

[7] M. C. Chandorkar, D. M. Divan, Y. Hu, and B. Banerjee, "Novel architecture and control for distributed UPS systems," in *Proc. IEEE APEC*, 1994, pp. 683–689.

[8] M. Arias, D. G. Lamar, M. Rodriguez, M. Hernando, and A. Fernandez, "Simple droop voltage control system for parallel operation of UPS," in *Proc. IEEE APEC*, 2004, pp. 1946–1951.

[9] W. Yao, M. Chen, J. Chen, and Z. Qian, "An improved multiple-loop controller for parallel operation of single-phase inverters with no control interconnections," in *Proc. IEEE PESC*, 2007, pp. 448–452.

[10] J. M. Guerrero, J. Matas, L. Garcıacute;a de Vicuña, M. Castilla, and J. Miret, "Wireless-control strategy for parallel operation of distributed generation inverters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1461–1470, Oct. 2006.

[11] J.-W. Kim, H.-S. Choi, and B. H. Cho, "A novel droop method for converter parallel operation," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 25–32, Jan. 2002.

[12] A. R. Bergen, *Power Systems Analysis*. Englewood Cliffs, NJ: Prentice-Hall, 1986.

[13] H. Tuladhar, T. Jin, K. Unger, and K. Mauch, "Control of parallel inverters in distributed ac power systems with consideration of line impedance," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 131–138, Jan./Feb. 2000.

[14] T.-P. Chen, "Dual-modulator compensation technique for parallel inverters using space-vector modulation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3004–3012, Aug. 2009.

[15] U. Borup, F. Blaabjerg, and P. N. Enjeti, "Sharing of nonlinear load in parallel-connected three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1817–1823, Nov./Dec. 2001.

[16] S. J. Chiang and J. M. Chang, "Parallel control of the UPS inverters with frequency-dependent droop scheme," in *Proc. IEEE PESC*, 2001, pp. 957–961.

[17] J. M. Guerrero, J. C. Vasquez, J. Matas, M. Castilla, and L. G. de Vicuna, "Control strategy for flexible microgrid based on parallel line-interactive UPS systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 726–736, Mar. 2009.

[18] J. M. Guerrero, L. G. de Vicuña, J. Matas, M. Castilla, and J. Miret, "Output impedance design for parallel-connected UPS inverters with wireless load-sharing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1126–1135, Aug. 2005.

[19] J. Hongxin, D. Ming, S. Jianhui, D. Yan, and C. Liuchen, "Communicationless parallel inverters based on inductor current feedback control," in *Proc. IEEE APEC*, 2007, pp. 1385–1389.

[20] L. Corradini, P. Mattavelli, M. Corradin, and F. Polo, "Analysis of parallel operation of uninterruptible power supplies loaded through long wiring cables," in *Proc. IEEE APEC*, 2009, pp. 1276–1282.

[21] S. J. Chiang, C. Y. Yen, and K. T. Chang, "A multimodule parallelable series-connected PWM voltage regulator," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 506–516, Jun. 2005.

[22] K. De Brabandere, B. Bolsens, J. Van den Keybus, A. Woyte, J. Driesen, and R. A. Belmans, "Voltage and frequency droop control method for parallel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1107–1115, Jul. 2007.

[23] Y. W. Li and C. Kao, "An accurate power control strategy for power electronics interfaced distributed generation units operating in a low voltage multibus microgrid," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2977–2988, Dec. 2009.

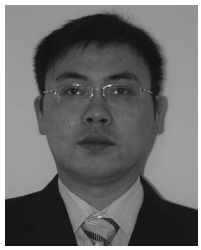
[24] L. Mihalache, "Paralleling control technique with no intercommunication signals for resonant controller-based inverters," in *Conf. Rec. IEEE IAS Annu. Meeting*, 2003, vol. 3, pp. 1882–1889.

[25] J. M. Guerrero, J. Matas, L. G. de Vicuna, M. Castilla, and J. Miret, "Decentralized control for parallel operation of distributed generation inverters using resistive output impedance," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 994–1004, Apr. 2007.

[26] P. Rodriguez, A. Luna, M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "Advanced grid synchronization system for power converters under unbalanced and distorted operating conditions," in *Proc. IEEE IECON*, 2006, pp. 5173–5178.

Wei Yao received the B.S. degree in electronic and information engineering in 2005 from Zhejiang University, Hangzhou, China, where he is currently working toward the Ph.D. degree in power electronics and power driver in the College of Electrical Engineering.

His research interests include digital control in power electronics, renewable energy systems, uninterruptible power systems, and distributed power systems.



Min Chen received the B.S. degree in applied electronics and the Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2000 and 2006, respectively.

From 2007 to 2009, he was a Postdoctoral Researcher with the College of Electrical Engineering, Zhejiang University, where he is currently a Lecturer. Since 2007, he has been responsible for the Lighting Research and Development Laboratory, National Engineering Research Center for Applied Power Electronics. His research interests include modern lighting systems for HID lamps and LED, regenerative energy systems, inverter systems, energy storage systems, and the stability of modern power electronics systems. He has published more than 30 technical papers. He is the holder of eight (granted) out of 12 applied patents of inventions.

José Matas received the B.S., M.S., and Ph.D. degrees in telecommunications engineering from the Technical University of Catalonia, Barcelona, Spain, in 1988, 1996, and 2003, respectively.

From 1988 to 1990, he was an Engineer with a consumer electronics company. Since 1990, he has been an Associate Professor with the Department of Electronic Engineering, Technical University of Catalonia. His research interests include power-factor-correction circuits, active power filters, uninterruptible power systems, distributed power systems, and nonlinear control.

Josep M. Guerrero (S'01–M'03–SM'08) received the B.S. degree in telecommunications engineering, the M.S. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, Spain, in 1997, 2000, and 2003, respectively.

From 1998 to 2004, he was an Assistant Professor with the Department of Automatic Control Systems and Computer Engineering, Technical University of Catalonia, where he is currently a Senior Lecturer, teaching courses in digital signal processing, control theory, and microprocessors. Since 2004, he has been responsible for the Sustainable Distributed Generation and Renewable Energy Research Group, Escola Industrial de Barcelona. His research interests include DSP/FPGA-based control, uninterruptible power systems, inverters for photovoltaic applications, and wind energy conversion in microgrids.

Dr. Guerrero is an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS. He is a Guest Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS SPECIAL ISSUE ON POWER ELECTRONICS FOR WIND ENERGY and the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS SPECIAL SECTION ON UNINITERRUPTIBLE POWER SUPPLY (UPS) SYSTEMS. He has organized and chaired sessions at several conferences, including the Annual Conference of the IEEE Industrial Electronics Society (IECON), IEEE Applied Power and Electronics Conference (APEC), and IEEE Power Electronics Specialists Conference (PESC).

Zhao-Ming Qian (SM'92) received the B.S. degree in radio engineering from Zhejiang University, Hangzhou, China, in 1961 and the Ph.D. degree in applied science from the Catholic University of Leuven, Leuven, Belgium, and the Interuniversity Microelectronics Center (IMEC), Leuven, in 1989.

Since 1961, he has been teaching and conducting research work on electronics, electronic measurements, photovoltaic, and power electronics with Zhejiang University, where he has been a Professor with the College of Electrical Engineering since 1992. From 1992 to 2000, he was the Director of the Power Electronics Research Institute. He is the Deputy Director of the National Engineering Research Center for Applied Power Electronics and the Deputy Director of the Scientific Committee, National Key Laboratory of Power Electronics. His research interests include power electronics and its industrial applications, as well as EMC in power electronic systems. He has published one book on EMC design and edited one book on power electronics. He has published more than 220 papers in journals and 279 papers in conference proceedings of international conferences.

Dr. Qian received the Excellent Education Award from the China Education Commission and Zhejiang University in 1993, 1997, and 1999, respectively, the Science and Technology Development Award from the China Education Commission in 1999 and 2003, respectively, and several other Excellent Paper Awards.