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An Improved Droop Controller for Parallel Operation of Single-phase Inverters using R-C Output Impedance

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***Abstract*—This paper proposes a new droop-based approach for proportional load sharing among parallel-connected inverters in an islanded microgrid. For achieving accuracy in load sharing among the parallel connected inverters, R-C type virtual impedance is emulated as the output impedance of inverters. A new method of average power computation is proposed which significantly reduces the delay encountered in conventional approaches. In contrast with the conventional droop-control methods, the proposed approach results in effectively reduced line impedance, consequently improving the full-load voltage regulation. Simulation results are provided with two single phase inverters, of different rating, connected in parallel. It is shown that proportional sharing of active and reactive powers is obtained with excellent dynamic performance.**

I. Introduction

With rapid infiltration of power electronics in distributed generation (DG) systems, parallel connection of inverters has become the *de rigeur* configuration. This topology is being increasingly researched to obtain N+1 redundancy and hence create a modular power distribution system, which could be a smart micro-grid. The reliability as well as modularity of the supply system can be increased by replacing a single inverter unit with multiple low power inverter units in parallel. Several methods of operating inverters in parallel have been reported in [1], [2], [3]. These techniques need control interconnection among the parallel inverters with a central control unit which demand a dedicated fast communication infrastructure. Limitations of the physical layer of communication not only restrict the geographical spread of the inverter units but also act as a source of noise and failure.

Control schemes for parallel operation of inverters without control interconnection were presented in [4], [5], [6]. These are mainly based on the droop method which stems from the approach used in conventional power systems for paralleling large synchronous generators. For inductive line impedance, the frequency is made to droop with increase in active power while voltage is made to similarly respond to reactive power. Major advantage of the droop method is that it is based only on measurement of local variables. To achieve good active and reactive power sharing, the controller allows variation of the frequency and amplitude of the output voltage of each parallel inverter. Although this variation is usually restricted within very tight limits, the conventional droop method still has some major limitations, especially for single-phase systems.

Firstly, its transient response is either slow or oscillatory, chiefly due to the choice of pass-band of low-pass filters necessary to calculate the average active and reactive power. In [5], an improvement in transient response is achieved by introducing power derivative and integral terms into a conventional droop scheme, though limitations of the filter pass-band still exists. In [8], to improve the transient response active and reactive powers are measured by integrating the product of the current and voltage over one fundamental cycle and the average calculated from a presumed knowledge of the cycle time. Obviously this is strictly valid for periodic waveforms, but since the frequency is being continuously varied due to droop action, this method has some inherent inaccuracies. Although some improvement in response time is observed, it can still be further improved. Also, this method works satisfactorily only when line impedances are predominantly inductive or resistive [4], [5], [6]. For predominantly inductive line impedances, $\omega - P$ and $V - Q$ droops are used for power sharing while, conversely, for predominantly resistive lines $\omega - Q$ and $V - P$ droop characteristics are employed. In such cases, the frequency-linked power (active/reactive) is shared accurately while the voltage-linked power invariably is unequally shared [9]. The sharing inequality in such cases can be overcome if line impedances are in inverse proportion of the power rating of the inverters [9]. To overcome these problems, virtual inductor [5], virtual resistor [6] or complex impedance (R-L) [7] is emulated as output impedance of the inverter. Arguably, it is better to force the output impedance of the inverter to be resistive [6], [9] because its impedance does not change with the frequency and the effect of nonlinear loads on the voltage THD can be compensated more easily. But in both cases, effective impedance between inverter and load bus increases, which degrades the load bus voltage regulation. In the present work, a significant improvement in transient response is achieved by introducing a Second Order Generalized

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Integrator (SOGI) based power filter into a conventional droop scheme. It is proposed to emulate predominantly resistive line impedances through addition of virtual capacitances, which effectively reduce the line inductances, instead of augmenting the total resistance through virtual resistance emulation. This results in net decrease in the effective line impedance with significant improvement in output voltage regulation. Virtual resistances are added to compensate for the mismatch in per unit value of line resistances which results in improvement in active power sharing among the inverters. Thus the actual emulated impedance is of R-C type which is realized using proper transfer functions. Simulation results are reported, confirming the validity of this control technique.

II. System Configuration and Modeling

A. System Configuration

Fig.1 shows the typical configuration of a microgrid which consists of a combination of distributed micro-generator units, each coupled to the microgrid through its single phase inverter. Inverters from all the sources are paralleled to form the microgrid which can operate both in islanded and grid-tied mode. All the inverters are connected with a common load bus through interconnecting lines $(R_{l1}, L_{l1}; R_{l2}, L_{l2}; ...R_{ln}, L_{ln})$. Modulation signal for each single phase inverter is generated by a dedicated controller which takes feedback of local variables.

B. Plant Modeling

Second order filters are used at the inverter output terminals for attenuating the switching ripples in the output voltage. The inverter with filter forms the basic plant. The second-order filter comprises of a tuned inductor (L_f) and a capacitor (C_f) along with the internal resistance of inductor (R_f). The equivalent series resistance (ESR) of the filter capacitor is not considered in the model, since its effect appears far above the frequency range of concern [10]. Fig.2 shows the multi-loop structure of voltage control scheme for inverter having feedback loops using filter capacitor current, i_c, and the capacitor voltage, e. Nominally modeling the inverter as

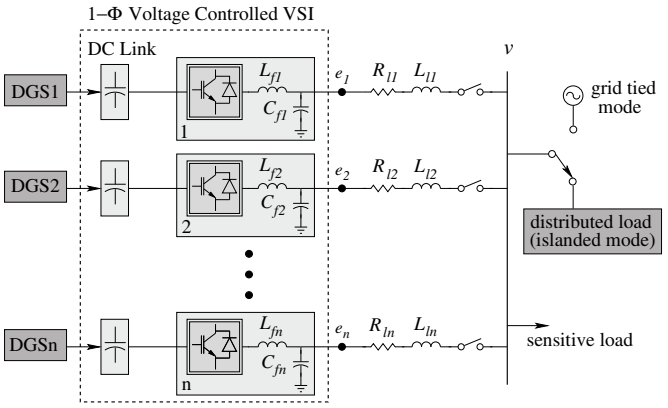


Fig. 1: Microgrid based on Parallel Inverters System

an algebraic gain (V_{dc}) [3], the control and disturbance transfer functions for the open-loop plant are derived from fig. 2 as

$$\frac{e(s)}{v_i(s)} \triangleq G_c(s) = \frac{1}{L_f C_f s^2 + R_f C_f + 1} \quad (1)$$

$$-\frac{e(s)}{i(s)} \triangleq G_d(s) = \frac{R_f + L_f s}{L_f C_f s^2 + R_f C_f + 1}. \quad (2)$$

Nominal parameter values used for control design and simulation are listed in Table I.

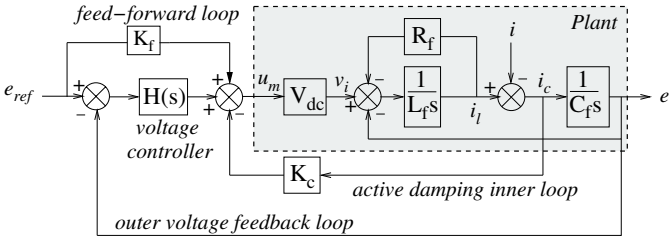


Fig. 2: Block diagram of close-loop voltage control

C. Design of Voltage Controller

To achieve good tracking performance and disturbance rejection, three control loops are introduced as shown in fig. 2.

1) Active Damping Loop: To damp out the resonant oscillations due to the filter, active damping is provided by an inner capacitor current loop with gain K_c. Modified system transfer functions in presence of active damping loop are as follows

$$\frac{e(s)}{v_i(s)} = G_c'(s) = \frac{1}{L_f C_f s^2 + (R_f + K_c) C_f + 1} \quad (3)$$

$$-\frac{e(s)}{i(s)} = G_d'(s) = \frac{R_f + L_f s}{L_f C_f s^2 + (R_f + K_c) C_f + 1}. \quad (4)$$

2) Voltage Regulation Loop: In order to track the reference inverter output voltage, a controller $H(s)$ is designed using loop shaping technique. Using this technique it is found out that a second order controller given by (5) can fulfill the desired control specifications.

$$H(s) = \frac{K(s + \omega_{z1})(s + \omega_{z2})}{s(s + \omega_p)} \quad (5)$$

3) Feed-Forward Loop: To reduce the phase error of the output voltage, a feed-forward loop with gain K_f is provided as shown in fig. 2. The usefulness of this loop can be explained by frequency-domain behavior of the close loop transfer function of the voltage control loop. The close-loop voltage gain transfer function, G_{cl}, and the disturbance transfer function, Z_d, are stated as follows

$$G_{cl} = \frac{e}{e_{ref}} = \frac{G_c'(H + K_f)}{1 + G_c' H} \quad (6)$$

$$Z_d = -\frac{e}{i} = \frac{G_d' H}{1 + G_c' H}. \quad (7)$$

Bode plot of G_{cl} is shown in fig. 3 for both the cases when the feed-forward loop is absent $(K_f = 0)$ and when a unity

gain feed-forward loop is present($K_f = 1$). It can be seen, the phase error for $K_f = 1$ at operating frequency of 50 Hz is -0.02° while for $K_f = 0$ it is -5°.

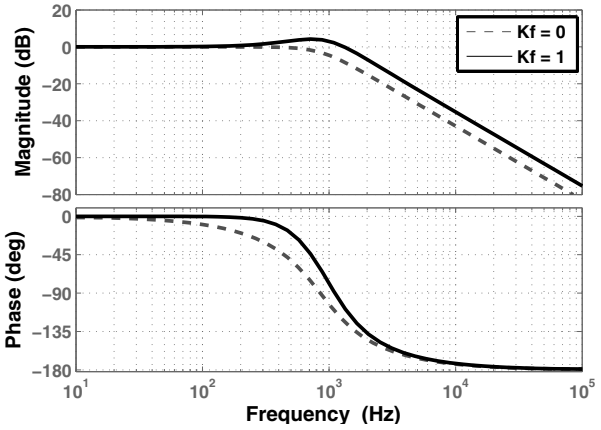


Fig. 3: Bode diagrams of the closed-loop transfer function $G_{cl}(s)$

III. Proposed Wireless Power Sharing Controller

A. R-C Output Impedance Based Droop Control Method

Fig.4 shows the equivalent circuit of an inverter connected to an ac bus. Here, net impedance, which is the aggregate of

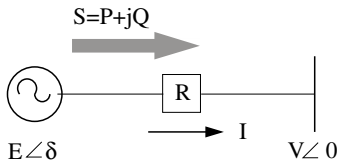


Fig. 4: Equivalent circuit of an inverter connected to an ac bus.

inverter output impedance and line impedance, between the inverter and load bus is considered as resistive. Denoting the inverter and bus voltage phasors as $\bar{E}$ (=$E\angle\delta$) and $\bar{V}$ (=$V\angle 0$), the power flow equations are given by

$$P = \frac{EV\cos(\delta) - V^2}{R} \quad (8)$$

$$Q = -\left(\frac{EV}{R}\right)\sin(\delta). \quad (9)$$

Generally, with low absolute values of the net impedance, δ is negligible. Therefore, the above equations reduce to

$$P \approx \frac{V}{R}(E - V) \quad (10)$$

$$Q \approx -\left(\frac{EV}{R}\right)\delta \quad (11)$$

From (10) and (11), it is clear that, predominantly, the real power depends on the magnitude difference $(E - V)$ while reactive power depends on the angle difference δ of $\bar{E}$ and $\bar{V}$. Hence, the droop equations are given by

$$E^* = E_o + nP \quad (12)$$

$$\omega^* = \omega_o - mQ \quad (13)$$

where, E^* and ω^* are reference peak voltage and frequency respectively. E_o and ω_o represent no-load peak voltage and frequency while m and n are respectively the frequency and voltage droop coefficients. The assumption of predominantly resistive line impedance is not strictly valid in actual practice, where the nature of line impedance depends on the interconnecting line length and is generally of R-L type. Therefore, to make the net interconnecting impedance predominantly resistive, an R-C type virtual impedance is emulated in series with each inverter. The capacitive component is added for compensating the inductive component of the natural interconnecting impedance while a virtual resistance is added to compensate for the mismatch in per unit value of line resistances, which improves active power sharing among the inverters [9].

Simplified version of fig. 2 along with droop control and virtual impedance loop is given in fig. 5. The resistive component of R-C virtual impedance (Z_v) is emulated by introducing a voltage drop in the output voltage reference, which varies proportionally with the output current. Capacitive component of the emulated impedance is introduced by drooping the output-voltage reference proportionally to the time integral of the output current (see fig. 5). Mathematical equations detailing these operations are as follows, with reference to fig. 5.

$$e(s) = e^*(s)G_{cl} - \{Z_v(s)G_{cl} + Z_d(s)\}i(s) \quad (14)$$

Now, if $Z_L(= R_l + sL_l)$ is the line impedance, the load bus voltage $v(s)$ can be given by

$$v(s) = e(s) - Z_L(s)i(s) \quad (15)$$

Using (14), (15) is expressed as

$$v(s) = G_{cl}(s)e^*(s) - \{Z_v(s)G_{cl} + Z_d(s) + Z_L(s)\}i(s) \quad (16)$$

Due to close loop voltage control, at operating frequency,

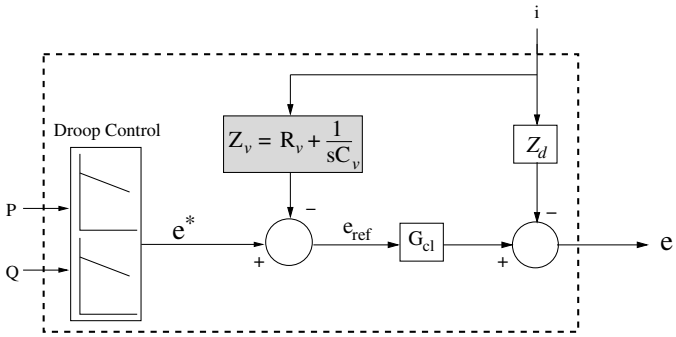


Fig. 5: Block diagram of R-C type Virtual impedance based Droop Control Method

$Z_d(s)$ is negligible and G_{cl} has almost unity gain with negligible phase lag. Therefore, equation (16) reduces to

$$v(s) \approx e^*(s) - \{Z_v(s) + Z_L(s)\}i(s)$$

$$\approx e^*(s) - \{(R_v + R_l) + (\frac{1}{sC_v} + sL_l)\}i \quad (17)$$

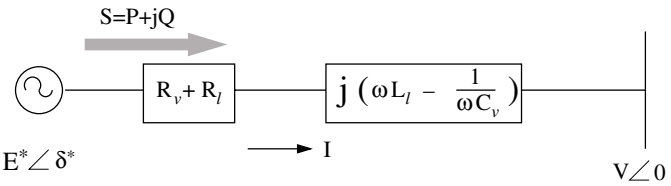


Fig. 6: Approximate equivalent circuit of an inverter connected to an ac bus after the emulation of R-C impedance

Using equation (17), the approximate equivalent circuit is drawn which is shown in fig.6. From fig.6, it is clear that virtual capacitive reactance compensates the inductive reactance of the interconnecting line and virtual resistance increases the aggregate resistance. Thus due to the cumulative effect of both type of virtual impedances, net $\frac{R}{X_L}$ ratio is improved.

B. Average Power Measurement using Proposed Filter

The reference inverter output voltage is given by using (12) and (13), where P and Q are the average value over one line-cycle of instantaneous active, p, and reactive, q, output power. Conventionally, the average is carried out using first order low pass filter [4], [5], [6]. The instantaneous power output from single phase inverter contains a double frequency ripple component superimposed on dc component. To attenuate this ripple component, the corner frequency (f_c) of low pass filter should be kept at very low value but this makes the system dynamics sluggish. However, increasing the cutoff frequency increases the power signal ripple which in turns causes fluctuations of the system frequency and voltage amplitude due to droop control action. This paper proposes a new power filtering technique which greatly improves the transient performance as well as mitigates the problem of frequency and voltage oscillations under steady state condition.

To capture the double frequency ripple component, SOGI is proposed whose resonant frequency is tuned at 100 Hz, for a system frequency of 50 Hz. The proposed power filter is shown in fig.7. A low pass filter is also used to filter out the high frequency component which remain in power signal due to switchings and sensor noise. The SOGI is represented by

$$H_r(s) = \frac{2\zeta\omega_r s}{s^2 + 2\zeta\omega_r s + \omega_r^2} \tag{18}$$

where, ζ is the damping factor and ω_r is the resonant frequency. Consequently, the measured power does not involve

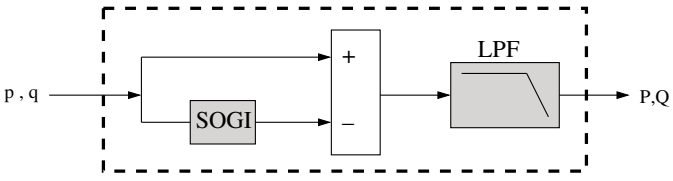


Fig. 7: Proposed Filter.

large delay nor is it corrupted by steady state ripple. Fig.8 shows the response of the two power measurement calculation methods. Fig.8a shows the response of a conventional first-order low pass filter with corner frequency of 10 Hz. This

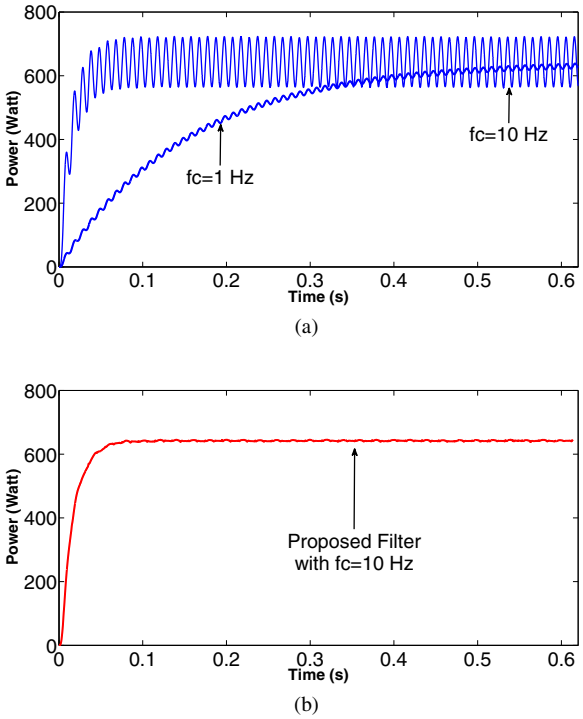


Fig. 8: (a) Response of Conventional Low Pass Filter (b) Response of Proposed Filter

results in an acceptably small settling time of 0.1 s but with disproportionately high peak to peak ripple (24%), in steady state. The ripple content can be reduced by using lower corner frequency (1 Hz) but at the expense of large settling time (0.6 s), as shown by the second plot in fig.8a. However, with the proposed filter, it is possible to obtain very low peak to peak ripple less than 1%, without compromising the settling time, as shown in fig. 8b. The proposed method thus clearly ensures a ripple free average-power signal with a very fast response, as compared to conventional low pass filter approaches. Complete block diagram of the proposed power-sharing controller is shown in fig. 9.

C. Design of Virtual R-C Impedance

In order to achieve proper parallel operation, the closed-loop output impedance of the inverter must be examined. Using fig. 5, the close loop output impedance, Z_o, is given by

$$Z_o(s) = -\frac{e(s)}{i(s)} = Z_d(s) + G_{cl}(s)\frac{1 + sR_vC_v}{sC_v} \tag{19}$$

Z_o can be obtained in terms of system parameters by substituting (6),(7) in (19). Fig. 10 shows the frequency response of the output impedance for nominal system parameters and virtual impedance selected as $R_v = 0.1\Omega, C_v = 20mF$. From fig. 10, in the frequency range of interest enclosing the line frequency 50 Hz, the phase varies between $-55°$ to $-58°$ ensuring that the output impedance is of R-C type. But the dc gain of output impedance is infinite as shown in fig. 10, which causes two problems. Whenever a step change in load occurs, oscillatory transient response appears. In addition to this, even

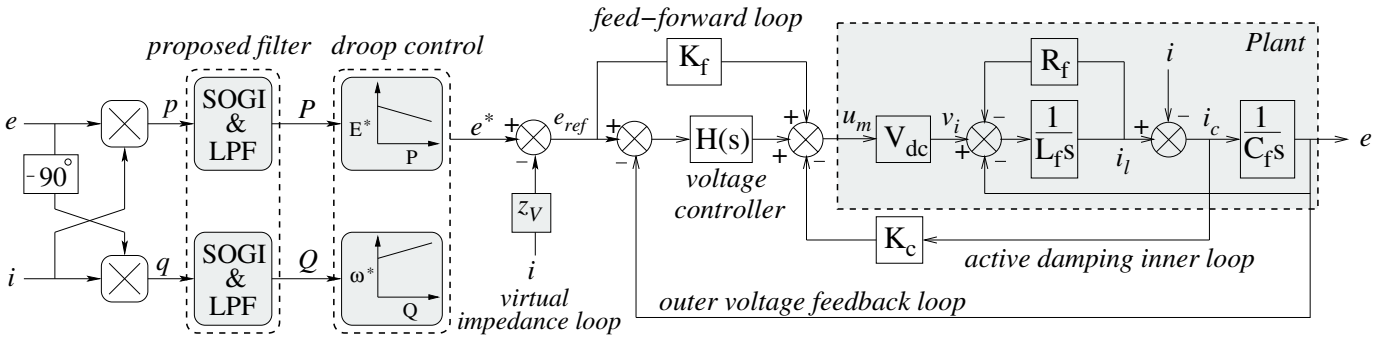


Fig. 9: Complete block diagram of the proposed power-sharing controller

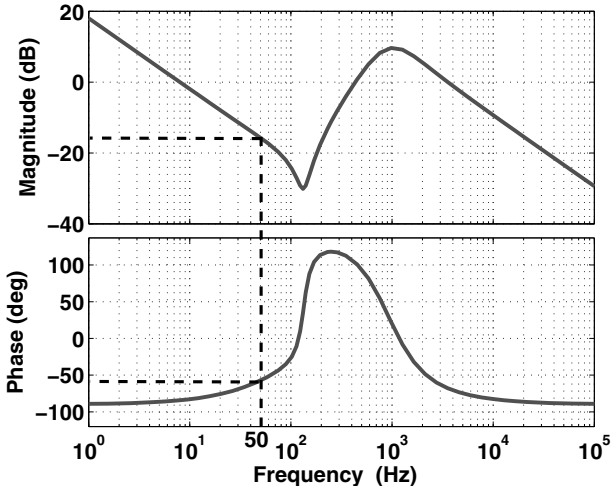


Fig. 10: Bode diagrams of the close loop output impedance

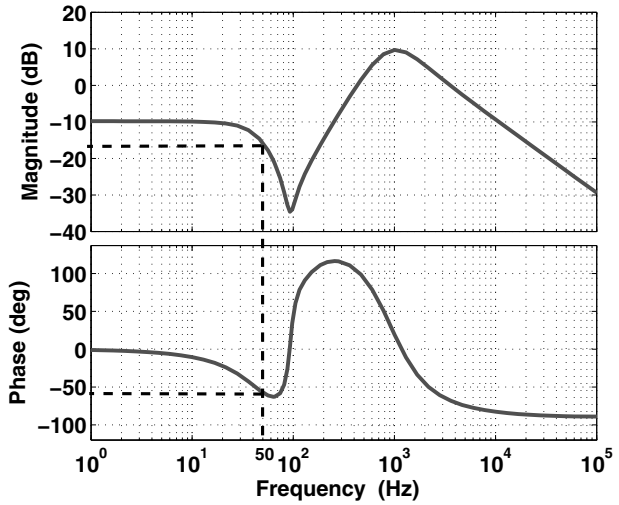


Fig. 11: Bode diagrams of the modified close loop output impedance

a negligible dc offset present in sensed output current can be amplified to a large value. So for stable parallel operation virtual impedance needs to be modified. The modified virtual impedance is given by

$$Z_v(s) = R_v + \frac{1}{sC_v}\frac{2\zeta\omega_r s}{s^2 + 2\zeta\omega_r s + \omega_r^2} \tag{20}$$

where, ζ and ω_r have usual meaning as described in (18). This modification ensures that the capacitive component becomes effective only for the desired frequency range as shown in Bode diagram of the output impedance given in fig. 11. Now, it can be seen that the output impedance at the line frequency is of R-C type and ensures attenuation of low frequencies.

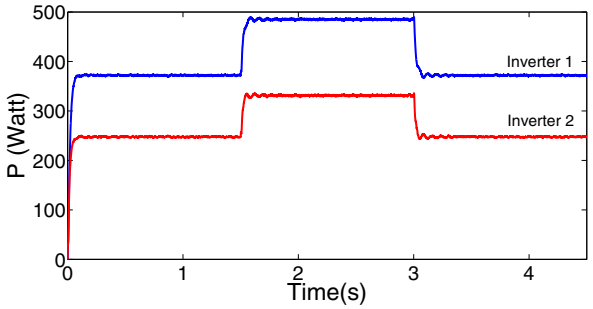
IV. Simulation Results

The proposed controller has been simulated for a micro-grid with two single phase inverters of different rating, connected in parallel, sharing a common load. System parameters are mentioned in Table I. To validate the feasibility of the proposed controller, lines connecting the inverters and the load are chosen with unequal per-unit impedances. For making net impedance predominantly resistive between inverter and load, virtual capacitances of values $C_{v1} = 6.34mF$ and $C_{v2} = 5.8mF$ are used respectively for inverter-1 and inverter-2.

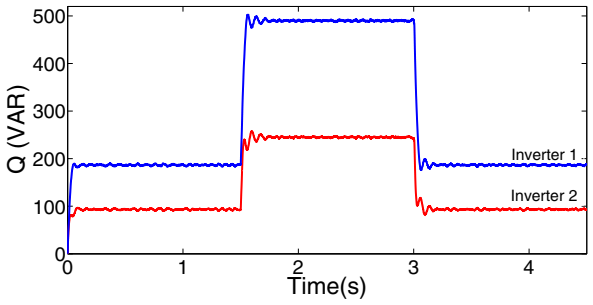
TABLE I: Nominal System Parameters

Parameters	Inverter1	Inverter2
Rating	2kVA	1kVA
Droop Coefficients	m_1=-0.0031 n_1=-0.0075	m_2=-0.0063 n_2=-0.0150
Nominal RMS Voltage	230V	230V
Nominal frequency	50Hz	50Hz
Filter Parameters	0.54mH,47μF	0.54mH,47μF
Line impedance	(0.7+j0.6)Ω	(0.72+j0.65)Ω
Switching frequency	10kHz	10kHz

Fig.12 shows the simulation result when only virtual capacitances are emulated and resistances are not emulated. It can be observed that the transient response at the startup and for load step changes (at 1.5 s and 3 s respectively) is well damped and having settling time of 0.1 s. It is interesting to note

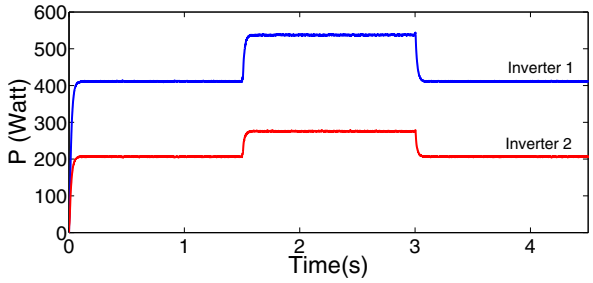


(a)

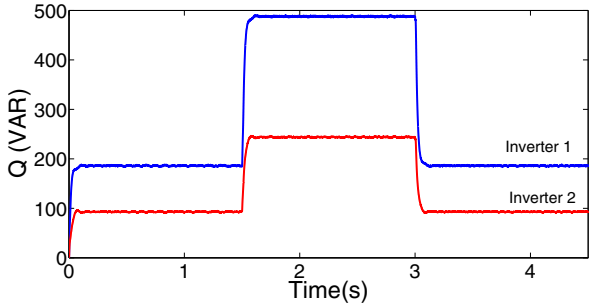


(b)

Fig. 12: Active and Reactive Power Shared by Inverters when $C_{v1} = 6.34mF$, $C_{v2} = 5.8mF$ and $R_{v1} = 0, R_{v2} = 0$ (a) Active Power (b) Reactive Power



(a)



(b)

Fig. 13: Active and Reactive Power Shared by Inverters when $C_{v1} = 6.34mF$, $C_{v2} = 5.8mF$ and $R_{v1} = 0.05\Omega$, $R_{v2} = 0.8\Omega$ (a) Active Power (b) Reactive Power

that the reactive power is proportionately shared between the inverter modules while the active power sharing is not strictly proportional.

Fig.13 shows the simulation result when virtual resistances are also emulated. It is observed that now both active and reactive powers are shared in almost exact proportion of the ratings of the inverters.

V. Conclusion

In this paper, a novel droop controller for parallel inverters has been proposed. Measuring the average power using SOGI was found to give superior performance compared to using a conventional low pass filter. Design of virtual R-C impedance is also discussed. By emulating an R-C type virtual impedance in the inverter output, the droop controller was found to be effective in power sharing accuracy.

Acknowledgment

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