MTDE - 201 ELECTRONIC SYSTEM DESIGN

UNIT -I DESIGN CONCEPTS & LOGIC CIRCUITS

Digital Hardware, Design Process, Design of Digital HardwareVariables & Functions Logic gates & Networks synthesis, SOP, POS forms, Introduction to VHDL.

UNIT- II OPTIMIZED IMPLEMENTATION OF LOGIC FUNCTIONS:

Strategy for minimization, Incompletely specified functions, Multiple output circuits, Multilevel synthesis & Analysis Building Block of combinational circuits, Multiplexers Decoders, Encoders Code Converters.

UNIT- III SYNCHRONOUS SEQUENTIAL CIRCUITS

Basic Design Steps, Mealy state Model, Design of FSM,

UNIT – IV ASYNCHRONOUS SEQUENTIAL CIRCUITS

Analysis, Synthesis, State Reduction, State Assignment, Hazards.

UNIT V TESTING OF LOGIC CIRCUITS

Fault Model, Path sensitizing, Random testing, Circuits with Tree Structure.

BOOK:

1. Introduction to Logic Design – MARCOVITZ – (Text)

REFERENCES:

1. Engineering Digital Design – TINDER
2. An Engineering Approach to Digital Design – FLETCHER
3. Logic and Computer Design Fundamentals – MANO

MTDE – 202 ADVANCE DIGITAL SIGNAL PROCESSING

UNIT -I

Review of Digital Signal Processing: Review of discrete–time sequences and systems, Linear Shift Invariant (LSI) systems. Causality and Stability Criterion, FIR & IIR representations, Z-Transform, Digital structures, Fast Fourier Transform, Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT) algorithms using decimation in time and decimation in frequency techniques, Chirp Z- Transform, Hilbert Transform and applications.

UNIT -II

Digital Filter design: FIR filter design, IIR filter design from analog filters, digital filter design based on least square method.

UNIT -III

Multirate Digital Signal Processing: Decimation & Interpolation, Sampling rate conversion, Filter design and implementation for sampling rate conversion, applications of multirate signal processing

UNIT -IV

Filter Banks: QMF, M-Channel uniform and non-uniform filter banks, transmultiplexers.

UNIT -V

Wavelets: Introduction, the short-time Fourier transform, the wavelet transform, discrete-time orthonormal wavelets, continuous-time orthonormal wavelets.

References

1. J.G.Proakis & D.G.Manolakis, “Digital Signal Processing, Principles, Algorithms and Applications”, PHI

2. P.P.Vaidyanathan, “Multirate Systems and Filter Banks”, Pearson

3. S.K. Mitra, “Digital Signal Processing”, TMH

MTDE – 203 MICROELECTRONIC

1.Introduction to IC Technology, Overview of MOS and BJT, Threshold Voltage, Body effect, basic DC equations, 2nd order Effect, MOS model, small-signal AC characteristics, CMOS inverter and its DC characteristics, static load MOS inverter.

2.Silicon semiconductor technology, wafer processing, oxidation, epitaxy, deposition, ion implantation, CMOS technology, N-Well and P-Well process and SOI.

3.MOSFET and BJT Current Mirrors and its applications, Op- Amp Design, Basic Gain Stage, Gain boosting techniques, Single-ended and differential operations, Basic differential pair: qualitative analysis and quantitative analysis, Common mode response, Differential pair with MOS loads, Gilbert Cell.

4.CMOS Logic gate design, Fan-in and Fan-out, typical NAND and NOR delays, Transistor sizing, CMOS logic structure, DC analysis of Complementary Logic, BiCMOS logic, Pseudo NMOS, dynamic CMOS logic, Pass transistor, CMOS Domino Logic, NP domino logic, Cascode voltage switch logic, source-follower pull-up logic (SFPL).

5.Memory cells and Arrays, Clocking disciplines, Design, Power optimization.

6.Fault Modeling and Simulation, Testability, Analysis Technique, Ad-hoc Methods and General guidelines, Scan Technique, Boundary Scan, Built in Self Test, Physics of Interconnects in VLSI, Scaling of Interconnects.

7. PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Text Books:

1. Randoll L. Geiger, Phillip E. Allen, Noel K. Strader “VLSI Design Techniques for Analog and Digital Circuits”, Mc Graw Hill International company, 1990.
2. Malcom R. Haskard, Lan C May, “Analog VLSI Design NMOS and CMOS”, Prentice Hall, 1998.
3. R. Jacob Baker, Harry W. LI., & David K. Boyce., “CMOS Circuit Design”. 3rd Indian reprint, PHI, 2000.
4. Microelectronic Circuits, 5th Edition, by Adel S. Sedra and Kenneth C. Smith, Oxford University press, 2004

Reference Books:

1. M.H Rashid, SPICE for Power Electronics and Electric Power, Englewood. Cliffs, N.J. Prentice Hall, 1993.
2. PSPICE Manual, Irvine, Calif: - Micro Sim Corporation, 1992.
3. Philip E. Allen Douglas and R. Holberg, “CMOS Analog Circuit Design”, Second Addition Oxford University Press-2003.
4. Fundamentals of Microelectronics, 1st Edition, by Behzad Razavi, Wiley Press, January 2008.

MTDE – 204 EMBEDDED SYSTEM

UNIT -I

8 Bit Micro controllers: Introduction to MCS-51 family, Peripheral of MCS-51 family, PIC Micro Controller –CPU architecture, registers, instruction sets addressing modes, loop timing, On chip Peripherals of PIC, Motorola MC68H11 Family Architecture Registers, Addressing modes, Interrupts- features of interrupts- Interrupt vector and Priority, timing generation and measurements, Input capture, Out capture.

UNIT -II

16 Bit Micro controller: Introduction to MCS-96 family, Peripherals of MCS-96 family, 80196-architecture, CPU operation, memory organization, I/O port, Operand addressing, instruction set, Interrupts, On chip Peripherals-PWM, Timers, HIS/HSO, Serial Port, External memory interfacing.

UNIT -III

32 bit Micro controller: Intel 80960-architecture, memory address space, Salient features of ARM processor family-ARM7 /ARM9/ ARM9E/ ARM10/ ARM11/ SecureCore /Strong ARM, XScale technology, ARM9200 Architecture,Pinouts, Peripheral Identifier, System Interrupts, External Interrupts, Product memory mapping, External memory mapping, Internal memory mapping, On chip Peripherals-Memory controllers, external Bus Interface(EBI), Advanced interrupt controller(AIC), USART, Timer counter.

UNIT -IV

Software development and tools: Embedded system evolution trends. Round- Robin, Round-robin with Interrupts, function- One- Scheduling Architecture, Algorithms. Introduction to- assembler- compiler- cross compilers and Integrated Development Environment (IDE) Object Oriented Interfacing, Recursion, Debugging strategies, Simulators.

UNIT -V

Real Time Operating Systems: Task and Task States, tasks and data, semaphores and shared Data Operating system Services- Message queues- Timer Function- Events- Memory Management, Interrupt Routines in an RTOS environment, basic design Using RTOS.

References:

- David E Simon, " An embedded software Primer" Pearson education Asia.
- John B Peat man " Design with Micro controller" Pearson education Asia.
- Jonartthan W. Valvano Brooks/cole " Embedded Micro Computer Systems. Real time Interfacing", Thomson learning

MTDE – 205 FAULT TOLERANT SYSTEMS

UNIT-I

Basic concepts of Reliability: Failures and faults, Reliability and failure rate, Relation between reliability & mean time between failure, Maintainability & Availability, reliability of series and parallel systems. Modeling of faults. Test generation for combinational logic circuits :conventional methods (path sesitisation,Boolean difference), Random testing, transition count testing and signature analysis.

UNIT-II

Fault Tolerant Design-I: Basic concepts ,static,(NMR,use of error correcting codes), dynamic, hybrid and self purging redundancy, Sift-out Modular Redundancy (SMR), triple modular redundancy, SMR reconfiguration.

UNIT-III

Fault Tolerant Design-II: Time redundancy, software redundancy, fail-soft operation, examples of practical fault tolerant systems, introduction to fault tolerant design of VLSI chips.

UNIT-IV

Self checking circuits: Design of totally self checking checkers, checkers using m-out of a codes, Berger codes and low cost residue code, self-checking sequential machines, partially self-checking circuits. Fail safe Design: Strongly fault secure circuits, fail-safe design of sequential circuits using partition theory and Berger codes, totally self checking PLA design.

UNIT-V

Design for testable combination logic circuits: Basic concepts of testability, controllability and observability. The Read-Muller expansion technique, level OR-AND-OR design, use of control and syndrome-testing design.

Built-in-test, built-in-test of VLSI chips, design for autonomous self-test, design in testability into logic boards.

Suggested Reading:

1. Parag K. Lala, *Fault Tolerant & Fault Testable Hardware Design,*(PHI) 1985

2. Parag K. Lala, *Digital systems Design using PLD's,* PHI 1990.

3. N.N. Biswas, *Logic Design Theory,* PHI 1990.

4. Konad Chakraborthy & Pinaki Mazumdar, *Fault tolerance and Reliability Techniques for high – density random – access memories Reason,* 2002.