RAJIV GANDHI PROUDYOGIKI VISHWAVIDYALAYA, BHOPAL

New Scheme Based On AICTE Flexible Curricula

Electronics Engineering (VLSI Design and Technology), III Semester

BT301	**Mathematics-III**	**3L-1T-0P**	**4 Credits**

OBJECTIVES

The objective of this course is to fulfill the needs of engineers to understand applications of Numerical Analysis, Transform Calculus, and Statistical techniques in order to acquire mathematical knowledge and solve a wide range of practical problems appearing in different sections of science and engineering. More precisely, the objectives are:

- To introduce effective mathematical tools for the Numerical Solutions of algebraic and transcendental equations.
- To enable young technocrats to acquire mathematical knowledge to understand Laplace transformation, Inverse Laplace transformation, and Fourier Transform which are used in various branches of engineering.
- To acquaint the student with mathematical tools available in Statistics needed in various fields of science and engineering.

Module 1: Numerical Methods – 1 (8 hours)

Solution of polynomial and transcendental equations: Bisection method, Newton-Raphson method, and Regula-Falsi method. Finite differences, Relation between operators, Interpolation using Newton's forward and backward difference formulae. Interpolation with unequal intervals: Newton's divided difference and Lagrange's formulae.

Module 2: Numerical Methods – 2 (6 hours)

Numerical Differentiation, Numerical integration: Trapezoidal rule, Simpson's 1/3rd and 3/8th rules. Solution of Simultaneous Linear Algebraic Equations by Gauss's Elimination, Gauss's Jordan, and Crout's methods. Jacobi's, Gauss-Seidal, and Relaxation methods.

Module 3: Numerical Methods – 3 (10 hours)

Ordinary differential equations: Taylor's series, Euler and modified Euler's methods. Runge-Kutta method of fourth order for solving first and second-order equations. Milne's and Adam's predictor-corrector methods. Partial differential equations: Finite difference solution of two-dimensional Laplace equation and Poisson equation. Implicit and explicit methods for one-dimensional heat equation (Bender-Schmidt and Crank-Nicholson methods). Finite difference explicit method for wave equation.

Module 4: Transform Calculus (8 hours)

Laplace Transform, Properties of Laplace Transform, Laplace transform of periodic functions. Finding inverse Laplace transform by different methods, convolution theorem. Evaluation of integrals by Laplace transform, solving ODEs by Laplace Transform method. Fourier transforms.

Module 5: Concept of Probability (8 hours)

Probability Mass Function, Probability Density Function. Discrete Distribution: Binomial, Poisson's. Continuous Distribution: Normal Distribution, Exponential Distribution.

Textbooks/References:

1. P. Kandasamy, K. Thilagavathy, K. Gunavathi, *Numerical Methods*, S. Chand & Company, 2nd Edition, Reprint 2012.
2. S. S. Sastry, *Introductory Methods of Numerical Analysis*, PHI, 4th Edition, 2005.
3. Erwin Kreyszig, *Advanced Engineering Mathematics*, 9th Edition, John Wiley & Sons, 2006.
4. B. S. Grewal, *Higher Engineering Mathematics*, Khanna Publishers, 35th Edition, 2010.
5. N. P. Bali and Manish Goyal, *A Textbook of Engineering Mathematics*, Laxmi Publications, Reprint, 2010.
6. P. G. Hoel, S. C. Port, and C. J. Stone, *Introduction to Probability Theory*, Universal Book Stall, 2003 (Reprint).
7. S. Ross, *A First Course in Probability*, 6th Ed., Pearson Education India, 2002.
8. W. Feller, *An Introduction to Probability Theory and its Applications*, Vol. 1, 3rd Ed., Wiley, 1968.

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Electronics Engineering (VLSI Design and Technology), III Semester

ED 302 - Introduction to HDL

Unit 1: Introduction to Verilog HDL

Verilog as HDL, Levels of Design Description, Concurrency, Program Structure,Top-down and Bottom-up Design Methodology, Differences Between Modules and Module Instances, Parts of a Simulation, Design Block, Stimulus Block, Verilog Data Types and Operators, System Tasks, Compiler Directives

Unit 2: Gate-Level Modelling

Modelling Using Basic Verilog Gate Primitives, Description of *and*, *or*, and *buf/not* Type Gates, Rise, Fall, and Turn-off Delays, Minimum, Maximum, and Typical Delays, Design of Decoders, Multiplexers, Flip-Flops, Registers, and Counters in Gate-Level Modelling

Unit 3: Dataflow Modelling

Continuous Assignments, Delay Specification, Expressions, Operators, Design of Decoders, Multiplexers, Flip-Flops, Registers, and Counters in Dataflow Model

Unit 4: Behavioral Modelling

Procedural Assignments, Initial and Always Blocks, Blocking and Non-Blocking Statements, Delay Control, Conditional Statements, Multiway Branching, Loops, Sequential and Parallel Blocks, Design of Decoders, Multiplexers, Flip-Flops, Registers, and Counters in Behavioral Model

Unit 5: Components Test and Verification

Test Bench for Combinational Circuits Testing, Test Bench for Sequential Circuits Testing, Test Bench Techniques, Design Verification, Assertion Verification

Reference & Textbooks:

1. *Digital Design with RTL Design, Verilog, and VHDL* by Frank Vahid and Roman Lysecky
2. *Verilog HDL: A Guide to Digital Design and Synthesis* by Samir Palnitkar
3. *HDL Programming: VHDL and Verilog* by Nazeih M. Botros
4. *Digital Design with Verilog® HDL* by Elizer Sternheim

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Electronics Engineering (VLSI Design and Technology), III Semester

ED 303 - Digital Electronics

Unit 1: Number Systems: Decimal, Binary, Octal, and Hexadecimal systems; conversion from one base to another; Codes – BCD, Excess-3, Gray Reflected, ASCII, EBCDIC. Logic gates and binary operations – AND, OR, NOT, NAND, NOR, Exclusive-OR, and Exclusive-NOR. Implementation of Logic Functions using gates, NAND-NOR implementations, Multi-level gate implementations, Multi-output gate implementations. Boolean postulates and laws, De-Morgan's Theorem, Principle of Duality, Boolean function, Canonical and standard forms, Minimization of Boolean functions, Minterm, Maxterm, Sum of Products (SOP), Product of Sums (POS), Karnaugh map minimization, Don't care conditions, Quine-McCluskey method of minimization.

Unit 2: Combinational Logic Circuits: Half Adder, Full Adder, Half Subtractor, Full Subtractor, Parallel Binary Adder, Parallel Binary Subtractor, Fast Adder, Carry Look Ahead Adder, Serial Adder/Subtractor, BCD Adder, Binary Multiplier, Binary Divider, Multiplexer/De-multiplexer, Decoder, Encoder, Parity Checker, Parity Generators, Code Converters, Magnitude Comparator.

Unit 3: Sequential Logic Design: Building blocks like S-R, JK, and Master-Slave JK Flip-Flop, Edge Triggered Flip-Flop, Finite State Machines, Design of Synchronous FSM, Algorithmic State Machines Charts, Designing Synchronous Circuits like Pulse Train Generator, Pseudo-Random Binary Sequence Generator, Clock Generation.

Unit 4: Registers and Counters: Asynchronous Ripple or Serial Counter, Asynchronous Up/Down Counter, Synchronous Counters, Synchronous Up/Down Counters, Programmable Counters, Design of Synchronous Counters: State Diagram, State Table, State Minimization, State Assignment, Excitation Table and Maps, Circuit Implementation, Modulo-n Counter, Registers, Shift Registers, Universal Shift Registers, Shift Register Counters, Ring Counter, Shift Counters, Sequence Generators.

Unit 5: Logic Families and Semiconductor Memories: TTL NAND Gate, Specifications, Noise Margin, Propagation Delay, Fan-in, Fan-out, Tri-State TTL, ECL, CMOS Families and Their Interfacing, Memory Elements, Concept of Programmable Logic Devices like FPGA, Logic Implementation Using Programmable Devices.

Text/Reference Books:

1. Malvino & Leach, *Digital Principles and Applications*, TMH.
2. M. Morris Mano, *Digital Logic Design*, PHI.
3. R.P. Jain, *Modern Digital Design*, TMH.
4. S. Salivahanan & S. Arivazhagan, *Digital Circuits and Design*, Vikas Publishing.
5. D. Roy Chaudhuri, *Digital Circuits: An Introduction Part-1 & 2*, Eureka Publisher.
6. Ronald J. Tocci, *Digital Systems: Principles and Applications*, PHI.
7. Taub & Schilling, *Digital Integrated Electronics*, TMH.

Digital Electronics Lab:

1. Study of different basic digital logic gates and verification of their truth table.
2. Study and verification of the laws of Boolean Algebra and De-Morgan's Theorem.
3. Construction and verification of various combinational circuits such as Half Adder, Full Adder, and Half & Full Subtractor.

4. Study of Multiplexer and De-multiplexer.
5. Study of different Code Converters, Encoder, and Decoder.
6. Construction and verification of various types of Flip-Flops using gates and ICs.
7. Construction and verification of different Shift Registers.
8. Construction and verification of different types of Counters.
9. Study of important TTL technologies and verification of important TTL circuit parameters.

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Electronics Engineering (VLSI Design and Technology), III Semester

ED 304 - Electronic Devices

Unit 1: Semiconductor Material Properties: Elemental and compound semiconductor materials; bonding forces and energy bands in intrinsic and extrinsic silicon; charge carriers in semiconductors; carrier concentration; junction properties; equilibrium condition; biased junction; steady-state condition; breakdown mechanism (Rectifying Diodes, Zener Diodes); Metal-Semiconductor Junction. Special diodes include Tunnel diodes, Varactor diodes, Schottky diode, Photodiodes, Photodetector, LED, and Solar cell.

Unit 2: Diode Circuits: Ideal and practical diode, Clipper, Clamper. Power Supply: Rectifiers - Half Wave, Full Wave, Bridge Rectifier; filter circuits; voltage regulation using shunt and series regulator circuits; voltage regulation using ICs.

Unit 3: Fundamentals of BJT: Construction, basic operation, current components and equations; CB, CE, and CC configurations; input and output characteristics; Early effect; regions of operation: active, cut-off, and saturation; BJT as an amplifier. Ebers-Moll model; power dissipation in transistor (Pd, max rating); Photo Transistor. Transistor biasing circuits and analysis: Introduction, various biasing methods: Fixed bias, Self bias, Voltage Divider bias, Collector to Base bias; Load-line analysis: DC and AC analysis, operating point and bias stabilization, thermal runaway. Transistor as a switch.

Unit 4: Small Signal Analysis: Small signal amplifier, amplifier bandwidth, hybrid model, analysis of transistor amplifier using h-parameters. Multistage amplifier: Cascading amplifier, Bootstrapping technique, Darlington amplifier, Cascode amplifier; coupling methods in multistage amplifier. Low and high-frequency response, Hybrid π-model, current mirror circuits. Large Signal Analysis and Power Amplifiers: Class A, Class B, Class AB, Class C, Class D amplifiers; Transformer coupled and Push-Pull amplifiers.

Unit 5: FET Construction - JFET: Construction, n-channel and p-channel, transfer and drain characteristics, parameters, equivalent model and voltage gain; analysis of FET in CG, CS, and CD configurations. Enhancement and Depletion MOSFET drain and transfer characteristics. Unijunction Transistor (UJT) and Thyristors: UJT principle of operation, characteristics, and UJT relaxation oscillator.

Text/Reference Books:

1. Millman & Halkias, *Electronic Devices And Circuits*, TMH.
2. Salivahanan, Kumar & Vallavaraj, *Electronic Devices And Circuits*, TMH.
3. Boylestad & Neshelsky, *Electronic Devices & Circuits*, PHI.
4. Schilling & Belove, *Electronic Circuits: Discrete & Integrated*, TMH.
5. Chattopadhyay & Rakhshit, *Electronic Fundamentals & Applications*, New Age.
6. Adel S. Sedra & Kenneth C. Smith, *Microelectronic Circuits*, OUP.
7. R. A. Gayakwad, *Op-Amps And Linear Integrated Circuits*, PHI.
8. Theodore F. Bogart & Jeffrey S. Beasley, *Guillermo Rico Electronic Devices & Circuits*.
9. Allen Mottershead, *Electronic Devices & Circuits*.

Electronic Devices Lab:

1. Diode Characteristics:
   a) pn junction diode characteristics and static & dynamic resistance measurement from graph.
   b) Plot Zener diode characteristics curve.

2. Clipper/Clamper:
   a) Plot the characteristics curve of various clipper circuits.
   b) Plot the characteristics curve of various clamper circuits.
3. Half Wave, Full Wave & Bridge Rectifier:
   a) Measure Vrms and Vdc for half-wave, full-wave, and bridge rectifier.
   b) Measure ripple factor and rectification ratio for full-wave and half-wave rectifiers.
4. Voltage Regulation:
   Using Zener diode shunt regulator and transistor series voltage regulator in the following cases:
   a) Varying input.
   b) Varying load.
5. Characteristics of BJT:
   a) Plot input and output characteristics curve in CB and CE configurations.
   b) Find α and β and Q point from the curve.
   c) Plot the characteristics curve of various clipper circuits.
6. h-Parameters:
   Measure h-parameters (Av, Ai, Ro, and Ri) in CE amplifier.
7. Multistage Amplifier:
   a) Plot the characteristics curve for direct-coupled amplifier.
   b) Plot the characteristics curve for RC-coupled amplifier.
   c) Plot the characteristics curve for transformer-coupled amplifier.
8. FET Characteristics:
   a) Plot the characteristics curve for n-channel JFET in CS configuration.
   b) Find the pinch-off voltage from the characteristics curve.
9. UJT Characteristics:
   a) Plot the characteristics curve for UJT.
   b) Determine intrinsic stand-off ratio.

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ED 305 - Circuit Analysis

Unit 1: Introduction to Circuit Theory: Basic circuit elements R, L, and C, and their characteristics in terms of linearity and time-dependent nature; voltage and current sources; controlled and uncontrolled sources. KCL and KVL analysis, steady-state sinusoidal analysis using phasors; concept of phasor and vector, impedance and admittance, nodal and mesh analysis. Analysis of magnetically coupled circuits, dot convention, coupling coefficient, tuned circuits, series and parallel resonance.

Unit 2: Network Graph Theory: Concept of network graph, tree, tree branch and link, incidence matrix, cut set and tie set matrices, dual networks.

Unit 3: Network Theorems: Thevenin's and Norton's theorems, superposition, reciprocity, compensation, substitution, maximum power transfer, Millman's theorem, Tellegen's theorem. Problems involving dependent and independent sources.

Unit 4: Transient Analysis: Transients in RL, RC, and RLC circuits; initial and final conditions, time constants. Steady-state analysis. Laplace transform: Solution of integro-differential equations, transform of waveform synthesized with step ramp, gate and sinusoidal functions, initial and final value theorems, network theorems in the transform domain.

Unit 5: Two-Port Parameters: Z, Y, ABCD, hybrid parameters, their inverse and image parameters, relationship between parameters, interconnection of two-port networks, reciprocity and symmetry in all parameters.

Text/Reference Books:

1. M.E. Van Valkenburg, *Network Analysis*, Pearson.
2. S.P. Ghosh & A.K. Chakraborty, *Network Analysis & Synthesis*, McGraw-Hill.
3. NPTEL: Networks and Systems.

Reference:

1. Sudhakar, *Circuit Network Analysis & Synthesis*, TMH.
2. J. David Irwin, *Engineering Circuit Analysis*, Tenth Edition, Wiley India.
3. Kuo, *Network Analysis & Synthesis*, Wiley India.
4. Robert L. Boylestad, *Introductory Circuit Analysis*, Pearson.
5. Smarajit Ghosh, *Network Theory: Analysis and Synthesis*, PHI.
6. Roy Choudhary D., *Network and Systems*, New Age Publishers.
7. Bhattacharya and Singh, *Network Analysis & Synthesis*, Pearson.

Experiments List:

1. To verify Thevenin's theorem and Superposition theorem.
2. To verify Reciprocity theorem and Millman's theorem.
3. To verify Maximum Power Transfer theorem.
4. To determine open circuit and short circuit parameters of a two-port network.
5. To determine A, B, C, D parameters of a two-port network.
6. To determine h-parameters of a two-port network.
7. To find frequency response of RLC series and parallel circuits and determine resonance and 3 dB frequencies.
8. To determine charging and discharging times of capacitors.

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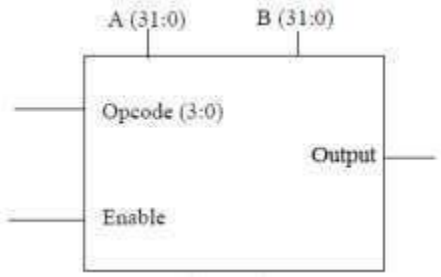
ED 306 - Verilog HDL Lab

Part–A: Programming

1. Write Verilog code to realize all the logic gates.
2. Write a Verilog program for the following combinational designs:
   a. 2-to-4 decoder.
   b. 8-to-3 encoder (without priority & with priority).
   c. 8-to-1 multiplexer.
   d. 4-bit binary to Gray code converter.
   e. Multiplexer, de-multiplexer, comparator.
3. Write a VHDL and Verilog code to describe the functions of a Full Adder using three modeling styles.
4. Write a Verilog code to model a 32-bit ALU using the schematic diagram shown below:



• ALU should use combinational logic to calculate an output based on the four-bit op-code input.
• ALU should pass the result to the out bus when the enable line is high, and tri-state the out bus when the enable line is low.
• ALU should decode the 4-bit op-code according to the example given.

OPCODE	ALU Operation
1.	A+B
2.	A-B
3.	A Complement
4.	A*B
5.	A AND B
6.	A OR B
7.	A NAND B
8.	A XOR B

5. Develop Verilog code for the following flip-flops: SR, D, JK, and T.
6. Design a 4-bit binary, BCD counters (synchronous reset and asynchronous reset), and "any sequence" counters using Verilog code.

Part–B: Interfacing (At least four of the following must be covered using VHDL/Verilog)

1. Write HDL code to display messages on an alphanumeric LCD display.
2. Write HDL code to interface a Hex keypad and display the key code on a seven-segment display.
3. Write HDL code to control the speed and direction of a DC and stepper motor.
4. Write HDL code to accept an analog signal, temperature sensor, and display the data on an LCD or seven-segment display.
5. Write HDL code to generate different waveforms (Sine, Square, Triangle, Ramp, etc.) using DAC and change the frequency.
6. Write HDL code to simulate elevator operation.