Rajiv Gandhi Proudyogiki Vishwavidyalaya, Bhopal(M.P.)

Scheme of Examination

First Semester- Master of Engineering

(Embedded System and VLSI Design,Micro electronics and VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End. Sem. Exam.	Tests (Two)	Assign ments /Quiz	End. Sem. Practical/ Viva	Practical Record/ Assignm ent/Quiz /Present ation	
1.	MEVD-101	Advanced Mathematics	3	1	-	4	70	20	10	-	-	100
2.	MEVD-102	CMOS VLSI Design	3	1	-	4	70	20	10	-	-	100
3.	MEVD-103	Advanced Logic Design	3	1	-	4	70	20	10	-	-	100
4.	MEVD-104	Digital Signal Processing	3	1	-	4	70	20	10	-	-	100
5.	MEVD-105	Embedded Microcontroller Programming	3	1	-	4	70	20	10	-	-	100
6.	MEVD-106	Lab-I Embedded System Design	-	-	6	6	-	-	-	90	60	150
7.	MEVD-107	Lab-II Digital Design	-	-	6	6	-	-	-	90	60	150
		Total	15	5	12	32	350	100	50	180	120	800

L: Lecture - T: Tutorial - P: Practical

w.e.f. July-2010