Rajiv Gandhi Proudyogiki Vishwavidyalaya, Bhopal(M.P.)

Scheme of Examination

Second Semester- Master of Engineering

(Embedded System and VLSI Design,Micro electronics and VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End. Sem. Exam.	Tests (Two)	Assignments /Quiz	End. Sem. Practical/ Viva	Practical Record/Assignment/Quiz/Presentation	
1.	MEVD-201	VLSI Technology	3	1	-	4	70	20	10	-	-	100
2.	MEVD-202	Real Time Operating System	3	1	-	4	70	20	10	-	-	100
3.	MEVD-203	VLSI Test and Testability	3	1	-	4	70	20	10	-	-	100
4.	MEVD-204	Microelectronics	3	1	-	4	70	20	10	-	-	100
5.	MEVD-205	Embedded Computing System Design	3	1	-	4	70	20	10	-	-	100
6.	MEVD-206	Lab-III Real Time Operative System	-	-	6	6	-	-	-	90	60	150
7.	MEVD-207	Lab-IV VLSI Technology	-	-	6	6	-	-	-	90	60	150
		Total	15	5	12	32	350	100	50	180	120	800

L: Lecture - T: Tutorial - P: Practical

w.e.f. July-2010