MEVD – 201 VLSI Technology

Unit I

Overview of Semiconductor Processing: Electronic grade silicon preparation, Crystal growth, Czochralski process,wafer-preparation, slicing, Marking, polishing, evaluation. Basic wafer fabrication operations, wafer sort, clean room construction and maintenance.

Unit II

Oxidation: Objectives, Silicon dioxide layer uses, Thermal oxidation mechanism and methods, Kinetics of oxidation, Deal Grove model, Oxidation processes, post oxidation evaluation.

Unit III

Basic Patterning: Overview of Photo-masking process, Ten step process, Basicphotoresist chemistry, comparison of positive and negative photoresists, X-ray lithography, Electron beam exposure system.

Unit IV

Doping: Definition of a junction, Formation of doped region and junction by diffusion, diffusion process steps, deposition, drive-in-oxidation, Ion implantation- concept and system, implant damage, Comparison of diffusion and ion-implantation techniques.

Unit V

Deposition: Chemical Vapor Deposition (CVD), CVD Processsteps, CVD System types, Low-Pressure CVD (LPCVD), Plasma-enhanced CVD (PECVD), Vapor Phase Epitaxy (VPE), Molecular Beam Epitaxy (MBE), Metalorganic CVD (MOCVD), SOS (Silicon on Sapphire) and SOI (silicon on Insulator). Brief Introduction to Metallization.

Text/ References

6. S.M. Sze, *VLSI Technology*, McGraw-Hill, 2nd Ed.
7. S. K. Gandhi, *VLSI Fabrication Principles*, Wiley
8. W. R. Runyan, *Silicon Semiconductor Technology*, McGraw-Hill.

MEVD – 202 Real Time Operating System

Unit-I

Introduction to OS, Process Management & Inter Process Communication. Memory management, I/O subsystem, File System Organization.

Unit-II

(a) Real Time Systems Concepts: Foreground/Background Systems, Critical Section of Code, Resource, Shared resource, Multitasking, task, context switch, Kernel, Schedules, Premptive & Non-Premptive Kernel, various scheduling methods.

(b) Real Time Scheduling. Real-Time task scheduling:Clock-driven,Event-driven, Scheduling of real-time task on auniprocessor. Rate Monotonic Analysis (RMA), Earliest Deadline First (EDF),Scheduling with limited priority levels

Unit-III

Kernel structure, Task scheduling, Task management, Resource sharing among tasks,Priority inversion problem,Priority inheritance protocol

An overview of scheduling in multiprocessor and distributed systems

Unit-IV

Performance Metrics of RTOS, Programming in VxWorks, or COS-II Overview of C/OS-II Overview of some other commercial embedded operating systems: PSOS, VRTX, RT Linux, WinCE.Benchmarking real-time operating systems.

Unit-V

Commercial real-time operating systems:Unix as areal-time operating system, Windows as a real-time operating system,Extensions to Unix : Host target approach,Preemption points,Fully preemptable kernel

Text/References

1. Jean J. Labrosse, M*icroC/OS-II, The Real Time Kernel*
2. VxWorks details from Internet.

3.C/OS-II Manuals

4. David E. Simon, A*n Embedded Software Primer,* Pearson Education
5. Dr. Rajib Mall, *Real time Systems, Theory and practices,* Pearson Education.

MEVD – 203 VLSI TEST AND TESTABILITY

Unit I

Introduction to Testing Process:
CMOS Testing, Reliability, Failures & Faults, Levels of Testing, Test economics, Elementary Testing Concepts, System and Field Testing, Burn in boards.

Unit II

Logic Simulation & Fault modelling: Delay Models, Event driven simulation, general fault simulation, fault detection and redundancy, fault equivalence and fault dominance. Stuck-at faults, bridging faults, transistor faults, delay faults etc. Fault detection using Boolean Difference, Path Sensitization. Fault Collapsing

Unit III

Test generation for combinational & sequential circuits: D-algorithm, PODEM, SPOOF. Automatic Test Pattern Generation. Primitive and Propagation Cubes. Fanout Oriented Test Generation. Controllability and Observability. Testing of sequential circuits as iterative combinational circuits, state table verification, random testing.

Unit IV

Design for testability: Ad-hoc methods, Full scan & Partial scan design. Boundary scans. Testability analysis.

Unit V

Built-in self-test & IDDQ testing: RAM BIST, Logic BIST Random and weighted random pattern testability BIST Pattern generator and response analyzer Scan-based BIST architecture Test point insertion for improving random testability. IDDQ testing, IDDQ test patterns, IDDQ measurement Case studies, Design for IDDQ testability

Text/Reference

1. Parag K. Lala, *Fault Tolerant and Fault Testable Hardware Design*, BS Publication.
2. N. Weste and K. Eshraghian, *Principles of CMOS VLSI design,* Addison-Wesley.

MEVD – 204 Micro Electronics

Unit I

Review of quantum mechanics theory. Motion of electron in a periodic lattice. Band theory of solids, effective mass, holes.

Unit II

Statistics of carriers in semiconductors. Lifetime and recombination theory. Boltzmann transports equation. Carrier transport in semiconductors, including high field effect.

Unit III

P-N junction theory. Excess currents and breakdown in p-n junctions. Bipolar transistors. Ebers-Moll and small signal models. Switching characteristics. Nonuniformly doped transistors. High current and high frequency effects.

Text/References

1. J.L. Moll, *Physics of Semiconductors,* McGraw Hill
2. F.Y. Wang, *Introduction to Solid State Electronics,* North Holland.
3. S.M. Sze, *Physics of Semiconductor Devices*, Weiley Easter.
4. D.J. Roulston, *Dipolar Semiconductors Devices*, McGraw Hill
5. R.L. Pritchnard, *Electrical Characteristics of Transistors*, McGraw Hill

MEVD – 205 Embedded Computing System Design

Unit-I

Introduction: Embedding Complex Systems and Microprocessors, Embedded System Design Process, Designing Hardware and Software Components, Formalization of System Design, Application Examples.

Unit-II

Instruction Sets: Assembly Language, ARM processor and memory organization. Data Operations and Control of Flow. SHARC Processor, Memory organization, Data Operations and flow control, Parallelism within the instructions.

Unit-III

CPUs: Performance, Power Dissipation, Design Example, Data Compression. CPU Bus Protocols in ARM, Design, Development and Debugging.

Unit-IV

Program design and Analysis: Program Design, Models of Program, Assembling, Linking, Compiling, Analysis and optimization of the Program Size and Execution times. Design Example: Software Modem.

Unit-V

System Design Techniques: Design Methodologies, Requirement Analysis, Specifications, System Analysis, quality Assurance, Two Design Examples in Networking and Internet Enabled Systems and Automobile Applications.

Text/References

1. Wayne Wolf, *Computers as Components,* Harcourt India Private Ltd.