Microprocessors & Microcontrollers
: Arm Cortex M0+
(Using RP2040)

ESM_16

Logical, Shift and Rotate Instructions

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Focus

- **Logical** instructions
- **Shift** and **Rotate** instructions
- Demo of **Asm** program

Ref:
Ref3_ARM-Cortex-M0+ Technical Reference Manual.pdf
Ref4_ARM-Cortex-M0+ Devices Generic User Guide.pdf

Logical Instructions

Technical Reference Manual of Cortex-M0+
(Ref 3) - Logical

Page: 27/51

Table 3-1 Cortex-M0+ instruction summary (continued)

Operation	Description	Assembler	Cycles
Logical	AND	ANDS Rd, Rd, Rm	1
	Exclusive OR	EORS Rd, Rd, Rm	1
	OR	ORRS Rd, Rd, Rm	1
	Bit clear	BICS Rd, Rd, Rm	1
	Move NOT	MVNS Rd, Rm	1
	AND test	TST Rn, Rm	1

Note: Do not add the **S suffix** to the instructions
It **is not supported** on **RP2040** only without S suffix.
It is not supported in **Thumb 16** mode.

- The AND, EOR, and ORR instructions perform bitwise AND, exclusive OR, and inclusive OR operations on the values in Rd and Rm.
- The BIC instruction performs an AND operation on the bits in Rd with the logical negation of the corresponding bits in the value of Rm.
- In these instructions, Rd, Rn, and Rm must only specify R0-R7.
- These instructions only update the N and Z flags according to the result and do not affect the C or V flag.

Shift and Rotate Instructions

Technical Reference Manual of Cortex-M0+
(Ref 3) – Shift and Rotate

Page: 27/51

Table 3-1 Cortex-M0+ instruction summary (continued)

Operation	Description	Assembler	Cycles
Shift	Logical shift left by immediate	LSLS Rd, Rm, #<shift>	1
	Logical shift left by register	LSLS Rd, Rd, Rs	1
	Logical shift right by immediate	LSRS Rd, Rm, #<shift>	1
	Logical shift right by register	LSRS Rd, Rd, Rs	1
	Arithmetic shift right	ASRS Rd, Rm, #<shift>	1
	Arithmetic shift right by register	ASRS Rd, Rd, Rs	1
Rotate	Rotate right by register	RORS Rd, Rd, Rs	1

Note: Do not add the **S suffix** to the instructions
It **is not supported** on **RP2040** only without S suffix.
It is not supported in **Thumb 16** mode.

- ASR, LSL, LSR, and ROR perform an arithmetic-shift-left, logical-shift-left, logical-shift-right or a right-rotation of the bits in the register **Rm** by the number of places specified by the immediate **imm** or the value in the least-significant byte of the register specified by **Rs**.
- In these instructions, Rd, Rm, and Rs must only specify R0-R7.
- For non-immediate instructions, Rd and Rs must specify the same register.

Demo of Asm Program

prog_lec_2_4_2.ino and main_asm.S

Summary

- **Logical** instructions
- **Shift** and **Rotate** instructions
- Demo of **Asm** program

Ref: Ref3_ARM-Cortex-M0+ Technical Reference Manual.pdf