

AIM: Design and Implementation of 2nd and 4th order I.P Butterworth Filters
APPARATUS REQUIRED:

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1. Breadboard with components of desired values (IC 741-2No's, Resistors and Capacitors)
 2. RC Oscillator (1 No)
 3. DC Dual transistor power supply (0-35V)
 4. CRO

OTHER ACCESSORIES:

Connecting wires and probes.

THEORY:

THEORY: Butter Worth filter is one of the most commonly used practical filters that approximate the ideal response. The key characteristics of Butter Worth filter is that it has flat pass band as well as stop band. For this reason it is sometimes called flat approximation for an ideal low pass filter is

$A_{ns} = 1/P_n(s)$(i)
 $P_n(s)$ is a polynomial in variable(s) with zeros in left hand plane.

DESIGN RULE: The typical second order B.F. transfer function is of the form.

$$\frac{A_v(s)}{A_v(0)} = \frac{1}{(s/\omega_0)^2 + 2K(s/\omega_0) + 1} \quad \text{.....(ii)}$$

Where $\omega_0 2f_0$ is the high frequency 3dB point.

First order filter

$$\frac{A_v(s)}{A_v(0)} = \frac{1}{(s/\omega_0) + 1}. \quad \text{(iii)}$$

First order and second order filter section have been shown in figure.(iv)

From the above equation $\omega_0 = 1/RC$, $2K = 3 - A_v(0)$ or $A_v(0) = 3 - 2K$.

Normalized Order (n)	Butterworth Polynomial Factors of polynomial
1	$(s+1)$
2	$s^2 + 1.414s + 1$
3	$(s+1)(s^2 + s + 1)$
4	$(s^2 + 0.765s + 1)(s^2 + 1.848s + 1)$

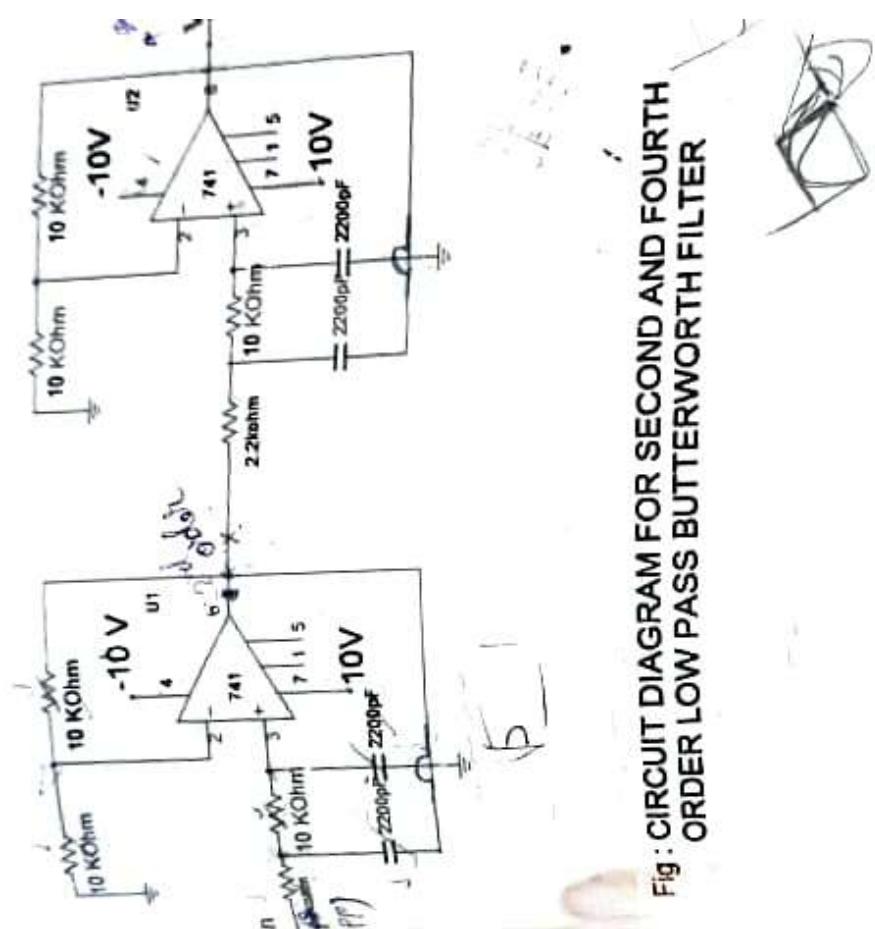


Fig : CIRCUIT DIAGRAM FOR SECOND AND FOURTH ORDER LOW PASS BUTTERWORTH FILTER

PROCEDURE:

1. Connect the circuit as shown in the figure.
2. Connect the power supply to the circuit at pin no. 4 and 7 of IC 741.
3. Vary the frequency of RC Oscillator.
4. Measure the output voltage at pin no. 6 on CRO for different frequencies and calculate gain in dB.

OBSERVATION TABLE:

S. No	FREQUENCY f(Hz)	$\log_{10}(f)$	Amplitude Peak to peak V_{out} (V)	$A = \frac{V_{out}}{V_{in}}$	Gain in dB $20 \log_{10}(A)$
-	-	-	-	-	-

RESULT:

CONCLUSION:

PRECAUTIONS:

2. All the connections should be perfect.
3. At the time of taking reading from the measuring equipments the errors of reading must be avoided.
4. DC supply should not exceed 12V.

REFERENCES:

1. Pamphlet to be supplied.
2. Op-Amps and Linear Integrated Circuits by Ramakant A. Gayakwad
3. Communication system by S. Haykin, IInd Edition.

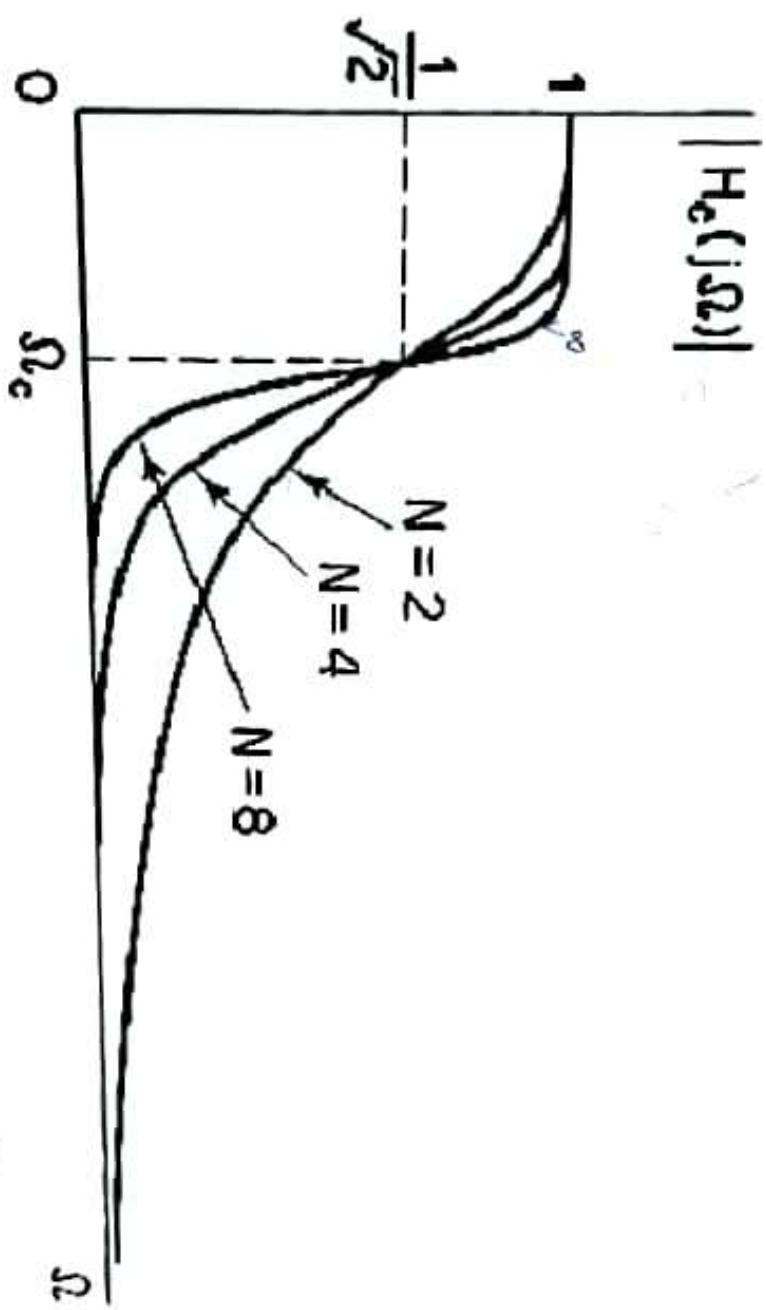


Fig. : Response of Butterworth low pass filter

Exp - 4

~~11~~ 2nd order

$$V_{IN} = 2V$$

No.	Frequency	Amplitude (Vout)
1	100.8 Hz	4V
2	500 Hz	4V
3	1000 Hz	4V
4	3 kHz	4V
5	6 kHz	4V
6	8.7 kHz	4V
7	9.3 kHz	3.6V
8	9.8 kHz	3.6 3.2V
9	10.43 kHz	3.6 2.8V
10	11.22 kHz	2.4V
11	11.98 kHz	2.0V
12	13.15 kHz	1.6V
13	14.35 kHz	1.2V
14	17.19 kHz	0.8V

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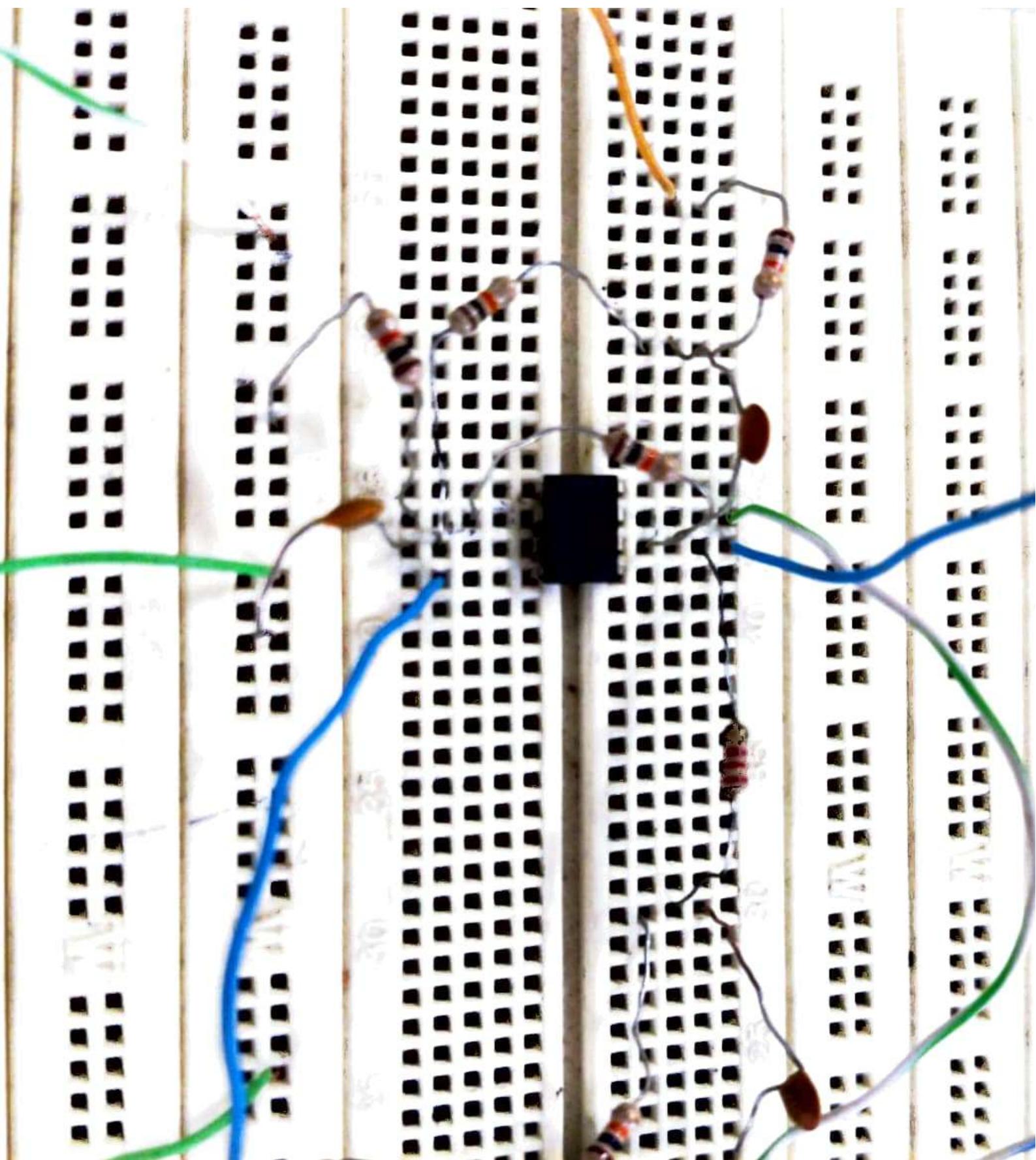
15	25.75 kHz	0.4V
16	29.23 kHz	0.2V
17	50 kHz	0V
18	olden, $V_o = 2V$	

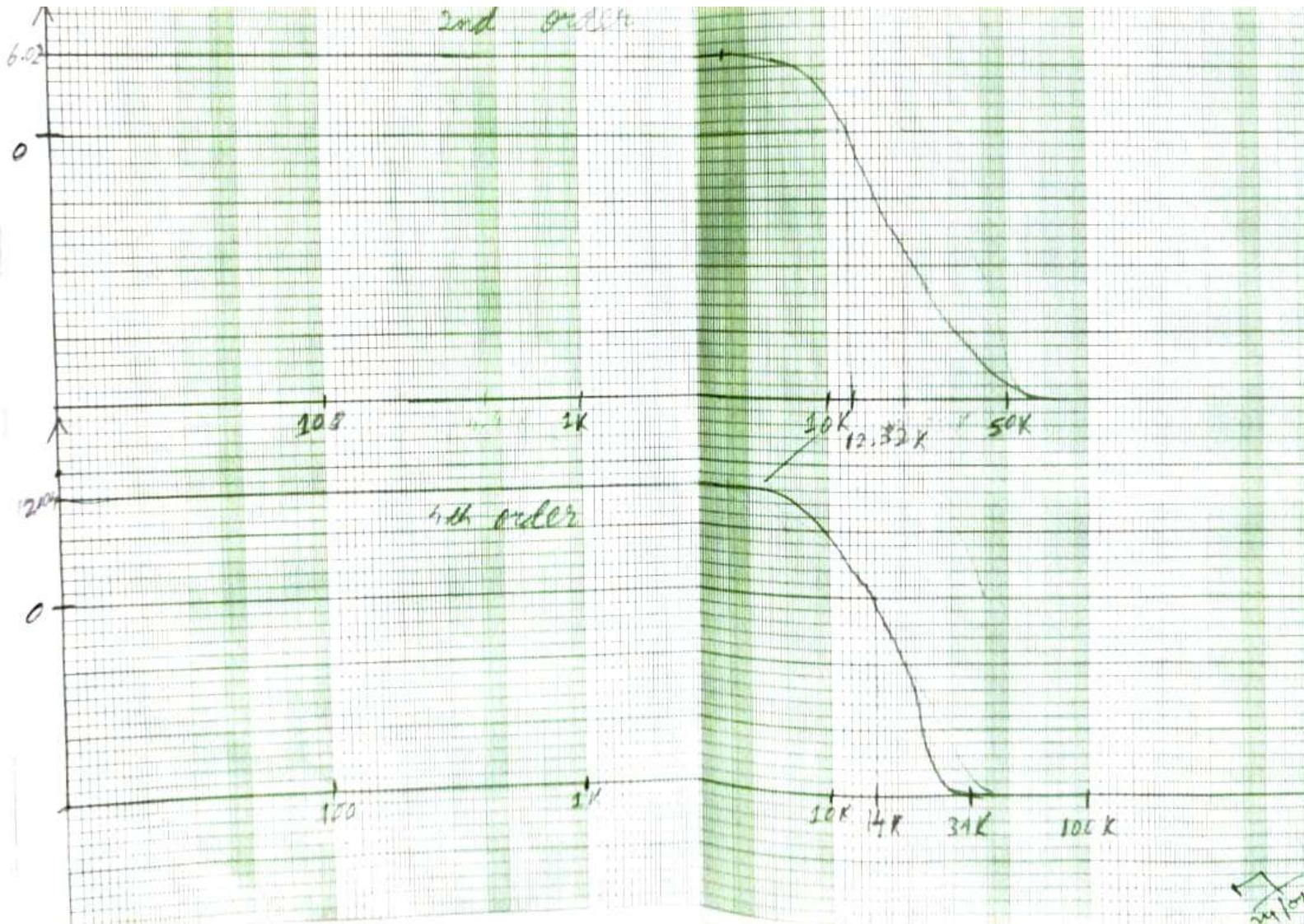
Sl.No.	Frequency	Amplitude (Next)
1	100 Hz	8V
2	500 Hz	8V
3	1000 Hz	8V
4	3 kHz	8V
5	6 kHz	8V
6	6.10 kHz	8V
7	7.6 kHz	7.6V
8	9.2 kHz	7.2V
9	8.4 kHz	6.8V
10	8.5 kHz	6.4V

Conclusion:
Bandwidth decreased with increase in
order.

~~2nd Bandwidth \rightarrow 10.4 kHz~~

~~3rd Bandwidth \rightarrow 8.6 kHz~~





AIM: Signal sampling and reconstruction using DCL 01 Falcon kit and investigation of

- i. The effect of sampling frequency variation
- ii. Change of duty cycle
- iii. Output at Second Order LP Butterworth filter
- iv. Output at Fourth order LP Butterworth filter

THEORY:

The kit is used to study Analog Signal Sampling and its reconstruction. It basically consists of functional blocks, namely Function generator, Sampling Control Logic, Clock section, Sampling Circuitry and Filter Section.

FUNCTION GENERATOR:

This Block generates two sine wave signals of 1KHz clock to the shift register. The serial to parallel shift register with the resistive ladder network at the output generates 1KHz and 2KHz sine waves respectively by the serial shift operation. The R-C active filter suppresses the ripple and smoothens the sine wave. The unity gain amplifier buffer takes care of the impedance matching between sine wave generation and sampling circuit.

SAMPLING CONTROL LOGIC:

This unit generates two main signals used in the study of Sampling theorem, namely the analog signals (5V pp, frequency 1KHz and 2KHz) & sampling signal of frequency 2KHz, 4KHz, 8KHz, 16Khz, 32Khz, and 64Khz.

The 6.4 MHz Crystal Oscillator generates the 6.4 MHz clock. The decade counter divides the frequency by 10 and the ripple counter generates the basic sampling frequencies from 2Khz to 64Khz and the other control frequencies.

From among the various available sampling frequencies, required sampling frequency is selected by using the frequency selectable switch. The selected sampling frequency is indicated by means of corresponding LED.

CLOCK SECTION:

This section facilitates the user to have his choice of external or internal clock feeding to the sampling section by using a switch (SW4).

SAMPLING CIRCUITRY:

The unit has three parts namely, Natural Sampling Circuit, Flat top Sampling Circuit, and Sampling and Hold Circuit.

The Natural sampling section takes sine wave as analog input and samples the analog input at the rate equal to the sampling signal.

For sample and hold circuit, the output is taken across a capacitor, which holds the level of the samples until the next sample arrives.

For flat top sampling clock used is inverted to that of sample & hold circuit. Output of flat top sampling circuit is pulses with flat top and top corresponds to the level of analog signal at the instant of rising edge of the clock signal.

FILTER SECTION:

Two types of Filters are provided on board, viz., 2nd Order and 4th Order Low Pass Butterworth Filter.

EQUIPMENTS:

Experimenter kit DCL -01.

Connecting Chords.

Power supply.

20 MHz Dual trace Oscilloscope.

NOTE: KEEP ALL THE SWITCH FAULTS (EXCEPT SWITCH 1) IN OFF POSITION.

1) NATURAL SAMPLING AND ITS RECONSTRUCTION.

1KHz
1ms

PROCEDURE:

1. Refer to the Block Diagram (Fig. 1.1) & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit DCL-01 & switch it on.
3. Connect the **1KHz**, 5Vpp Sine wave signal, generated onboard, to the **BUF IN** post of the BUFFER and **BUF OUT** post of the BUFFER to the **IN** post of the Natural Sampling block by means of the Connecting chords provided.
4. Connect the sampling frequency clock in the internal mode INT CLK using switch (**SW4**).
5. Using clock selector switch (**S1**) select **8KHz** sampling frequency.
6. Using switch (**SW2**) select **50%** duty cycle.
7. Connect the **OUT** post of the Natural Sampling blocks to the input **IN1** post of the 2nd Order Low Pass Butterworth Filter and take necessary observation as mentioned below. (Fig. 1.4)
8. Repeat the procedure for the 2 KHz sine wave signal as input.

OBSERVATIONS:

Observe the following waveforms in order for every setting and plot it on the paper.

- a. 1 KHz analog Input waveform.
- b. Sampling frequency waveform.
- c. Natural Sampling Signal and its corresponding reconstructed output of 2nd Order Low Pass Butterworth Filter.

SWITCH FAULTS:

Note: Keep the connection as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

1. Put switch 6 of SF2 in switch fault section to ON position. This will open B1 bit from the B input 94-bit DIP switch output) of the comparator. This introduces the faults in duty cycle section. With effect change in duty cycle will not be observed for (10%, 40%, 50%, 80% and 90% settings).
2. Put switch 7 of SF2 in switch fault section to ON position. This will open the bypass capacitor of the 2nd order low pass butterworth filter, which results in the induction of ripples at the filter output.
3. Put switch 8 of SF2 in switch fault section to ON position. This removes the capacitor (c6) used in the generation of 1KHz sine wave. Which makes the sine wave signal very distorted. The Observation can be made on this signal by changing the sampling frequencies and the duty cycle.

2) SAMPLE AND HOLD AND ITS RECONSTRUCTION.

PROCEDURE:

1. Refer to the Block Diagram (Fig. 1.2) & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it ON.
3. Connect the **1 KHz**, 5Vpp sine wave signal, generated onboard, to the **BUF IN** post of the BUFFER and the **BUF OUT** post of the BUFFER to the **IN** post of the sample and hold Block by means of the Connecting chords provide.
4. Connect the sampling frequency clock in the internal mode **INT CLK** using switch (**SW4**).
5. Using clock selector switch select **8 KHz** sampling frequency.
6. Using switch **SW2** select **50%** duty cycle.
7. Connect the **OUT** post of the Sample and Hold block to the input **IN 1** post of the 2nd Order Low Pass Butterworth Filter and take necessary observation as mentioned below. (Fig. 1.5).
8. Repeat the procedure for the 2 KHz sine wave signal as input.

OBSERVATIONS:

Observe the following waveforms in order for every setting and plot it on the paper.

- a. 1KHz analog Input waveform.
- b. Sampling frequency waveform.

- c. Sample and hold signal and its corresponding reconstructed output of 2nd order Low Pass Butterworth Filter.

SWITCH FAULTS:

Note: Keep the connections as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

By changing the position of the switch in the SF1 you are changing the Capacitance value of the Sample and Hold circuit, you can find the variation accordingly at the output of the S/H circuit.

1. Put Switch 1 so **SF1** in switch fault section to **ON** position, the capacitor C11 (10nF) is at the output of sample and hold circuit.
2. Put Switch 2 so **SF1** in switch fault section to **ON** position, the capacitor C10 (1.5pF) is at the output of sample and hold circuit.
3. Put Switch 3 so **SF1** in switch fault section to **ON** position, the capacitor C9 (0.22μF) is at the output of sample and hold circuit.
4. Put Switch 6 so **SF1** in switch fault section to **ON** position, this will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle will not be observed for (10%, 40%, 50%, 80% and 90% settings).
5. Put Switch 7 so **SF1** in switch fault section to **ON** position. This will open the bypass capacitor of the 2nd order low pass butterworth filter, which result in the induction of ripples at the filter output.
6. Put switch 8 of **SF2** in switch Fault section to **ON** position. This Removes the capacitor (C6) used in the generation of 1 KHz sine wave. Which makes the sine wave signal very distorted. The Observed can be made on this signal by changing the sampling frequencies and the duty cycle.

3) FLAT TOP SAMPLING AND ITS RECONSTRUCTION:

PROCEDURE:

1. Refer to the Block Diagram (Fig. 1.3) & Carry out the following connections and switch settings
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
3. Connect the **1 KHz, 5Vpp** Sine wave signal, generated onboard to the **BUF IN** post of the Buffer and the **BUF OUT** post of the Buffer to the **IN** post of the Flat Top sampling block by means of the Connecting chords provided.
4. Connect the sampling frequency clock in the internal mode **INT CLK** using switch (**SW4**).
5. Using clock selector switch **S1** select **8KHz** sampling frequency.
6. Using switch **SW2** select **50%** duty cycle.
7. Connect the **OUT** post of the Flat top sampling block to the input **IN 1** of the 2nd Order Low Pass Butterworth Filter and take necessary observation as mentioned below. (Fig. 1.6).
8. Repeat the procedure for the 2 KHz sine wave signal as input.

OBSERVATION:

Observe the following waveforms in order for every setting and plot it on the paper.

- a. 1KHz Analog Input waveform.
- b. Sampling frequency waveform.
- c. Flat Top signal and its corresponding reconstructed output of 2nd order Low Pass Butterworth Filter.

In this manner we observe all the three types of sampling, which can be compared with the waveforms at the end of this experiment.

We observe that, during the ON time of Sampling frequency the analog signal is transmitted. During the OFF time, the sample output signal drops towards zero. Whereas for Sampled and Hold output, the signal maintains the voltage level i.e. the sample is held at least sampled value until next sample arrives. For flat top sampling first switching portion from sample & hold signal is dropped and next switching portion is taken as pulse output, i.e. only hold portion from sample & hold signal is taken at flat top sampling output.

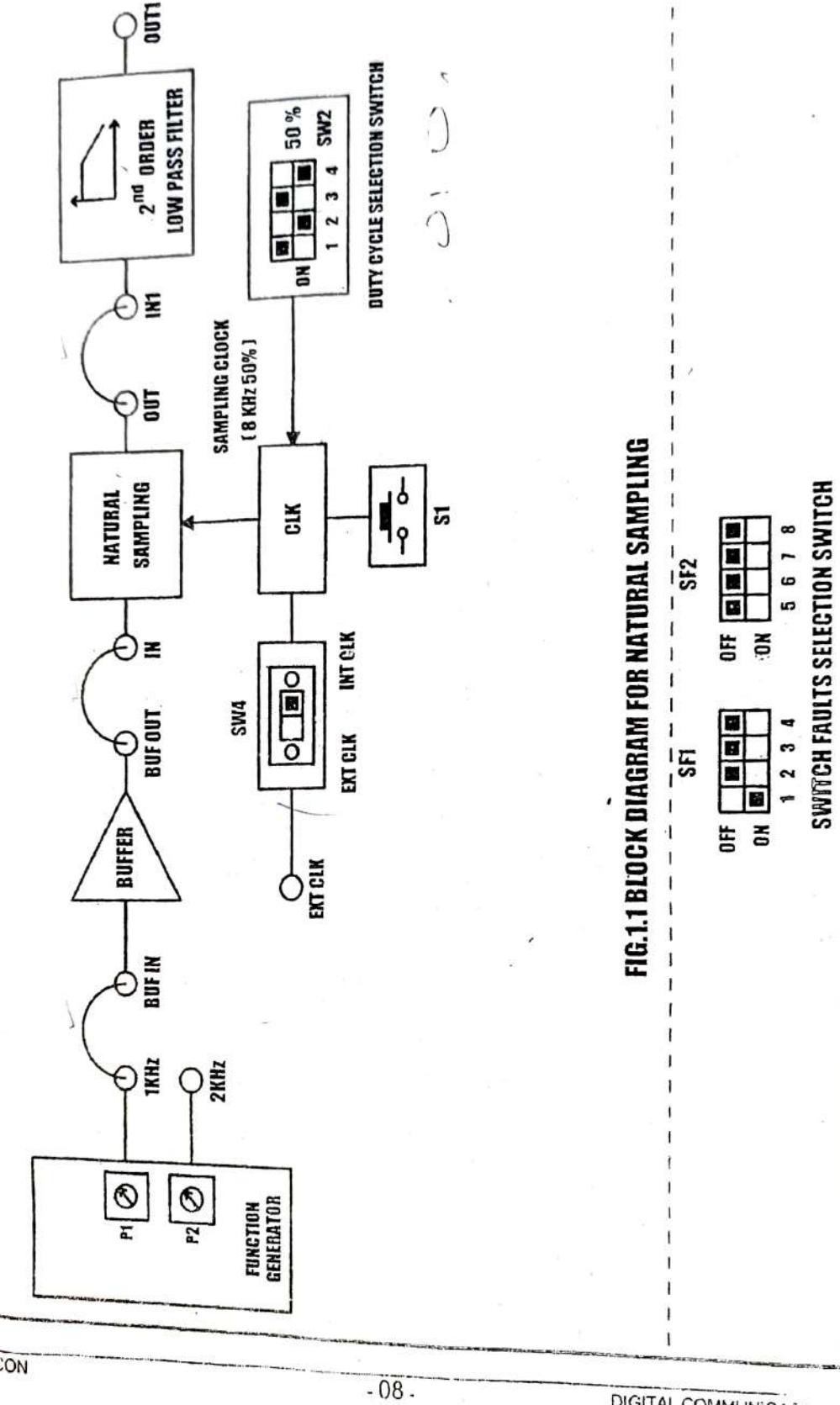
SWITCH FAULTS:

Note: Keep the connections as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

1. Put switch 5 of SF2 in switch Fault section to ON position. This will open the capacitor C12 of the Flat Top Sampling Circuit, which makes the Flat Top sample output appears to be slant.
2. Put switch 6 of SF2 in switch Fault section to ON position. This will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle will not be observed for (10%, 40%, 50%, 80% and 90% settings).
3. Put switch 7 of SF2 in switch Fault section to ON position. This will open the bypass capacitor of the 2nd order low pass butterworth filter, which results in the induction of ripples at the filter output.
4. Put switch 8 of SF2 in switch Fault section to On position. This Removes the Capacitor (C6) used in the generation of 1KHz sine wave. Which makes the sine wave signal very distorted. The observation can be made on this signal by changing the sampling frequencies and the duty cycle.

CONCLUSION:

Comparing the reconstruction output of 2nd order Low Pass Butterwirth Filter for all the three types of sampling, it is observed that the output of the sample and hold is the best as compared to the output of natural sampling and the output of the flat top sampling.



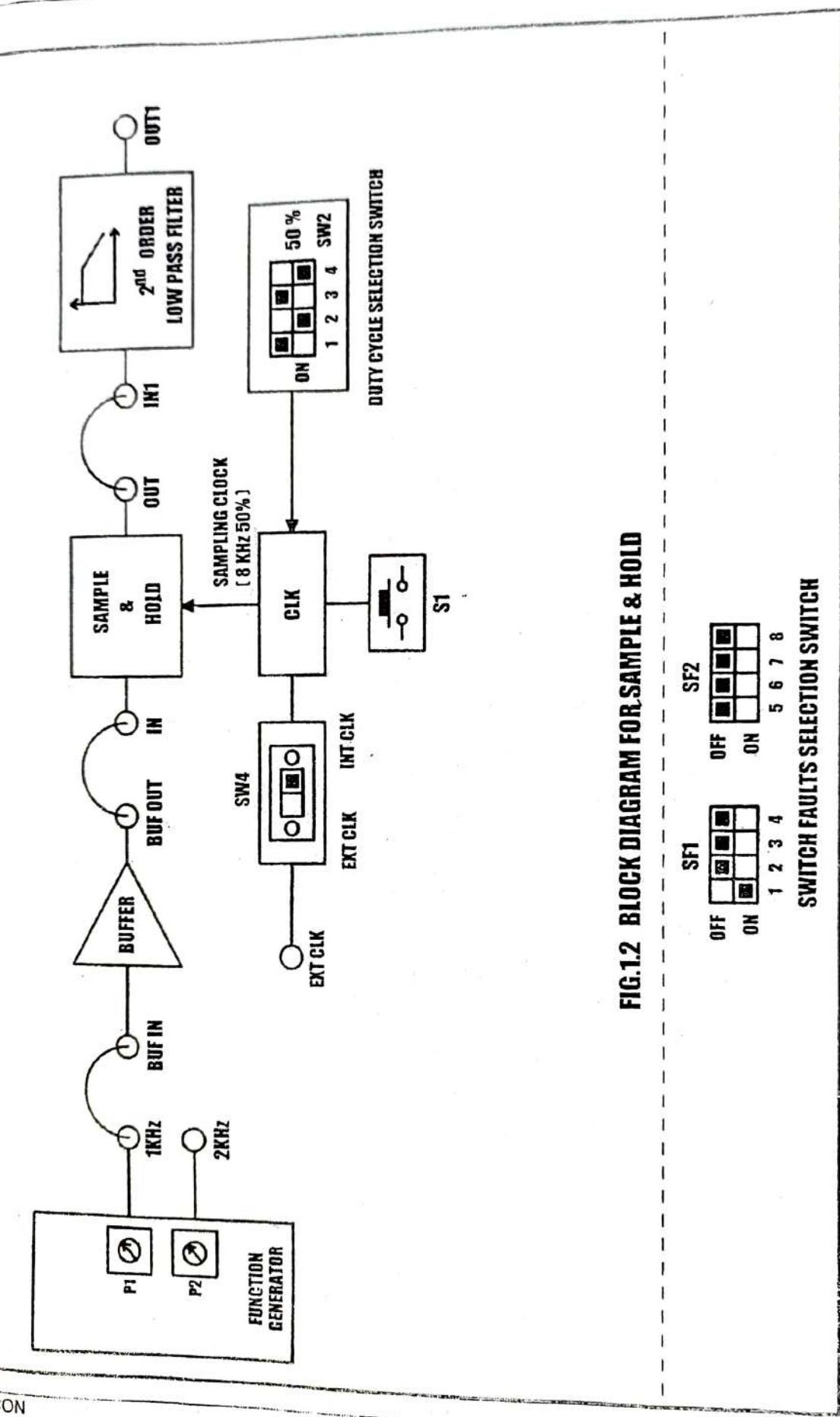
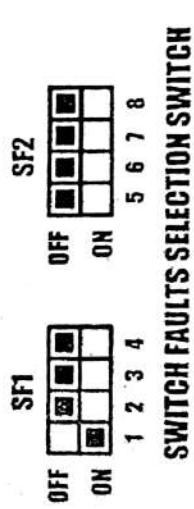


FIG.1.2 BLOCK DIAGRAM FOR SAMPLE & HOLD



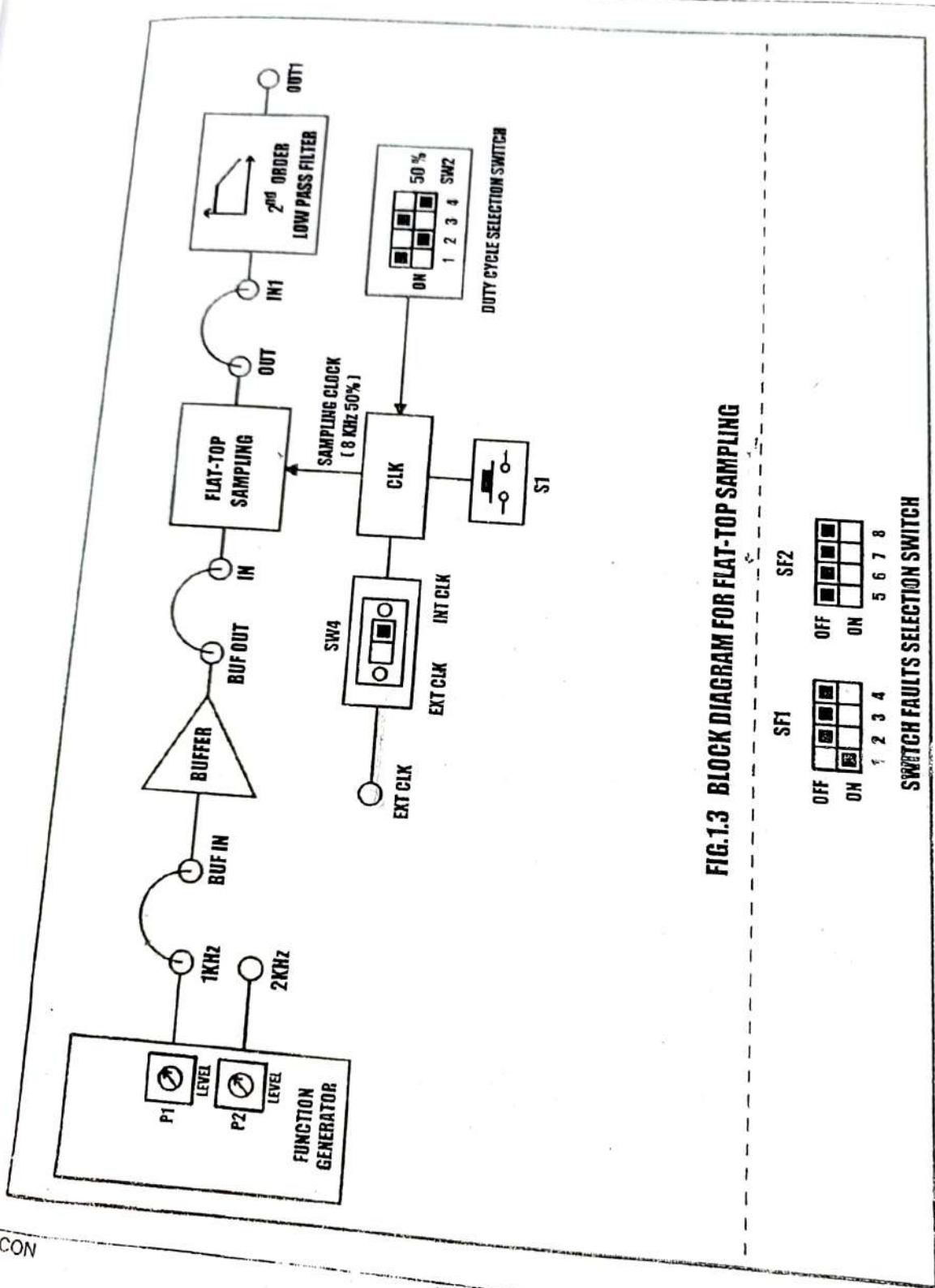


FIG.1.3 BLOCK DIAGRAM FOR FLAT-TOP SAMPLING

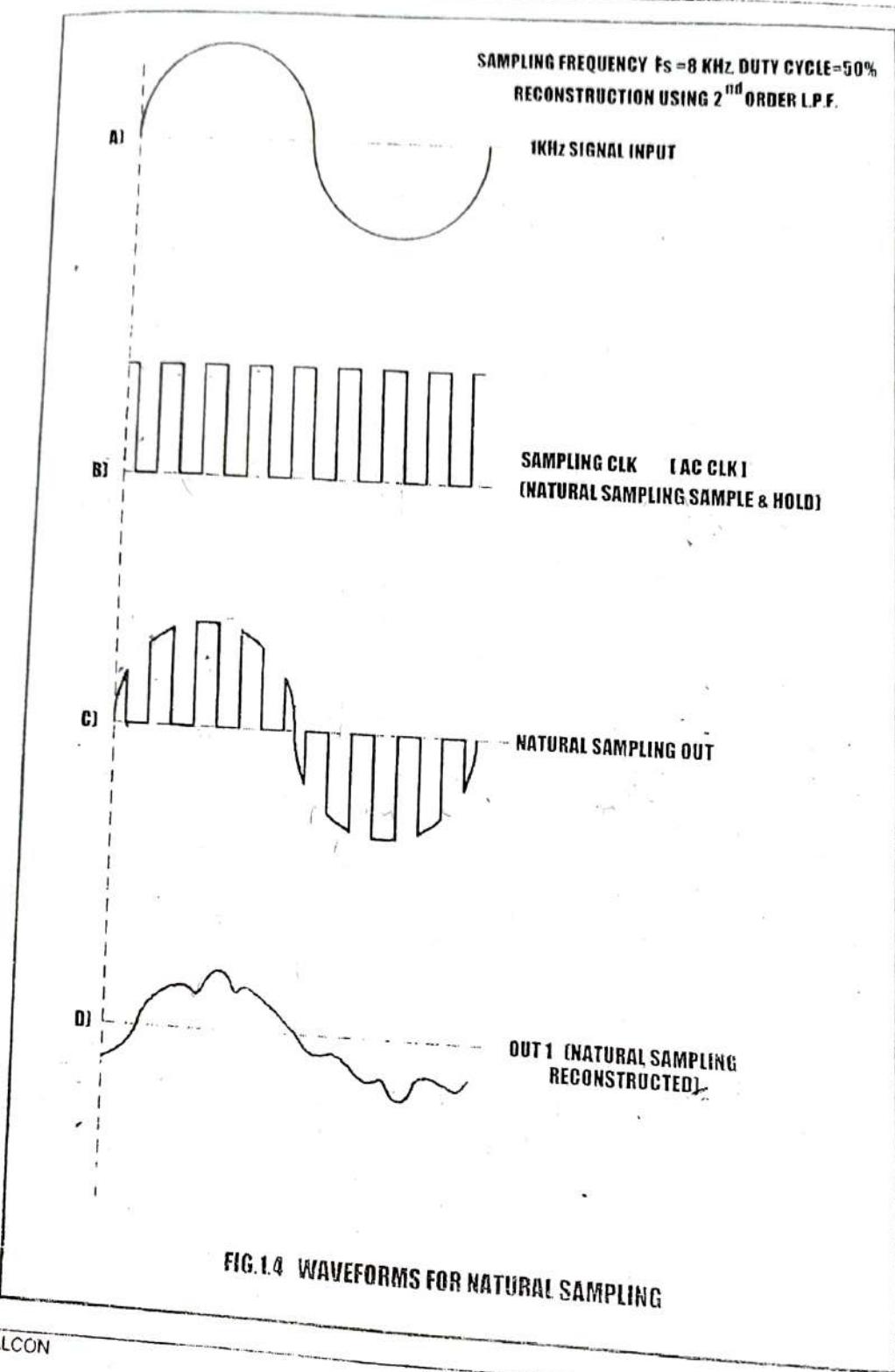


FIG.1.4 WAVEFORMS FOR NATURAL SAMPLING

ANALOG SIGNAL SAMPLE & HOLD RECONSTRUCTION

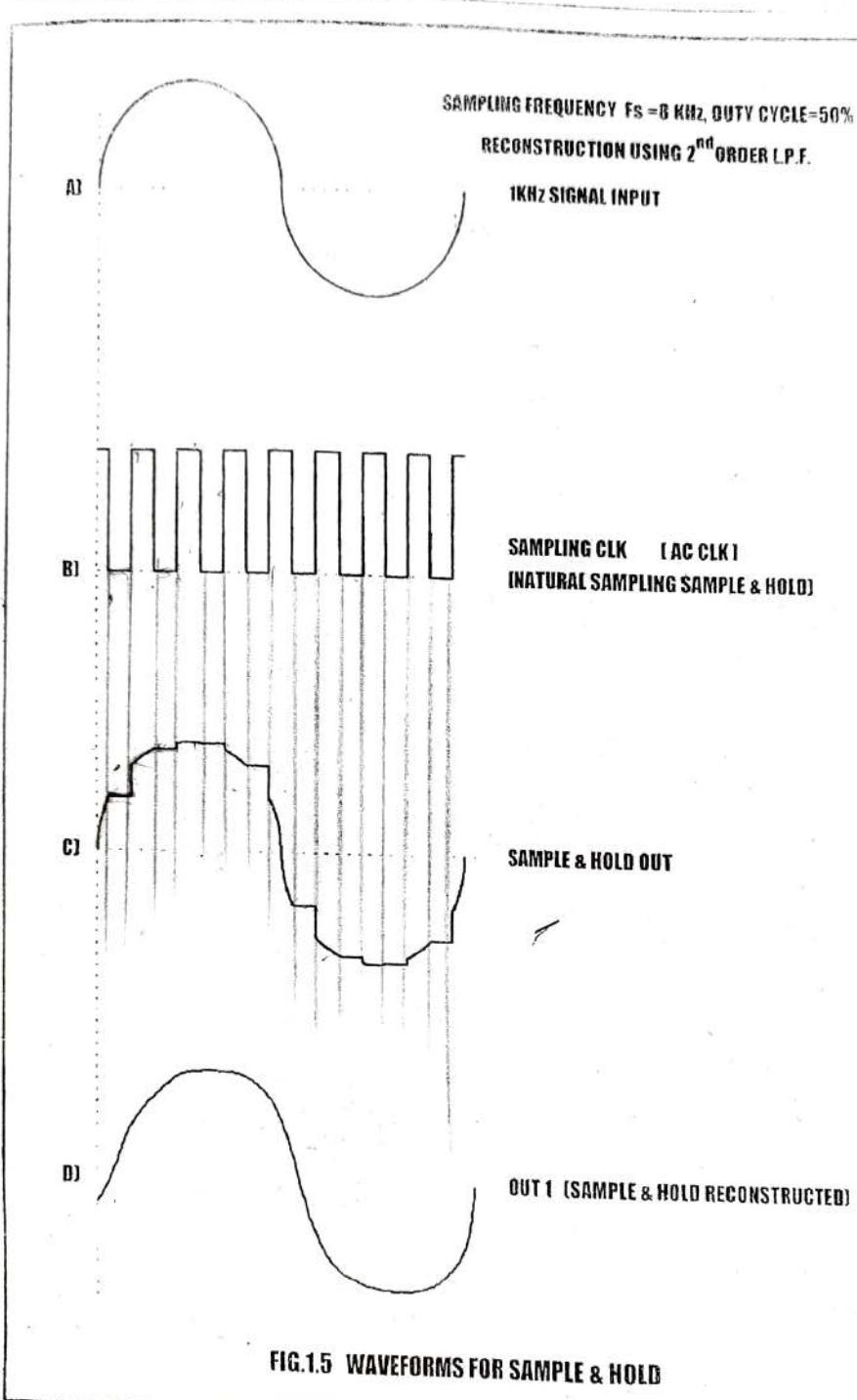


FIG.1.5 WAVEFORMS FOR SAMPLE & HOLD

SAMPLING FREQUENCY $F_s = 8 \text{ KHz}$, DUTY CYCLE=50%
RECONSTRUCTION USING 2nd ORDER LPF

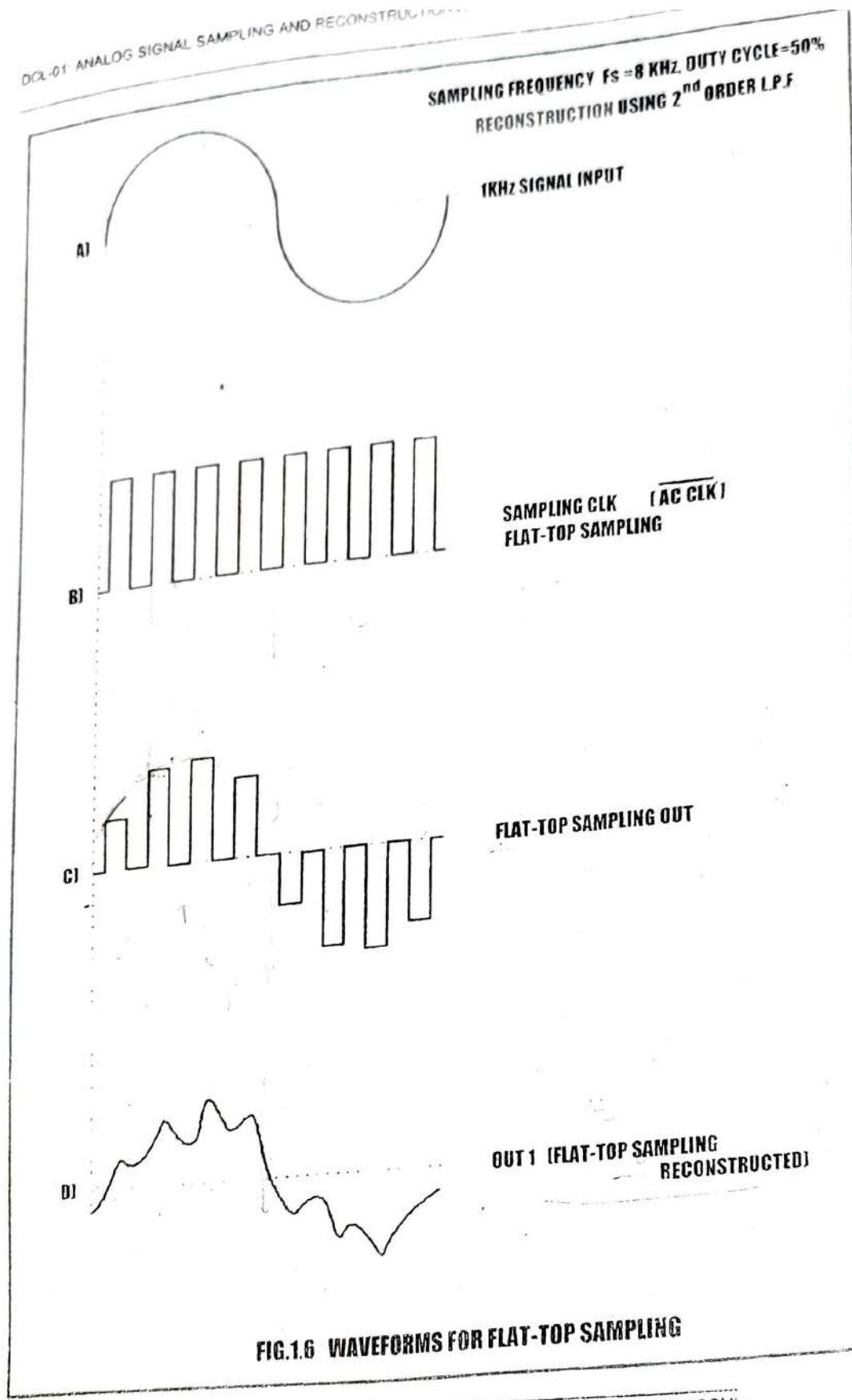


FIG.1.6 WAVEFORMS FOR FLAT-TOP SAMPLING

AIM: Signal sampling and reconstruction using DCL 01 Falcon kit and investigation of

- i. The effect of sampling frequency variation
- ii. Change of duty cycle
- iii. Output at Second Order LP Butterworth filter
- iv. Output at Fourth order LP Butterworth filter

THEORY:

The kit is used to study Analog Signal Sampling and its reconstruction. It basically consists of functional blocks, namely Function generator, Sampling Control Logic, Clock section, Sampling Circuitry and Filter Section.

FUNCTION GENERATOR:

This Block generates two sine wave signals of 1KHz clock to the shift register. The serial to parallel shift register with the resistive ladder network at the output generates 1KHz and 2KHz sine waves respectively by the serial shift operation. The R-C active filter suppresses the ripple and smoothens the sine wave. The unity gain amplifier buffer takes care of the impedance matching between sine wave generation and sampling circuit.

SAMPLING CONTROL LOGIC:

This unit generates two main signals used in the study of Sampling theorem, namely the analog signals (5V pp, frequency 1KHz and 2KHz) & sampling signal of frequency 2KHz, 4KHz, 8KHz, 16Khz, 32Khz, and 64Khz.

The 6.4 MHz Crystal Oscillator generates the 6.4 MHz clock. The decade counter divides the frequency by 10 and the ripple counter generates the basic sampling frequencies from 2Khz to 64Khz and the other control frequencies.

From among the various available sampling frequencies, required sampling frequency is selected by using the frequency selectable switch. The selected sampling frequency is indicated by means of corresponding LED.

CLOCK SECTION:

This section facilitates the user to have his choice of external or internal clock feeding to the sampling section by using a switch (SW4).

SAMPLING CIRCUITRY:

The unit has three parts namely, Natural Sampling Circuit, Flat top Sampling Circuit, and Sampling and Hold Circuit.

The Natural sampling section takes sine wave as analog input and samples the analog input at the rate equal to the sampling signal.

For sample and hold circuit, the output is taken across a capacitor, which holds the level of the samples until the next sample arrives.

For flat top sampling clock used is inverted to that of sample & hold circuit. Output of flat top sampling circuit is pulses with flat top and top corresponds to the level of analog signal at the instant of rising edge of the clock signal.

FILTER SECTION:

Two types of Filters are provided on board, viz., 2nd Order and 4th Order Low Pass Butterworth Filter.

EQUIPMENTS:

Experimenter kit DCL -01.

Connecting Chords.

Power supply.

20 MHz Dual trace Oscilloscope.

NOTE: KEEP ALL THE SWITCH FAULTS (EXCEPT SWITCH 1) IN OFF POSITION.

1) NATURAL SAMPLING AND ITS RECONSTRUCTION.

1KHz
1ms

PROCEDURE:

1. Refer to the Block Diagram (Fig. 1.1) & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit DCL-01 & switch it on.
3. Connect the **1KHz**, 5Vpp Sine wave signal, generated onboard, to the **BUF IN** post of the BUFFER and **BUF OUT** post of the BUFFER to the **IN** post of the Natural Sampling block by means of the Connecting chords provided.
4. Connect the sampling frequency clock in the internal mode INT CLK using switch (**SW4**).
5. Using clock selector switch (**S1**) select **8KHz** sampling frequency.
6. Using switch (**SW2**) select **50%** duty cycle.
7. Connect the **OUT** post of the Natural Sampling blocks to the input **IN1** post of the 2nd Order Low Pass Butterworth Filter and take necessary observation as mentioned below. (Fig. 1.4)
8. Repeat the procedure for the 2 KHz sine wave signal as input.

OBSERVATIONS:

Observe the following waveforms in order for every setting and plot it on the paper.

- a. 1 KHz analog Input waveform.
- b. Sampling frequency waveform.
- c. Natural Sampling Signal and its corresponding reconstructed output of 2nd Order Low Pass Butterworth Filter.

SWITCH FAULTS:

Note: Keep the connection as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

1. Put switch 6 of SF2 in switch fault section to ON position. This will open B1 bit from the B input 94-bit DIP switch output) of the comparator. This introduces the faults in duty cycle section. With effect change in duty cycle will not be observed for (10%, 40%, 50%, 80% and 90% settings).
2. Put switch 7 of SF2 in switch fault section to ON position. This will open the bypass capacitor of the 2nd order low pass butterworth filter, which results in the induction of ripples at the filter output.
3. Put switch 8 of SF2 in switch fault section to ON position. This removes the capacitor (c6) used in the generation of 1KHz sine wave. Which makes the sine wave signal very distorted. The Observation can be made on this signal by changing the sampling frequencies and the duty cycle.

2) SAMPLE AND HOLD AND ITS RECONSTRUCTION.

PROCEDURE:

1. Refer to the Block Diagram (Fig. 1.2) & Carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it ON.
3. Connect the **1 KHz**, 5Vpp sine wave signal, generated onboard, to the **BUF IN** post of the BUFFER and the **BUF OUT** post of the BUFFER to the **IN** post of the sample and hold Block by means of the Connecting chords provide.
4. Connect the sampling frequency clock in the internal mode **INT CLK** using switch (**SW4**).
5. Using clock selector switch select **8 KHz** sampling frequency.
6. Using switch **SW2** select **50%** duty cycle.
7. Connect the **OUT** post of the Sample and Hold block to the input **IN 1** post of the 2nd Order Low Pass Butterworth Filter and take necessary observation as mentioned below. (Fig. 1.5).
8. Repeat the procedure for the 2 KHz sine wave signal as input.

OBSERVATIONS:

Observe the following waveforms in order for every setting and plot it on the paper.

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1. Put Switch 1 so **SF1** in switch fault section to **ON** position, the capacitor C11 (10nF) is at the output of sample and hold circuit.
2. Put Switch 2 so **SF1** in switch fault section to **ON** position, the capacitor C10 (1.5pF) is at the output of sample and hold circuit.
3. Put Switch 3 so **SF1** in switch fault section to **ON** position, the capacitor C9 (0.22μF) is at the output of sample and hold circuit.
4. Put Switch 6 so **SF1** in switch fault section to **ON** position, this will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle will not be observed for (10%, 40%, 50%, 80% and 90% settings).
5. Put Switch 7 so **SF1** in switch fault section to **ON** position. This will open the bypass capacitor of the 2nd order low pass butterworth filter, which result in the induction of ripples at the filter output.
6. Put switch 8 of **SF2** in switch Fault section to **ON** position. This Removes the capacitor (C6) used in the generation of 1 KHz sine wave. Which makes the sine wave signal very distorted. The Observed can be made on this signal by changing the sampling frequencies and the duty cycle.

3) FLAT TOP SAMPLING AND ITS RECONSTRUCTION:

PROCEDURE:

1. Refer to the Block Diagram (Fig. 1.3) & Carry out the following connections and switch settings
2. Connect power supply in proper polarity to the kit **DCL-01** & switch it on.
3. Connect the **1 KHz, 5Vpp** Sine wave signal, generated onboard to the **BUF IN** post of the Buffer and the **BUF OUT** post of the Buffer to the **IN** post of the Flat Top sampling block by means of the Connecting chords provided.
4. Connect the sampling frequency clock in the internal mode **INT CLK** using switch (**SW4**).
5. Using clock selector switch **S1** select **8KHz** sampling frequency.
6. Using switch **SW2** select **50%** duty cycle.
7. Connect the **OUT** post of the Flat top sampling block to the input **IN 1** of the 2nd Order Low Pass Butterworth Filter and take necessary observation as mentioned below. (Fig. 1.6).
8. Repeat the procedure for the 2 KHz sine wave signal as input.

OBSERVATION:

Observe the following waveforms in order for every setting and plot it on the paper.

- a. 1KHz Analog Input waveform.
- b. Sampling frequency waveform.
- c. Flat Top signal and its corresponding reconstructed output of 2nd order Low Pass Butterworth Filter.

In this manner we observe all the three types of sampling, which can be compared with the waveforms at the end of this experiment.

We observe that, during the ON time of Sampling frequency the analog signal is transmitted. During the OFF time, the sample output signal drops towards zero. Whereas for Sampled and Hold output, the signal maintains the voltage level i.e. the sample is held at least sampled value until next sample arrives. For flat top sampling first switching portion from sample & hold signal is dropped and next switching portion is taken as pulse output, i.e. only hold portion from sample & hold signal is taken at flat top sampling output.

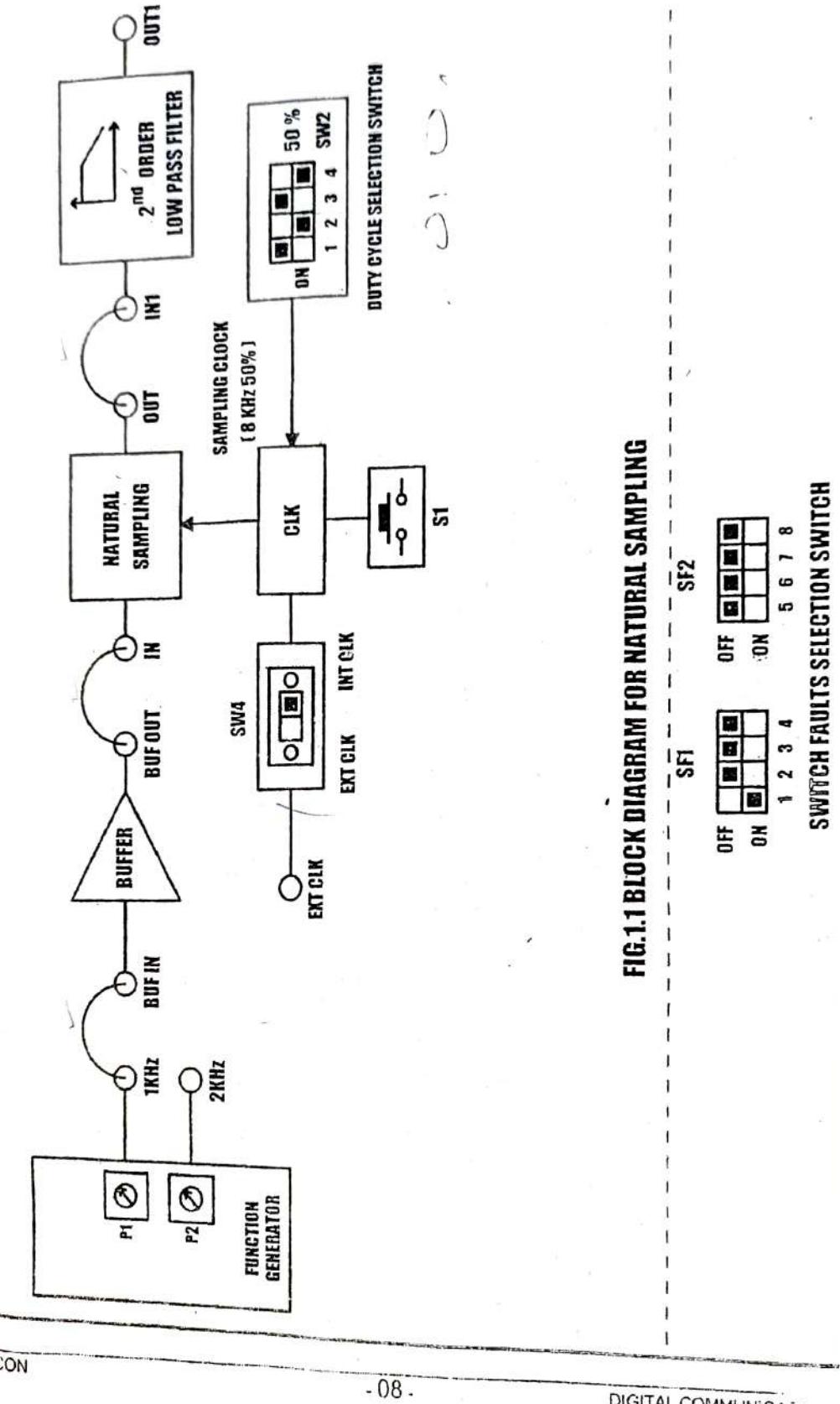
SWITCH FAULTS:

Note: Keep the connections as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

1. Put switch 5 of SF2 in switch Fault section to ON position. This will open the capacitor C12 of the Flat Top Sampling Circuit, which makes the Flat Top sample output appears to be slant.
2. Put switch 6 of SF2 in switch Fault section to ON position. This will open B1 bit from the B input (4-bit DIP switch output) of the comparator. This introduces the fault in duty cycle section. With effect, change in duty cycle will not be observed for (10%, 40%, 50%, 80% and 90% settings).
3. Put switch 7 of SF2 in switch Fault section to ON position. This will open the bypass capacitor of the 2nd order low pass butterworth filter, which results in the induction of ripples at the filter output.
4. Put switch 8 of SF2 in switch Fault section to On position. This Removes the Capacitor (C6) used in the generation of 1KHz sine wave. Which makes the sine wave signal very distorted. The observation can be made on this signal by changing the sampling frequencies and the duty cycle.

CONCLUSION:

Comparing the reconstruction output of 2nd order Low Pass Butterwirth Filter for all the three types of sampling, it is observed that the output of the sample and hold is the best as compared to the output of natural sampling and the output of the flat top sampling.



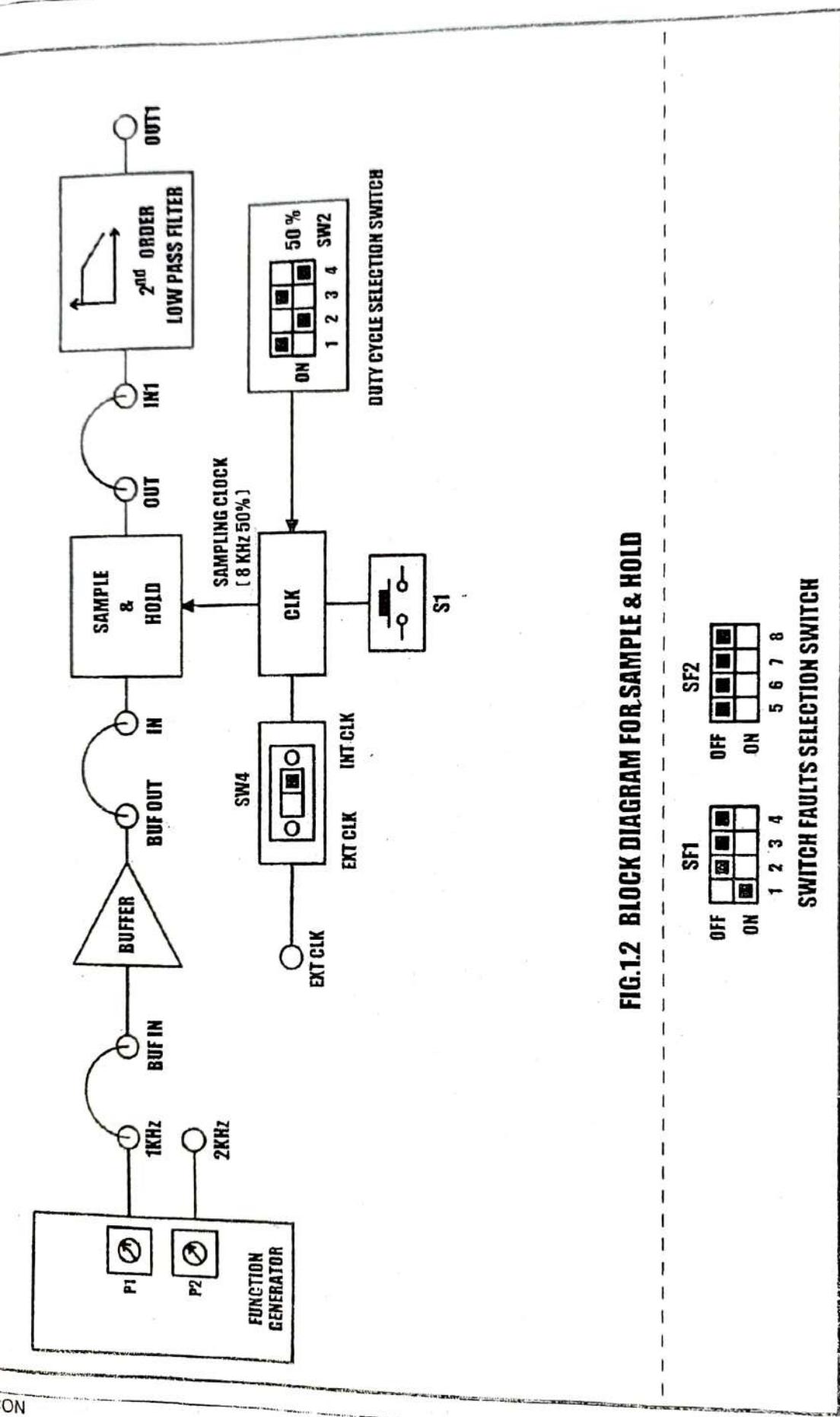
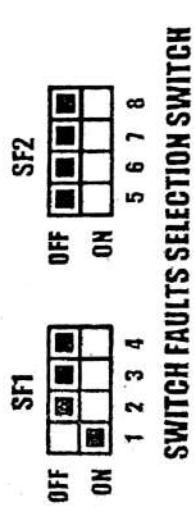


FIG.1.2 BLOCK DIAGRAM FOR SAMPLE & HOLD



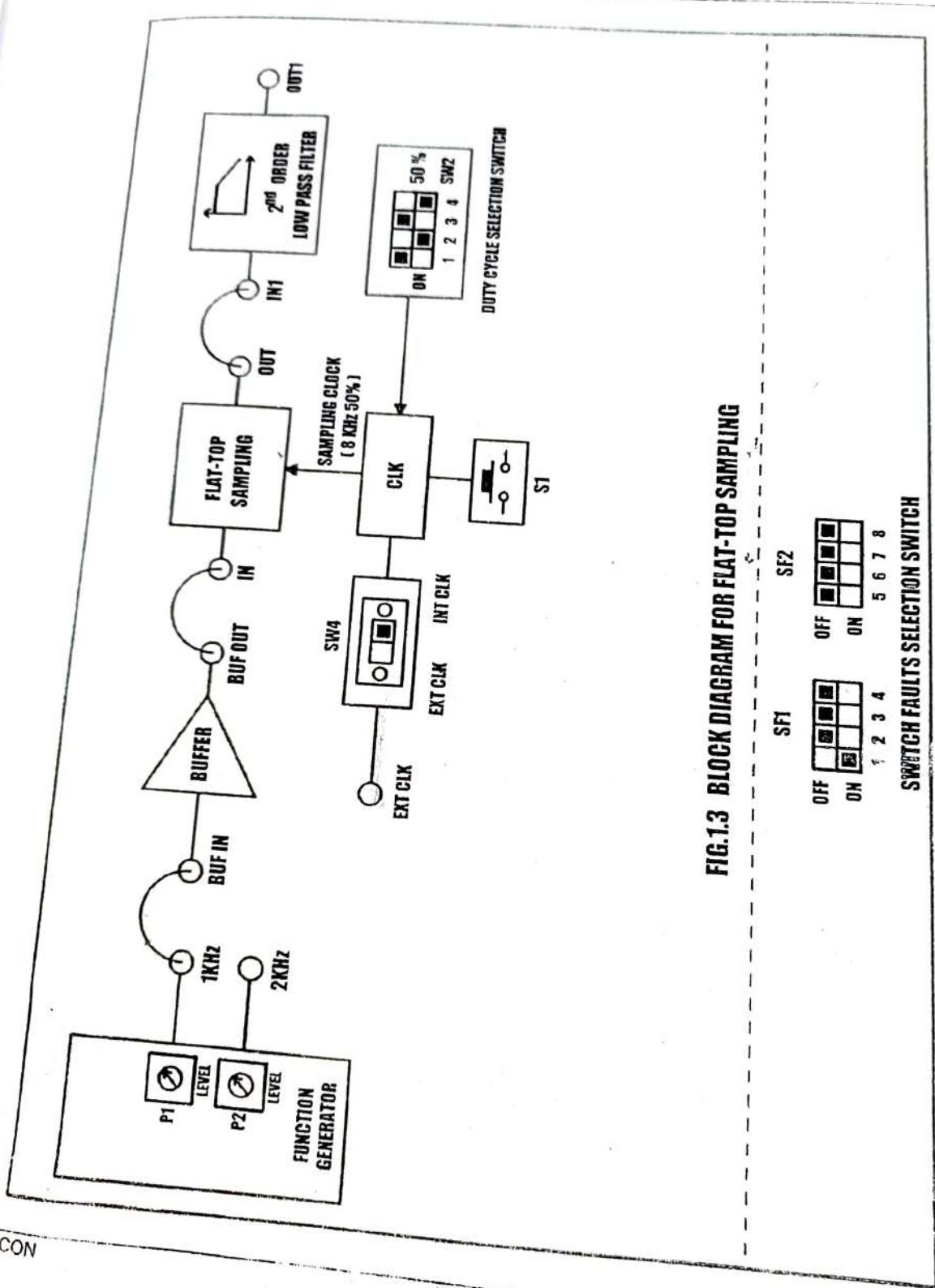


FIG.1.3 BLOCK DIAGRAM FOR FLAT-TOP SAMPLING

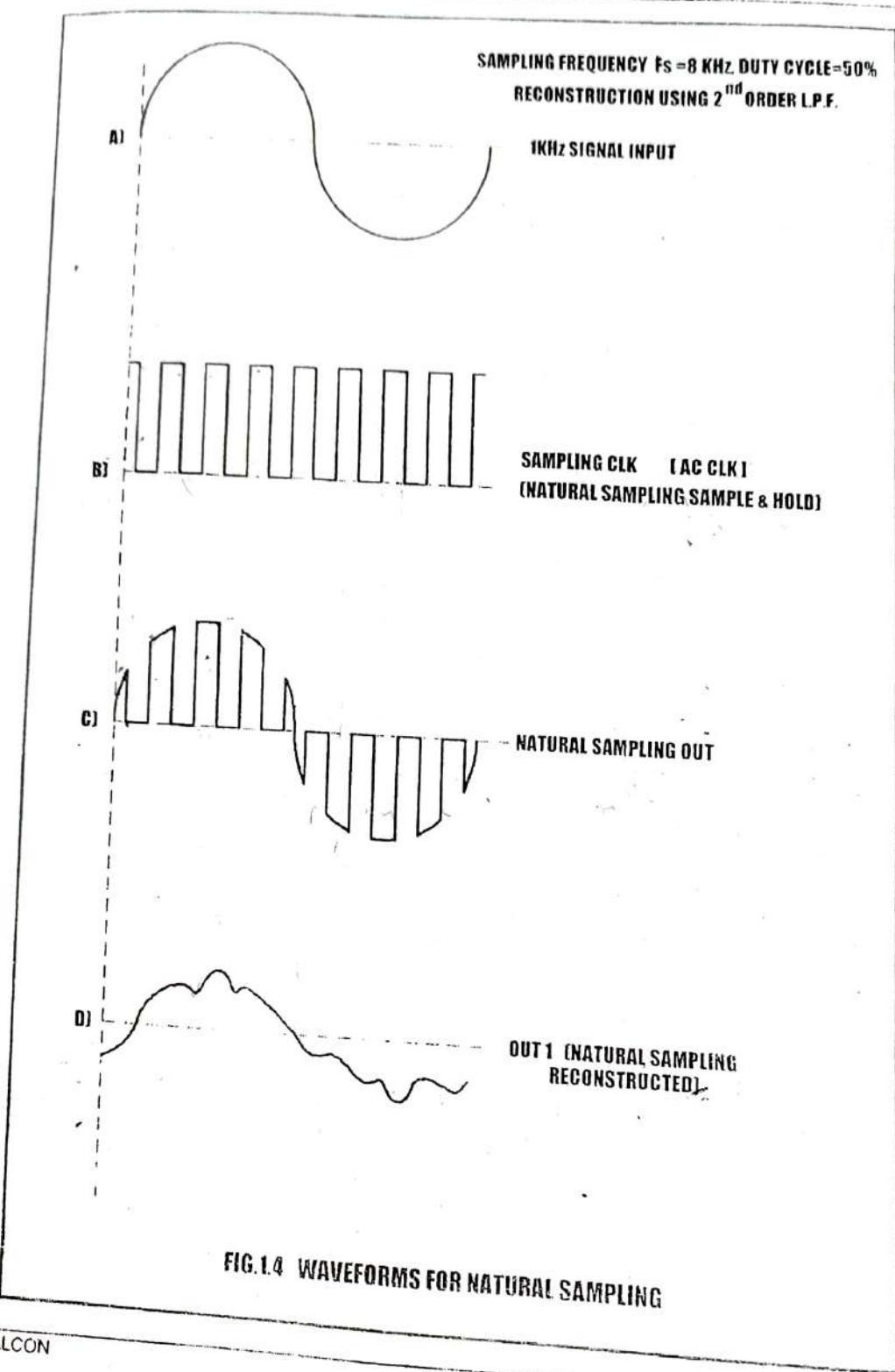


FIG.1.4 WAVEFORMS FOR NATURAL SAMPLING

ANALOG SIGNAL SAMPLE & HOLD RECONSTRUCTION

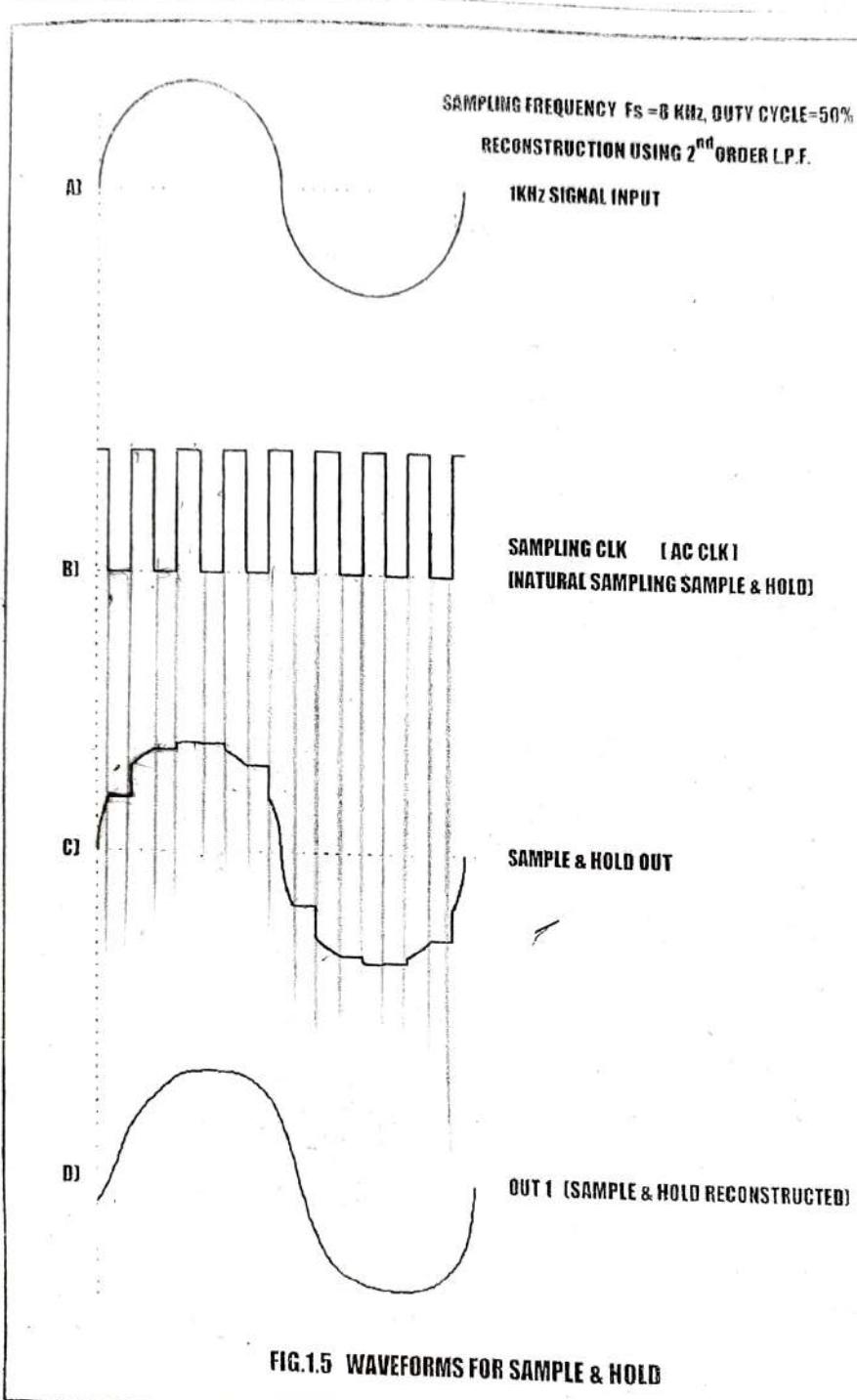


FIG.1.5 WAVEFORMS FOR SAMPLE & HOLD

SAMPLING FREQUENCY $F_s = 8 \text{ KHz}$, DUTY CYCLE=50%
RECONSTRUCTION USING 2nd ORDER LPF

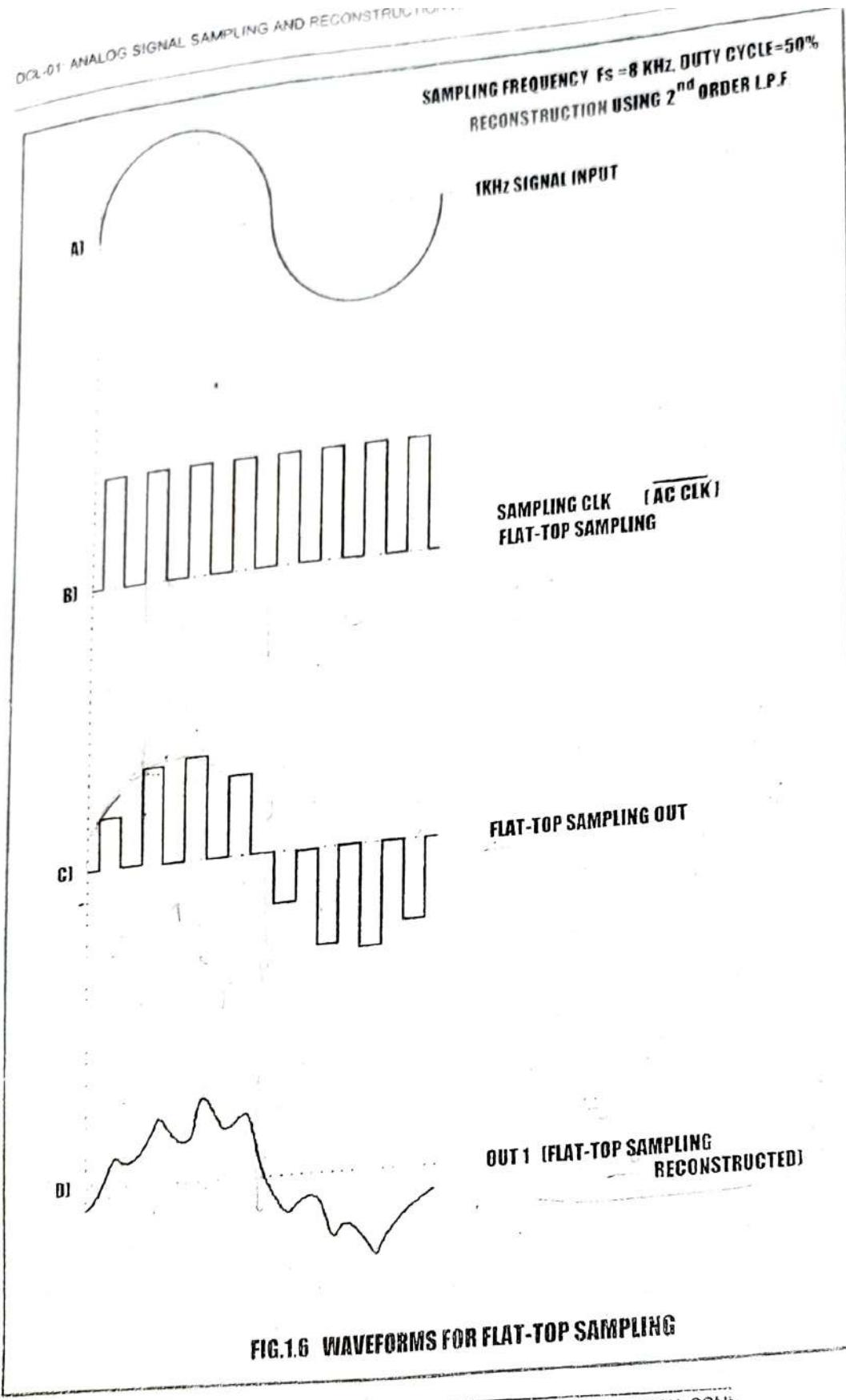


FIG.1.6 WAVEFORMS FOR FLAT-TOP SAMPLING

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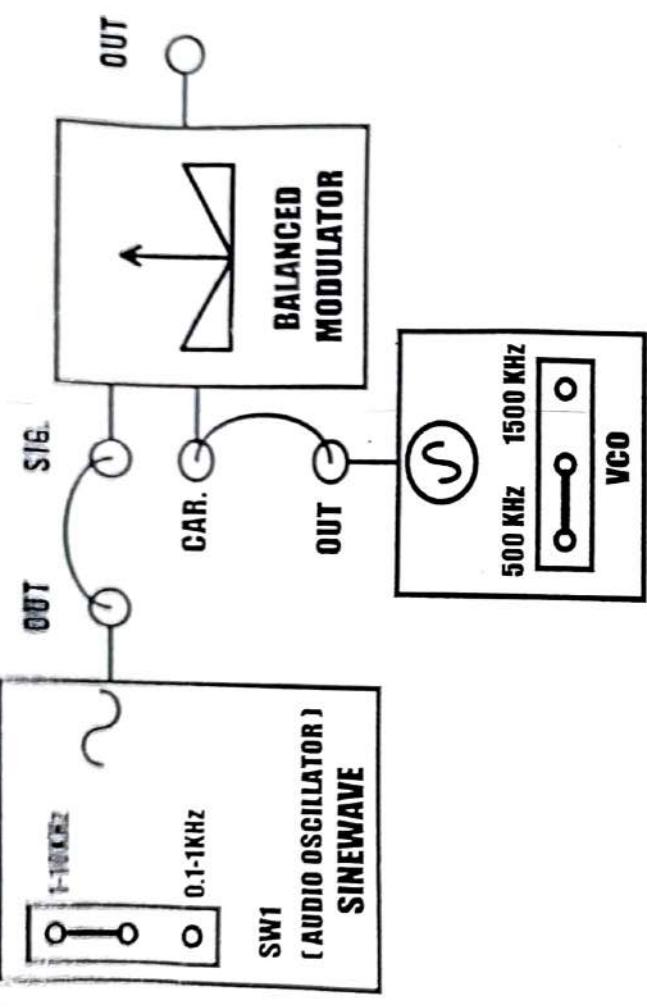
LAB INSTRUCTIONS FOR CARRYING OUT PRACTICAL

ON

**GENERATION OF THE AMPLITUDE MODULATED WAVE
AND CALCULATION OF % MODULATION USING
ACL01 KIT & ACL02**

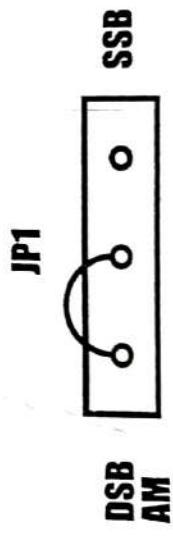


**BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI**



**FIG 1.14 BLOCK DIAGRAM FOR EXP. 1
STUDY OF DSB AM GENERATION**

JUMPER DIAGRAM FOR EXPERIMENT NO. 1



EXPERIMENT NO.1

NAME: DOUBLE SIDE BAND AM GENERATION.

OBJECTIVE:

- To study the operation of an DSB AM Modulator.
- To calculate the modulation index of an AM modulated wave.

A. To study the operation of an DSB AM Modulator.

EQUIPMENT:

Modules ACL-01 & ACL-02.

Power supply +/-12 V

20MHz Oscilloscope

Connecting Links.

frequency counter.

PROCEDURE:

- Refer to the fig.1.14 & Carry out the following connections.
Connect OUT post of SINEWAVE SECTION (ACL-01) to the i/p of Balance Modulator (ACL-01) SIG. Post (signal post).
- Connect o/p of VCO (ACL-01) OUT post to the input of Balance modulator CAR. post. (ACL-01)
- Connect the power supply with proper polarity to the kit, While connecting this, ensure that the power supply is OFF.
- Switch on the power supply and Carry out the following presetting:
 - SINEWAVE: OUT post LEVEL about 0.5Vpp; FREQ. About 1 kHz.
 - VCO: LEVEL about 1 Vpp; FREQ. about 450 kHz, Switch on 500KHz.
 - BALANCED MODULATOR: CARRIER NULL completely rotated clockwise or counter clockwise, so as "unbalance" the modulator and to obtain an AM signal with not suppressed carrier across the output; OUT LEVEL in fully clockwise.
- Connect the oscilloscope to the inputs of the modulator post (SIG and CAR) and detect the modulating signal and the carrier signal (fig.1.15a/b). Move the probe from post SIG to post OUT (output of the modulator), where signal modulated in amplitude is detected (fig.1.15c). Note that the modulated signal envelope corresponds to the wave form of the DSB AM modulating signal.
- Vary the amplitude of the modulating signal and check the 3 following conditions: modulation percentage lower than the 100% (fig. 1.15c), equal to the 100% (fig. 1.15d), superior to 100% (over modulation,

1414

fig. 1.15e)

Vary the frequency and amplitude of the modulating signal, and check the corresponding variations of the modulated signal.

Vary the amplitude of the modulating signal and note that the modulated signal can result saturation or over modulation.

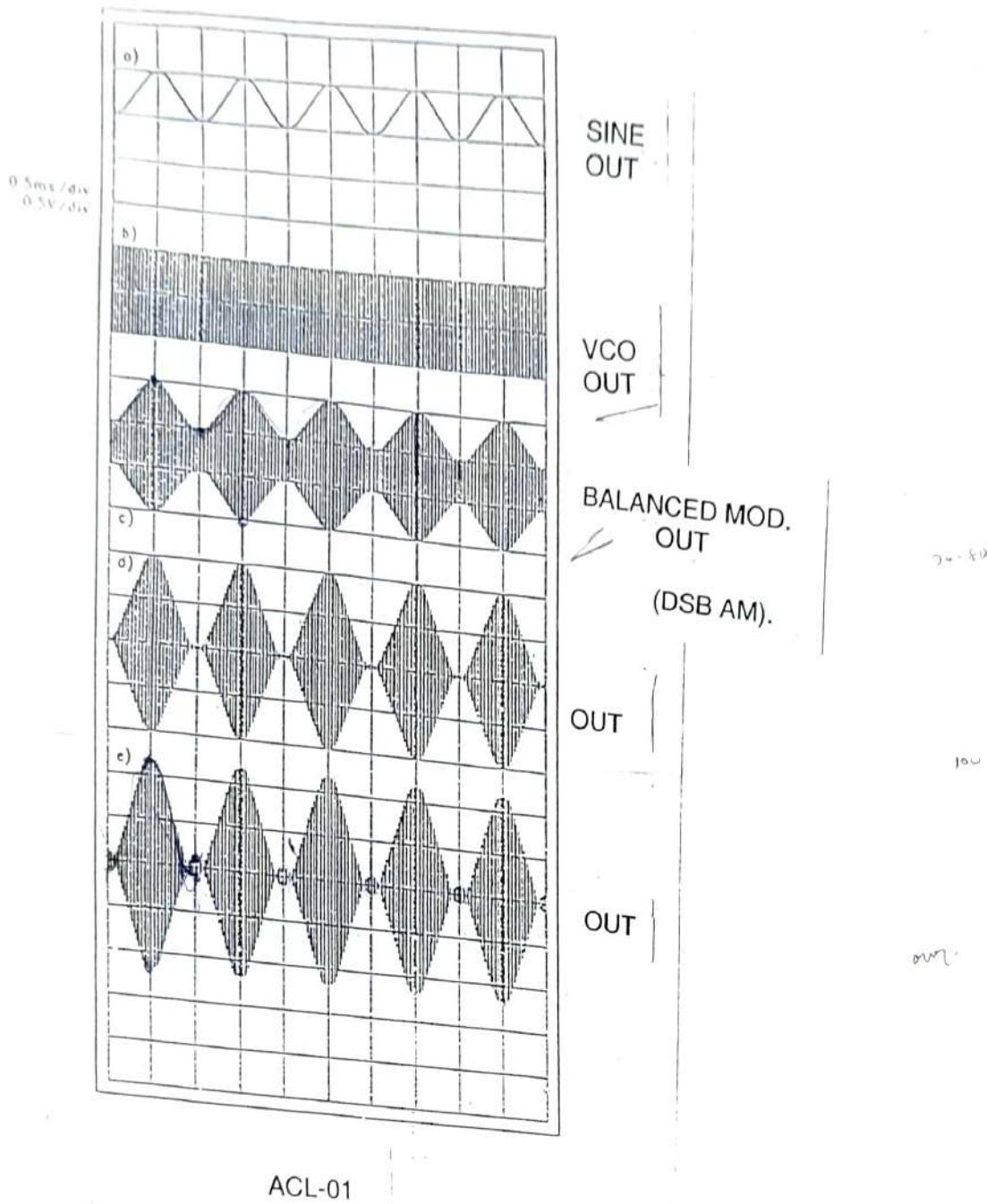


FIG 1.15 | Wave form of the DSB AM modulator.

10/10/17

Page No. 1

B. To calculate the modulation index of an AM modulated wave.

OBJECTIVE:

To study modulation index of DSB AM modulated wave.

EQUIPMENTS:

Modules ACL-01
Power supply +/-12 V
20MHz Oscilloscope
Connecting Links.

PROCEDURE:

1. Perform the operation as done in Procedure (a) and obtain the AM modulated wave as shown in fig. (1.16).
2. Using the oscilloscope measure from the wave form. The amplitude B of the modulation signal at post OUT of balance modulator ACL-01) The amplitudes H and h of the modulated signal, and the amplitude C of the envelope of the modulated signal post OUT of balance modulator (ACL-01)
3. Calculate the constant k of the modulator, equal to: $k = C/B$ You find a value a little over 1.
4. Calculate the amplitude A of the carrier, equal to:

$$A = \frac{H+h}{2}$$

5. Calculate the percentage index of modulation m, equal to:

$$m = \frac{H-h}{H+h} * 100\%$$

0.25
0.5
0.75

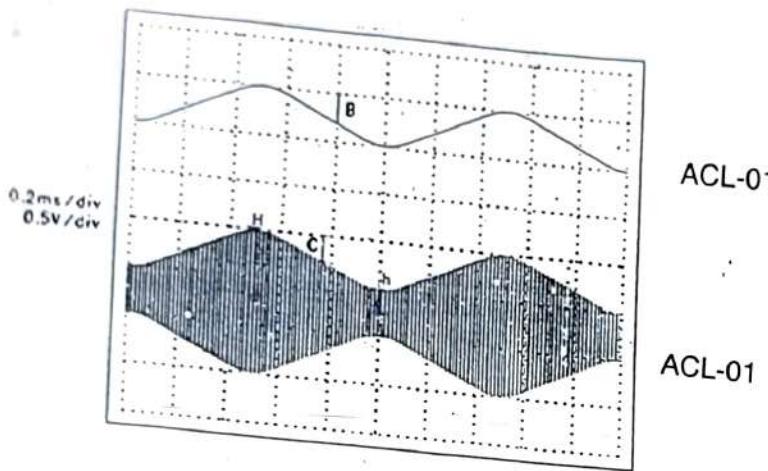
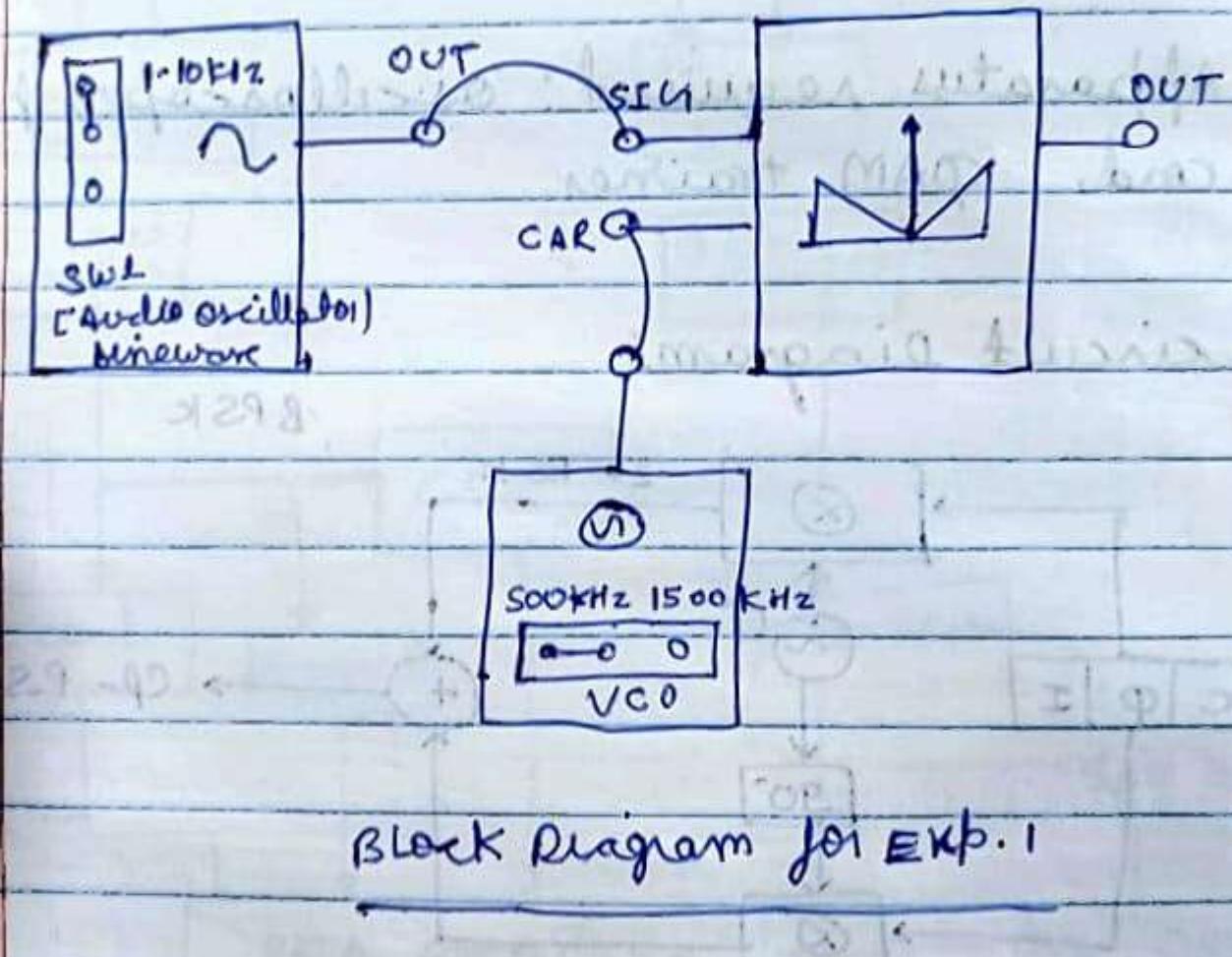


FIG. 1.16 : Calculation of the modulation index

Exp - 1

AIM:- Generation of the amplitude modulation wave and calculation of it's modulation using ACLOLA kit

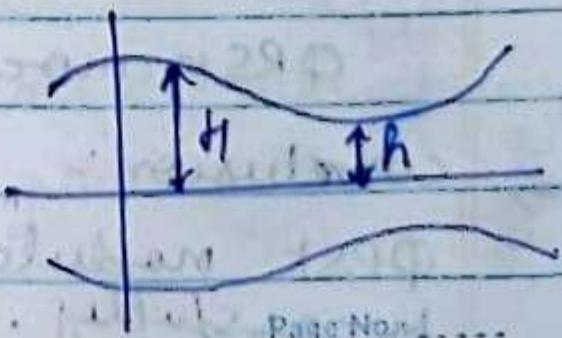


Calculation :-

Amplitude of carrier

$$A = H + h$$

2.



$$m = \frac{H-h}{H+h} \times 100$$

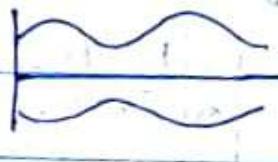
case I :-

undermodulation :-

$$m = \frac{1.2 - 0.28}{1.2 + 0.28} \times 100, \quad H = 1.2 \times 0.5 \text{ volts}$$

$$= 71.42\%.$$

$$h = \cancel{0.28} \times 0.5 \text{ volts}$$

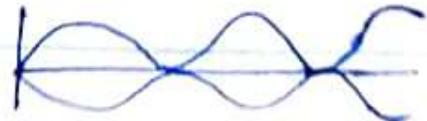


case II :-

$$m = \frac{H}{h} \times 100 \quad H = 0.8 \times 0.5 \text{ volts}$$

$$= 0 \times 0.5 \text{ volts}$$

$$\frac{0.8 \times 100}{0.8} = 100\%.$$



case III :-

~~Burst~~

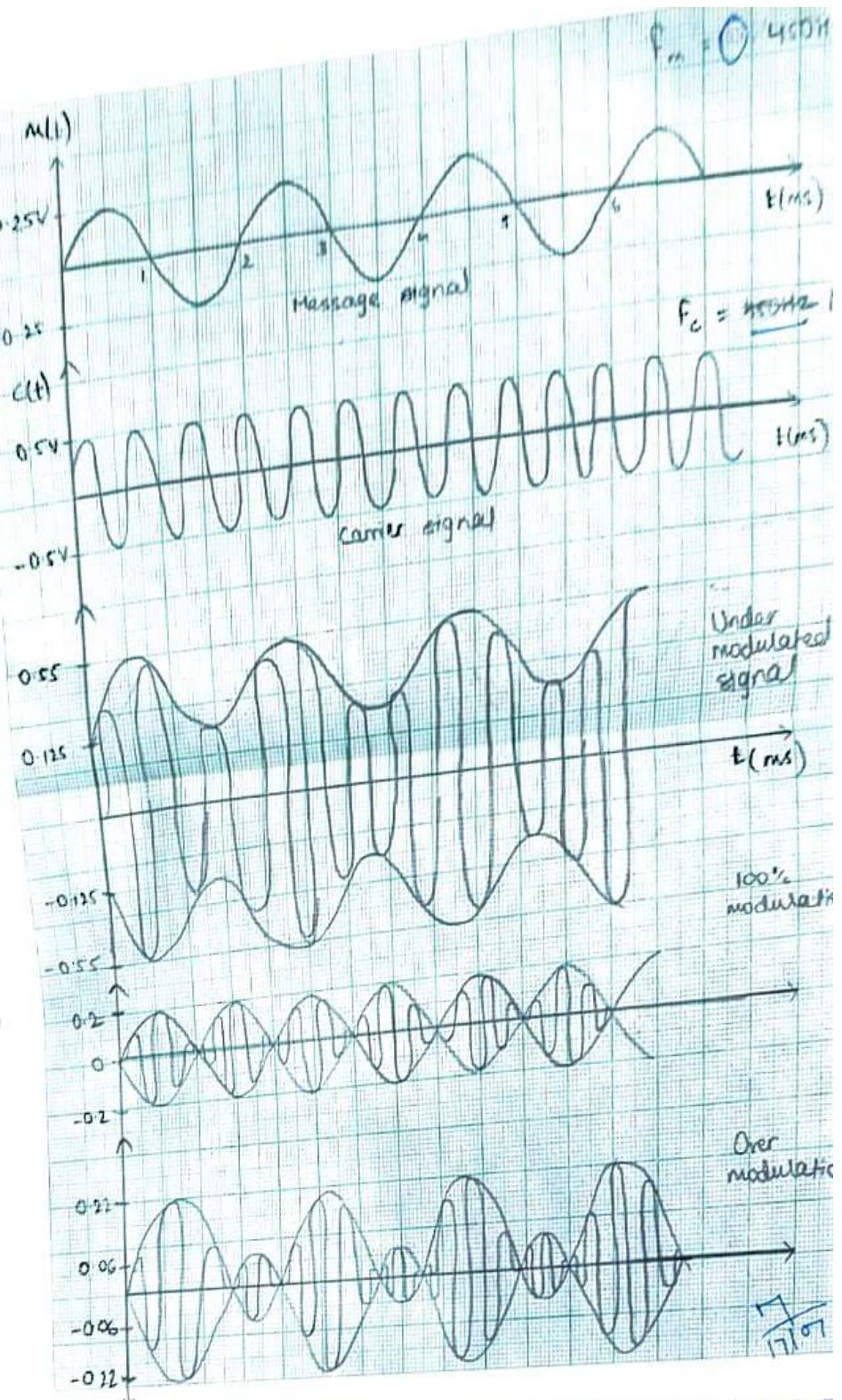
~~mod~~

$$H = 0.7 \times 0.5 \text{ V}$$

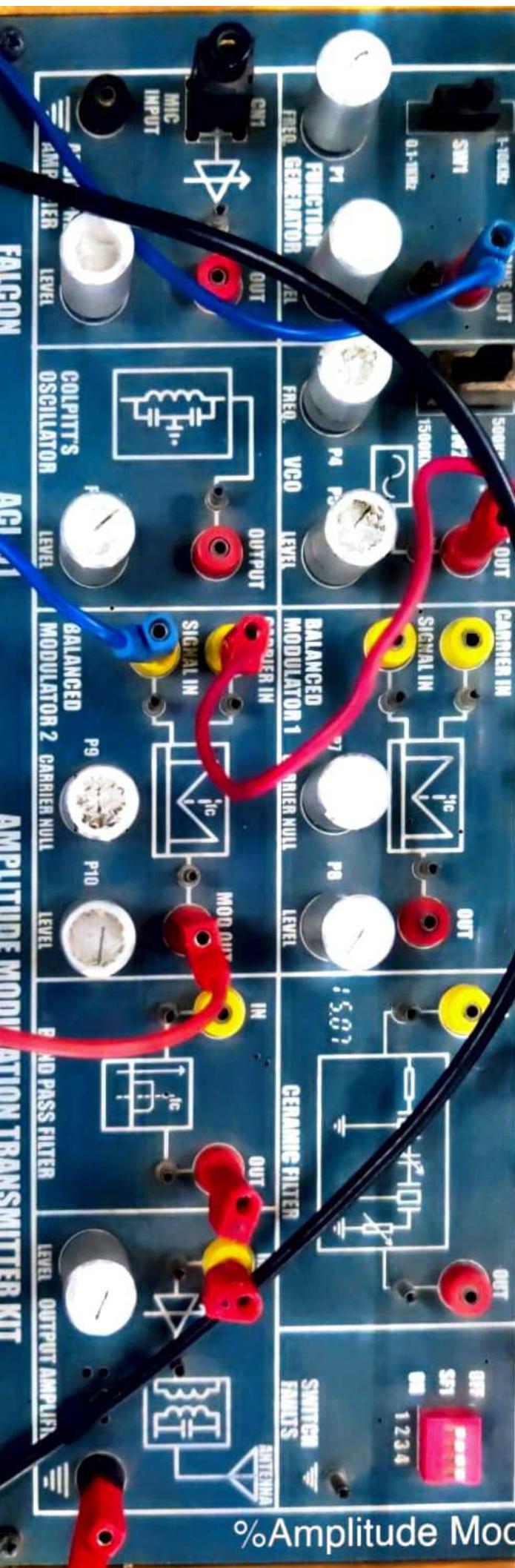
$$h = 0.1 \times 0.5 \text{ V}$$

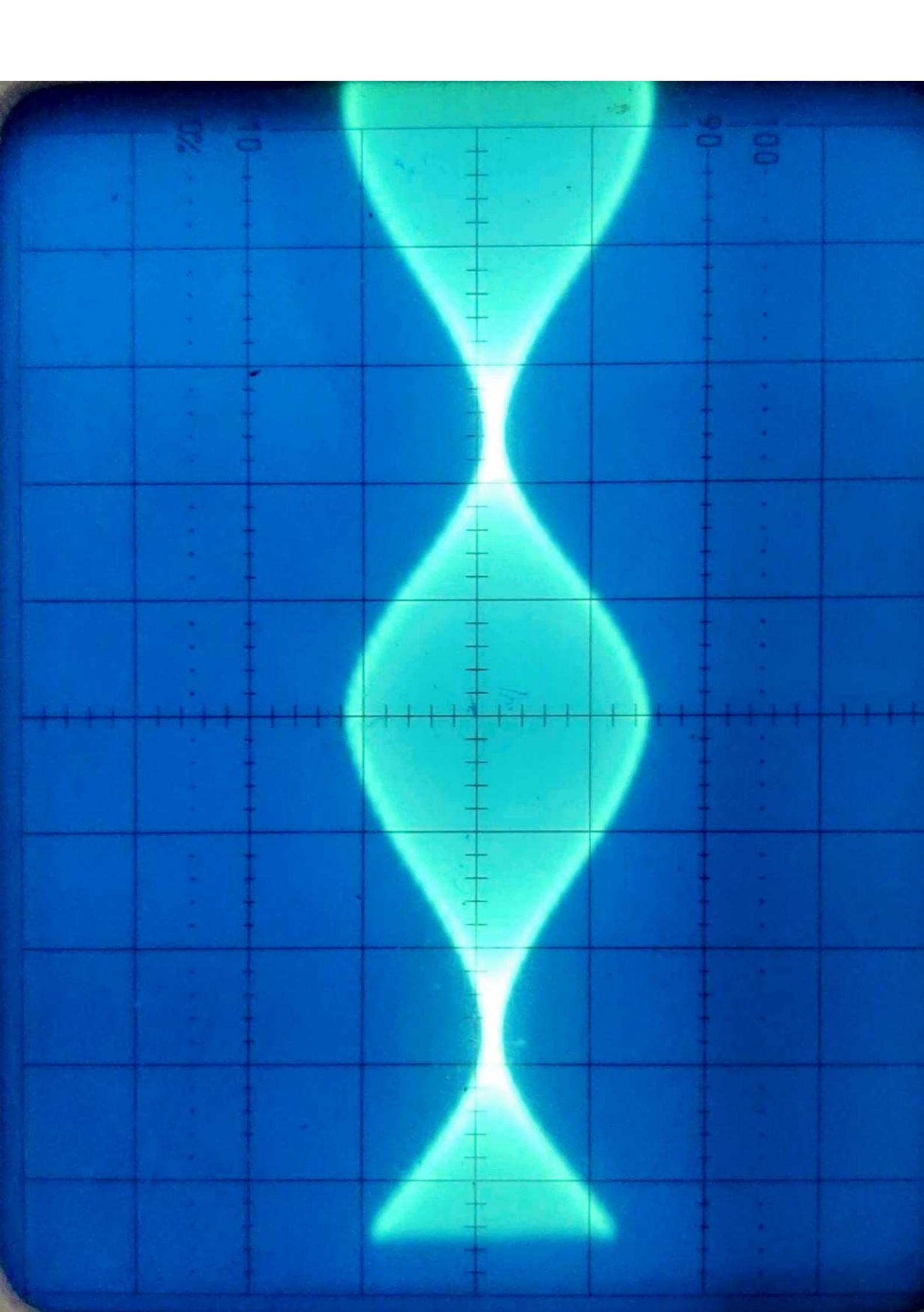


$$m = \frac{H-h}{H+h} \times 100 : 12.5\% \text{ / } 12.5\%$$



Here shown to point out where signal goes is detected
 i.e. the modulating signal and check
 whether : modulation percentage
 so, equal to the 100%, superior
 and amplitude of the modulating
 e corresponding variations of the
 e at the modulating signal and note
 signal can result saturation or over
 under modulation was observed and
 was calculated for undermodulation
 + over modulation
 $\frac{1}{2} \times 1$





**DEPARTMENT
OF
ELECTRONICS AND COMMUNICATION ENGINEERING**

ANALOG COMMUNICATION LABORATORY

LAB INSTRUCTIONS FOR CARRYING OUT PRACTICAL

ON

**GENERATION OF FM WAVE AND ITS DETECTION
USING ACL 03 AND ACL 04 FM TRAINER KIT**



**BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI**

AIM: Generation of FM wave and its detection using ACL 03 and ACL 04 FM Trainer kit

OBJECTIVE:

- A. To plot the modulation characteristics of varactor modulator.
- B. To calculate the modulation sensitivity of varactor modulator.
- C. To observe and measure frequency deviation and modulation index of FM.

To plot the modulation characteristics of varactor modulator:

EQUIPMENT:

- Modules ACL-03
- Power supply +/-12V.
- Oscilloscope.
- Volt meter
- Frequency meter
- Connecting links

PROCEDURE:

The characteristic modulation curve is given by the output frequency of the modulator as function of the input modulating voltage (fig.1.7). It is possible to plot the curve of fig.1.7 post by post, using a potentiometer to statically an amplitude variation of the modulating signal, and measuring the corresponding output frequency of the modulator.

1. Connect the power supply with proper polarity to the kit. While connecting this, ensure that the power supply is OFF.
2. Switch ON the power supply and Carry out the following presetting as shown in the fig1.6.
 - FREQUENCY MODULATOR: LEVEL about 2Vpp; FREQ. To the minimum; switch on 1500KHz.
3. Connect oscilloscope and frequency meter to the output of the modulator FM/RF OUT.
4. Connect the voltmeter to the cursor of the frequency regulation potentiometer post V below Sw2.
5. Vary the voltage at steps of 0.5 volt and fill a table with the voltage values and the corresponding frequencies.
6. Plot a graph with the measured voltage and frequency values. You obtain a curve similar to the one of fig. 1.8
7. From the analysis of the curve you can note that some segments have not a linear behavior, while if you consider the whole characteristic you find a high non-linearity.

RESULT:

ii. To calculate the modulation sensitivity of FM modulator. :

EQUIPMENT:

- Modules ACL-03
- Power supply +/-12 V
- 20 MHz oscilloscope
- Voltmeter.
- Frequency meter.
- Connecting Links.

PROCEDURE:

1. Perform the procedure as done in Exp: 1(A).
2. Consider the modulator operation in the segment of curve within 700 to 1300 kHz, with central frequency of 1000 kHz. From the analysis of the curve of fig. 1.8 it is possible to calculate the modulation sensitivity of the modulator.
3. The modulation sensitivity S is defined as:

$$S = \frac{dF(v)}{dv}$$

Where $F(v)$ is the instantaneous frequency function of the modulating voltage

v. The last relation can be approximated writing the incremental ratio:

$$S = \frac{\Delta F}{\Delta v}$$

With reference to the curve of fig. 1.8, in correspondence to the central frequency (1000kHz) you obtain:

$$\Delta F = 50 \text{ kHz} \quad v \approx 125 \text{ mv} \text{ from which: } S_0 = 50 / 125 = 0.4 \text{ kHz/mv}$$

RESULT:

CONCLUSION:

C. To observe and measure frequency deviation and modulation index of FM.

EQUIPMENT:

- Modules ACL-03
- Power supply +/-12 V
- Oscilloscope
- Voltmeter
- Frequency meter
- Connecting Links

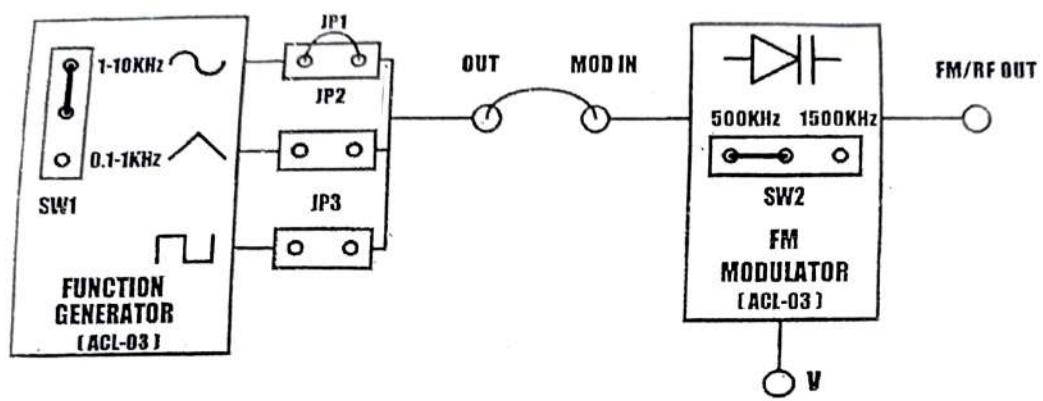
PROCEDURE:

1. Refer to the fig. 1.6 & carry out the following connections.
2. Connect the power supply with proper polarity to the kit while connecting this; ensure that the power supply is OFF.
3. Connect the o/p of function generator **OUT** post to the modulation **IN** of **FREQUENCY MODULATOR MOD IN** post.
4. Switch ON the power supply and carry out the following presetting:
 - FUNCTION GENERATOR: sine wave (J1); LEVEL about 0.2Vpp; FREQ. About 1kHz
 - FREQUENCY MODULATOR LEVEL about 2Vpp; FREQ. on the center; switch on 1500kHz
5. Connect the oscilloscope to the output of the modulator FM/RF OUT. You obtain a waveform similar to the one of Fig.1.10.
6. The frequency deviation ΔF can be calculated as follows (refer to fig. 11).
 - From the oscilloscope evaluate F_M and F_m , detecting the periods of the respective sine waves
 - The frequency deviation ΔF is defined as: $\Delta F = (F_M - F_m)/2$. You can note that if the modulator operates in a linear zone so F_M and F_m are over and under the central frequency F of the same quantity ΔF , otherwise this does not occur.
7. The value of the modulation index mf is calculated by the relation $mf = \Delta F/f$, where f is the frequency of the modulating signal.
8. Then observe the FM signal as shown in fig. 1.1 in theory

RESULT:

CONCLUSION:

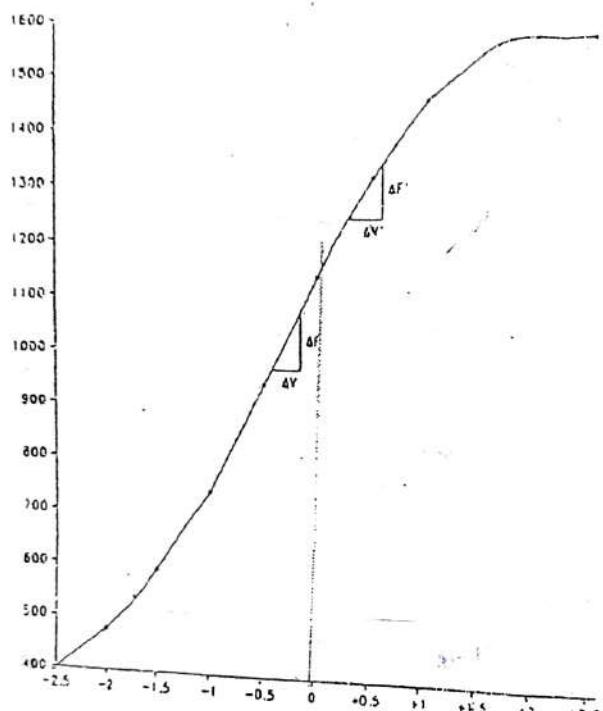
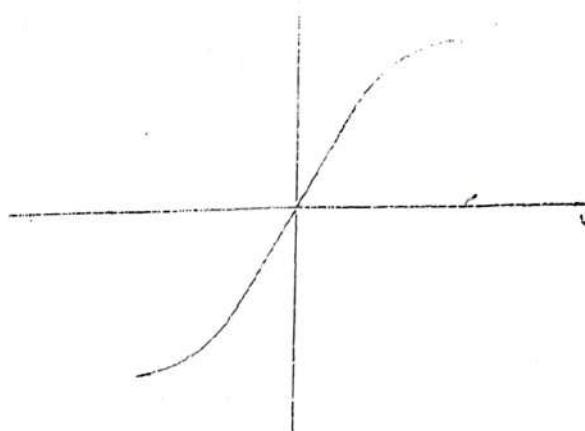
PRECAUTION :



BLOCK DIAGRAM FOR EXP. 1
STUDY OF VARACTOR MODULATOR (fig 1.6)

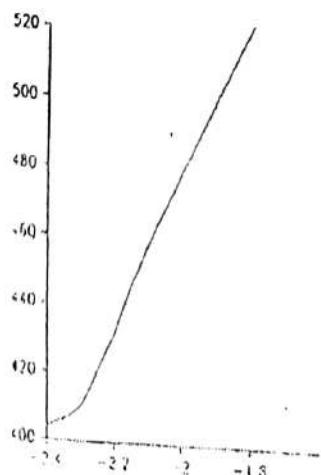
fig.1.7

Modulation
characteristic



VOLTAGE [V]	FREQUENCY [kHz]
-2.8	404
-2.5	404
-2	478
-1.5	592
-1	740
-0.5	940
0	1140
0.5	1317
1	1454
1.5	1536
2	1571
2.5	1573

fig.1.8



VOLTAGE [V]	FREQUENCY [kHz]
-2.4	406
-2.3	410
-2.2	432
-2.1	456
-2	480
-1.9	502
-1.8	523

fig.1.9

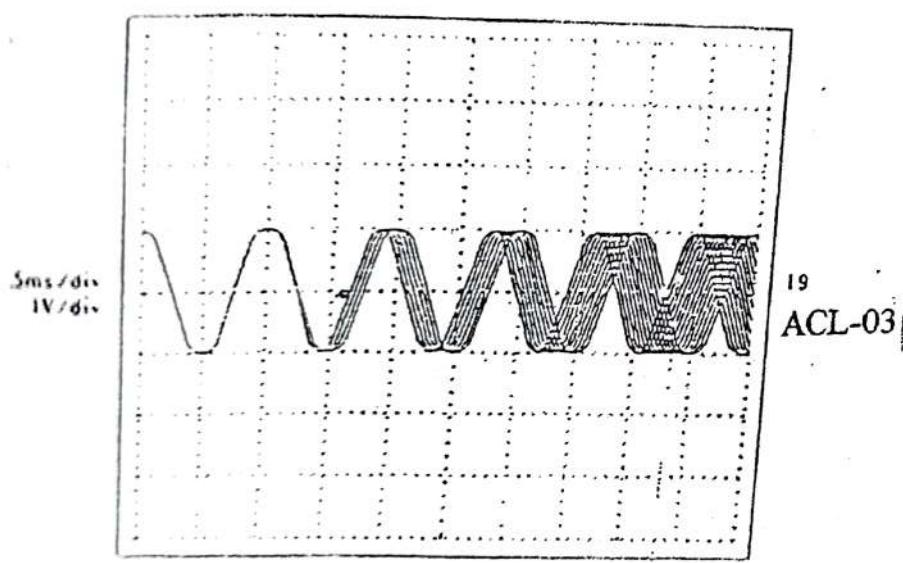


fig.1.10

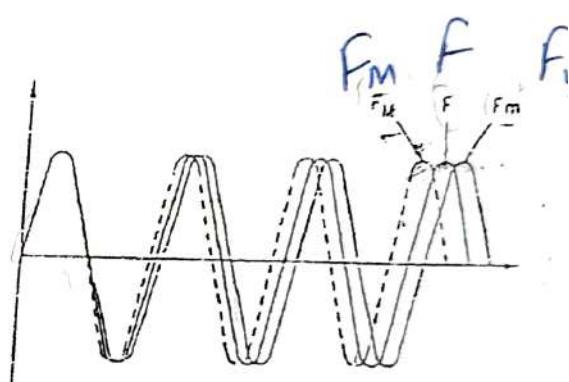
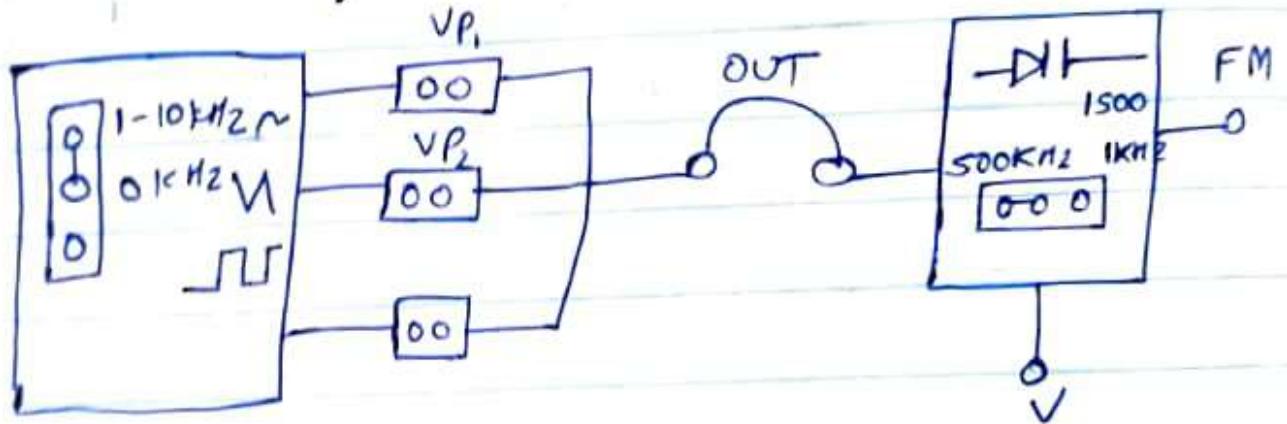


fig.1.11

Exp → 2Aim

Generation of amplitude FM wave and detection using AC103 of ACL04 FM trainers kit.

Circuit diagram :Observation :

<u>voltage</u>	<u>Time</u>	<u>Freq (kHz)</u>
-4.4 V	2.5 μs	400
-4 V	2.5 μs	400
-3 V	2.5 μs	400
-2 V	2	500
-1.6 V	1.5	666.67
-1 V	1.1	909

or

$$m(t) = A_m \cos(2\pi f_m t)$$

$$c(t) = A_c \cos(2\pi f_c t)$$

frequency modulated wave will be

$$f_m(t) = f_c + K A_m \cos(2\pi f_m t)$$

$$f_m(t) = f_c + K m(t)$$

f_m = Frequency modulated wave

$m(t)$ = modulating signal

K = proportionality constant

The maximum deviation in freq.

$$\Delta f_{max} = |f_m(t) - f_c|$$

$$= |K A_m \cos(2\pi f_m t)|$$

The maximum deviation is $K A_m$

$$\therefore \text{Modulation Index } \mu = \frac{\Delta f_{max}}{f_c}$$

CONCLUSION - Frequency modulation was observed and modulation index μ was calculated. Graph was also plotted. (with values?) ??

Ex

OBSERVATION

Voltage (V)	Time (μs)	Frequency (KHz)
-5	2.4	416.67
-4	2.4	416.67
-3	2.4	416.67
-2	2	500
-1.5	1	1000
-1	0.9	1111.11
-0.5	0.67	1492.5
0	0.63	1587.3
0.5	0.6	1666.67
1	0.6	1666.67
1.5	0.6	1666.67
2	0.6	1666.67

$$\text{Modulation sensitivity } S = \frac{\Delta f}{\Delta V} = \text{slope}$$

$$= \frac{1111.11 - 500}{-1 - (-2)} = \frac{511.11}{1}$$

$$= 511.11 \text{ KHz/V}$$

$$= 511.11 \text{ KHz/mV}$$

~~$$f_1 = 2.5 \mu\text{s}$$

$$f_2 = 2.4 \mu\text{s}$$

$$f_3 = 2.2 \mu\text{s}$$~~

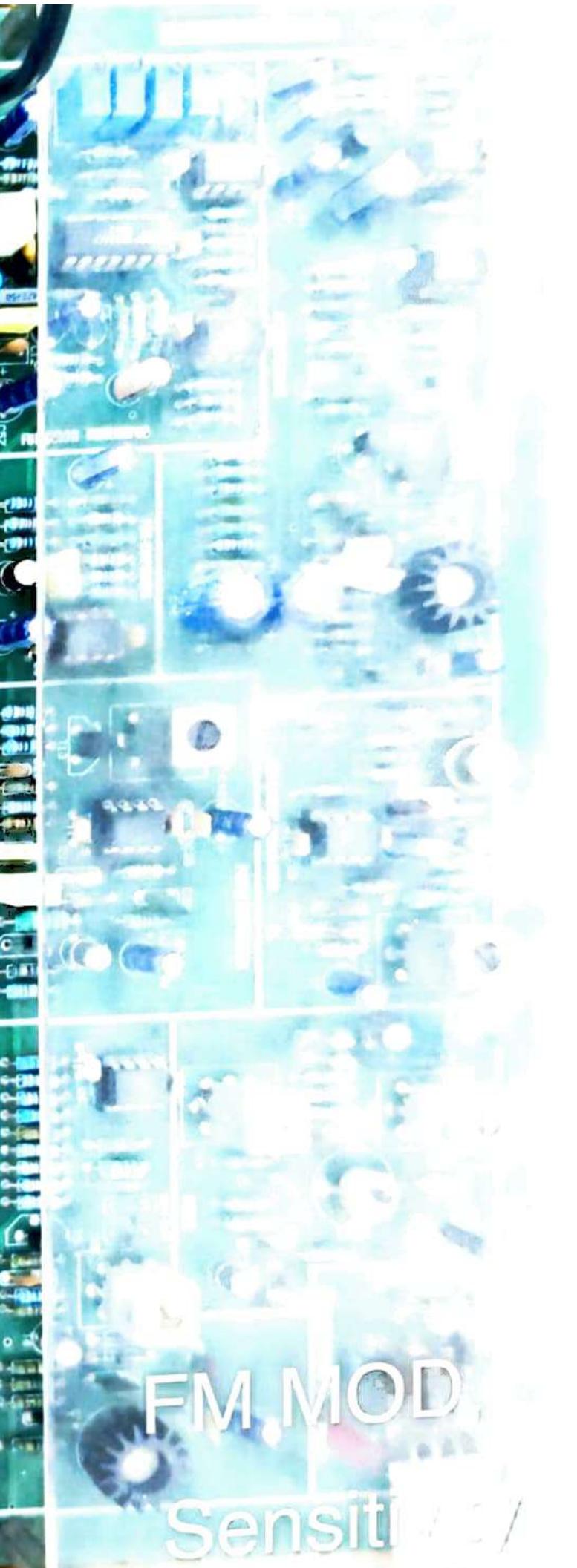
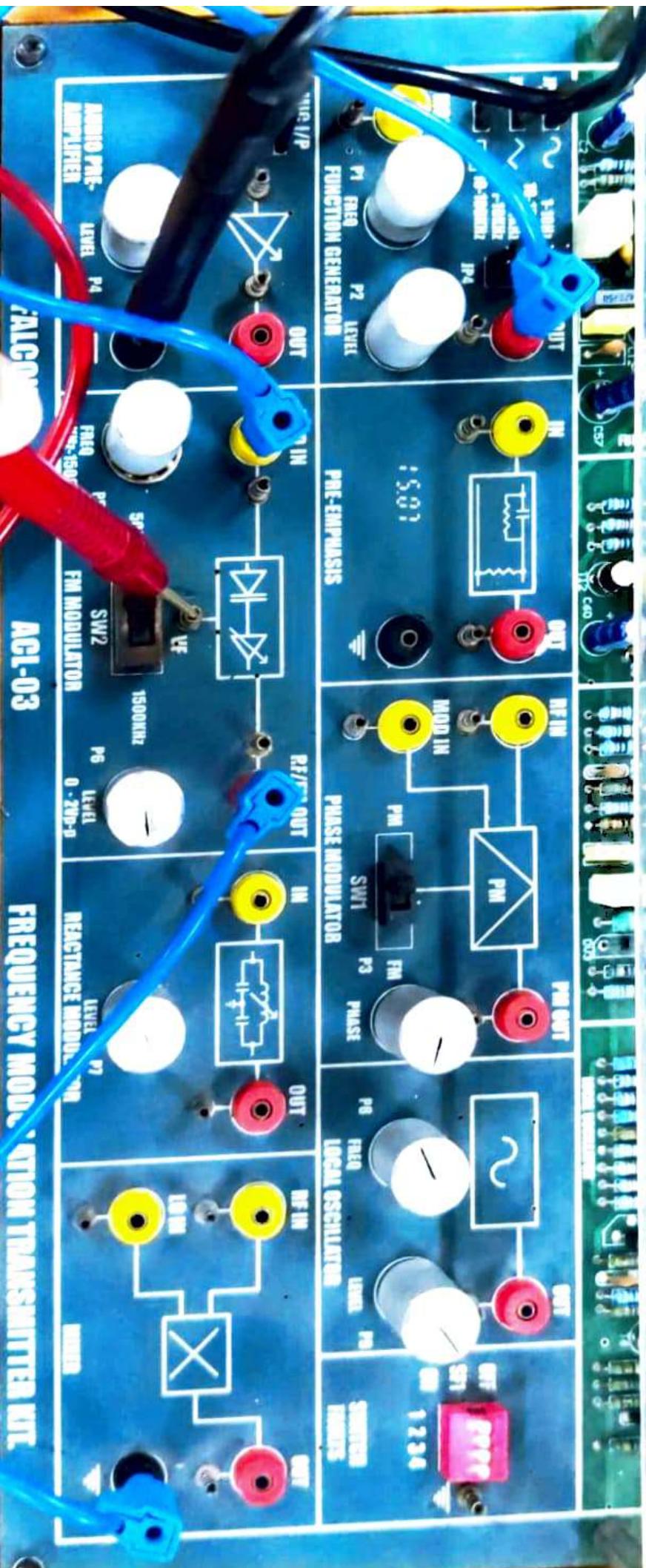
$$\therefore f_m = \frac{1}{2.2} \times 10^6 \quad f_m = \frac{1}{2.5} \times 10^6$$

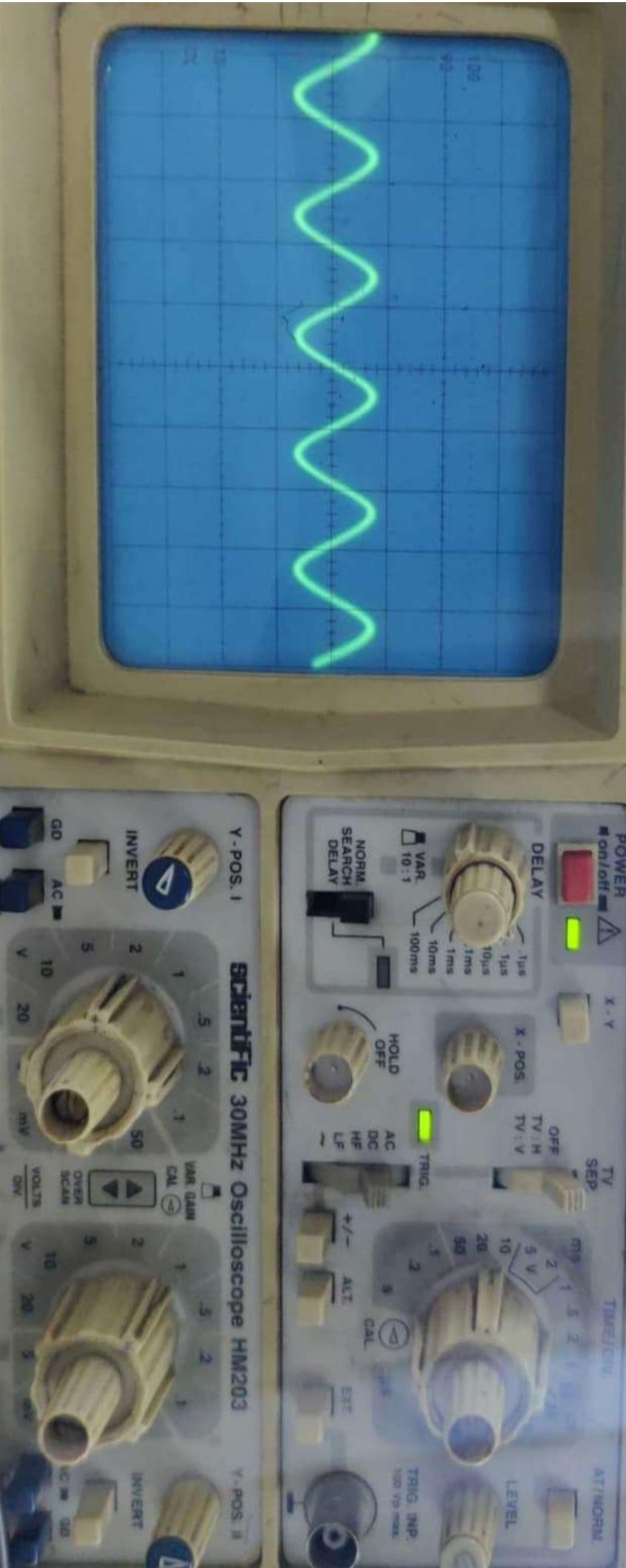
$$= 454.55 \text{ KHz} = 400 \text{ KHz}$$

$$f_c = \frac{1}{2.4} \times 10^6 = 416.67 \text{ KHz}$$

frequency deviation
 $\Delta f = (f_m - f_c)/2 = \frac{454.55 - 400}{2} = 27.275 \text{ KHz}$

$$\text{Modulation index } m = \frac{\Delta f}{f_c} = \frac{27.275}{416.67} = \frac{1}{15}$$





EXPT 12

12

**DEPARTMENT
OF
ELECTRONICS AND COMMUNICATION ENGINEERING**

DIGITAL COMMUNICATION LABORATORY

LAB INSTRUCTIONS FOR CARRYING OUT PRACTICAL
ON

**INVESTIGATION OF QPSK MODULATION AND
DEMODULATION USING ST 2112 QAM TRAINER KIT**



**BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI**

EXPERIMENT - 3

bject :

udy & analysis of QPSK modulation.

theory

Phase PSK modulation.

In this modulation, called 4-PSK, or Quadrature PSK (QPSK), the sine carrier takes 4 phase values, separated of 90° and determined by the combinations of bit pairs (Dibit) of the binary data signal. Fig a shows an example of correspondence between Dibit and phase. The data are coded into Dibit by a circuit generating:

A data signal I (*Inphase*) consisting in voltage levels corresponding to the value of the first bit of the considered pair, for a duration equal to 2 bit intervals

A data signal Q (*Quadrature*) consisting in voltage levels corresponding to the value of the second bit of the pair, for duration equal to 2 bit intervals.

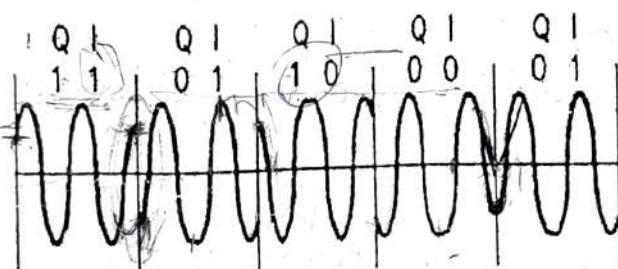


Fig. 16

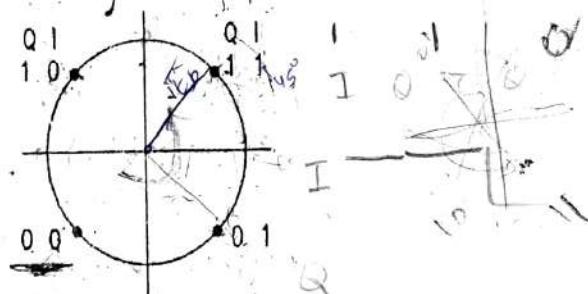


Fig. 17

Main aspects :

The main factors characterizing the QPSK are:

- Applications in data transmission modems (ITU- T V22N26, BELL 20 I) and digital radio transmission
- It needs circuits of high complexity

- Possibility of error lower than FSK but higher than 2-PSK
 - Called F_b the bit transmission speed, the minimum spectrum Bw of the modulated signal is equal to $F_b/2$
 - The transmission efficiency, defined as the ratio between F_b and Bw, is equal to 2.

4-PSK Modulator:

The 4 phases of the sine carrier can be obtained via the sum of 2 sine waves with the same frequency and shifted of 90° between them. We can call the sine waves respectively $\angle 0$ and $\angle 90$:

- $\angle 0 = \sin(\omega t)$
 - $\angle 90 = \cos(\omega t)$

By adding respectively $\angle 0$ and $\angle 90$ direct or inverted:

81 + 82

$$= \phi_1 + \phi_{21}$$

$$\phi_1 = \phi_{21}$$

$$-\phi_0 - \phi_{\psi_0}$$

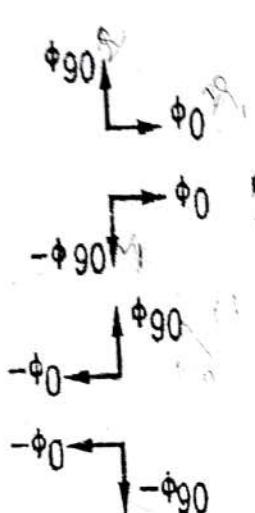


Fig. 18

You obtain the 4 phases for the QPSK signal. The modulator is carried out with two multipliers used as 2-PSK modulators, which supply the modulated PSK1 and PSKQ signals. The sum of the two generates the PSK signal with the 4 possible phases.

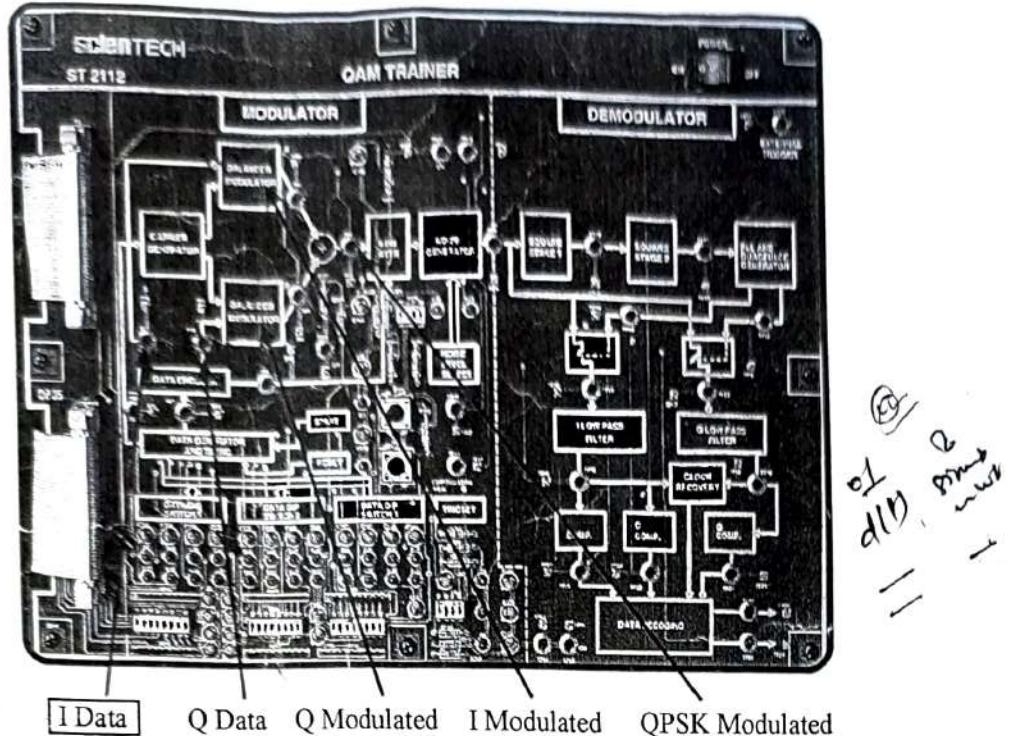


Fig.19

The block diagram of the modulator used on the trainer is shown in fig.b. Two 1 KHz sine carriers, shifted between them of 90° , are separately applied to 2 balanced modulators. The data (signals I and Q) reach the two modulators from the Dibit generator. Each modulator provides the direct sine-wave when the data signal is to low level (bit "0"), the inverted sine-wave (shifted of 180°) when the bit is "1". By adding the two outputs you get a 1 KHz sine signal, which phase can take 4 different values separated of 90° between them.

Procedure :

1. Ensure the following initial conditions on ST2112 trainer :
 - a. SW3, SW5, SW6, SW7, SW9 should be in the OFF mode.
 - b. Power supply should be OFF.
2. Switch on the power supply.
3. Connect Test point TP6 on Channel 1 & TP7 on Channel 2 of Oscilloscope; you will observe 1 KHz sine & cosine wave. *Use probes on TP6 & TP7 & Ground using other*
4. Set I & Q Channel data with the help of DIP switch SW5, SW6, SW7. As there are 24 bits data available on the trainer so, first bit is I bit then second bit is Q bit then third bit is C bit. But in this experiment you have to use I bit & Q bit so, you can select combination according to your requirement.

ST 2112

For example:

$$SW5 = 11000010$$

$$SW6 = 01001010$$

$$SW7 = 00100010$$



5. Switch ON all the DIP switches on SW3.
6. Now press SW8 which is reset switch then press SW4 which is start.
7. Now connect Channel 1 of Oscilloscope to TP2 & Channel 2 to TP1, you can observe Clock & Data which you have set.
8. Now to observe QPSK modulated signal with respect to data connect Channel 1 to TP1 & Channel 2 to TP8. You can observe QPSK modulated signal with respect to data.
9. Turn OFF the power.

Waveforms :

- a. Clock & Data :

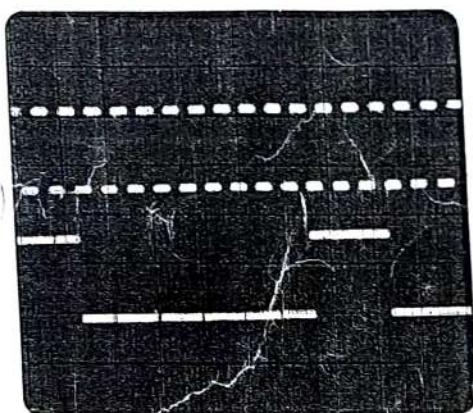


Fig. 20

- b. I Channel & I modulated signal :

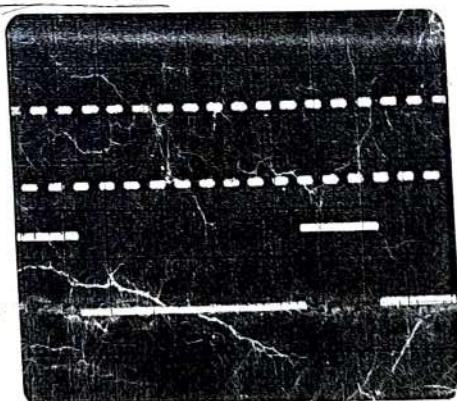


Fig. 21

ST 2112

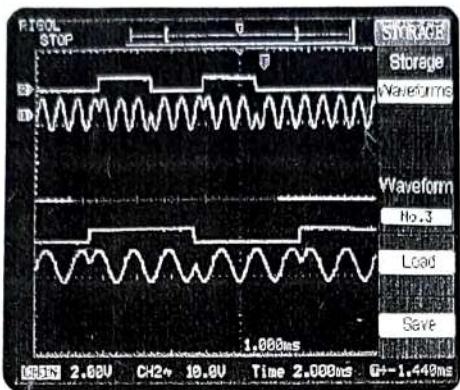


Fig. 22

c. Q Channel & Q modulated signal :

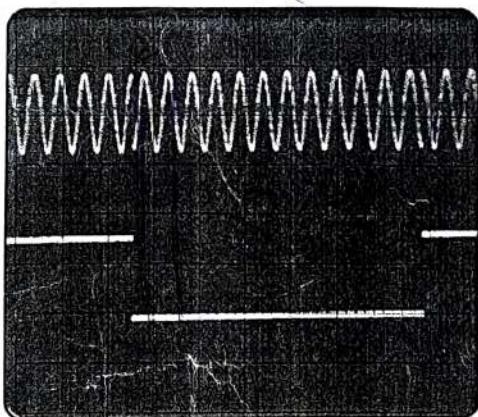


Fig.23

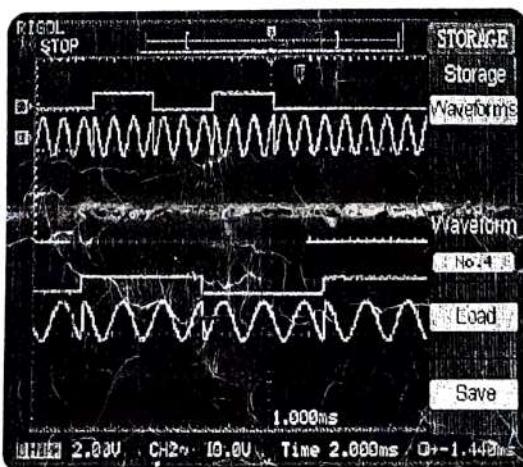


Fig. 24

d. Data & QPSK signal: ✓

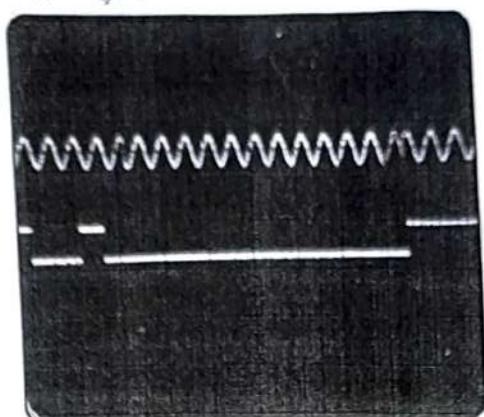


Fig. 25

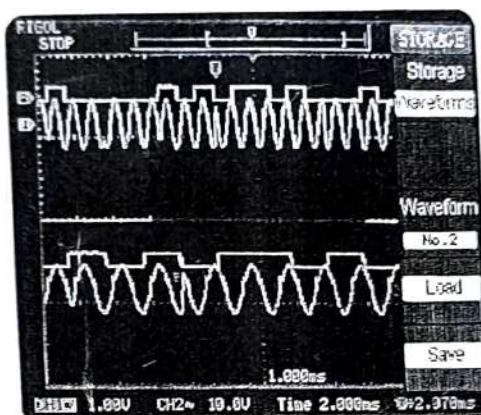


Fig. 26

Conclusion :

(2)

EXPERIMENT 4**Object :****Study & analysis of QAM modulation.****Theory :**

Quadrature Amplitude Modulation (QAM)

The QAM is a digital modulation where the information is contained into the phase as well as the amplitude of the transmitted carrier.

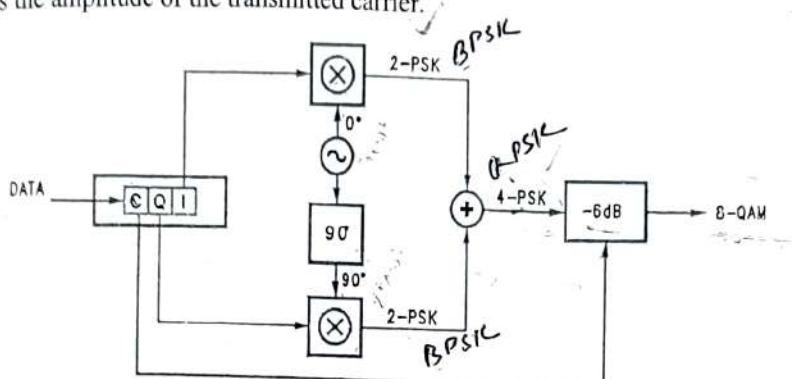


Fig. 27

8-QAM :

In the 8-QAM the data are divided into groups of 3 bits (Tribit), one of which varies the amplitude of the carrier, the last two the phase. The modulated signal can take 4 different phases and 2 different amplitudes, for a total of 8 different states .

16-QAM :

In the 16-QAM the data are divided into groups of 4 bits (Quadbit). The 16 possible combinations change amplitude and phase of the carrier, which can take 16 different states.

N-QAM :

At the moment we reach to a data subdivision into groups of 9 bits, obtaining constellations with 512 modulation points.

Main aspects

- The main aspects characterizing the QAM are:
- Applications in modems for high speed data transmission (ITU-TV22bis, V29, V32, V32bis, V33, V34, V34bis, BELL 209) and digital radio transmission. It needs circuits of high complexity
- Possibility of error higher than the PSK called F_b the bit transmission speed and "n" the number of bits. considered for the modulation, the minimum spectrum B_w of the modulated signal is equal to F_t/n

Name of the experiment: Investigation of QPSK modulation and demodulation using ST2112 QAM trainer kit.

Aim of the experiment: Investigation of QPSK modulation and demodulation using ST2112 QAM trainer kit.

Apparatus Required:

1. ST2112 trainer kit
2. Digital storage oscilloscope
3. path boards
4. power supply.

Theory:

Phase Shift Key (PSK):

In this kind of modulation, the sine carrier takes 2 or more phase values, directly determined by the binary data signal (phase modulation) or by the combination of a certain number of bits of the same data signal (N-phase modulation).

In binary PSK (BPSK), the sine carrier takes 2 phase values determined by the binary data signal A modulation technique is one using a balanced modulator is -the direct or inverted (in shift of 180°) input carrier, as function of the data signal.

The main aspects of characterizing the BPSK are:

- Use of digital radio transmission
- It requires circuits of analog - high amplitude
- High possibility of errors but lower than FSK
- If f_b is the bit transmission speed, the minimum spectrum B_{min} of

the modulated signal is higher than f_b .

4-phase PSK modulation:

In Quadrature PSK (QPSK) the sine carrier takes 4 phase values, separated by 90° and determined by the combinations of bit pair (Dbit) at the binary data signal. The data are coded into Dbit by a circuit generating,

- A data signal ϕ_1 (in phase) consisting of voltage levels corresponding to the value of the first bit of the considered pair, for a duration equal to 2 bit intervals.
- A data ϕ_2 (quadrature) consisting of voltage levels corresponding to the value of the second bit of the pair, for duration equal to 2 bit intervals.

Main aspects:

- Application in data transmission modems and digital radio transmission.
- It needs circuits of high complexity.
- Possibility of errors lower than FSK but higher than QPSK.
- If f_b is the bit transmission speed, the minimum spectrum B_m of the modulated signal is equal to $f_b/2$.
- The transmission efficiency, defined as the ratio between f_b/B_m is equal to 2.

Procedure:

1. Ensure the following initial conditions on signal train:

 - a. S1, S3, S4, S5, S6, S7, S8 should be in the off mode.
 - b. Power supply should be off.

2. Switch on the power supply.

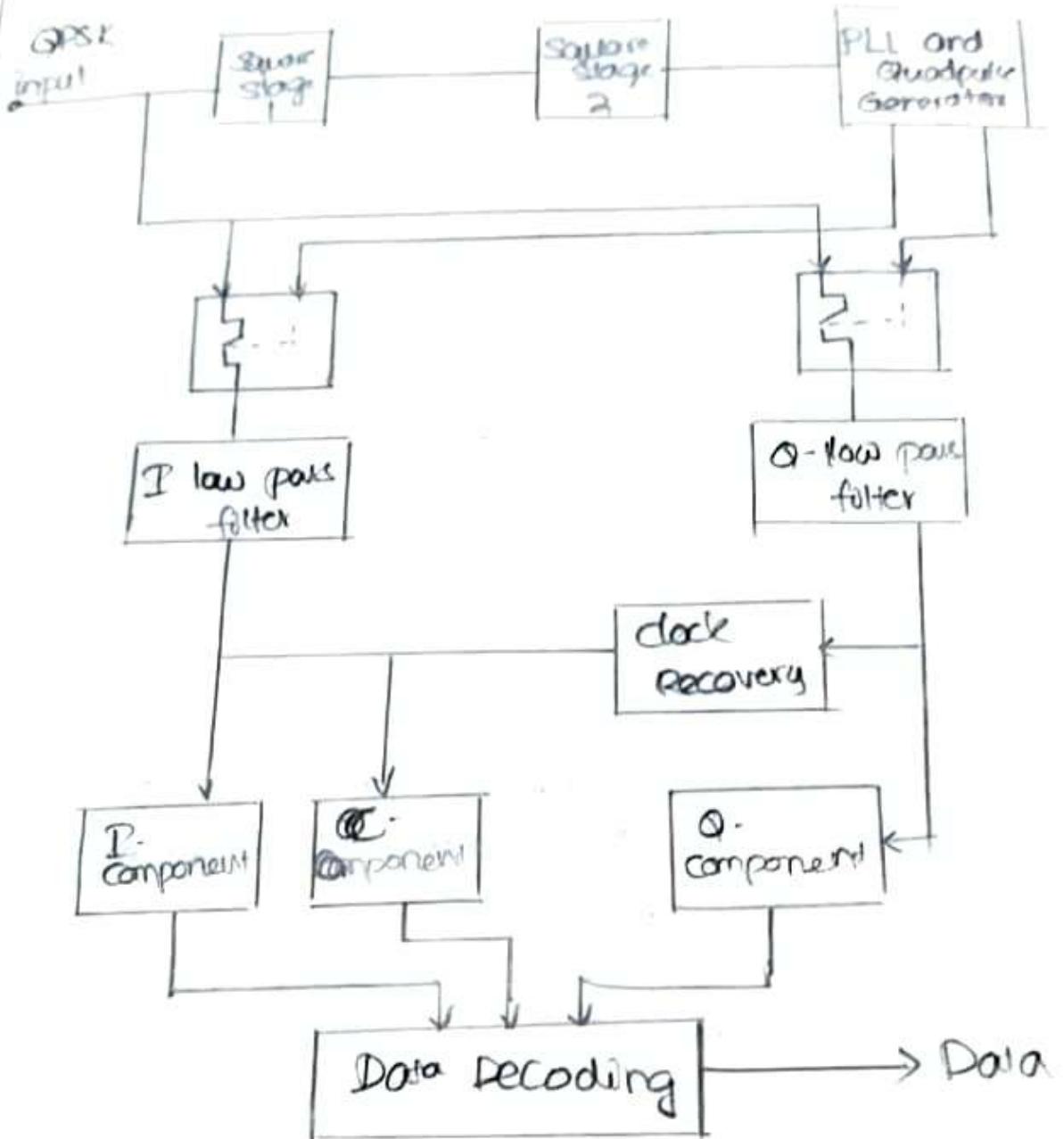
3. Connect TP6 on channel 1 & TP7 on channel 2 of oscilloscope ; you will observe 1KHz sine & cosine wave.
4. Set PA & Q channel data with help of DIP switch SW5, SW6, SW7.
As there are 2 bits data available on the trainer so, first bit is 1 bit & the second bit is 1 bit. Select combination according to your requirement. For example:
 $SW5 = 11\ 0000\ 10$
 $SW6 = 0100\ 1010$
 $SW7 = 00\ 10\ 0001$
5. Switch ON all the DIP switches on SW3.
6. Now press SW8 which is reset switch then press SW4 which is start.
7. Now, connect channel 1 of oscilloscope to TP2 & channel 2 to TP1. We can observe clock & data.
8. Now observe QPSK modulated signal with respect to data. Connect channel 1 to TP1 & channel 2 to TP8. We can observe QPSK modulated signal with respect to data.
9. Turn off the power.

Conclusion:

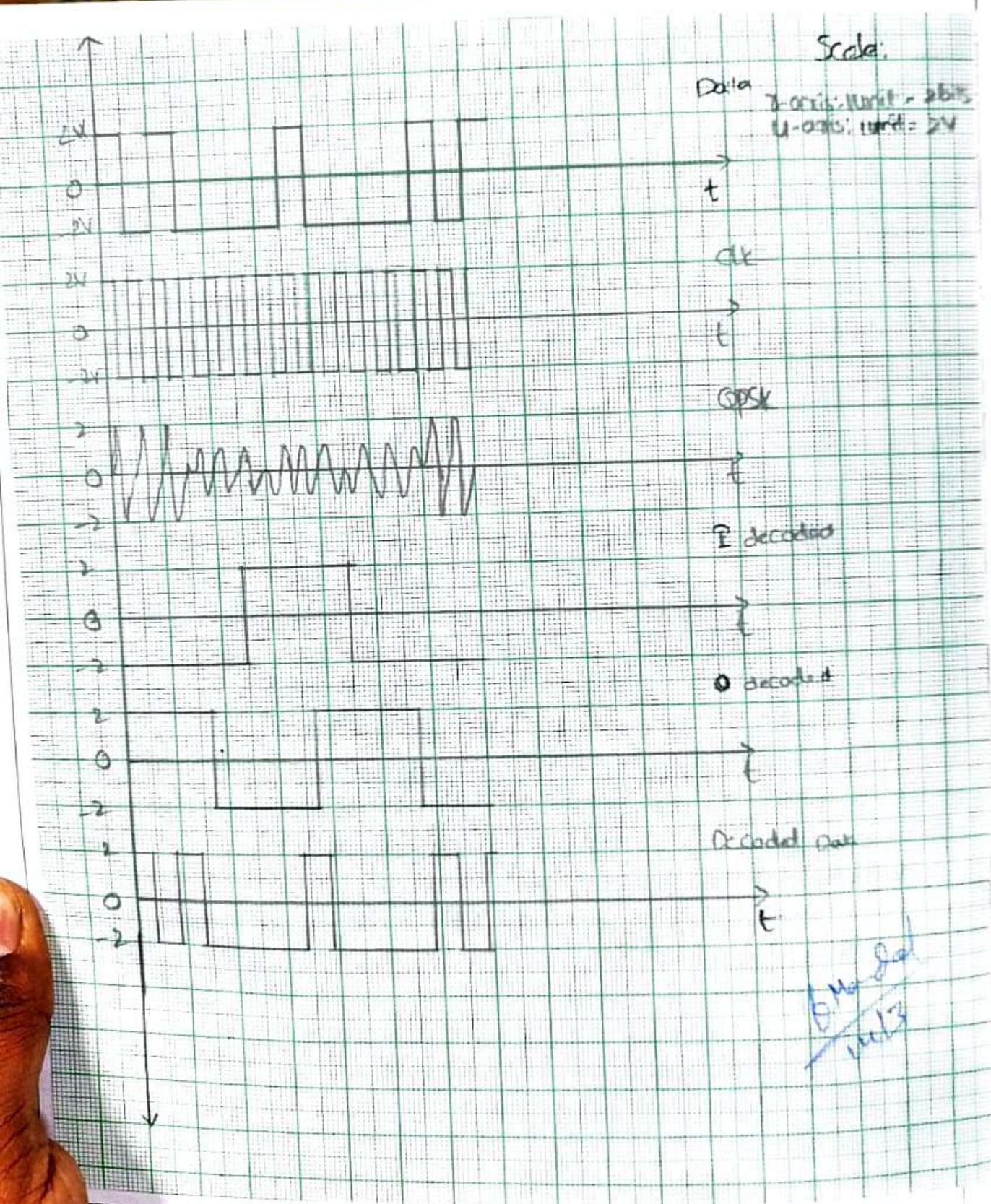
The graph for input and QPSK modulated signal was obtained & plotted. In QPSK the carrier wave takes 4 different phase values. We transmit two bits per second as 1 bit & 1 bit. Thus, bandwidth required in QPSK is less; i.e., half times the bandwidth required in PSK.

Precautions:

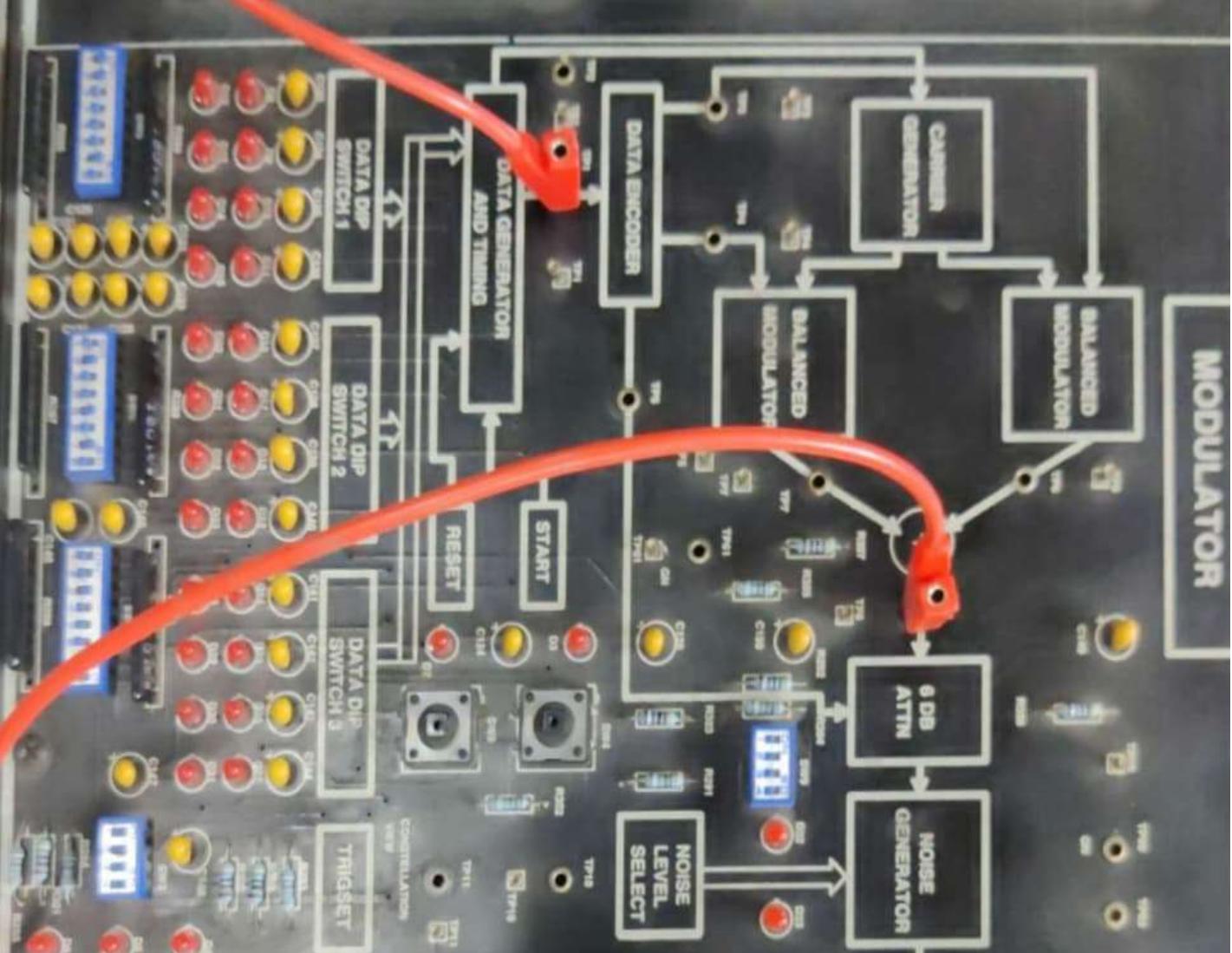
1. Make sure the SW3, SW5, SW6, SW7, SW8 are off initially.
2. The graph must be plotted carefully w.r.t initial input data.



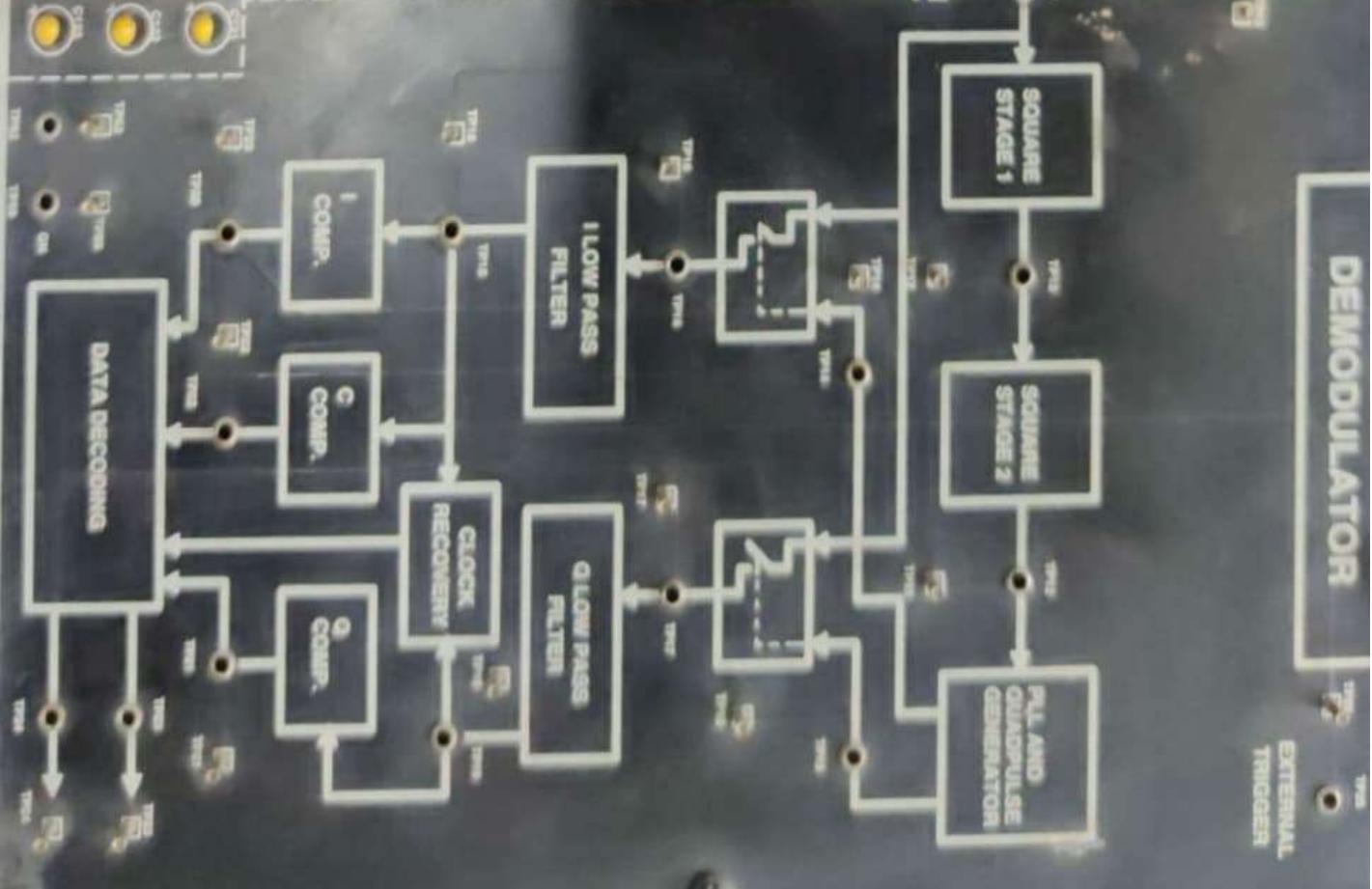
Block diagram of QPSK demodulator.



MODULATOR



DEMODULATOR



Name of the experiment: Investigation, study and analysis of QAM modulator and demodulator modulation process.

Aim of the experiment: Investigation of QAM modulation and demodulation using STALLA QAM trainer kit.

Apparatus Required:

1. STALLA trainer kit
2. Digital storage Oscilloscope
3. Patch cords
4. Power supply

Theory:

Quadrature Amplitude Modulation (QAM)

The QAM is a digital modulation where the information is contained into the phase as well as the amplitude of the transmitted carrier.

8-QAM:

In the 8QAM the data are divided into groups of 3 bits (3bit), one of which varies the amplitude of carrier, the last two the phase. The modulated signal can take 4 different phases and 2 different amplitudes, for a total of 8 different states.

Main aspects:

- Applications in moderns for high speed data transmission and digital radio transmission. It needs circuits of high complexity.
- Possibility of error higher than the PSK called for the bit transmission speed and in the noise bits. Considered for the modulation, the

- minimum spectrum BW of the modulated signal is equal to f_b/n .
- The transmission efficiency, defined as the ratio between (f_s, B_W) is equal to 'n'.

QAM modulator:

The 8QAM Signal can be seen as 4-PSK signal, whose amplitude can take 2 different values. In this way, each modulation interval depends on the state of 3 data bits ('i'; 'q'; 'c'): the first 2 ('i', 'q') determine the phase of the output signal, the third ('c') the amplitude.

8-QAM demodulator:

The 8QAM demodulator on the module uses the 4PSK demodulator to detect the signals 'i' and 'q', while the signal 'c' is obtained detecting the amplitude of the positive values of the signal 'P'. This amplitude can take 2 positive and 2 negative values, as function of the value of the signal 'C' in transmission. The demodulator 'c' detects which of the two levels is present in the coming signal. If the level is the highest, we obtain the value '1', if the value is the lowest, we obtain the value '0'.

Procedure:

1. Ensure the following initial conditions on S1012 trainer:
 - A. SW3, SW5, SW8, SW7, SW9 should be off.
 - B. Power supply should be off.
2. Switch on the power supply
3. Connect Tc on channel 1 & TP- on channel 2 of Oscilloscope; we will observe 1kHz sine and cosine.
4. Set I, Q, C channel data with the help of DIP switch SW5, SW6, SW7.
As there are 24 bits of data available on the trainer so first bit is

I bit then second bit is Q-bit, then 3rd bit is C-bit Select PA, C combination according to the requirement. Eg: SW5 = 11000110
 $SW_5 = 01011000$
 $SW_3 = 01100010$

5. Switch on all the DIP switches on SW3.
6. Now press SW8, which is reset switch then press SW4, that is start.
7. Now connect channel 1 of oscilloscope to TP2 & channel 2 to TP1, we can observe clock and data, which we have set.
8. Now to observe QAM modulated signal with respect to data, connect channel 1 to TP1 & channel 2 to TP9.
9. We can add noise by using SW9 (001/101/111).
10. To observe no demodulator section connect channel 1 of the oscilloscope to the test point TP12, we will observe square frequency.
11. To observe P switch and Q switch in the demodulator section, connect channel 1 to TP16 & channel 2 to TP15.
12. To observe PA & C demodulated signal connect oscilloscope to TP20, TP21, TP22.
13. To observe input data, output data, encoded data & decoded data we have to connect logic analyzer to test points TP1, TP2, TP3, TP4, TP5, TP6, TP21, TP22, TP23, TP24 etc..

Conclusion:

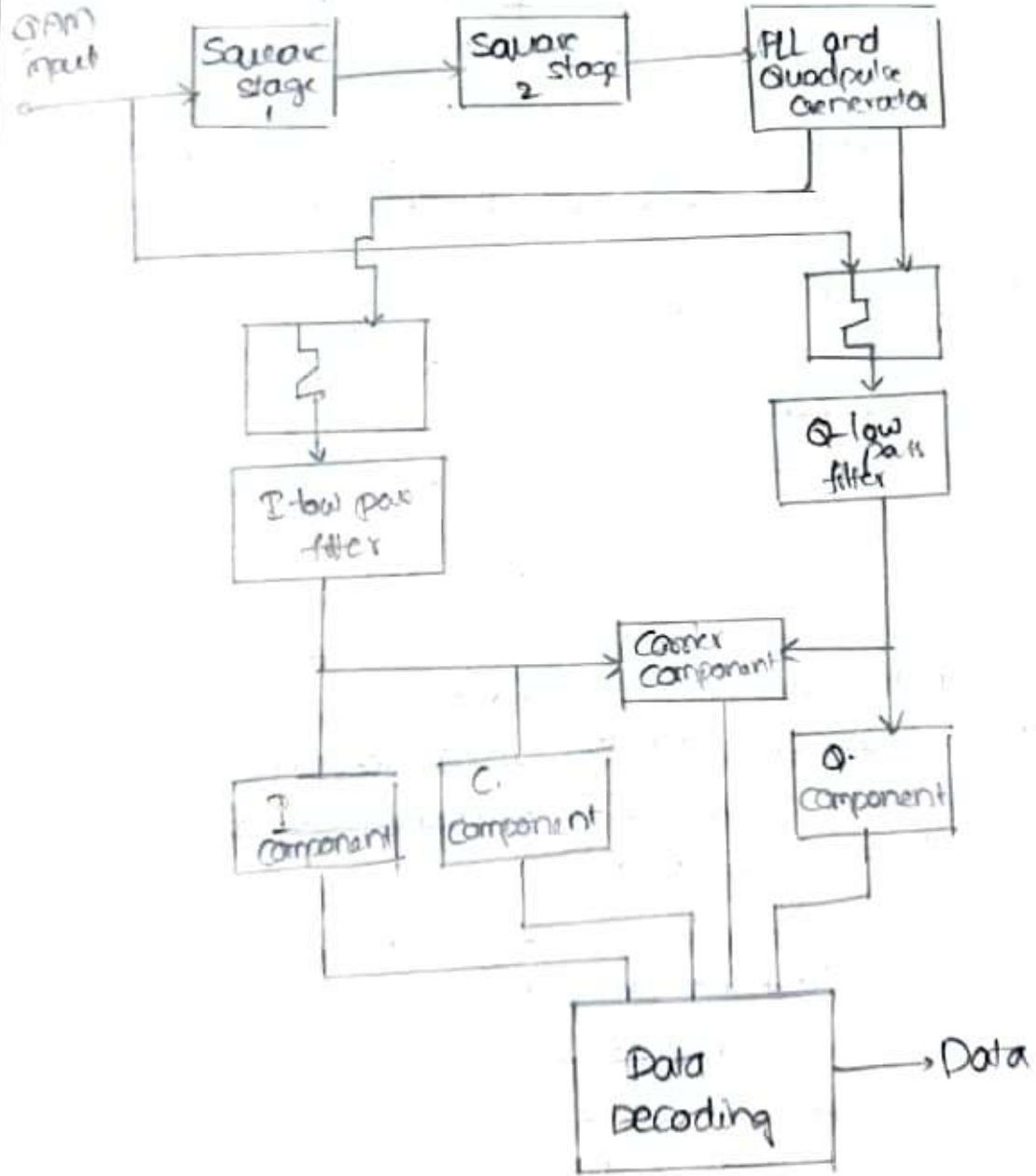
The graphs for QAM modulation and demodulation were observed and plotted. The information was found to be contained into the phase as well as amplitude of the carrier signal. Since, input data bits divided into 3 bits (I, Q, C) it is a 8-QAM. No attenuation was observed in the demodulated signal as compared to the input data.

Precautions:

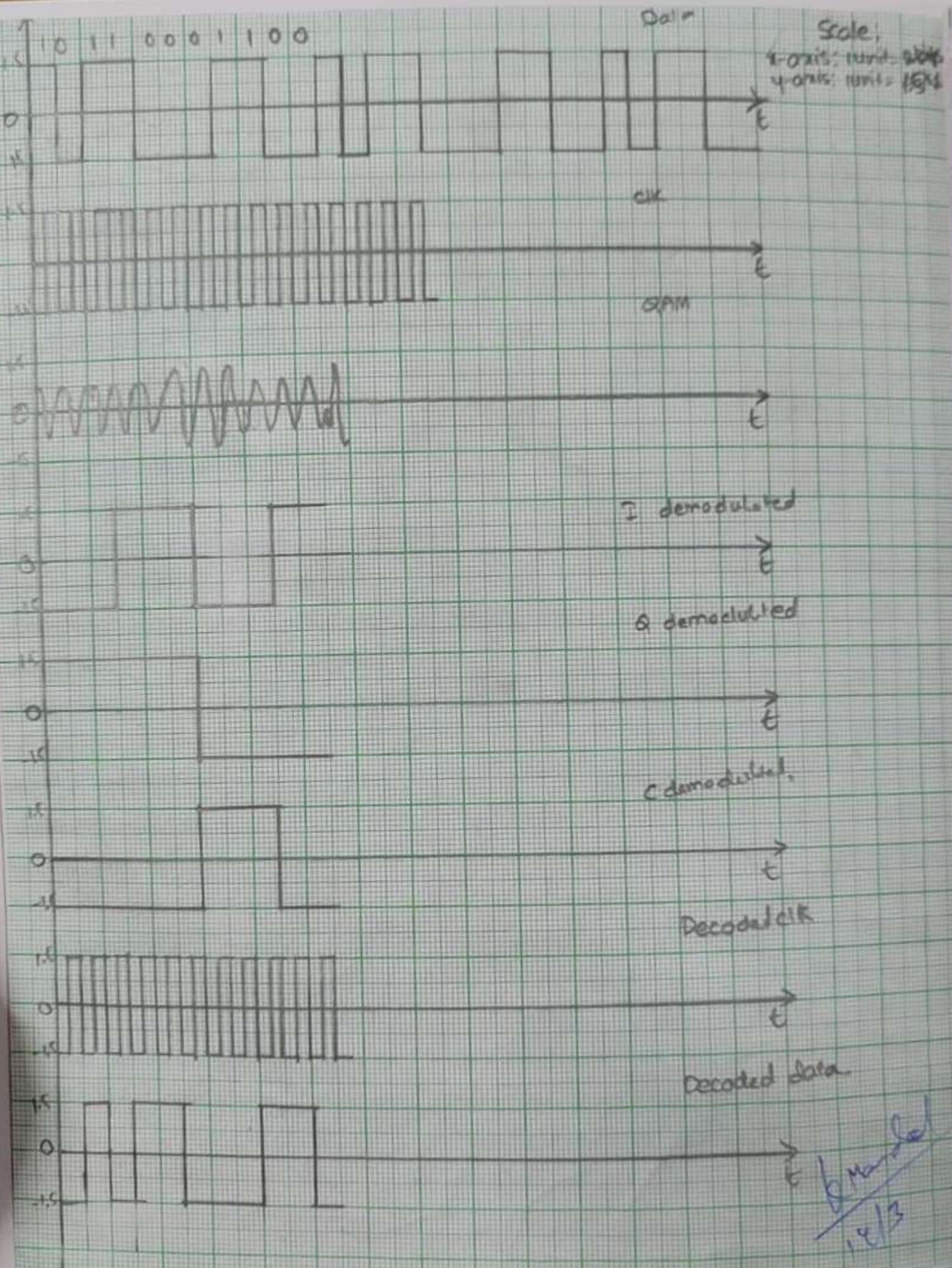
1. Make sure the SW3, SW5, SW7 & SW9 are OFF initially.
2. The graph must be plotted carefully, with respect to the initial input data.

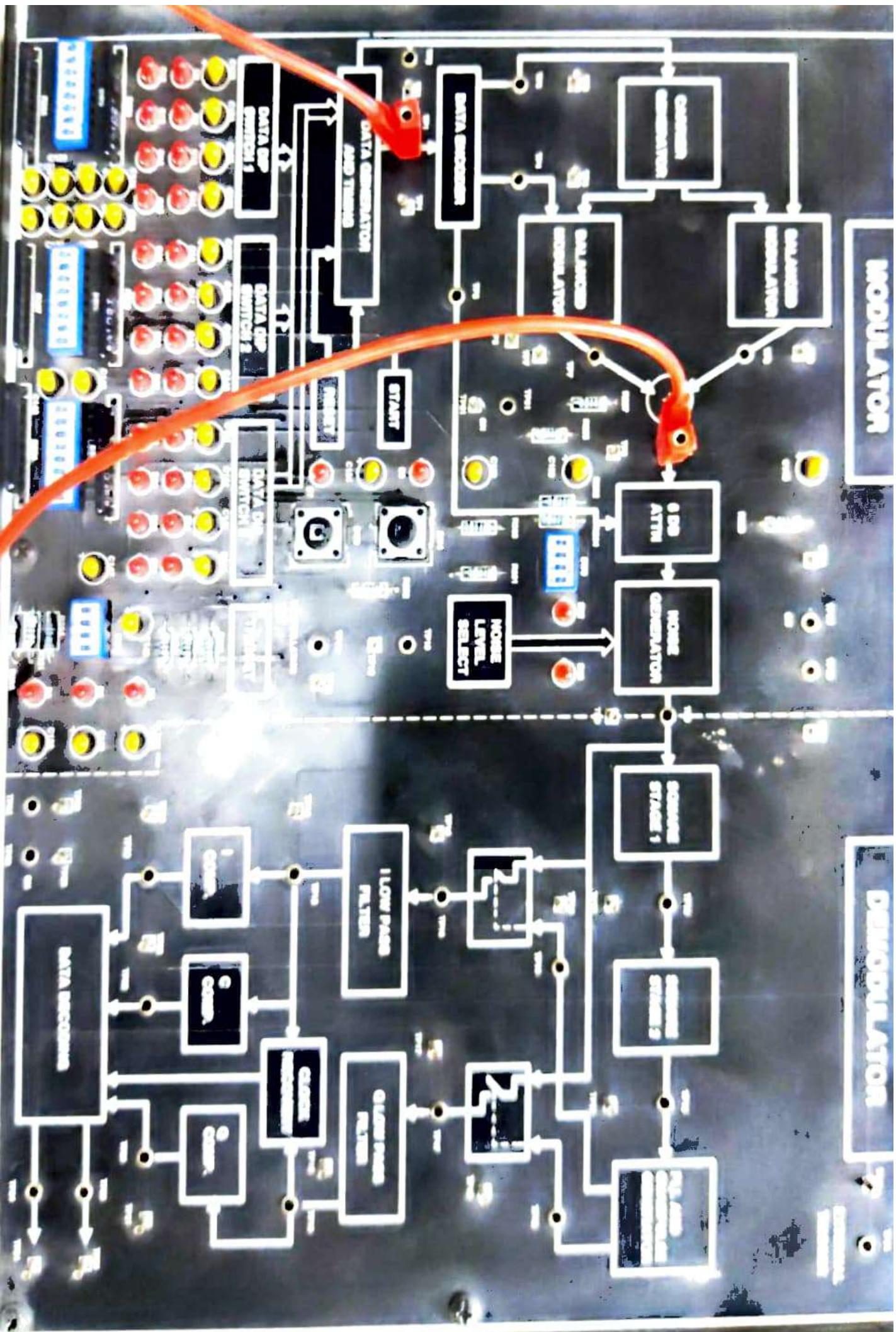


Expt. N



Block diagram of QAM demodulator





Date :

Expt. No. :

Page No. : ... 15

Experiment -6

Aim: Investigation of ASK, FSK, BPSK modulation/demodulation using trainer kit

- set up :-
- i) TechBook Board
 - ii) Power supply
 - iii) Oscilloscope
 - iv) Test probe

ASK Theory

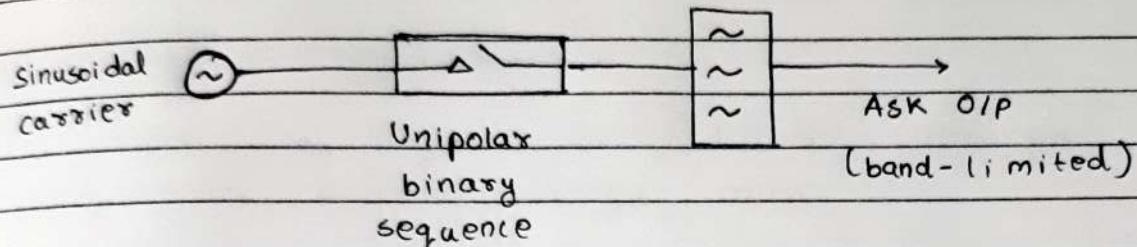
It is a type of Amplitude Modulation which requests the binary data in form of variations in the amplitude of a signal

Any modulated signal has a high frequency carrier. The binary signal when ASK modulated gives a zero value for low input while it gives the carrier output for high input

ASK Modulator

The ASK modulator block diagram comprises of the carrier signal generator, the binary sequence from the message signal and the band limited filter

Teacher's Signature :

ASK Demodulator

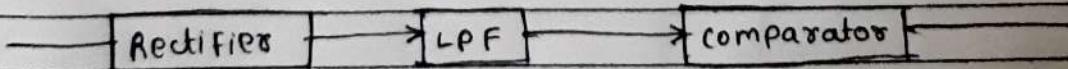
There are two types of Demodulator for ASK

- 1) Asynchronous ASK Demodulation
- 2) Synchronous ASK Demodulation

The clock frequency at the transmitted when matches with the clock frequency at receiver, it is known as synchronous method as the frequency gets synchronized otherwise it is called as Asynchronous

ASK Asynchronous demodulator

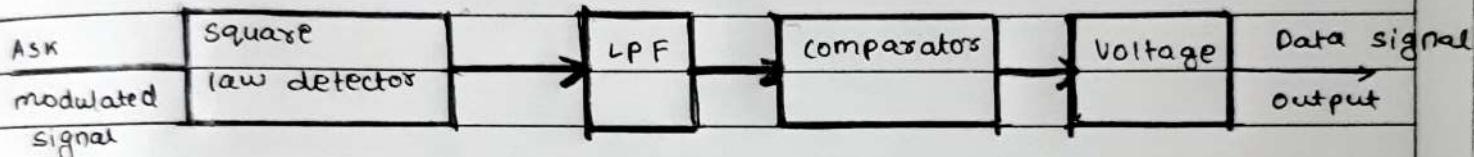
Asynchronous ASK detector consists of a half-wave rectifier, a lowpass filter, and a comparator



Expt. No. :

Synchronous ASK demodulator

It consist of square law detector, low pass filter a comparators and a voltage limiter

PSK { Phase shift keying }

It's the digital modulation technique in which the phase of the carrier signal is changed by varying the sine and cosine inputs at a particular time

These are two types of PSK

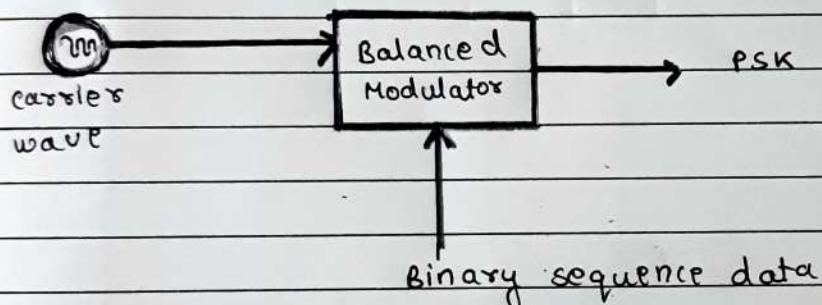
- 1) BPSK { Binary Phase shift keying)
- 2) QPSK { Quadrature Phase shift keying)

BPSK

This is also called as 2-phase PSK or Phase reversal keying. In this technique the sine wave carrier takes two phase reversal such as 0° or 180°

BPSK Modulator

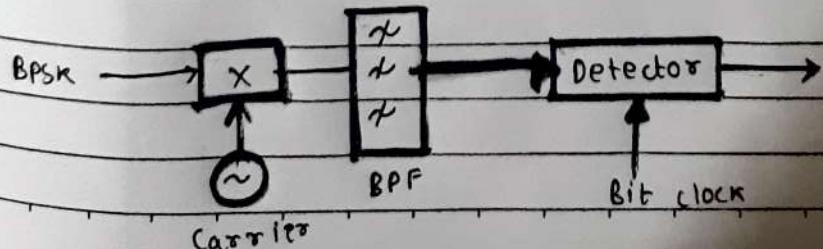
This is also called as 2-phase PSK. The BD of BPSK consists of Balance modulator which has the carrier sine wave as one input and the binary sequence as the other input.



The modulation is done using a balance modulator which multiplies the two signals applied at its input. For a zero binary input, the phase will be 0° and for a high input, the phase reversal of 180° .

BPSK Demodulator

It consists of a mixer with local oscillator circuit, a bandpass filter, a two input detector circuit



Date :

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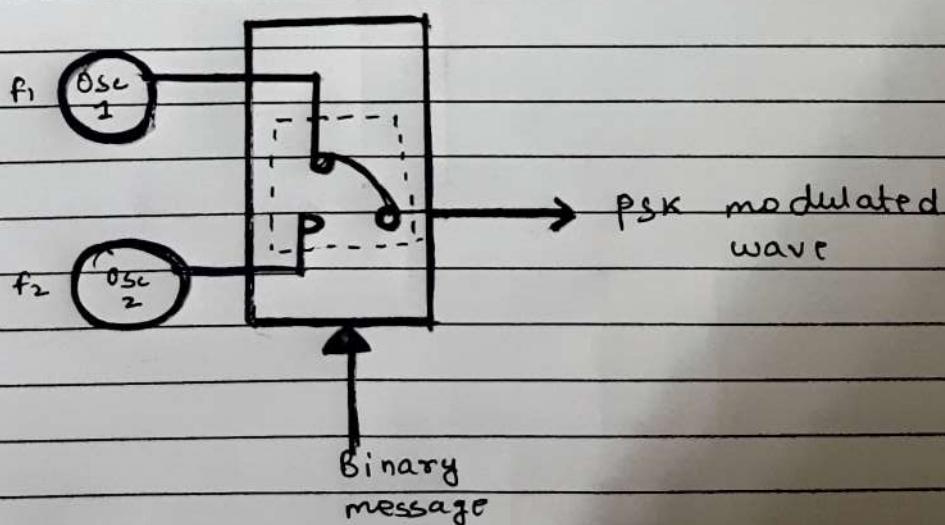
FSK {Frequency shift keying}

It is the digital modulation technique in which the frequency of the carrier signal varies according to the digital signal changes

FSK Modulator

The FSK modulator comprises of two oscillators with a clock and the input binary sequence.

The two oscillators producing a higher and lower frequency signals, are connected to a switch along with a interval clock



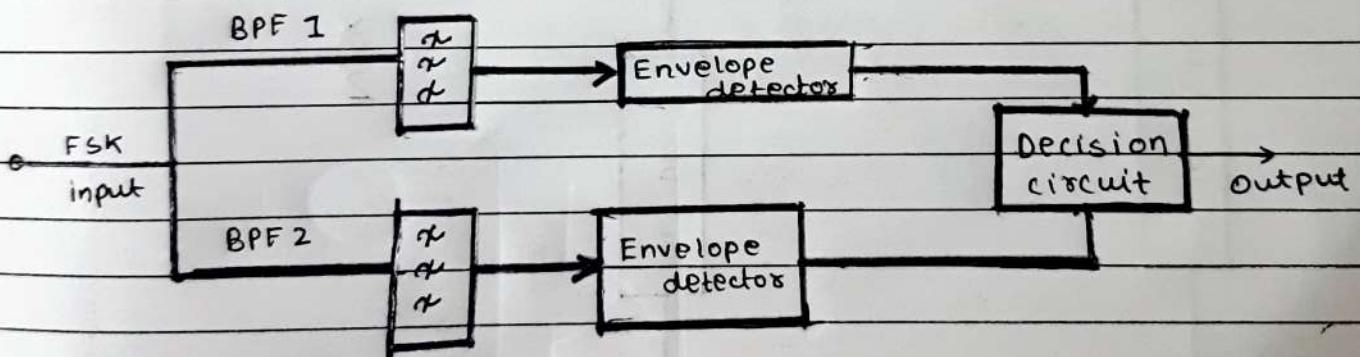
FSK Demodulator

Types of Demodulation

- i) Asynchronous demodulation
- ii) Synchronous detector

Asynchronous FSK Detector

It consists of two band pass filters, two envelope detectors and a decision circuit



Conclusion

From this experiment we understand how to modulate and demodulated the different types of Shift keying i.e ASK, PSK & FSK we also understand its theory and working of all shift keying techniques

**DEPARTMENT
OF
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DIGITAL COMMUNICATION LABORATORY

LAB INSTRUCTIONS FOR CARRYING OUT PRACTICAL
ON
INVESTIGATION OF PRACTICAL PCM SYSTEM
USING DCL03 AND DCL04 FALCON KIT



**BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI**

AIM: Investigation of practical PCM system using DCL03 and DCL04 Falcon kit

THEORY:

The sine waves (analog signal) of frequency 500Hz and 1KHz and DC signal DC1 and DC2 whose amplitude can be varied accordingly are generated onboard on DCL-03. These signals are fed to the input of the Sampling logic CH0 & CH1 and their samples are multiplexed by interleaving them properly in their assigned time slots.

The crystal oscillator generates a clock of 6.4MHz from which all the transmitter data and timing signals are derived. For fast mode operation the transmitter clock is 240KHz, and Sampling clock is 16KHz. For slow mode operation depending on jumper position the transmitter clock is 1.23Hz or 0.6Hz and sampling clock is 0.088Hz or 0.044Hz i.e. the sampling rate per channel is 11 or 22 seconds and serial data transmission rate is 813 milliseconds or 1.6 seconds.

The multiplexed data is Pulse Code Modulated before transmission. At the receiver after the pulse Code Demodulation, The recovered multiplexed data is sent to Demultiplexing Logic. The two demultiplexed samples are fed to reconstruction unit. Which consists of 4th order Low Pass Butterworth Filter, where frequency components are filtered out to recover the original base band signal at the receiver output CH0 and Ch1.

EQUIPMENTS:

Experimenter kits DCL-03 & DCL-04

Connecting chords.

Power supply

20 MHz Dual Trace Oscilloscopes.

NOTE: KEEP THE SWITCH FAULT IN OFF POSITION.

PROCEDURE:

1. Refer to the Block Diagram (Fig. 1.1) & Carry out the following connections.
2. Connect power supply in proper polarity to the kits **DCL-03** and **DCL-04** and switch it on.
3. Connect sine wave of frequency **500Hz** and **1KHz** to the input **CH0** and **CH1** of the sample and hold logic.
4. Connect **OUT 0** to **CH0 IN** & **OUT 1** to **CH1 IN**.
5. Set the speed selection switch **SW1** to **FAST** mode.
6. Select parity selection switch to **NONE** mode on both the kit **DCL-03** and **DCL-04** as shown in switch setting diagram (Fig. A.).
7. Connect **TXDATA**, **TXCLK** and **TXSYNC** of the transmitter section **DCL-03** to the corresponding **RXDATA**, **RXCLK**, and **RXSYSNC** of the receiver section **DCL-04**.
8. Connect posts **DAC OUT** to **IN** post of demultiplexer section on **DCL-04**.
9. Ensure that **FAULT SWITCH SF1** as shown in switch setting diagram (Fig. A) introduces no fault.

10. take the observations as mentioned below.
11. Repeat the above experiment with DC signal at the inputs of the Channel **CH 0** and **CH1**.
12. Connect ground points of both the kits with the help of connecting chord provided during all the experiments.

OBSERVATION:

Observe the following signal on oscilloscope and plot it on the paper.

ON KIT DCL-03 (Fig. 1.2) & (Fig. 1.3).

1. Input signal **CH0** and **CH1**.
2. Sample and Hold output **OUT 0** and **OUT 1**.
3. Multiplexer clock **CLK 1** and **CLK 2**.
4. Multiplexed data **MUX OUT**.
5. PCM Data **TXDATA**, **TXCLK**, **TXSYNC**.

CH₀ OUT, CH₁ OUT, OUT 0, OUT 1,
TX CLK, TX SYNC, SHOT 01, RE OUT,

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ON KIT DCL-04 (Fig. 1.4) & (Fig. 1.5)

1. **RXCLK**, **RXSYNC**, **RXDATA**.
2. **DAC OUT**.
3. Demultiplexer Data **CLK 1** and **CLK 2**.
4. Demultiplexed Data **CH 0** and **CH 1**.
5. Received signal **OUT 0** and **OUT 1**.

SWITCH FAULTS:

Note: Keep the connection as per the procedure. Now switch corresponding fault switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

1. Put switch 2 of **SF2 (DCL-03)** in switch Fault section to ON position. This will remove PRBS sequence from Transmitted Data. Synchronization will be only possible in case of direct connection of TXSYNC to RXSYNC. In any other case no synchronization is possible.
2. Put switch 3 of **SF2 (DCL-03)** in switch section to ON position. This will increase the duty cycle (on period) of CH0. Due to which, some portion of CH1 signals time slot. Hence demultiplexed output for CH1 is disturbed.
3. Put switch 4 of **SF2 (DCL-03)** in switch Fault section to ON position. This disable data from going to TX Data, only PRBS will be present.
4. Put switch 1 of **SF1 (DCL-04)** in switch Fault section to ON position. This will disable synch signal in Bit Synchronization. Filter output will be disturbed.
5. Put switch 2 of **SF1 (DCL-04)** in switch Fault section to ON position. This will disable clock signal for Demultiplexer. One channel output is absent and other channel output is disturbed.
6. Put switch 4 of **SF1 (DCL-04)** in switch Fault section to ON position. This will remove CH0 filter capacitor connection from ground. Filter output will be distorted.

CONCLUSION:

We conclude that at the transmitter side sampling for 500Hz and 1KHz signals is done by using 16KHz sampling clock, hereby satisfying the Nyquist criterion. Similarly the multiplexed output observed in the oscilloscope shows the proper alignment of samples in their respective time slots.

At the receiver side the 4th order low pass butterworth filter is used as reconstruction unit, which reproduce the signals (sine wave and DC signal levels) same as that of the transmitter side. It is observed in this case, that the reconstruction sine wave has good linearity.

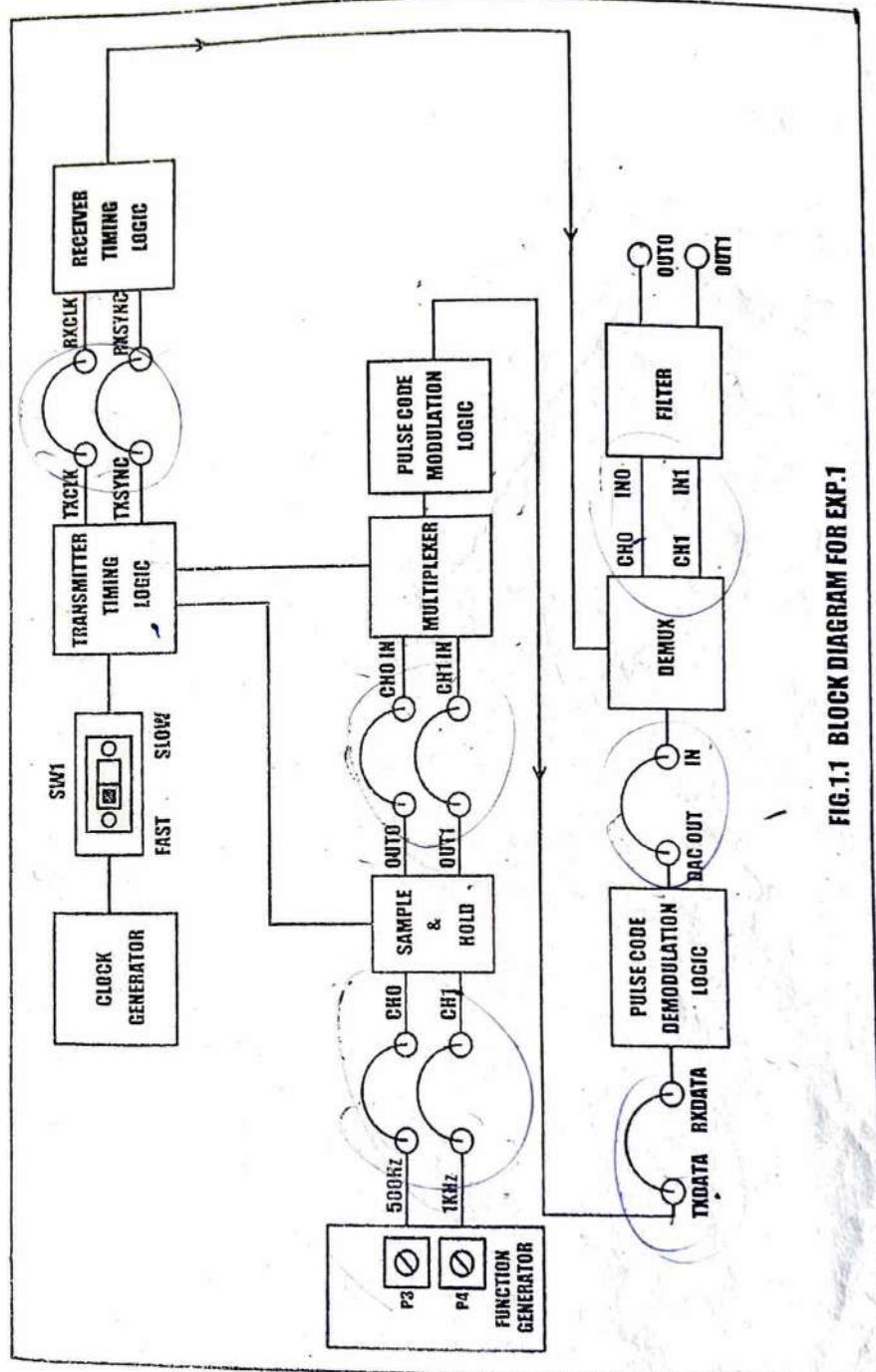
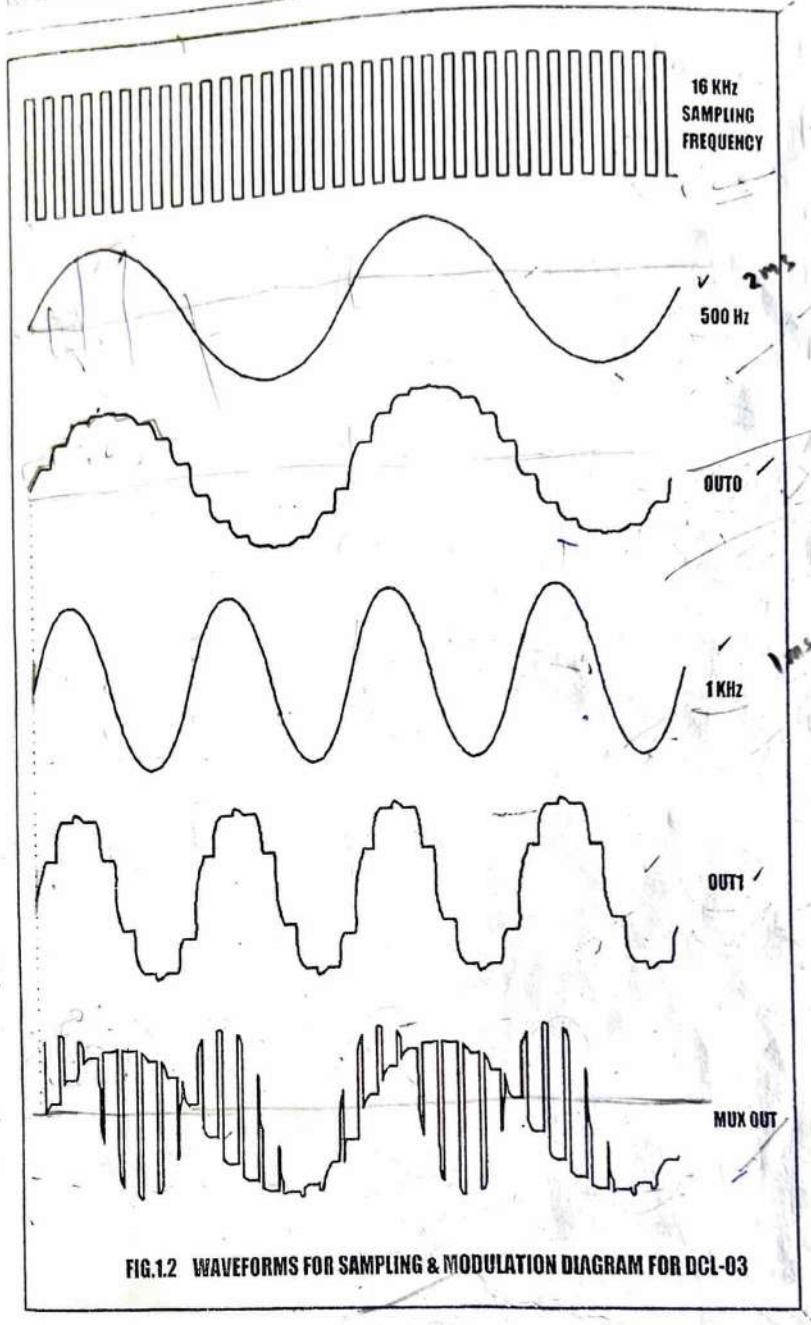


FIG.1.1 BLOCK DIAGRAM FOR EXP.1



FALCON

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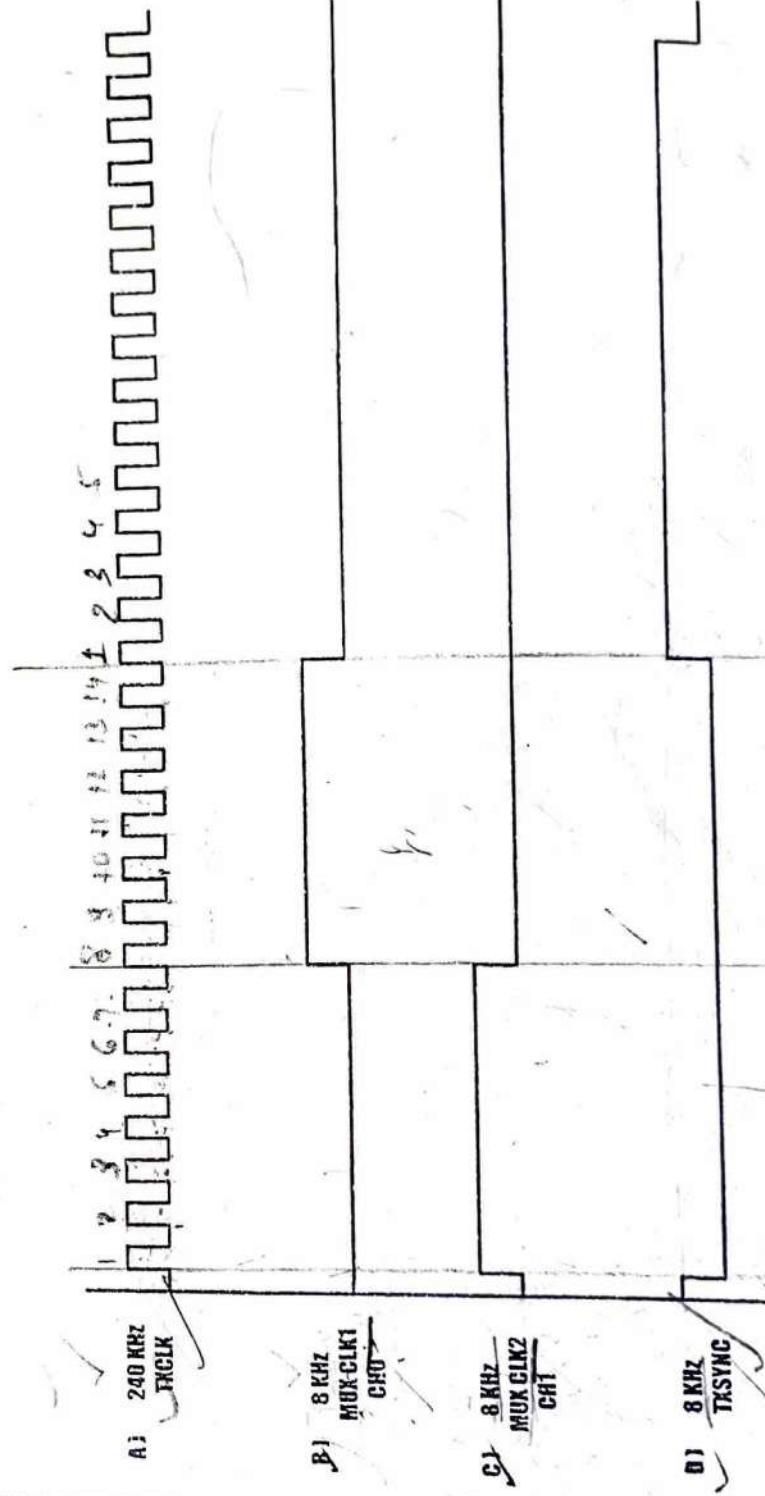


FIG.1.3 WAVEFORMS FOR TRANSMITTER TIMING DIAGRAM FOR DCL-03

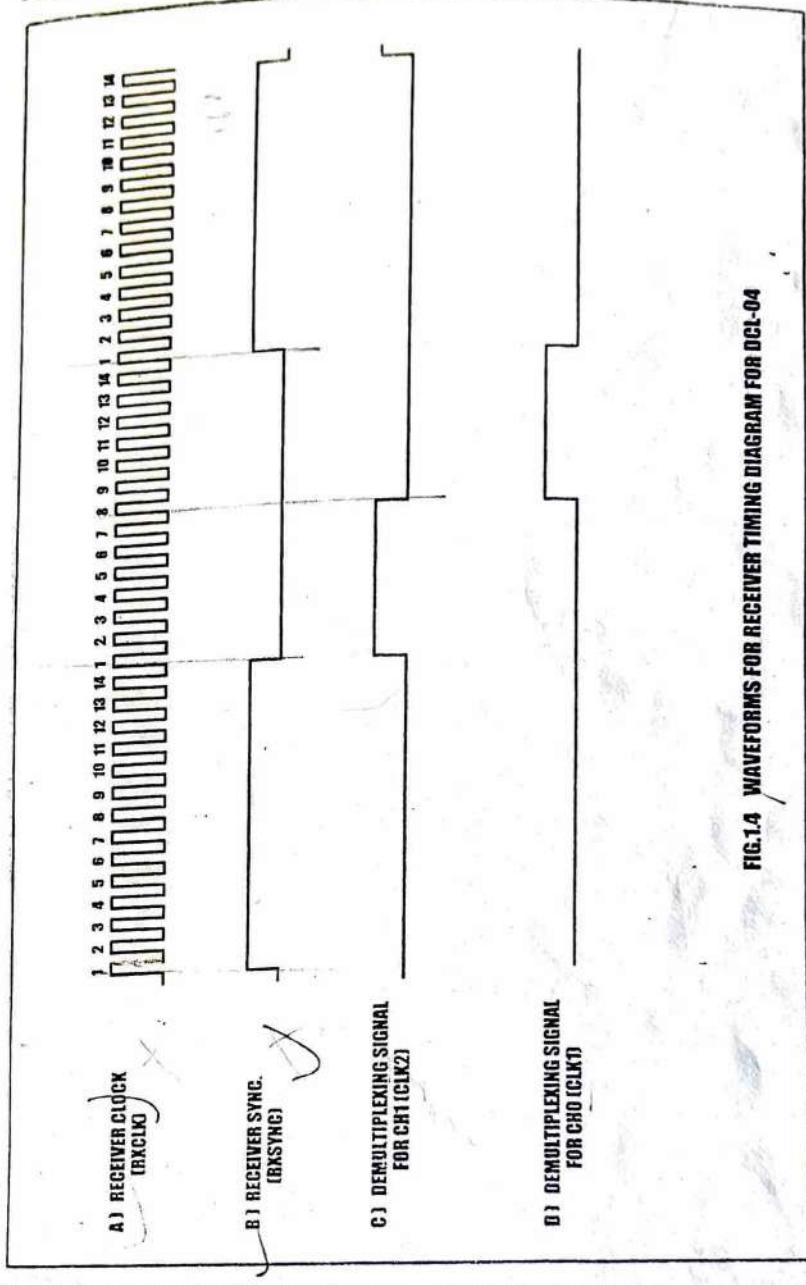


FIG.1.4 WAVEFORMS FOR RECEIVER TIMING DIAGRAM FOR DCL-04

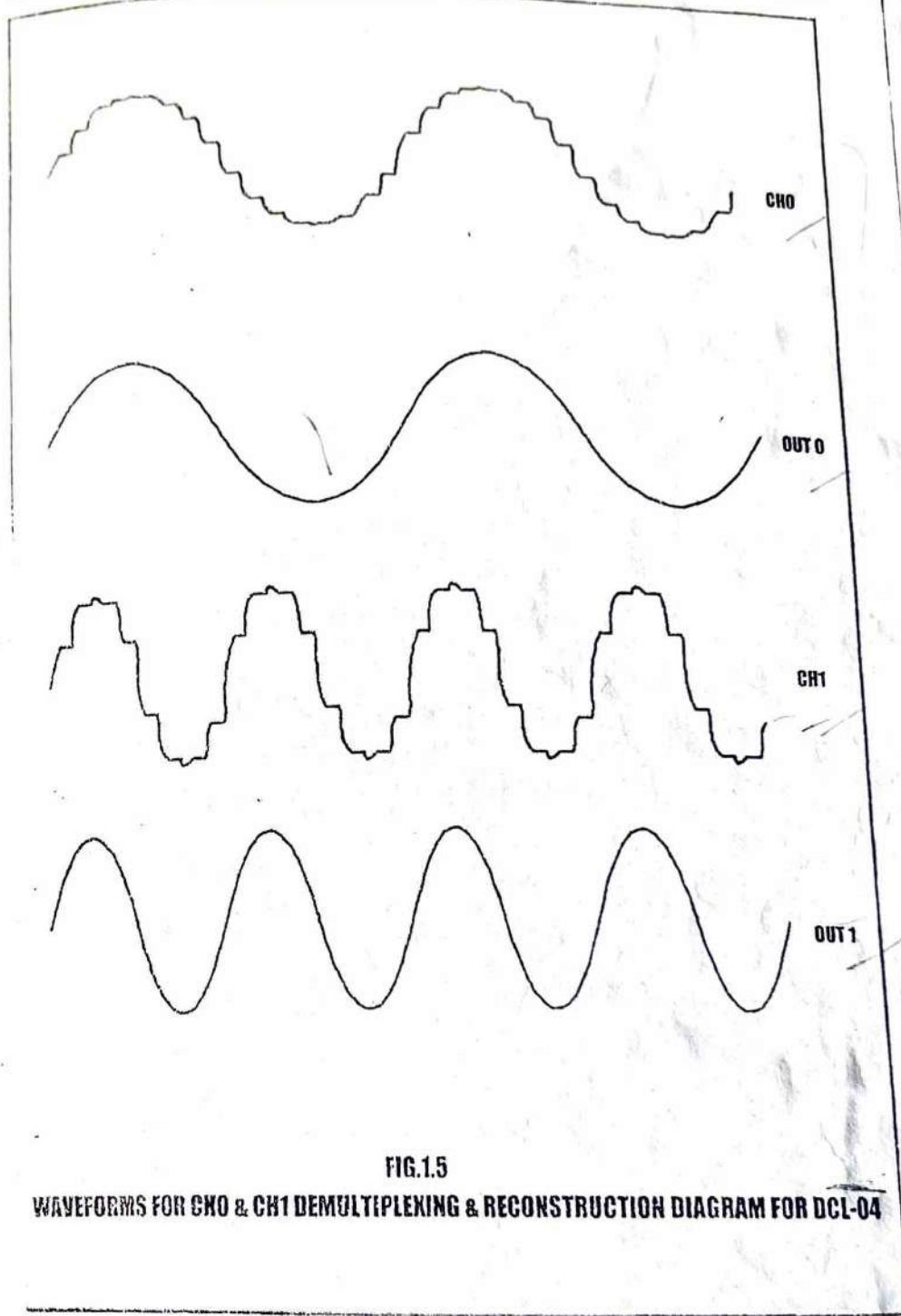
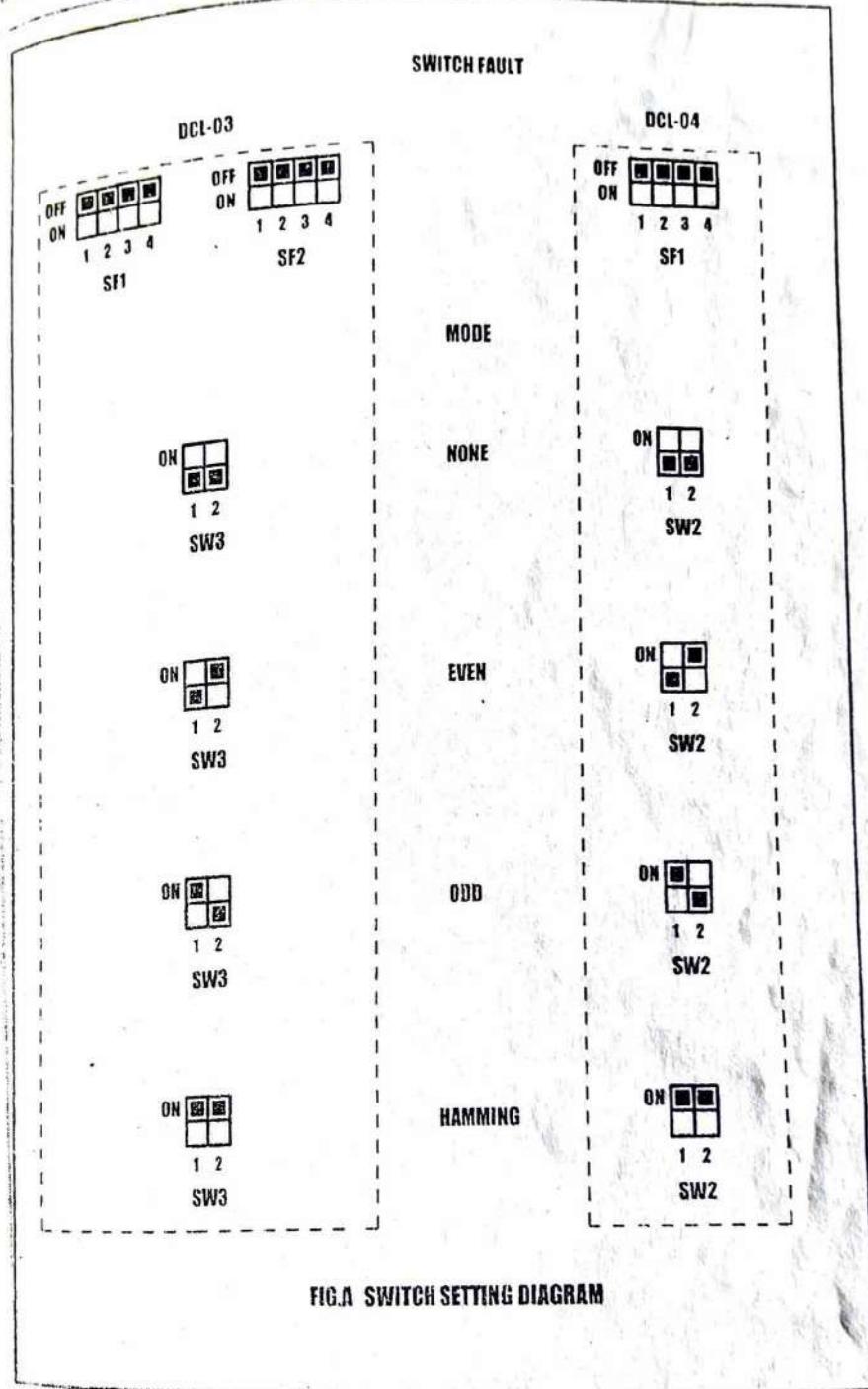
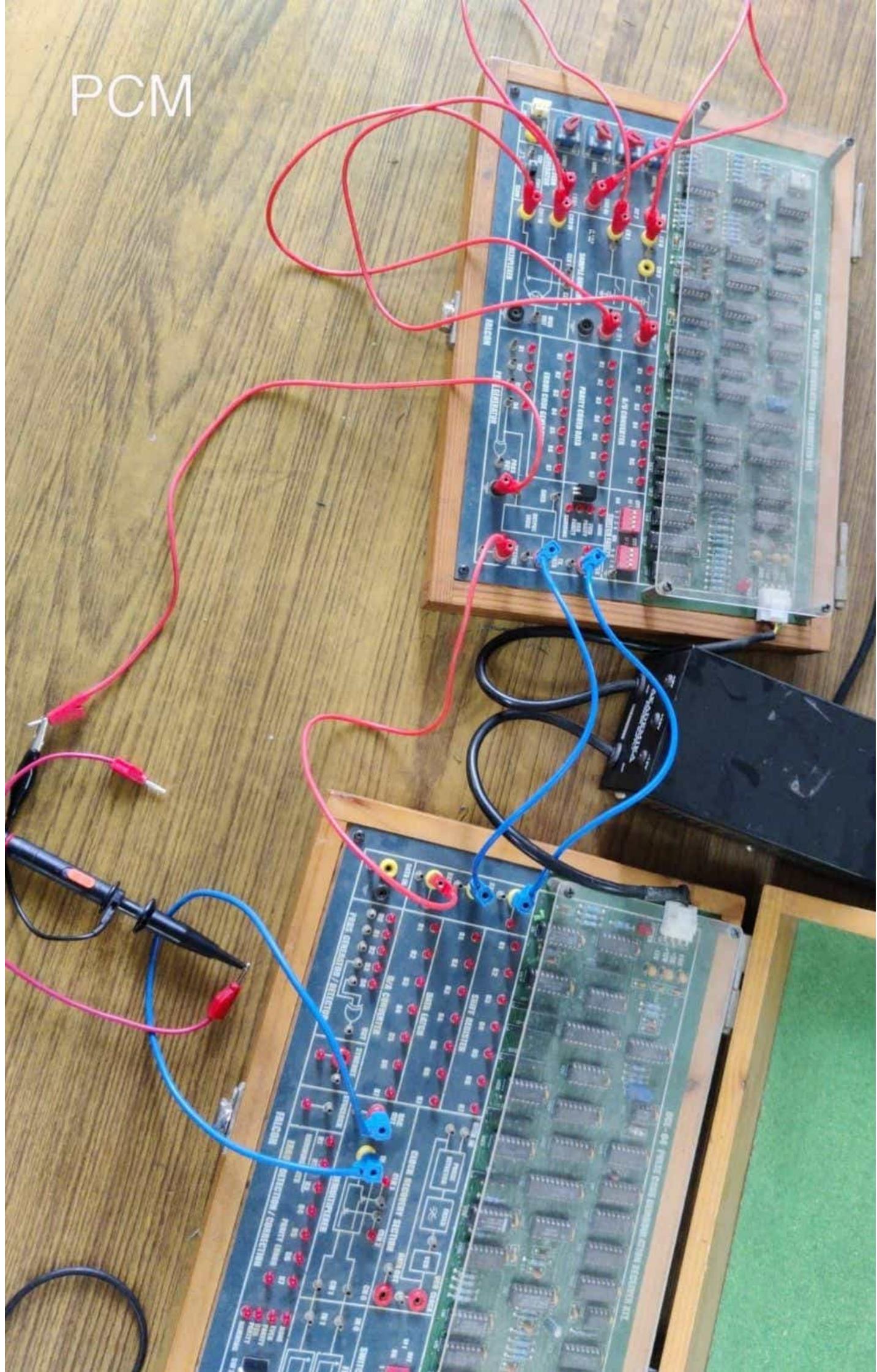


FIG.1.5
WAVEFORMS FOR CH0 & CH1 DEMULTIPLEXING & RECONSTRUCTION DIAGRAM FOR DCL-04



PCM



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LAB INSTRUCTIONS FOR CARRYING OUT PRACTICAL

ON

**INVESTIGATION OF TDM SYSTEM
USING DCL02 FALCON KIT**



**BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI**

AIM: Investigation of TDM system using DCL02 Falcon kit

THEORY:

This module basically consists of the following sections:

- a. The Onboard Function Generator.
- b. The Transmitter
- c. The Receiver with the associated synchronization circuitry.

ONBOARD FUNCTION GENERATOR:

This basically provides four Amplitude variables each (0 – 5 V) synchronized sine waves, each 250Hz, 1KHz, and 2KHz and an amplitude variable DC level (0-5V). For the generation of sine waves please refer to circuit description manual.

TRANSMITTER:

The Transmitter Section consists of four Analog Input Signals from the Function generator fed to the four channels of the Multiplexer where the signals fed are Time Division Multiplexed after undergoing the sampling. The sampling process makes the signals Pulse Amplitude Modulated. The frequencies for sampling are given from the decoder.

RECEIVER:

The Receiver Section consists of a Demultiplexer that demultiplexes the four Time Division Multiplexed signals, which it receives from the transmitter. This Demultiplexed signals are then fed to the reconstruction circuit, which is the filter section.

The receiver timing logic is very similar to the transmitter timing logic. The demultiplexed based on the control signals C0, C1, C2, C3 assigns the information to the corresponding channels. The success of the demultiplexer operation is fully dependent on how exactly, RXCH0, RXCH2, RXCH3 signals match with the TXCH0, TXCH1, TXCH2, TXCH3 signals. Thus, to ensure the proper demultiplexing, two dividers are reset by the RXCH0 signal, which corresponds with the TXCH0. The demultiplexed signals are then given to the corresponding reconstruction units.

The signal reconstruction unit is a 4th order Active Low Pass Butterworth Filter provided for each receiver channel. They filter out the sampling frequency and their harmonics from the demultiplexed signal and recover the base band by an integrate action. The cut-off frequency of the 4th Order Low Pass Butterworth Filter is 3.4KHz.

EQUIPMENTS:

Experimenter kit DCL-02
Connecting Chords
Power supply
20 MHz Dual trace oscilloscope.

NOTE: KEEP ALL THE SWITCH FAULTS IN ON POSITION.

PROCEDURE:

1. Refer to the Block Diagram (Fig. 1) & carry out the following connections and switch settings.
2. Connect power supply in proper polarity to the kit DCL-02 & switch it on.
3. Connect **250Hz, 500Hz, 1KHz**, and **2KHz** sine wave signal from the Function Generator to the multiplexer input channel **CH0, CH1, CH2, CH3** by means of the connecting chords provided.
4. Connect the multiplexer output **TXD** of the transmitter section to the demultiplexer input **RXD** of the receiver section.
5. Connect the output of the receiver section **CH0, CH1, CH2, CH3** to the **IN0, IN1, IN2, and IN3** of the filter section.
6. Connect the sampling clock **TX CLK** and channel Identification Clock **TXSYNC** of the transmitter section to the corresponding **RX CLK** and **RX SYNC** of the receiver section respectively.
7. Set the amplitude of the input sine wave as desired.
8. Take observations as mentioned below.

OBSERVATIONS:

Observe the following waveforms on oscilloscope and plot it on the paper.

- a. Input Channel **Ch0, Ch1, CH2, CH3**.
- b. Channel Selection Signal.
- c. **TX CLK** and **RX CLK**.
- d. Channel Identification Signal **TX SYNC And RX SYNC**.
- e. Multiplexer output **TXD**.
- f. Demultiplexer input **RXD**.
- g. Demultiplexer output **CH0, CH1, CH2, and CH3**.
- h. Reconstruction signal **OUT0, OUT1, OUT2, OUT3**.

SWITCH FAULTS:

Note: Keep the connection as per the procedure. Now switch corresponding faults switch button in ON condition & observe the different effect on the output. The faults are normally used one at a time.

1. Put switch 1 of **SF1** in Switch Fault section to **ON** position. This will short circuit 250Hz & 500Hz sine waves. We will get mixing of both the signals.

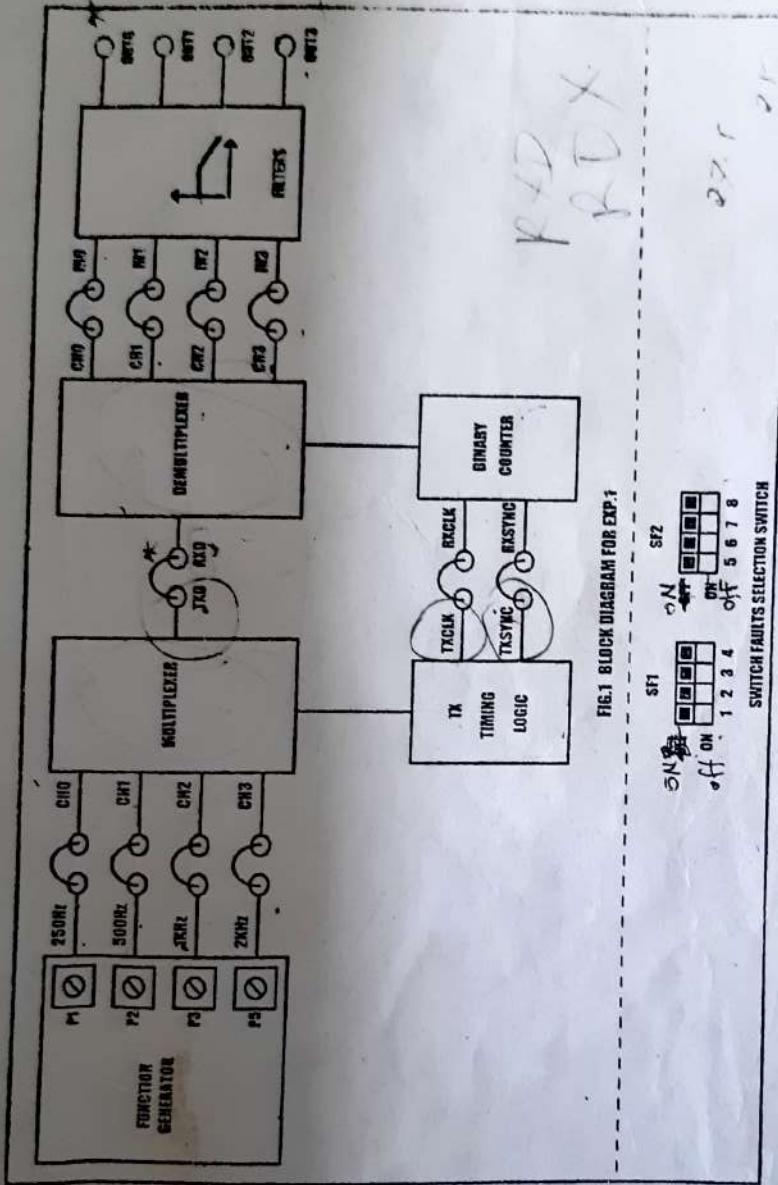
120V
80V
60V
20V

767.

2. Put switch **4** of **SF1** in switch Fault section to **ON** position. This will short MSB of ladder network used for 500Hz sine wave generation. Shape of this sine wave changes.
3. Put switch **5** of **SF2** in switch Fault section to **ON** position. This will remove TXCH0 signal. This will remove all receiver-decoding pulses. Receiver outputs are disturbed.
4. Put switch **6** of **SF2** in switch Fault section to **ON** position. This will remove control signal of first channel in demultiplexer section. Output for channel Zero is mixing of all signals.
5. Put switch **8** of **SF2** in switch Fault section to **ON** position. This will remove bypass capacitor from filter of third channel. Distorted output at channel three.

CONCLUSION:

In this experiment, the transmitter clock and the channel identification clock (sync) are directly linked to the receiver section. Hence transmitter and receiver are synchronized and proper reconstruction of the signal is achieved.



DEPARTMENT
OF
ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL COMMUNICATION LABORATORY

LAB INSTRUCTIONS FOR CARRYING OUT PRACTICAL
ON
**INVESTIGATION OF DELTA MODULATION AND ADAPTIVE
DELTA MODULATION SYSTEM USING DCL07 FALCON KIT**



BIRLA INSTITUTE OF TECHNOLOGY
MESRA, RANCHI

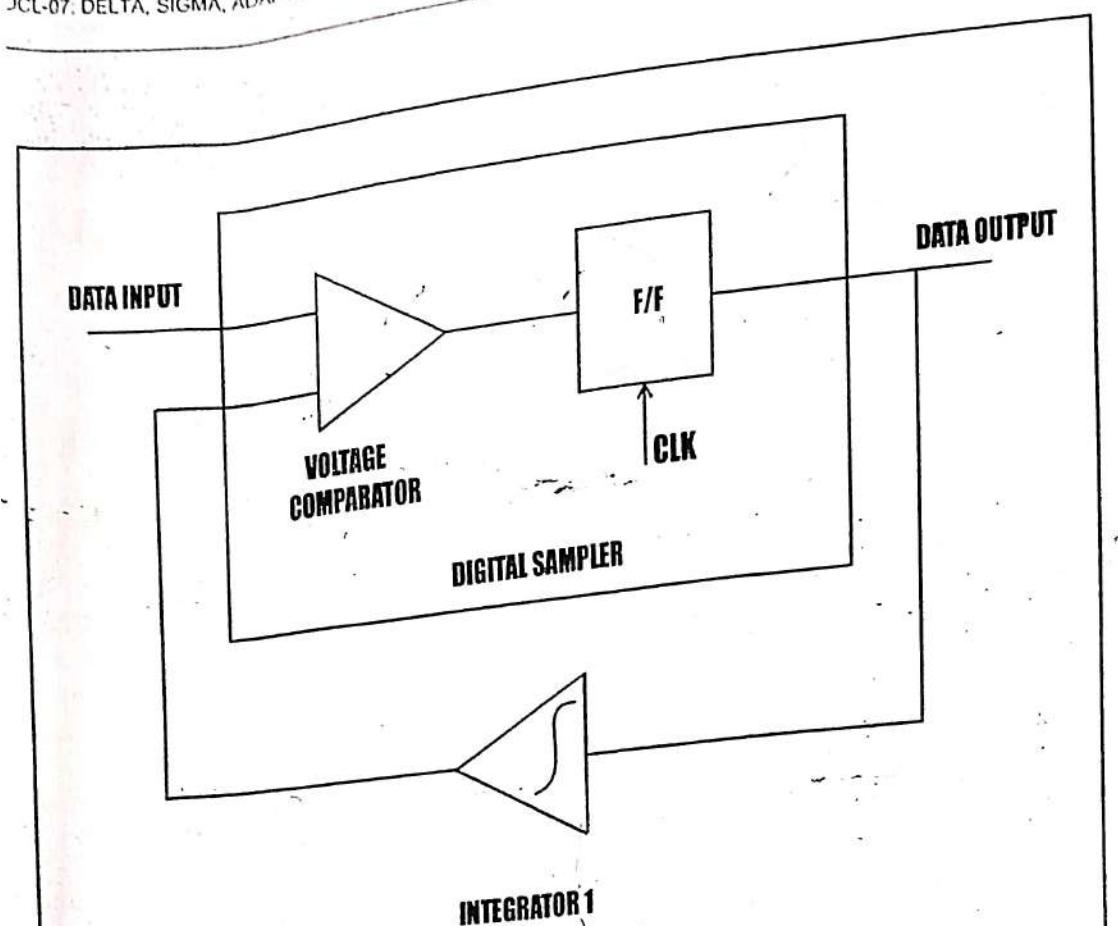


FIG.1.1 DELTA MODULATOR

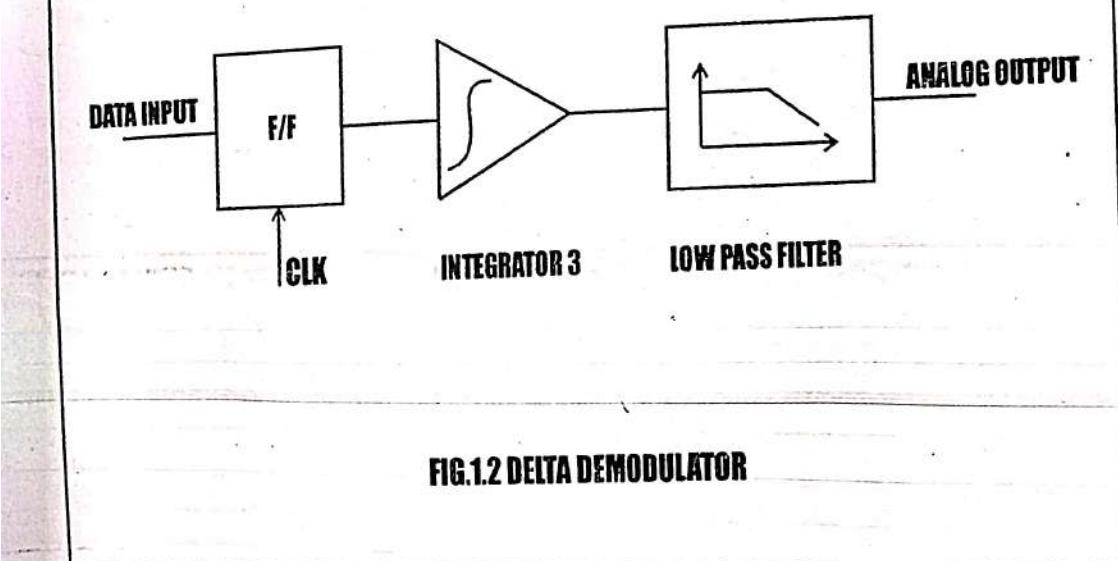


FIG.1.2 DELTA DEMODULATOR

EXPERIMENT NO: 1

NAME:

DELTA MODULATION AND DEMODULATION.

OBJECTIVE:

Study of Delta Modulation and Demodulation.

THEORY:

DELTA MODULATION:

Delta modulation is the differential pulse code modulation scheme in which the difference signal is encoded into just a single bit. In digital modulation system, the analog signal is sampled and digitally coded. This code represents the sampled amplitude of the analog signal. The digital signal is sent to the receiver through any channel in serial form. At the receiver the digital signal is decoded and filtered to get reconstructed analog signal. Sufficient number of samples are required to allow the analog signal to be reconstructed accurately. Delta modulation is a process of converting analog signal into one bit code, means only one bit is sent per sample. This bit indicates whether the signal is larger or smaller than the previous samples. The advantage of DM is that the modulator and demodulator circuits are much simpler than those used in traditional PCM.

Delta modulation is an encoding process where the logic levels of the transmitted pulses indicate whether the decoded output should rise or fall at each pulse. This is a true digital encoding process as compare to PAM, PWM and PPM.

If signal amplitude has increased in DM then modulated output is a logic level 1. If the signal amplitude has decreased the modulator output is logic level 0. Thus the output from the modulator is a series of zeroes and ones to indicate rise and fall of the waveform from the previous value.

The block diagram (Fig. 1.1) of Delta Modulation illustrates the components at the transmitter end. It consists of Digital Sampler and an Integrator at the feedback path of Digital sampler. Let assume that the base band signal $a(t)$ and its quantized approximation $i(t)$, are applied as inputs to the comparator. A comparator as its name suggests simply makes a comparison between inputs. The comparator has one fixed output $c(t)$ when $a(t) > i(t)$ and the different output when $a(t) < i(t)$ the comparator output is then latched in to a D-flip/flop which is clocked by the selected transmitter clock. Thus the output of the D-flip/flop is latched 1 or 0 synchronous with the clock edge. This binary data stream is transmitted to the receiver and is also fed to the input of integrator. The integrator output is then connected to the negative terminal of voltage comparator, thus completing the modulator circuit. The waveform of the Delta Modulator is as shown in the figure 1.5.

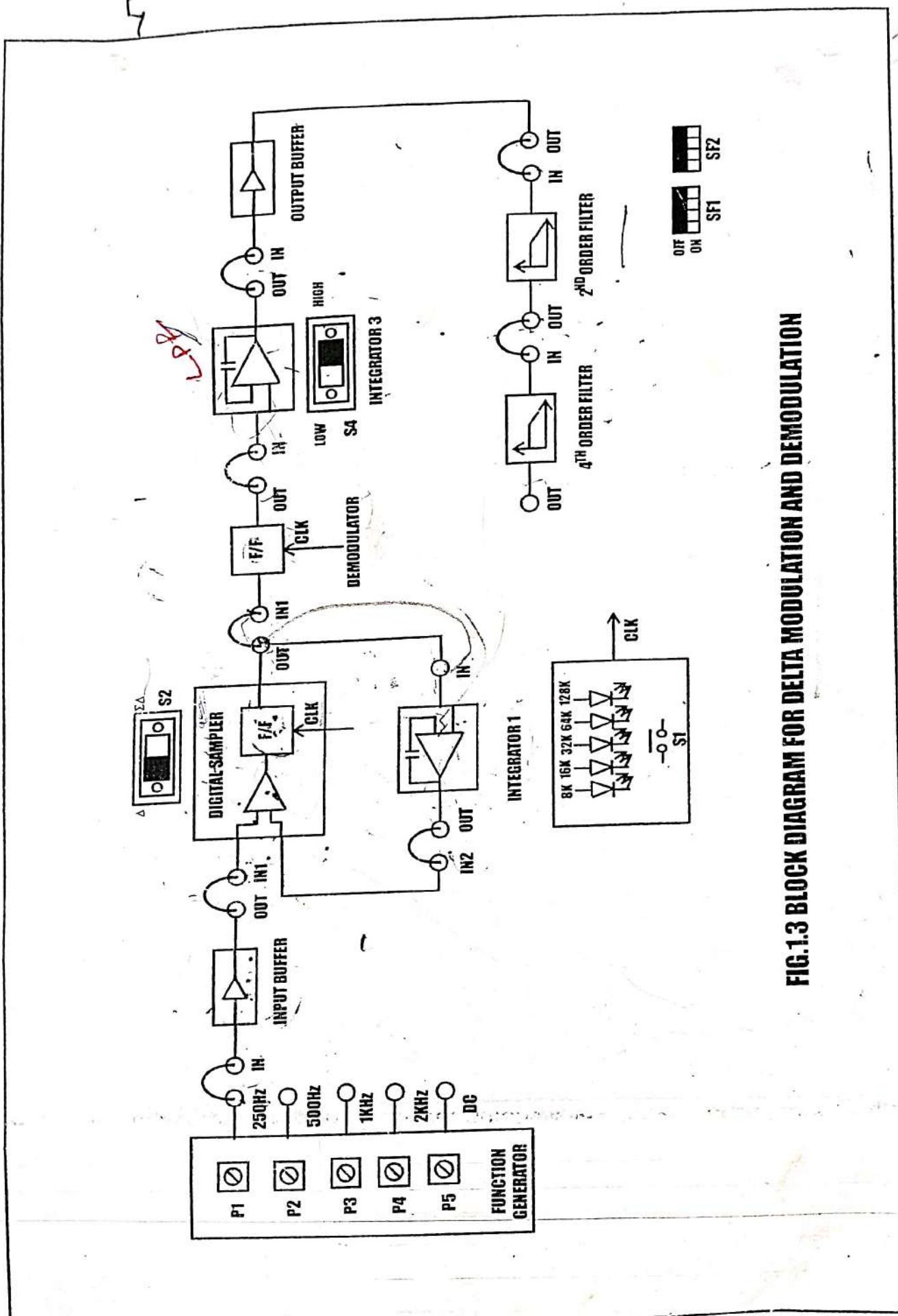


FIG.1.3 BLOCK DIAGRAM FOR DELTA MODULATION AND DEMODULATION

DELTA DEMODULATOR:

The Delta Demodulator (Fig. 1.2) consists of a D-flip/flop, followed by an integrator and a 2nd and 4th order low pass butterworth filter. The Delta Demodulator receives the data stream from D-flip/flop of Delta Modulator. It latches this data at every rising edge of receiver clock. This data stream is then fed to integrator, its output tries to follow the analog signal in ramp fashion and hence is a good approximation of the signal itself. The integrator output contains sharp edges, which is smoothed out by the 2nd order, and 4th order low pass butterworth filter whose cut-off frequency is just above the audio band.

The practical use of Delta Modulation is limited due to following drawbacks:

- i) NOISE: A noise is defined, as any unwanted random waveform accompanying the information signal. When the signal is received at the receiver irrespective of any channel it is always accompanied by noise.
- ii) DISTORTION: Distortion means that the receiver output is not the true copy of the analog input signal at the transmitter. In Delta modulation, when the analog signal is greater than the integrator output the integrator ramps up to meet the signal. The ramping rate of integrator is constant. Therefore if the rate of change of analog input is faster than the ramping rate, the modulator is unable to catch up with the input signal. This causes a large disparity between the information signal and its quantised approximation. This error phenomenon is known as Slope over loading and causes the loss of rapidly changing information. The slope overloading waveform is as shown in the figure. The problem of slope overload can be solved by increasing the ramping rate of the integrator. But as it can be seen from the figure the effect of the large step size is to add large sharp edges at the integrator output and hence it adds to noise.
- iii) Another problem of Delta Modulation is that it is unable to pass DC information. This is not a serious limitation of the speech communication.

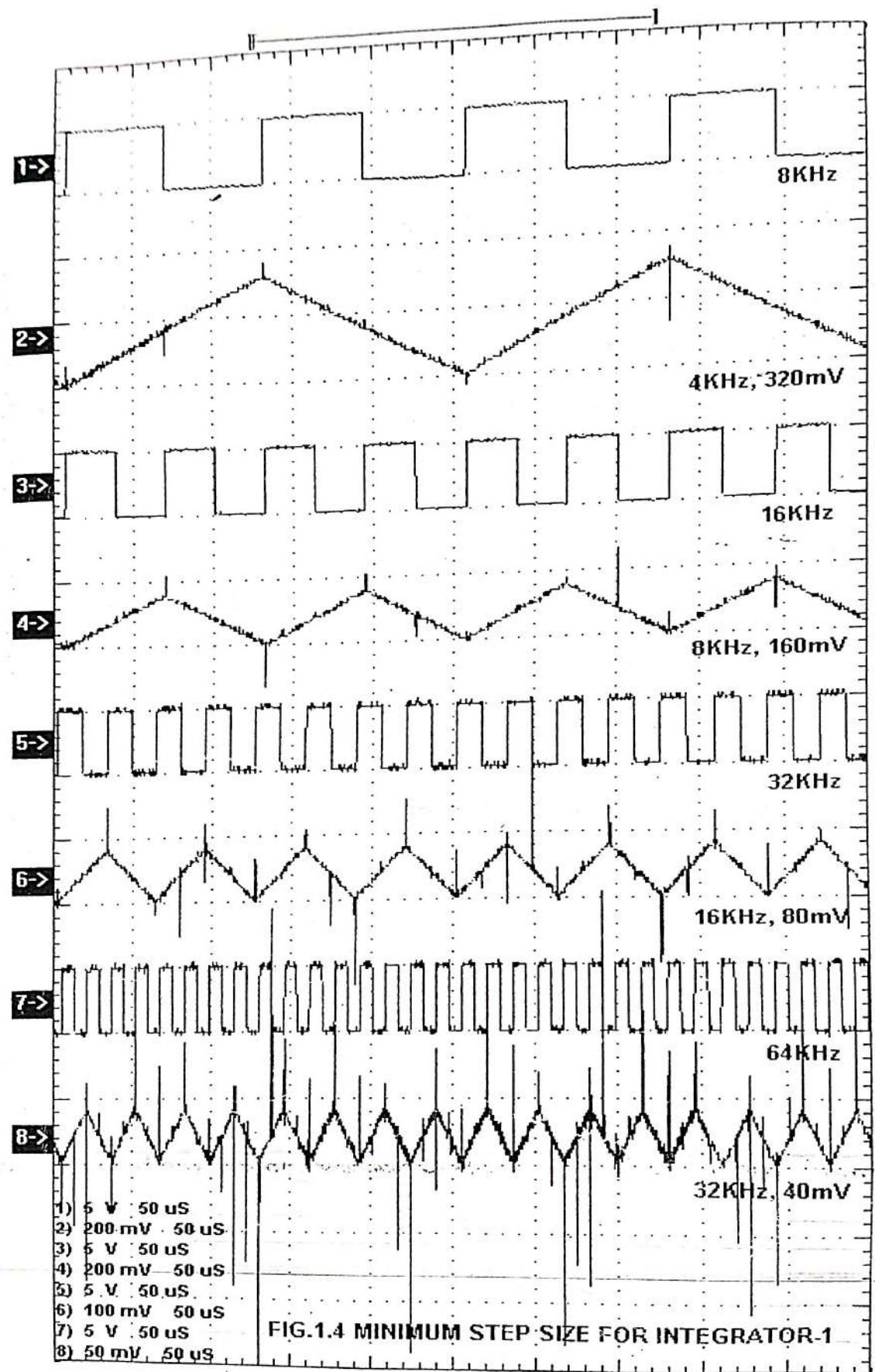
EQUIPMENTS:

DCL-07 kit.
Connecting chords.
Power supply.
20MHz Dual Trace Oscilloscope.

NOTE: KEEP ALL THE SWITCH FAULTS (SWITCH SF1 & SF2) IN OFF POSITION.

PROCEDURE:

1. Refer to the block diagram (Fig. 1.3) and carry out the following connections.
2. Connect the power supply with the proper polarity to the Kit **DCL-07** and switch it ON.



3. Select sine wave input 250Hz of 0V through pot P1 and connect post 250Hz to post IN of input buffer.

4. Connect output of buffer post OUT to Digital Sampler input post IN1.

Then select clock rate of 8 KHz by pressing switch S1 selected clock is indicated by LED glow.

Keep Switch S2 in Δ (Delta) position.

Connect output of Digital Sampler post OUT to input post IN of Integrator 1.

Connect output of Integrator 1 post OUT to input post IN2 of Digital Sampler.

Then observe the Delta modulated output at output of Digital Sampler post OUT and compare it with the clock rate selected. It is half the frequency of clock rate selected.

Observe the integrator output test point. It can be observed that as the clock rate is increased, amplitude of triangular waveform decreases. This is called minimum step size. These waveforms are as shown in figure 1.4. Then increase the amplitude of 250Hz sine wave upto 0.5V. Signal approximating 250Hz is available at the integrator output. This signal is obtained by integrating the digital output resulting from Delta modulation.

Then go on increasing the amplitude of selected signal through the respective pot from 0 to 2V. It can be observed that the digital high makes the integrator output to go upward and digital low makes the integrator output to go downwards. Observe that the integrator output follows the input signal. The waveforms are as shown in the figure 1.5. Observe the waveforms at various test-points in the Delta modulator section.

Increase the amplitude of 250Hz sine wave through pot P1 further high and observe that the integrator output cannot follow the input signal. State the reason.

Repeat the above mentioned procedures with different signal sources and selecting the different clock rates and observe the response of Delta Modulator.

Connect Delta modulated output post OUT of Digital Sampler to the input of Delta Demodulator section post IN of Demodulator.

Connect output of Demodulator post OUT to the input of Integrator 3 post IN.

Connect output of Integrator 3 post OUT to the input of output buffer post IN.

Connect output of output buffer post OUT to the input of 2nd order filter post IN.

Connect output of 2nd order filter post OUT to the input of 4th order filter post IN.

Keep Switch S4 in HIGH position.

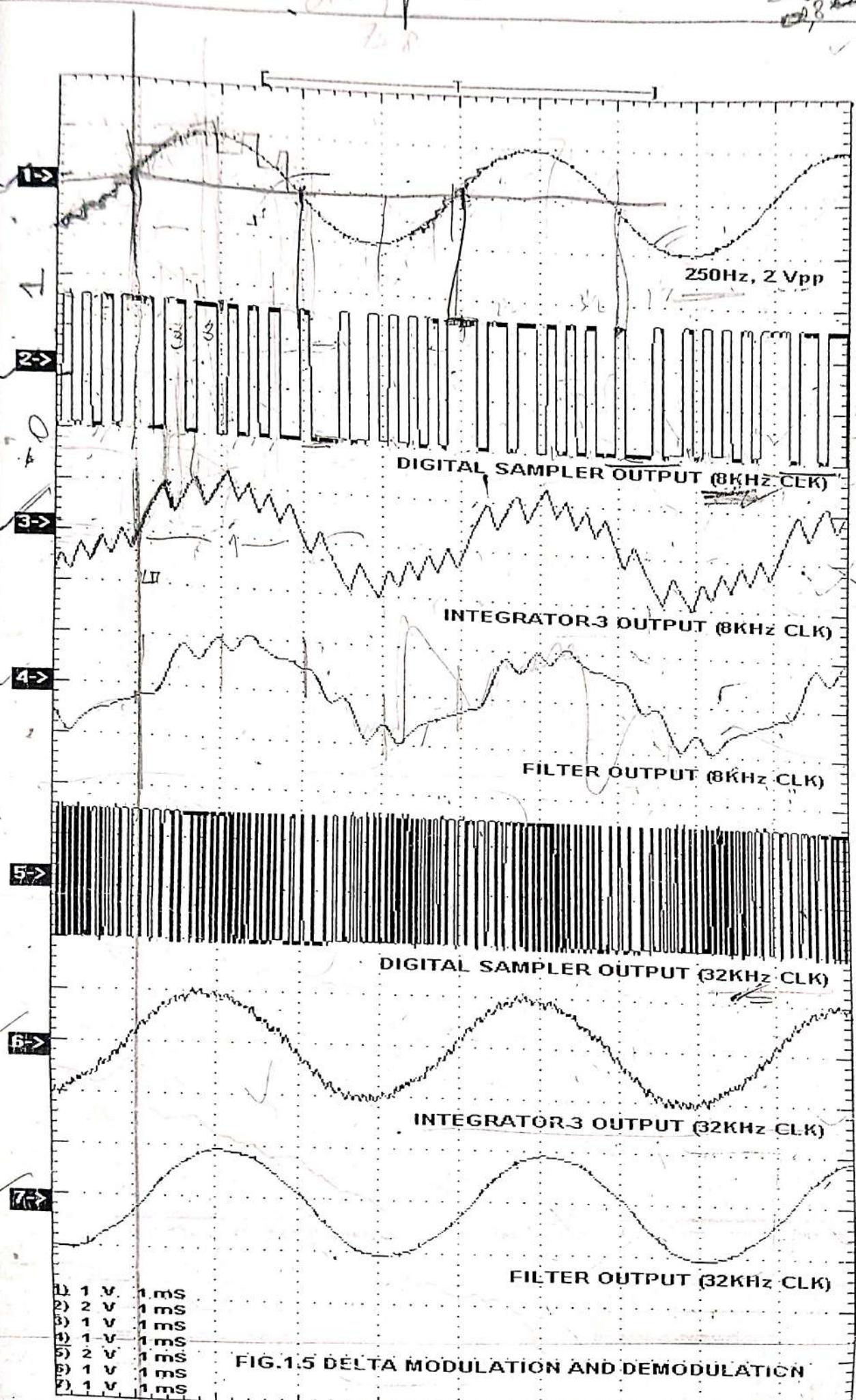
Then observed various test points in Delta Demodulator section and observe the reconstructed signal through 2nd order filter and 4th order filter. Observe the waveforms as shown in figure 1.5.

2 x 5

2 x 5

28

750



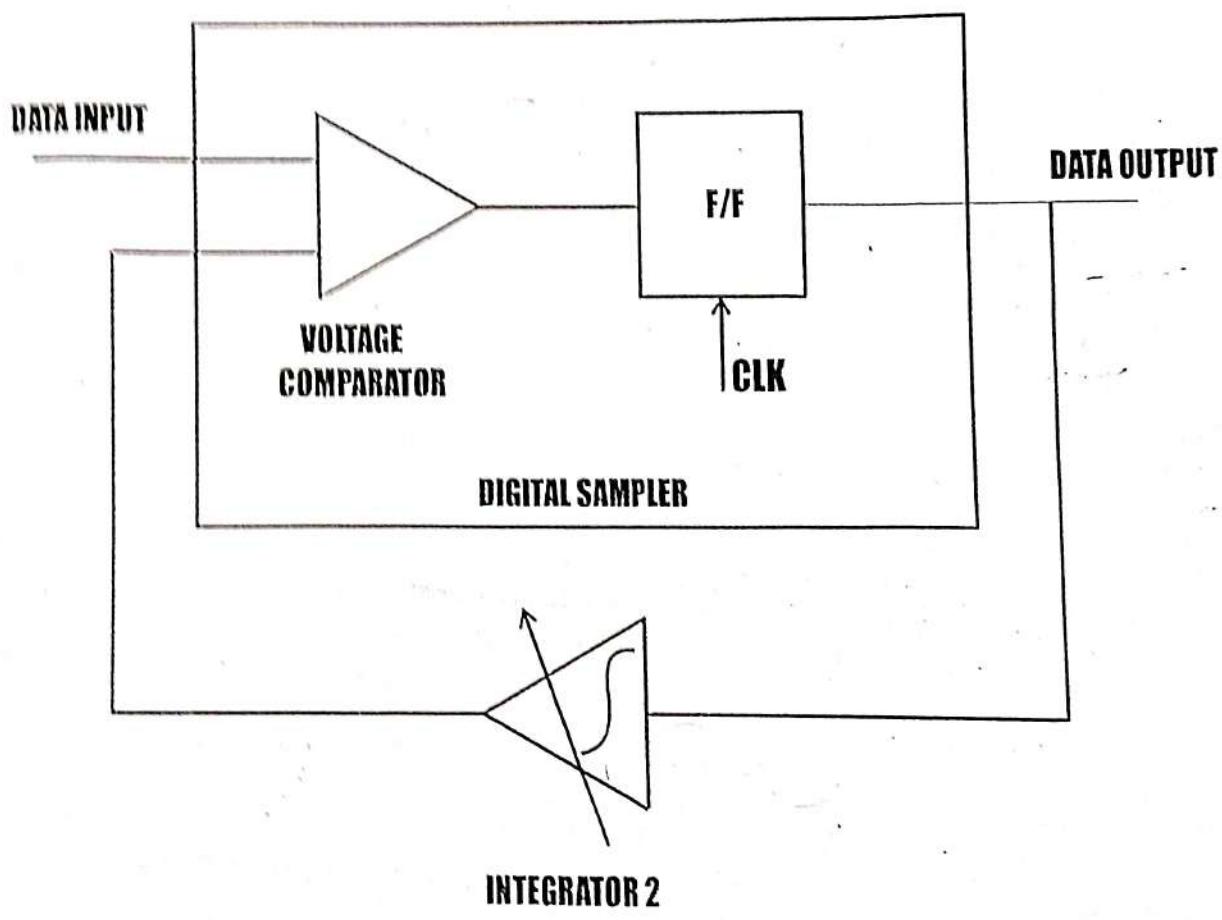


FIG.3.1 ADAPTIVE DELTA MODULATION

EXPERIMENT NO: 3

NAME:

ADAPTIVE DELTA MODULATION AND CVSD.

OBJECTIVE:

Study of Adaptive Delta Modulation and Demodulation with Continuously Variable Slope Delta Modulator (CVSD).

THEORY:

As seen in earlier system Delta Modulation system is unable to chase the rapidly changing information of the analog signal, which gives rise to distortion and poor quality reception. The problem can be overcome by increasing the integrator gain. Adaptive Delta Modulation is a variation of Delta Modulation, which offers relief from disadvantage of DM by adopting the step size to accommodate changing signal conditions. If the input signal is large, step is cause to increase, thereby reducing slope overload effects. The block diagram of ADM is as shown in fig 3.1. It is same as Delta Modulation except the variable gain circuit and step size controller. The controller keeps sensing the slope condition of the message conveyed. If the slope is large the controller output causes the variable gain circuit to have large gain. If the slope is small, the controller output causes a small gain.

In certain cases Adaptive Delta Modulation do not change step size on a pulse-to-pulse basis, but changes are made much more slowly, such slow control is referred to as syllabic. The usual implementation involves a continuously variable slope Delta (CVSD). There are varieties of IC's for CVSD encoding and decoding in today's semiconductor market.

The CVSD is the simple alternative to more complex conventional conversion techniques in system requiring digital communication of analog signals. The CVSD A/D is well suited for the requirements of digital communications. A Delta Modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The input to the comparator is the simple analog signal and the integrator output. The comparator output is the difference between the input voltage and the integrator output. That sign bit is the digital output and also control the direction of ramp in the integrator. The output of comparator is fed to the sampler. Then the sampler output is fed to the slope polarity switch and level detect algorithm. The level detect algorithm is again fed to the slope magnitude control followed by slope polarity switch. The output slope polarity switch is fed to the integrator in the control loop. With no input at the transmitter a continuous 1 and 0 alternations are transmitted. The outstanding characteristic is its ability to transmit the intelligible voice out at relatively low data rate. Companded PCM for telephone quality transmission requires about 64Kbits/sec. data rate/channel. CVSD produces equal quality at 32Kbit/sec. In CVSD Decoder CVSD mod output is fed to the input of comparator.

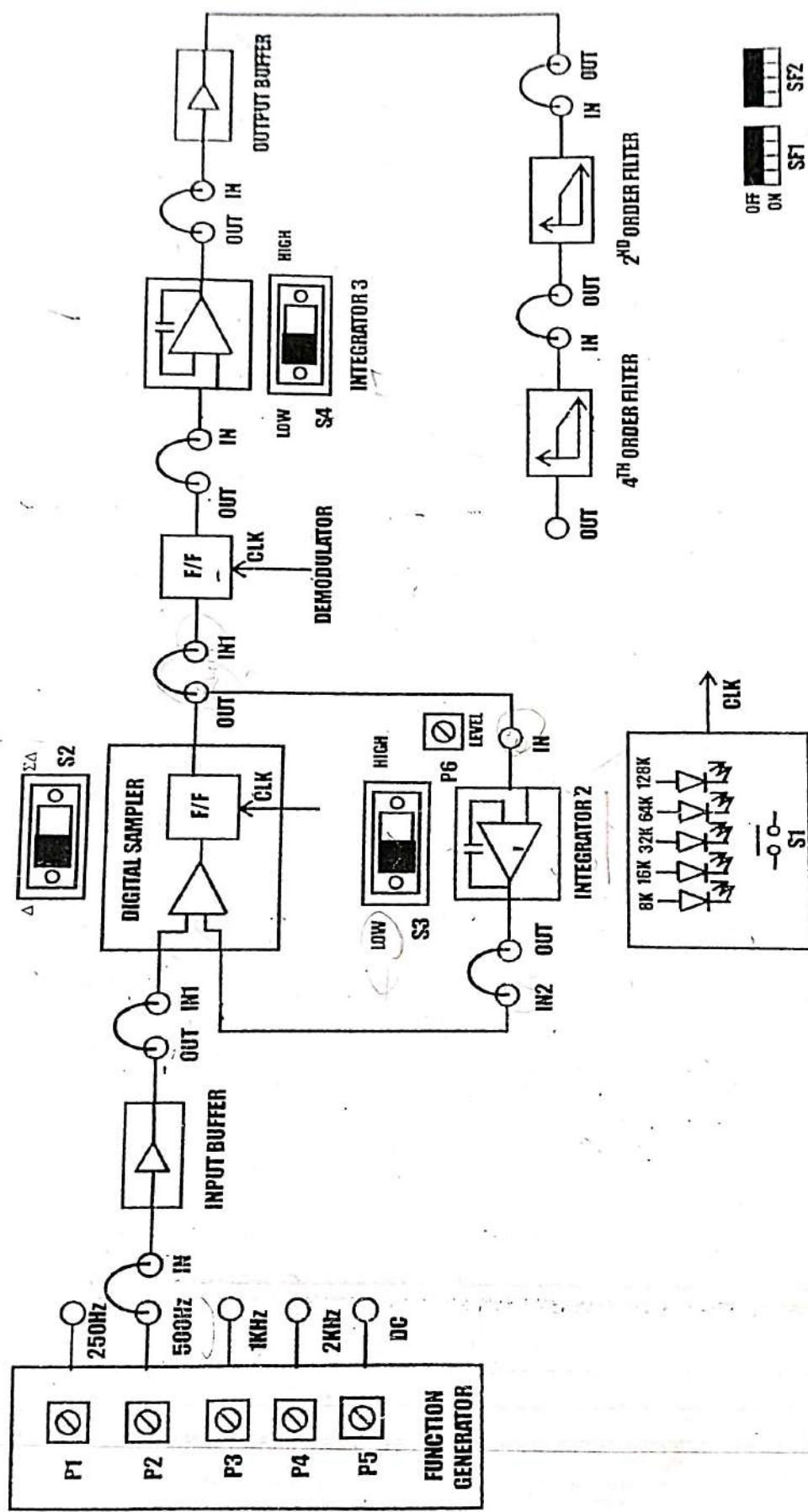


FIG.3.2 BLOCK DIAGRAM FOR ADAPTIVE DELTA MODULATION AND DEMODULATION

The comparator output is fed to the internal shift register. Then the output of internal shift register is fed to the digital logic followed by slope polarity switch and integrator. The output of integrator is fed to the low pass filters for the reconstruction of original signal.

EQUIPMENTS:

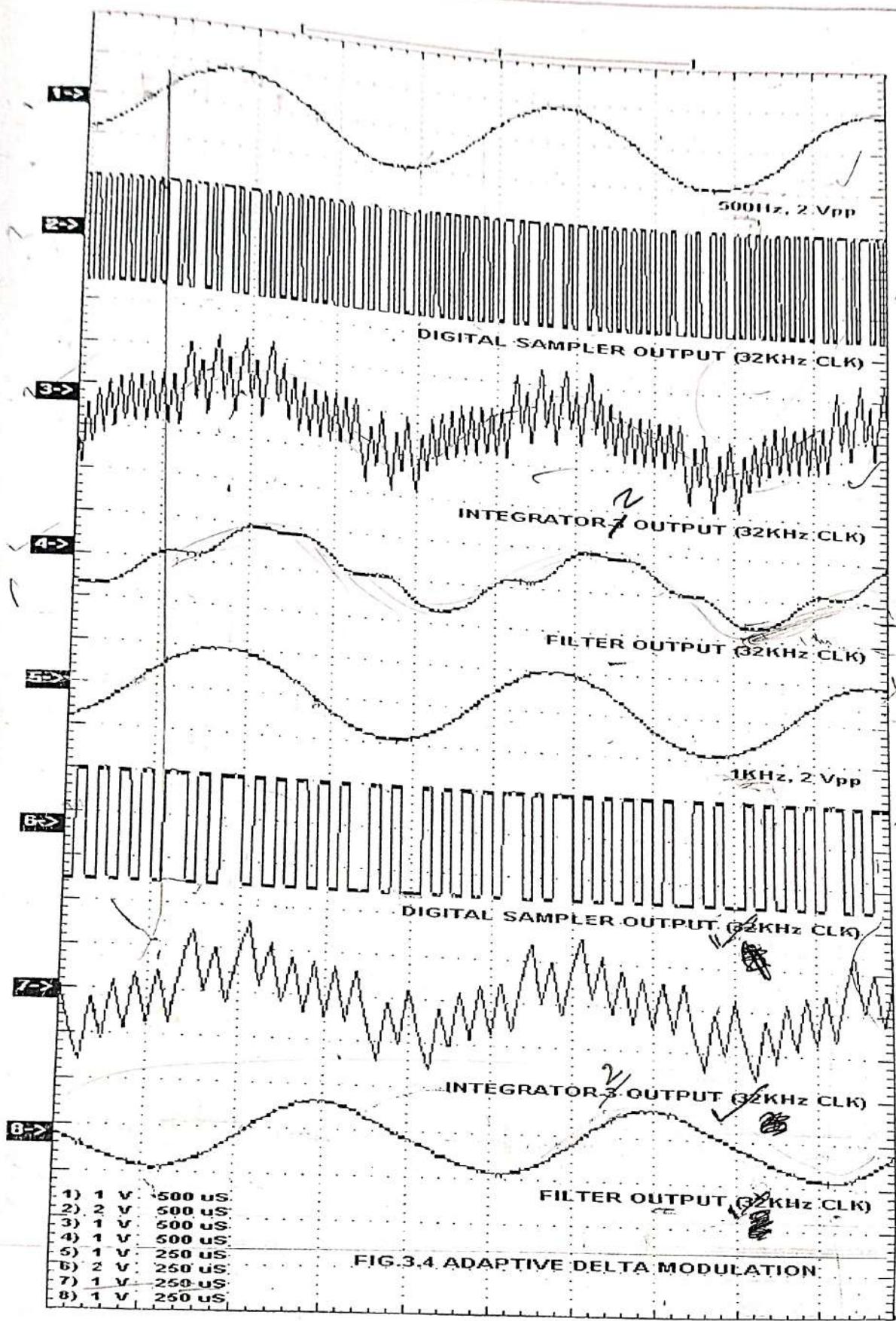
DCL -07 kit.
Connecting chords.
Power supply.
20MHz Dual Trace Oscilloscope.

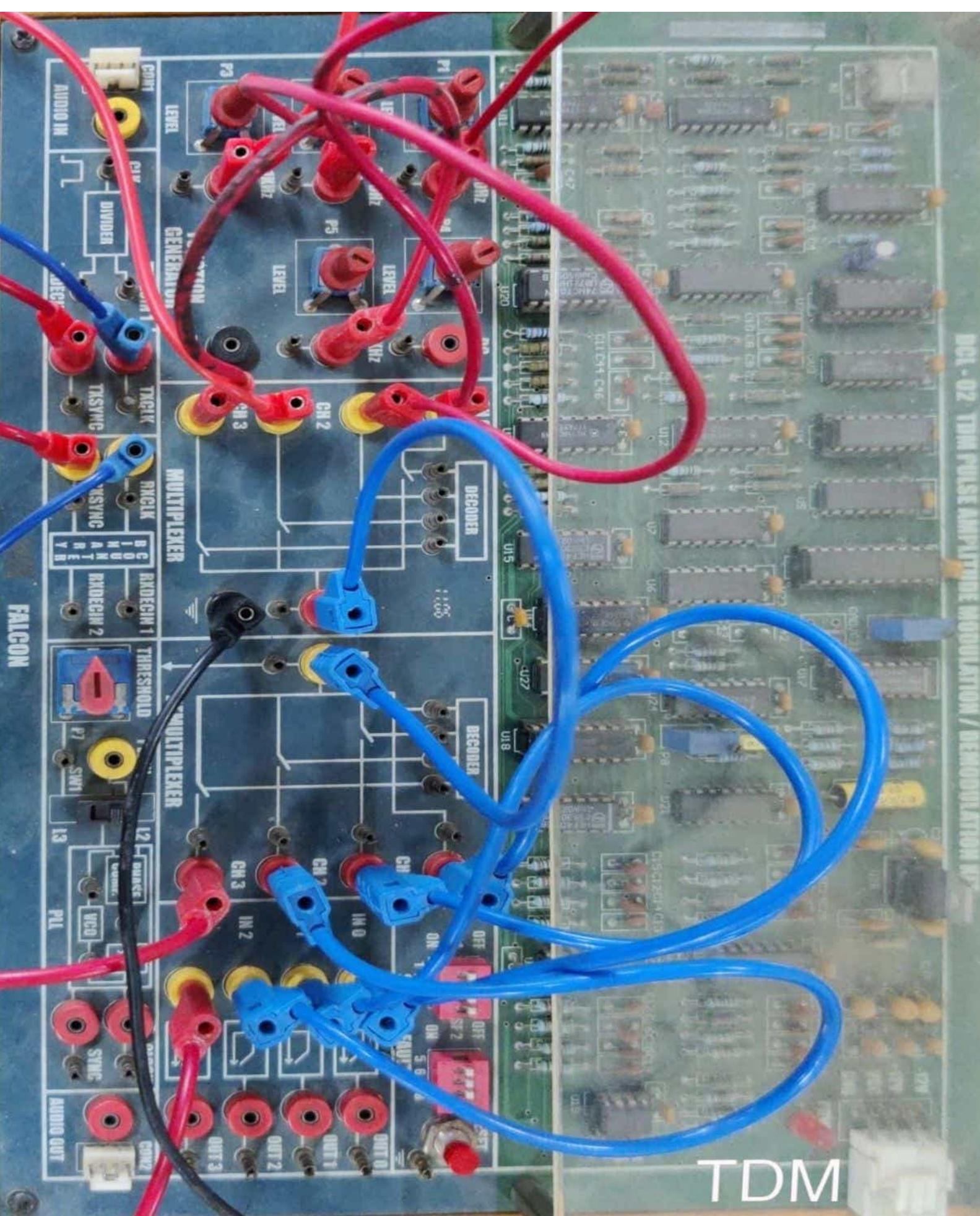
PROCEDURE:

NOTE: KEEP ALL THE SWITCH FAULTS (SWITCH SF1 & SF2) IN OFF POSITION.

ADAPTIVE DELTA MODULATION:

1. Refer to the block diagram (Fig. 3.2) and carry out the following connections.
2. Connect the power supply with the proper polarity to the Kit DCL-07 and switch it ON.
3. Select sine wave input **500Hz** of **2V** or above through pot **P2** and connect post **1KHz** to post **IN** of input buffer.
4. Connect output of buffer post **OUT** to Digital Sampler input post **IN1**.
5. Then select clock rate of **32 KHz** by pressing switch **S1** selected clock is indicated by LED glow.
6. Keep Switch **S2** in Δ (Delta) position.
7. Connect output of Digital Sampler post **OUT** to input post **IN** of Integrator 2.
8. Connect output of Integrator 2 post **OUT** to input post **IN2** of Digital Sampler.
9. Keep Switch **S3** in **LOW** position.
10. Connect Delta modulated output post **OUT** of Digital Sampler to the input of Delta Demodulator section post **IN** of Demodulator.
11. Connect output of Demodulator post **OUT** to the input of Integrator 3 post **IN**.
12. Connect output of Integrator 3 post **OUT** to the input of output buffer post **IN**.
13. Connect output of output buffer post **OUT** to the input of 2^{nd} order filter post **IN**.
14. Connect output of 2^{nd} order filter post **OUT** to the input of 4^{th} order filter post **IN**.
15. Keep Switch **S4** in **LOW** position.
16. Observe the output of filter at post **OUT** of 4^{th} order filter.
17. Repeat the above mention procedures with different signal sources and selecting the different clock rates and observe the response of Adaptive delta modulation. Which follows input signal even if amplitude & frequency of input signal increases. Adaptive delta modulator matches the slope of the input signal due to low time constant.





Experiment 2

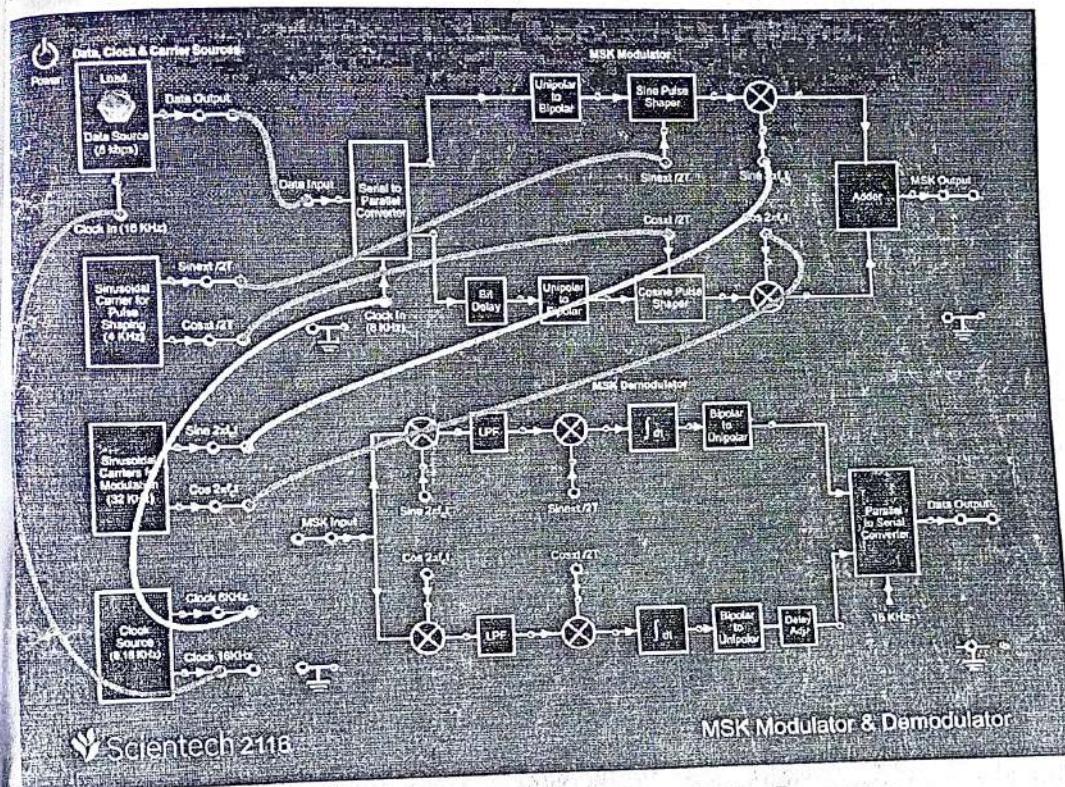
Objective: Study of MSK Modulator & Demodulator Modulation Process

Equipments Needed:

- Scientech 2116, MSK Modulator & Demodulator Board
- Cathode Ray Oscilloscope,
- 2MM Patch Cords.

Experimental Setup:

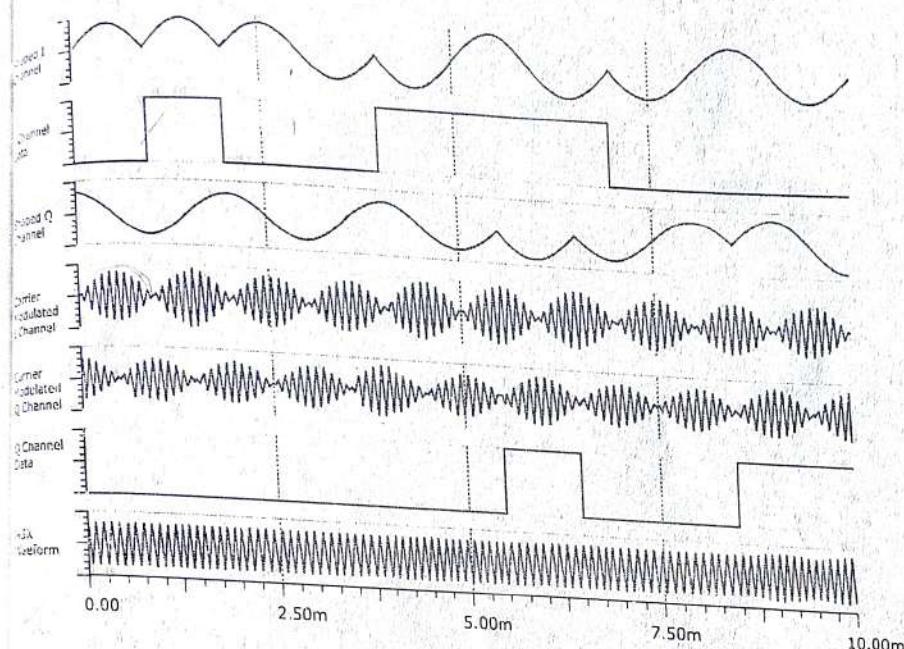
Refer to the following next figure to configure setup for the present experiment:



Setup for the Study of MSK Modulation Process

- Before making connections, make sure that Power Supply is switched off.
- Refer to the previous figure shown above while making connections.
- Connect 16 KHz clock output of clock source to the data generator's 'CLK IN' input.
- Connect the 'Data Out' of data source to the 'Data In' of serial to parallel converter.
- Connect 8 KHz clock out of clock source to the 'CLK In' of serial to parallel converter.
- Now connect 'Cos $\pi t/2T$ ' and 'Sin $\pi t/2T$ ' output of 'sinusoidal carrier for pulse shaping generator' to the inputs of 'Sin pulse shaper' and 'Cosine pulse shaper'.
- Connect the Sine and Cosine carrier outputs of 'sinusoidal carrier generator for modulation' block (32KHz) to the carrier inputs of the modulators as shown above in the figure.
- Now turn 'On' the Power Supply and reset the data source.
- Repeat the steps 4 to 14 of the Exp.1 and obtain the different waveforms.
- Now observe the outputs of the multipliers. Compare these results with the theoretical diagram shown in previous figure.
- Observe the output of the adder block. This is the complete MSK signal waveforms. (as shown in next figure)
- View both the serial data and modulated signal simultaneously on the CRO screen. Make the waveforms stable by adjusting the time base of the CRO. Observe the frequency shift in the modulated waveform. Also this shift is much lesser than generally seen in an FSK waveform. By our intuitive observation of the modulated signal we can immediately make some conclusions such as the modulated waveform is not having any abrupt phase changes as was seen in BPSK, QPSK and OQPSK which assures that the modulated waveform does not contain very high frequency contents and also the frequency shift is very low. All these features suggest the improvements in the bandwidth of the Modulated signal.
- Verify the phase continuity of the MSK waveform. Also verify that the modulated waveform has almost constant envelop.

Scientech 2116



Simulated Results for MSK Modulator

Questions:

- Write the process to modulate the signal using MSK Modulator & Demodulator?
- What do you mean by FSK and ASK.
- Define the term QPSK.

Experiment 3

Objective: Study of MSK Modulator & Demodulator (MSK) Demodulation Process

Equipments Needed:

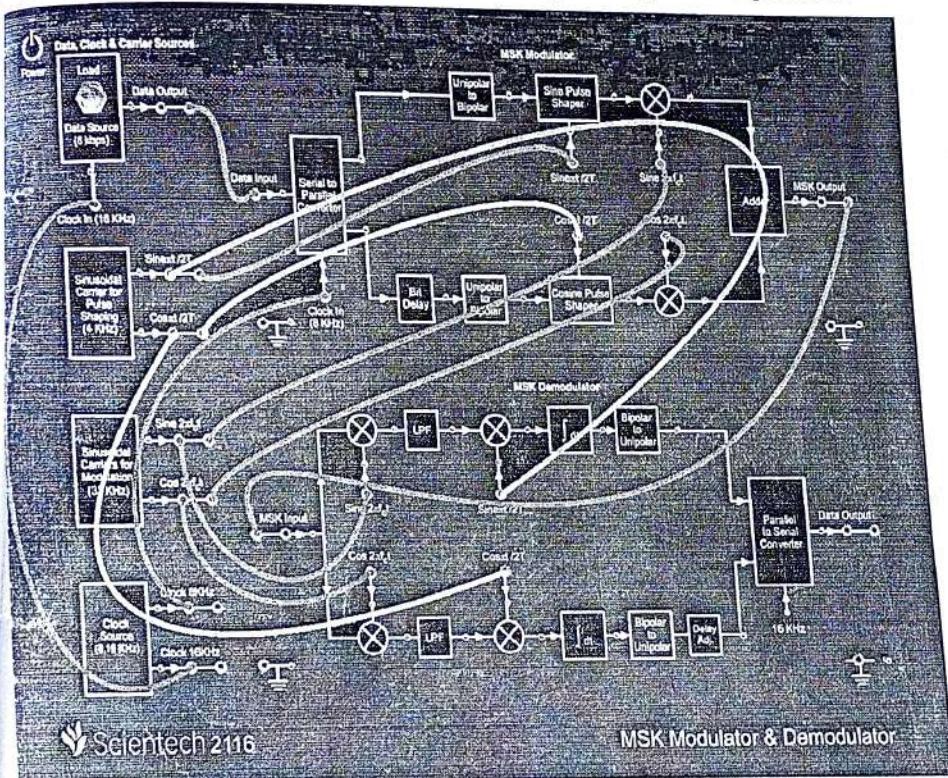
- Scientech 2116, MSK Modulator & Demodulator Board

- 2MM Patch Cords

- Oscilloscope

Experimental Setup:

Refer to the following diagram to configure your setup for the present experiment



Setup for MSK Demodulation

Procedure:

- Make the connections for modulation as described in the Experiment 1 and 2. refer to the previous figure & previous next figure for making connections.
- For Demodulation connect the modulated signal to the input of demodulator.
- Connect the orthogonal sinusoidal carriers to the input of the first stage of multipliers.
- Connect the Wave shaping carriers to the second stage of multipliers.
- Now turn 'On' the Power Supply.
- Reset the data source and observe the MSK modulated waveform at the modulator Output.
- Observe the outputs of first stage of multipliers in the demodulator section.
- Observe the output of Second stage of multipliers in the demodulator section.
- Observe the output of integrators and try to make some inferences from these waveforms.
- Finally observe the output of parallel to serial converter and compare this recovered data with original modulating data. Verify that recovered data is received without any error.

Questions:

- Write the process to demodulate the signal using MSK Modulator & Demodulator?
- What do you mean by FSK and ASK.
- Define the term QPSK.

MSK Modulator & Demodulator

