DEPARTMENT
OF
ELECTRONICS AND COMMUNICATION ENGINEERING

EC204
DIGITAL SYSTEM DESIGN LAB SECTIONAL RECORD

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EXPT - 1

ON

Design and implement a controlled CMOS inverter using IC CD 4007/CD4001

AIM: Design and implement a controlled CMOS Inverter using IC CD4007/CD4001.

Detailed objective of the experiment:

To design and implementation of CMOS Inverter, NAND & NOR Gate with enable inputs and verify its truth table. Draw the I_D- V_D characteristics. Draw the Voltage Transfer curve of CMOS logic circuit and evaluate and demonstrate the position of V_{OH}, V_{IH}, V_{OL}, V_{IL} in VTC using the ICs of CD4007/ CD4001. Write the switching action of the transistor. Determine Noise Margin & Propagation Delay of CMOS Circuits.

APPARATUS REQUIRED:

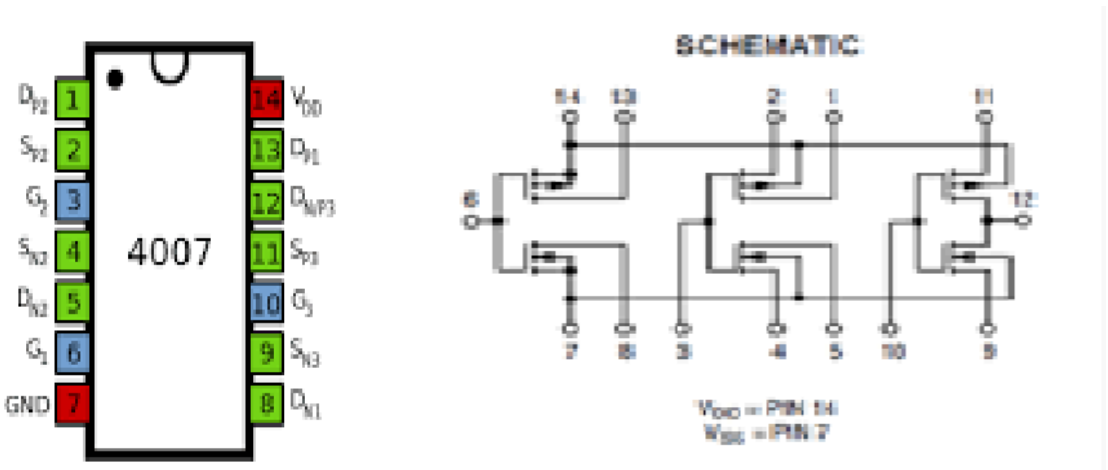
1. Trainer Kit (Micro LABORATORY Kit -II) or
   Wish board, Power supply

CIRCUIT COMPONENTS:

1. ICs CD4007/CD4001
2. Connecting Wires

PIN DIAGRAM:

PIN DIAGRAM OF IC CD4007 CMOS Inverter



Pin Diagram of CMOS Inverter CD4007

THEORY:

Complementary MOSFET (CMOS) technology is widely used today to form circuits in numerous and varied applications. Today's computers CPUs and cell phones make use of CMOS due to several key advantages. CMOS offers low power dissipation, relatively high speed, high noise margins in both states, and will operate over a wide range of source and

input voltages (provided the source voltage is fixed). Next I will attempt to explain just how this logic gate works now that you have some idea of how important CMOS is in your day-to-day life.

As you can see from Figure 1(a), a CMOS circuit is composed of two MOSFETs. The top FET (MP) is a PMOS type device while the bottom FET (MN) is an NMOS type. The body effect is not present in either device since the body of each device is directly connected to the device's source. Both gates are connected to the input line. The output line connects to the drains of both FETs.

Take a look at the VTC in Figure 1(b). The curve represents the output voltage taken from node 3. You can easily see that the CMOS circuit functions as an inverter by noting that when VIN is five volts, VOUT is zero, and vice versa. Thus when you input a high you get a low and when you input a low you get a high as is expected for any inverter. You might be wondering what happens in the middle, transition area of the curve. You might also be curious as to what modes of operation the MOSFETs are in. We will look at these issues next. Truth table of CMOS Inverter is shown in Fig.1(c). Two input CMOS NAND Gate Circuit diagram shown in Fig.2(a) and observation table shown in Fig.2(b). Two input CMOS NOR Gate Circuit diagram shown in Fig.3(a) and observation table shown in Fig.3(b). Pin diagram of CMOS Inverter CD4007 shown in Fig.4.

Fig.1(a) CMOS Inverter Circuit

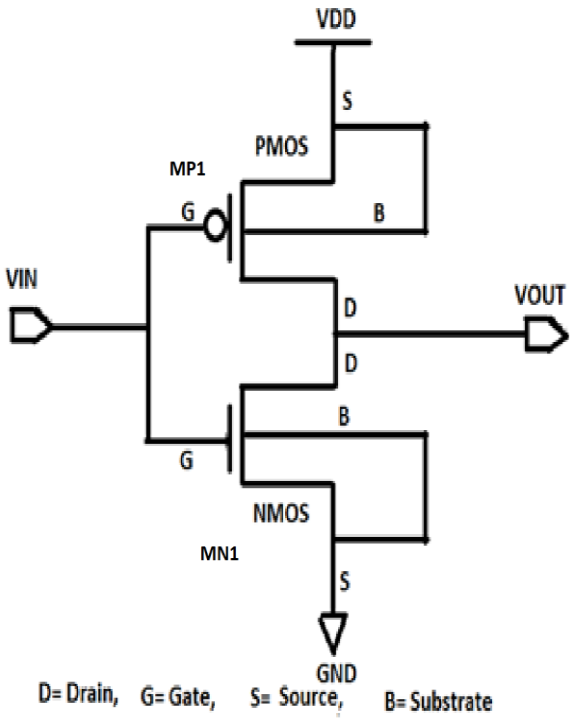
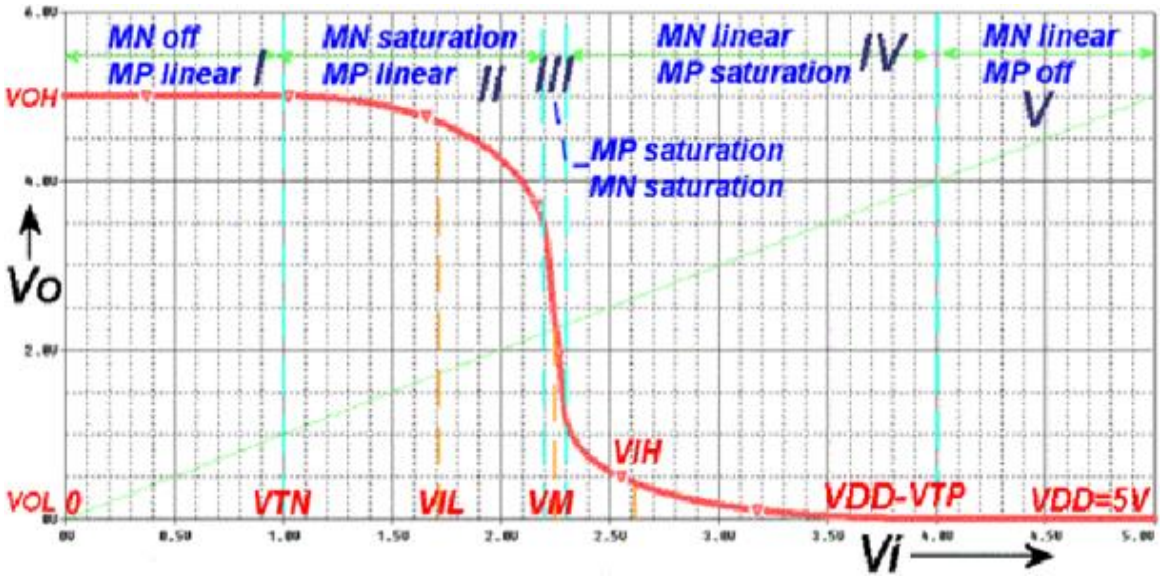


Fig.1 (b) Transfer Characteristics of CMOS Inverter



CIRCUIT DIAGRAM:

Fig.1 (c) Controlled CMOS Inverter Circuit

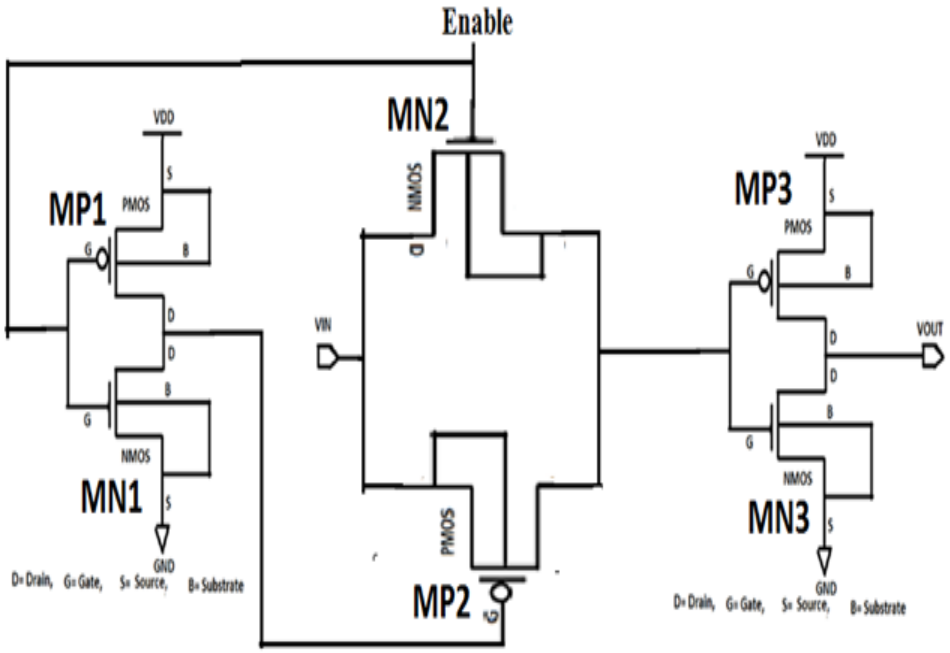


Fig.2 (a) 2-input CMOS NAND Gate

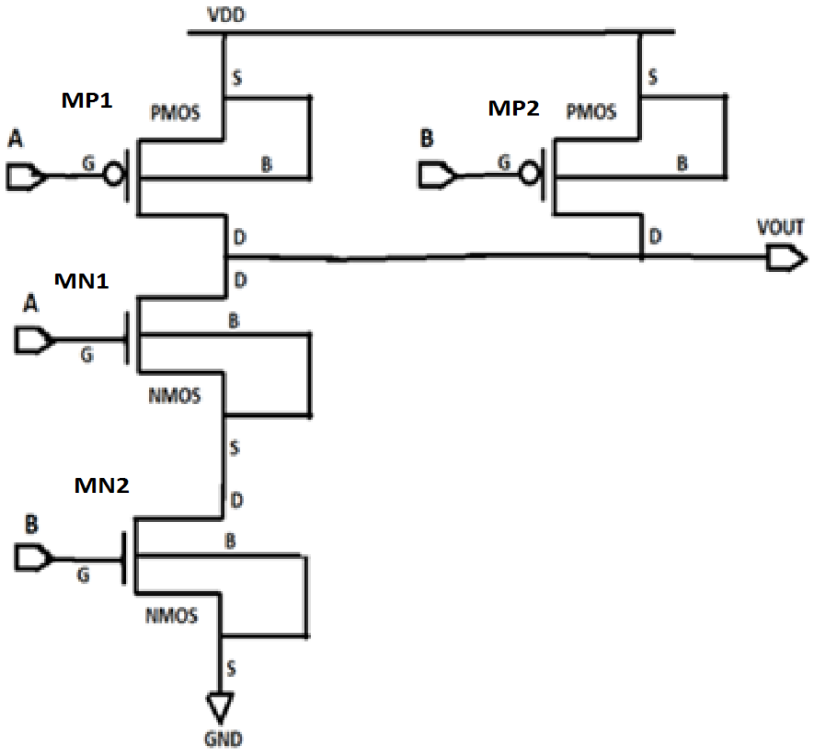
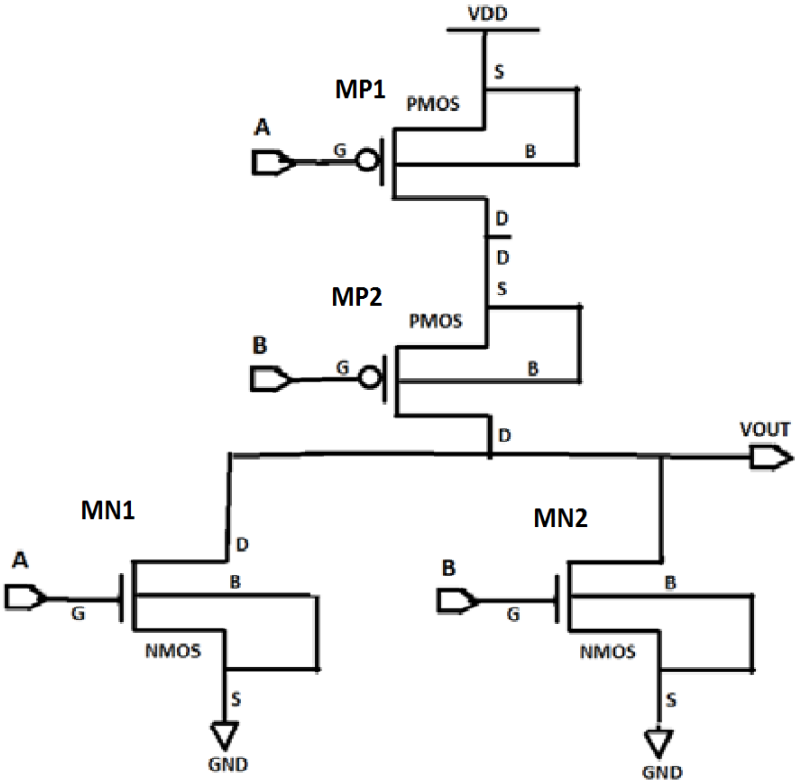


Fig.3 (a) 2-input CMOS NOR Gate



PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Before switching ON Power Supply, make sure that the connections arecorrect.
3. Apply the input logic states as per Truth Table, in terms of +5 volts for 'state-1' and 0 volts for 'state-0'.
4. Observe the output states and complete the observation table.
5. Verify the results of truth ness.
6. Repeat steps as per need.

OBSERVATION TABLE:

Table 1: Truth Table and status of various MOS of CMOS Inverter

Enable	Input			Output
	VIN=A	MP1	MN1	Y=VOUT
0	0			
0	1			
1	0			
1	1			

Table 2: Truth table of 2-input CMOS NAND Gate

Input		Switching Action of the Transistors				Output
A	B	MP1	MP2	MN1	MN2	Y
0	0					
0	1					
1	0					
1	1					

Table 3: Truth table of 2-input CMOS NOR Gate

Input		Switching Action of the Transistors				Output
A	B	MP1	MP2	MN1	MN2	Y
0	0					
0	1					
1	0					
1	1					

RESULTS & DISCUSSION:

CONCLUSION:

PRECAUTION:

a) Make the connections according to the IC pin diagram

b) The connection should be tight

DESIGN TASK: Implement XOR using CMOS logic **.**

EXPT - 2

ON

To study and verify the truth table of NAND and XOR gate using IC 7400

AIM: To study and verify the truth table of NAND and EX-OR gate using IC 7400

APPARATUS REQUIRED:

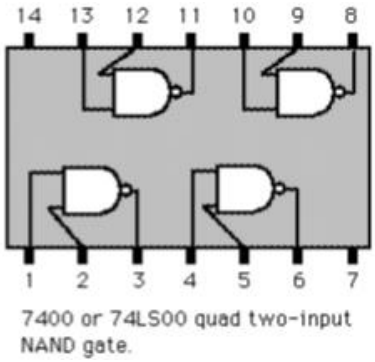
1. Trainer Kit (Micro LABORATORY Kit -II) or
   Wish board, Power supply

CIRCUIT COMPONENTS:

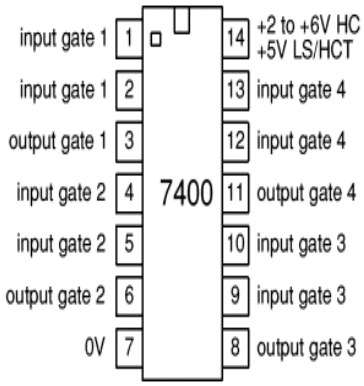
1. ICs 7400
2. Connecting Wires

PIN DIAGRAM:

Pin Diagram of IC 7400 (QUAD, 2-INPUT NAND GATE)



7400 or 74LS00 quad two-input NAND gate.

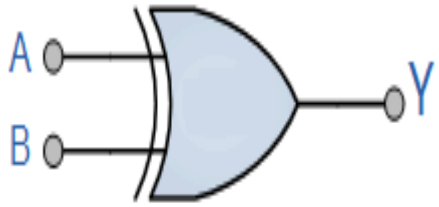


THEORY:

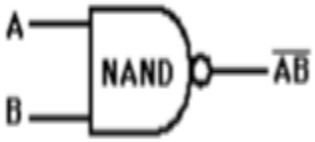
An Ex-OR (Exclusive OR) one of the universal gate logic gate obeys the definition:

"The output of a two input exclusive-OR assume the 1 state if one and only if any one input assume the 1 state."

Symbol & Truth Table of Ex-OR Gate:

Symbol	Truth Table		
	A	B	Y
	0	0	0
	0	1	1
	1	0	1
	1	1	0
Boolean Expression $Y = A \oplus B$			

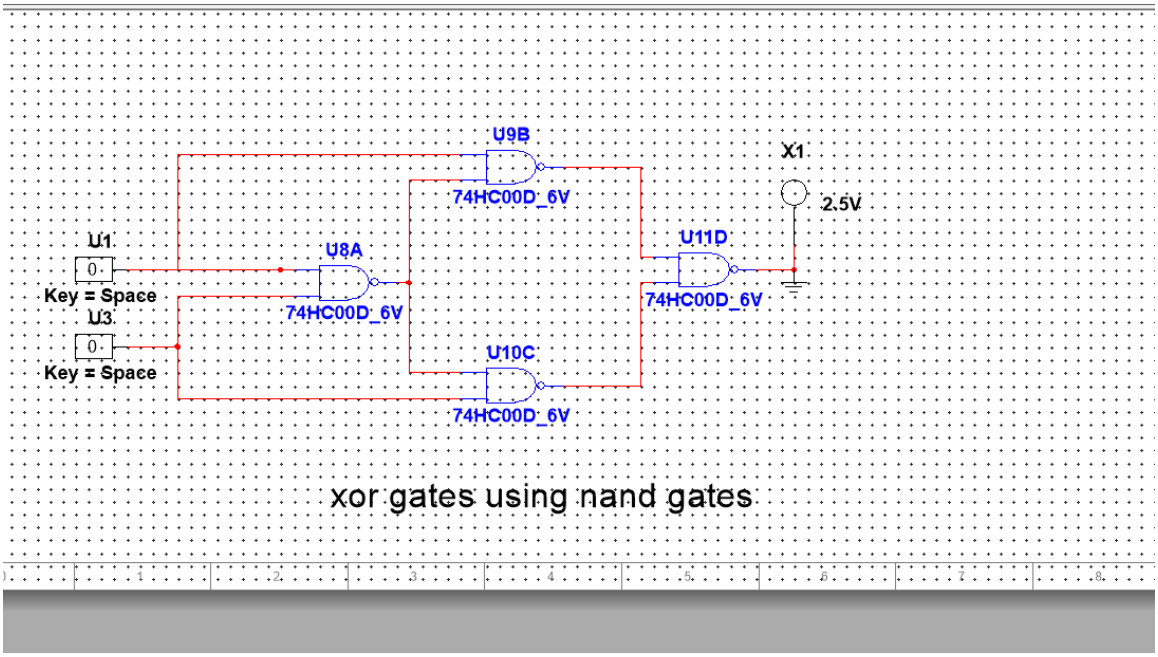
Symbol & Truth Table of NAND Gate:

Symbol	Truth Table		
	A	B	Y
	0	0	1
	0	1	1
	1	0	1
	1	1	0
Boolean Expression $Y = \underline{AB}$			

Design Equation:

$$\begin{aligned} Y = A \oplus B &= A\underline{B} + \underline{A}B \\ &= \underline{\underline{A\underline{B} + \underline{A}B}} \\ &= \underline{\underline{A\underline{A} + A\underline{B} + B\underline{B} + \underline{A}B}} \\ &= \underline{\underline{A(\underline{A} + \underline{B}) + B(\underline{B} + \underline{A})}} \\ &= \underline{\underline{A.\underline{AB} + B.\underline{AB}}} \\ &= \underline{\underline{(A.\underline{AB}).(B.\underline{AB})}} \end{aligned}$$

Circuit Diagram:



PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Before switching ON Power Supply, make sure that the connections are correct.
3. Apply the input logic states as per Truth Table, in terms of +5 volts for state-1 and 0 volts for state-0.
4. Observe the output states.
5. Verify the results of truth ness.
6. Repeat steps from 3 to 5 for all possible combinations of function table.

OBSERVATION TABLE:

INPUT		OUTPUT			
A	**B**	$\underline{AB}$	$\underline{(A.AB)}$	$\underline{(B.AB)}$	$A \oplus B$
0	**0**	**1**	**1**	**1**	**0**
0	**1**	**1**	**1**	**0**	**1**
1	**0**	**1**	**0**	**1**	**1**
1	**1**	**0**	**1**	**1**	**0**

CONCLUSION: We have used the basic universal NAND gate to make XOR circuit and verified the truth table

PRECAUTION:

a) Make the connections according to the IC pin diagram

b) The connection should be tight

EXPT -3

ON

Design and implement seven segment display unit using IC-7447 & 7404

AIM: Design and implement SEVEN segment display unit using IC-7447 & 7404

APPARATUS REQUIRED:

1. Trainer Kit (Micro LABORATORY Kit -II) or
   Wish board, Power supply

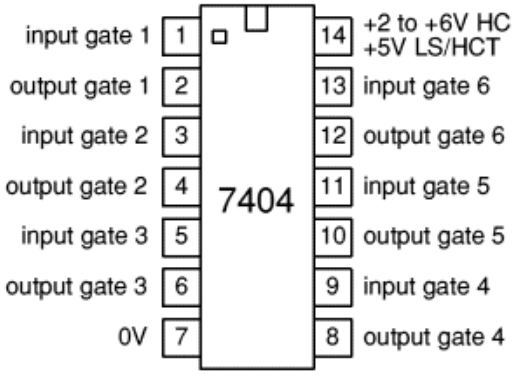
CIRCUIT COMPONENTS:

1. IC 7447 & IC 7404
2. Connecting Wires
3. Seven Segment display IC-LT543

PIN DIAGRAM:

PIN DIAGRAM OF IC 7404

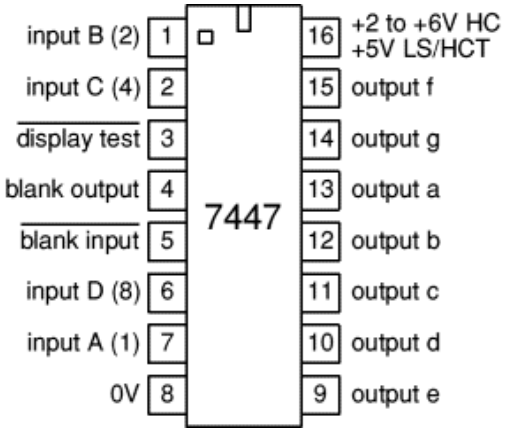
HEX NOT GATE



Quad 2-inputs NOR GATE

PIN DIAGRAM OF IC 7447

BCD TO 7 SEGMENT DISPLAY DRIVER



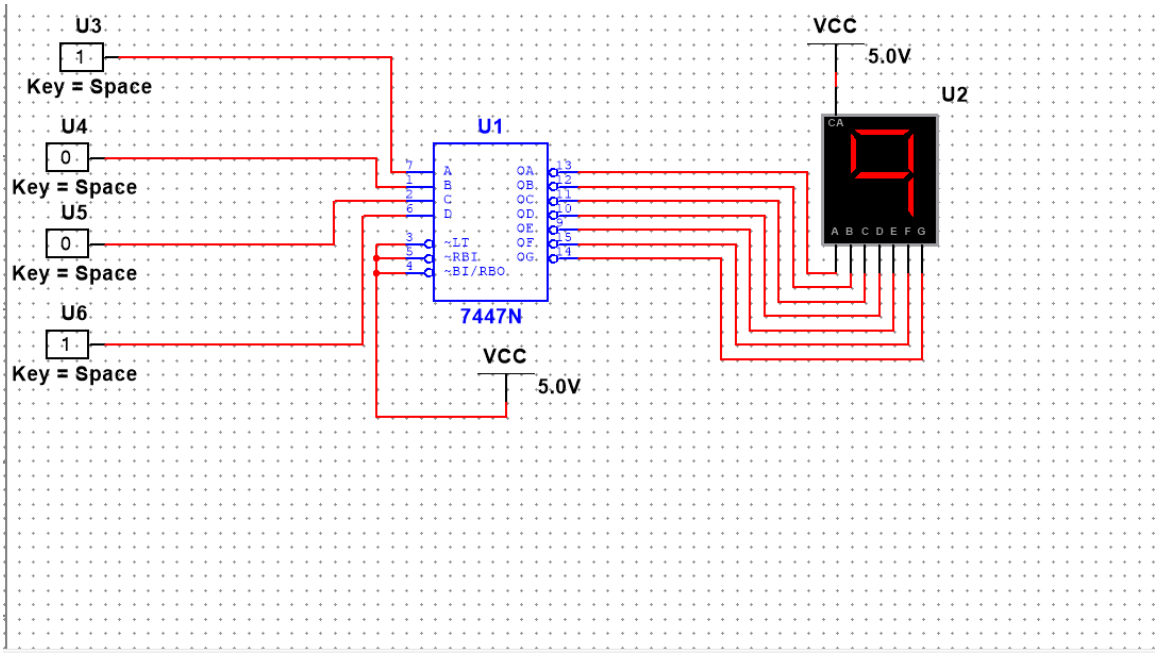
THEORY:

In seven segment display experiment has a seven-segment driver (IC 7447). This is a decoder IC and based on the BCD binary number supplied at its inputs A-D, the appropriate **outputs a-g** of IC 7447 become low to display the digital value of the given BCD (binary coded decimal) number on seven segment Display.

a) The IC 7447 has open collector outputs a-g which can sink up to 40mA. The 7-segment display segments must be connected between +Vs and the outputs with a resistor in series (330 with a 5V supply). A common anode seven segment display is required for it.
b) Lamp/Display test (LT) and Ripple Blank Input (RBI) are active-low, so they should be high for normal operation.
c) When Lamp/Display test (LT) is low all the display segments should light (showing number 8).
d) If the RBI input is low (that is when higher stage display has no significant value to display i.e. when the higher stage display count input is zero), the display in seven segments will be blank (0000) to save power. So this can be used to blank the leading zeros at higher stage display when there are several display digits driven by a chain of counters.
e) To achieve this Ripple Blank Output (RBO) of lower stage decoder should be connected to the Ripple Blank Input (RBI) of the next display of the counter chain (the next most significant digit).

The 7447 is intended for BCD (binary coded decimal), which is input values 0 to 9 (0000 to 1001 in binary). So the inputs from 10 to 15 (1010 to 1111 in binary) will light odd display segments but will do no harm

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Before switching ON power supply, make sure that the connection are correct.
3. Apply the input logic state code mentioned in observation Table in terms of +5 volts for state-1 and 0 volts for state-0.
4. Observe the output states.
5. Verify the displayed digit with decimal equivalent of applied input binary code.
6. Repeat steps from 3 to 5 for all possible combination.

OBSERVATION TABLE:

Note: Show the Displayed Digital output of seven-segment display in observation.

S. No.	BINARY CODE				a	b	c	d	e	f	g	Displayed Digit
	A3	A2	A1	A0								
1	0	0	0	0	1	1	1	1	1	1	0	
2	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**
3	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**2**
4	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**3**
5	**0**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**4**
6	**0**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**0**	**1**	**1**	**5**
7	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**6**
8	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**7**
9	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**8**

CONCLUSION: We have implemented a seven segment display unit which displays 0-9 decimal values.

PRECAUTION:

a) Make the connections according to the IC pin diagram

b) The connection should be tight

EXPT -4

ON

Design and verify half adder and full adder circuits using gates and IC 7483

AIM: Design and verify half adder and full Adder circuits using gates and IC 7483.

APPARATUS REQUIRED:

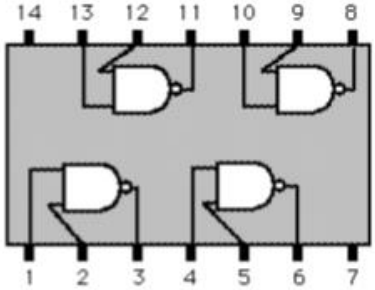
1. Trainer Kit (Micro LABORATORY Kit -II) or
   Wish board, Power supply

CIRCUIT COMPONENTS:

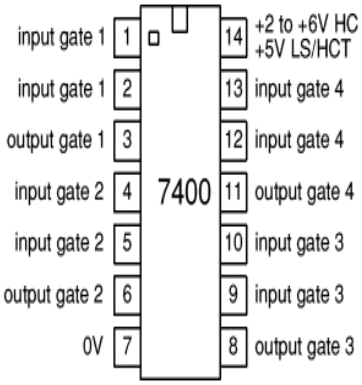
1. IC 7400, IC 7408, IC 7486, IC 7432 and IC7483
2. Connecting Wires

PIN DIAGRAM:

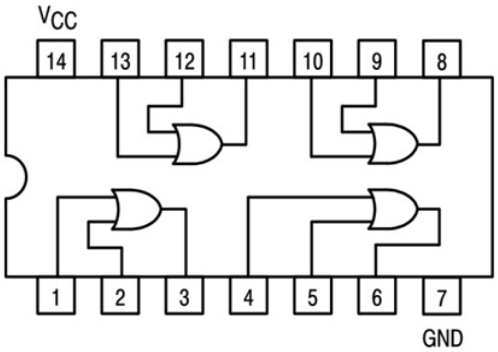
Pin Diagram of IC 7400 (QUAD, 2-INPUT NAND GATE)



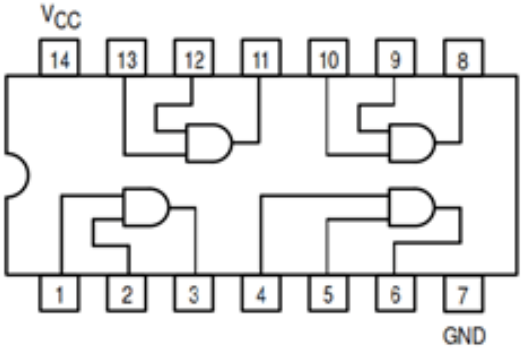
7400 or 74LS00 quad two-input NAND gate.



Pin Diagram of IC 74LS32 (QUAD 2-INPUT OR GATES) & IC 7408 (QUAD 2-INPUT AND GATES)



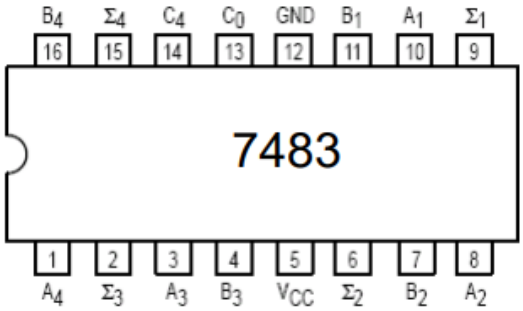
2 input OR gate IC (74LS32)



2 input AND gate IC (7408)

Pin Diagram of IC 7486 (QUAD, 2-INPUT GATE)

Pin Diagram of IC 7483 (4-bit Full adder circuit Adder)



THEORY:

Half-Adder: A combinational logic circuit that performs the partial addition i.e. addition of two data bits, A and B is called a half-adder. Half adder circuit does not include input carry in its addition hence known as half adder.

Addition of Half Adder circuit will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C.

The Boolean functions describing the half-adder are:

$S = A \oplus B$ $\qquad\qquad$ $C = A\,B$

Full-Adder: As stated the half-adder does not take the carry bit from its previous stage into account. The carry bit from its previous stage called carry-in bit C_{in}. A combinational logic circuit that perform the addition of two data bits, 'x' and 'y' and one carry-in bit, Cin, is called a full-adder. The Boolean functions describing the full-adder are:

$S = (x \oplus y) \oplus Cin$ $\qquad\qquad$ $C = xy + Cin\,(x \oplus y)$

The related circuits are given below

I. TO REALIZE HALF ADDER

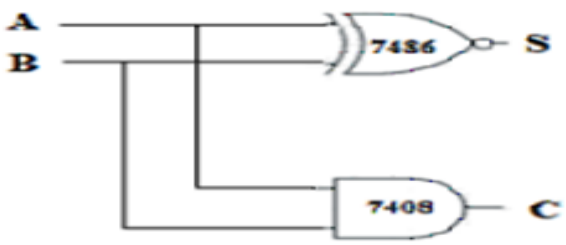
TRUTH TABLE

INPUTS		OUTPUTS	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

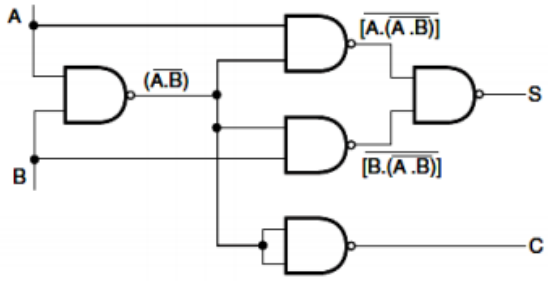
BOOLEAN EXPRESSIONS:

S=A ⊕ B
C=A B

USING Basic gates



USING NAND GATES ONLY



II. FULL ADDER

TRUTH TABLE

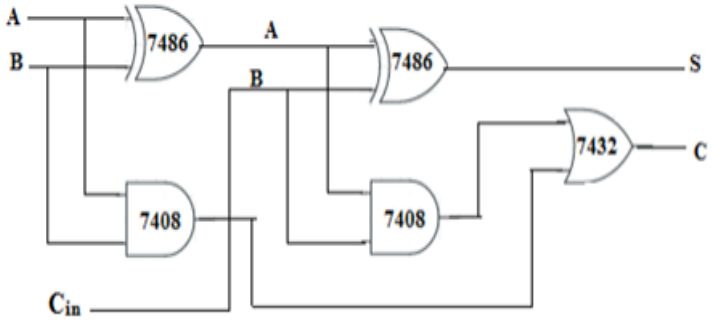
INPUTS			OUTPUTS	
A	B	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

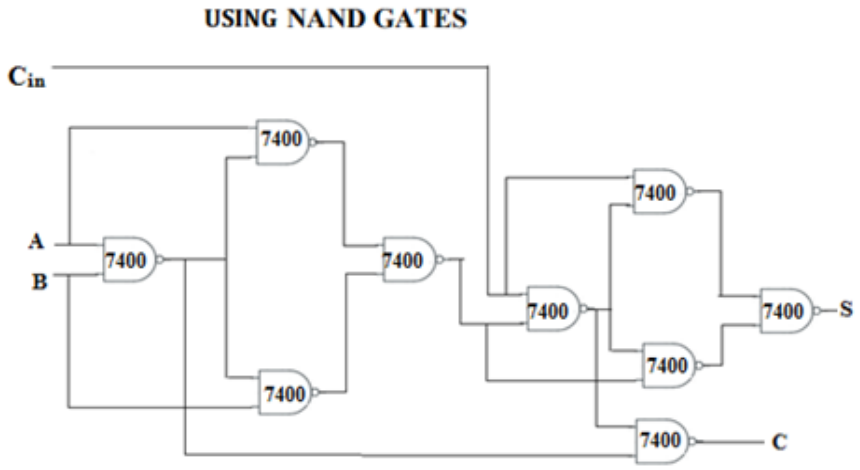
BOOLEAN EXPRESSIONS:

$S = A \oplus B \oplus C$

$C = A\,B + B\,Cin + A\,Cin$

USING BASIC GATES



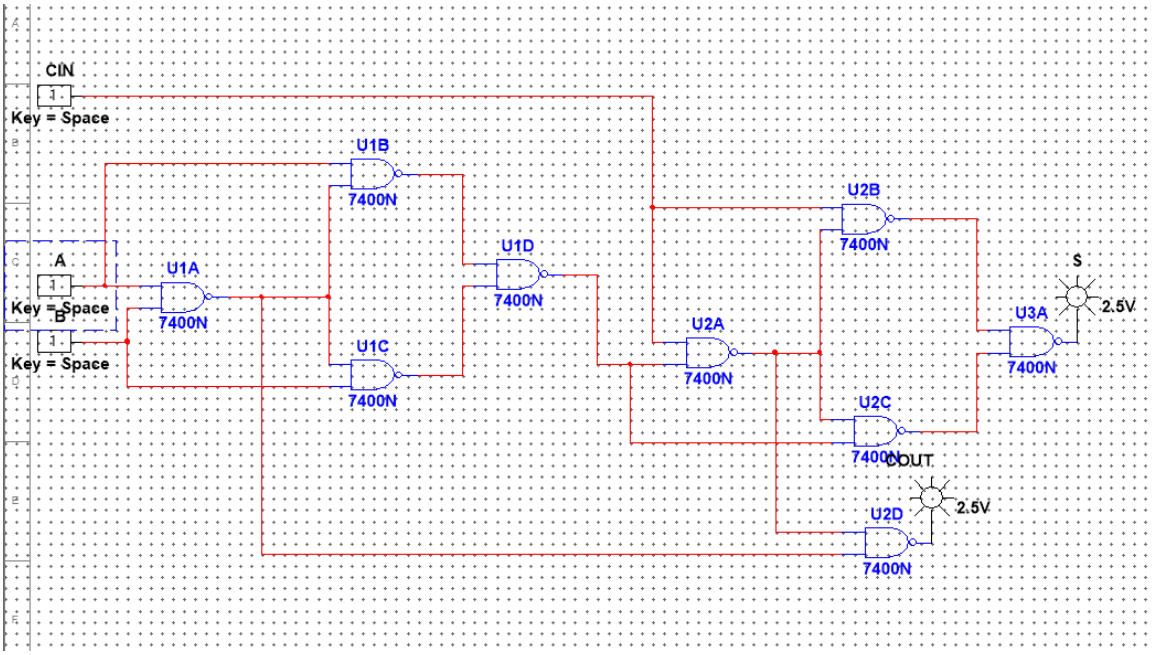


Full Adder Circuit using IC7483:

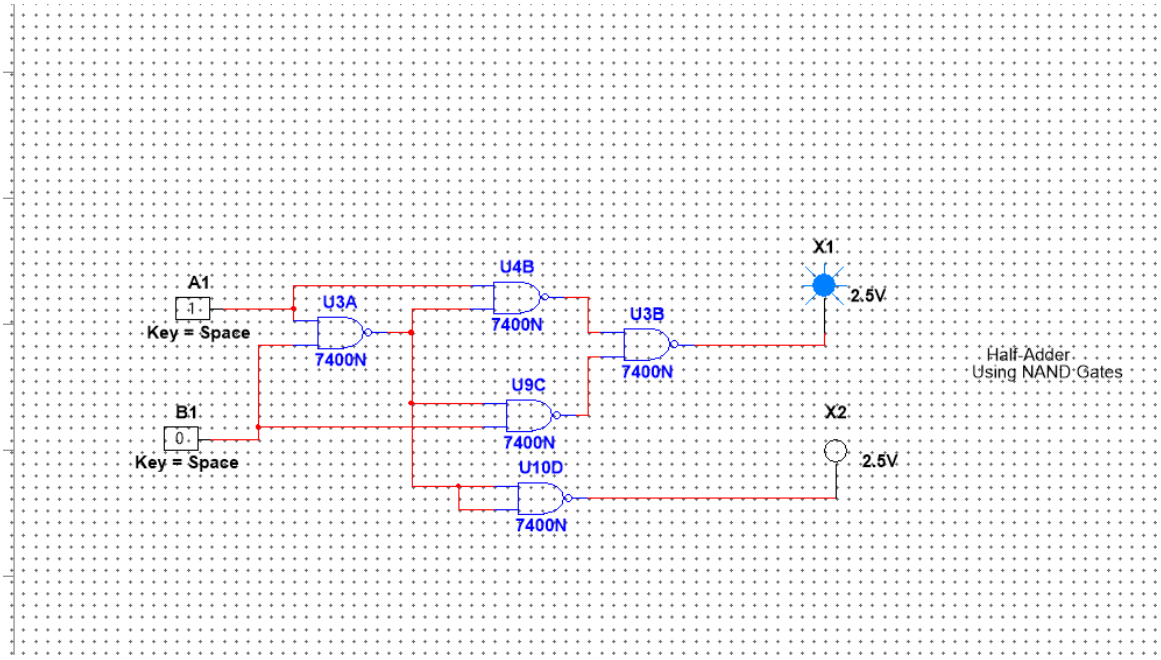
A Full adder can add single-digit binary numbers and carries. The largest sum that can be obtained using a full adder is 11_2. Parallel adders can add multiple-digit numbers. If full adders are placed in parallel, we can add two- or four-digit numbers or any other size desired.

Figure below uses standard symbols to show a parallel adder capable of adding two; two-digit binary numbers. The addend would be on A inputs, and the augend on the B inputs. For this explanation we will assume there is no input to C_0 (carry from a previous circuit)

CIRCUIT DIAGRAM:



FULL ADDER USING NAND GATES



PROCEDURE:

1. Connect one set of inputs from A1 to A4 pins and the other set from B1 to B4, on the IC 7483.
2. Connect the pins from S1 to S4 to output terminals.
3. Short S,C0 to XOR gate 1 input and other input take from C4 and obtain the
4. Output Carry Cout (Output Borrow Bout).
5. In order to Perform Addition take S=0.
6. Apply the inputs to the adder circuits as shown in the truth tables.
7. Check the outputs and note them down in the table for the corresponding inputs.
8. Verify that the outputs match with the expected results.

OBSERVATION TABLE

a. Half Adder

A	B	S	C_{in}
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

b. Full Adder

A	B	C	S	C_{in}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

CONCLUSION: We implemented using NAND gate for the full adder and half adder.

PRECAUTION:

a) Make the connections according to the IC pin diagram.

b) The connection should be tight.

EXPT - 5

ON

Design and implement a 3:8 decoder

AIM: Design and implement a 3:8 Decoder.

Detailed objective of the experiment:

To design and implement a 3:8 decoder circuit with enable input and verify its truth table.

APPARATUS REQUIRED:

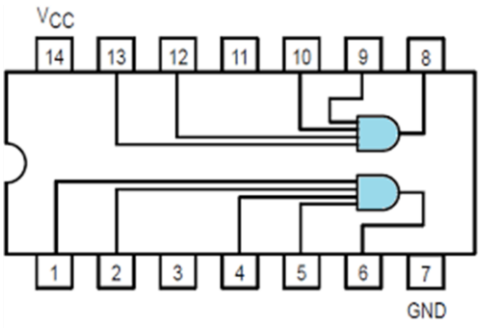
1. Trainer Kit (Micro LABORATORY Kit -II) or
   Wish board, Power supply

CIRCUIT COMPONENTS:

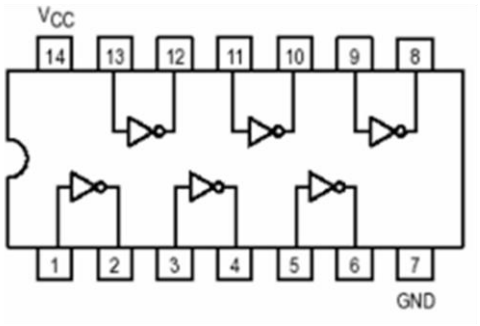
1. 4-input AND gate IC: 7421 (4 Nos.)
2. NOT gate-IC: 7404 (1 No.)
3. Connecting wires

PIN DIAGRAM:

Pin Diagram of IC 7421 (Dual 4-INPUT AND GATES) & IC 7404 (HEX NOT GATES)



IC 7421

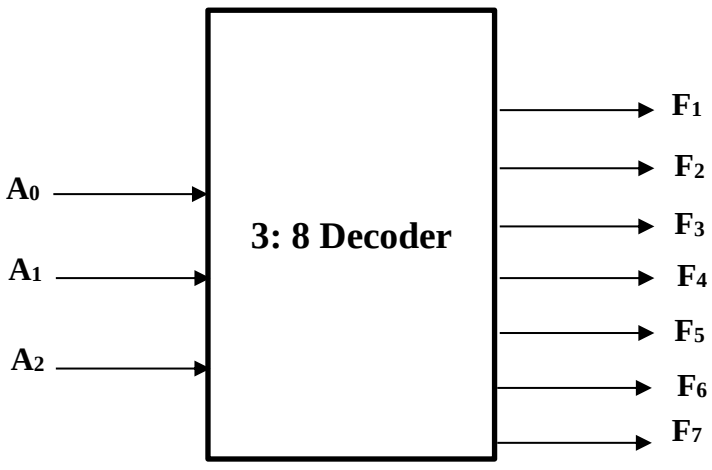


IC 7404

THEORY:

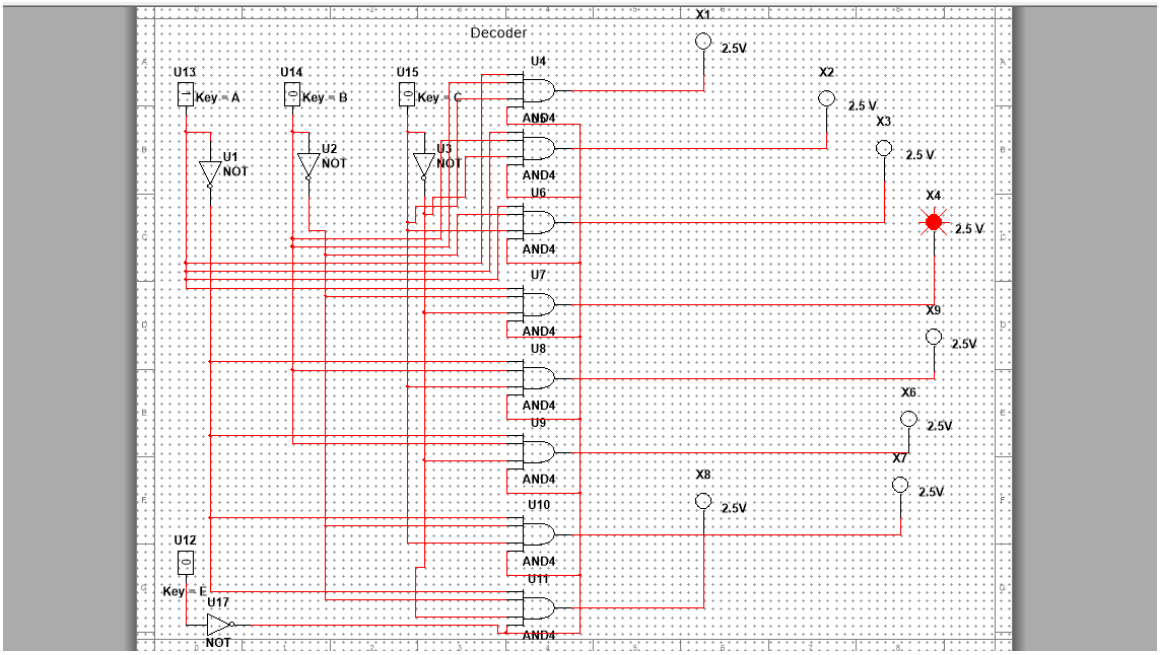
A decoder is a logic circuit that detects the presence of a specific binary number or word. The input to the decoder is a parallel binary number and the output is a binary signal that indicates the presence or absence of that specific number. It is a combinational circuit that converts binary information from 'n' input lines to a maximum of '2^n' unique output lines.

Design of 3: 8 Decoder:



There are 3 input lines (A_0, A_1, A_2) and 8 output lines (F_0, F_2, . . . ,F_7). The input 'EN' is used for enabling the device. EN input mentioned in the figure is active low. The truth table mentioned below describes the operation of the circuit.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Before switching ON Power Supply, make sure that the connections are correct.
3. Apply the input logic states as per Truth Table, in terms of +5 volts for state-1 and 0 volts for state-0.
4. Observe the output states.
5. Verify the results of truth ness.
6. Repeat steps from 3 to 5 for all possible combinations of function table.

OBSERVATION TABLE:

Inputs				Outputs							
A_2	A_1	A_0	EN	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	1	0	0	0	1	0	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0	0	0

CONCLUSION: We implemented a 3-8 Decoder and verified the truth table

PRECAUTION:

a) Make the connections according to the IC pin diagram

b) The connection should be tight

EXPT - 6

ON

Design and implement 8:3 priority encoder

AIM: Design and implement 8:3 priority encoder.

Detailed objective of the experiment:

To design and implement 8:3 Priority Encoder and verify its truth table

APPARATUS REQUIRED:

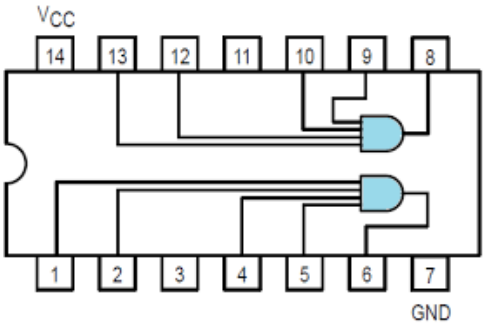
1. Trainer Kit (Micro LABORATORY Kit -II) or
   Wish board, Power supply

CIRCUIT COMPONENTS:

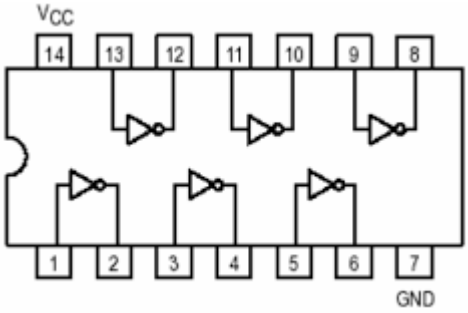
1. 4-input AND gate IC: 7421 (4 Nos.)
2. NOT gate-IC: 7404 (2 No.)
3. 2-input AND gate IC:7408 (2Nos.)
4. 2-input OR gate IC:7432 (2Nos.)
5. Connecting Wires

PIN DIAGRAM:

Pin Diagram of IC 7421 (Dual 4-INPUT AND GATES) & IC 7404 (HEX NOT GATES)

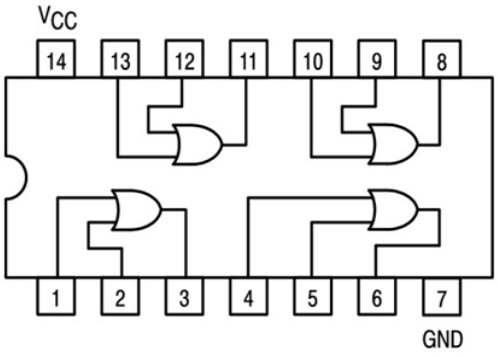


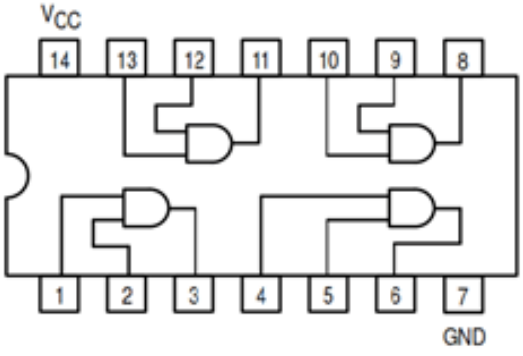
IC 7421



IC 7404

Pin Diagram of IC 74LS32 (QUAD 2-INPUT OR GATES) & IC 7408 (QUAD 2-INPUT AND GATES)





2 input OR gate IC (74LS32) 2 input AND gate IC (7408)

THEORY:

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if two or more inputs are high, i.e., equal to 1 then the input which is having the highest priority will take precedence.

Design of an 8:3 priority encoder

An 8:3 priority encoder has 2^3 i.e 8 inputs, namely, D0, D1, …, D8 and 3 outputs, namely, O0, O1 and O2 as shown in the Figure 1 below. Along with the 3 outputs, it also has a fourth output V for indicating whether the inputs are valid or not. If all the inputs are 0 then it's an invalid input and the output V will become 1 in this case. Therefore, a valid input is one, in which at least one input has a value of 1.

The subscript having the higher decimal value in the input is having the higher priority. Therefore, D7 is having the highest priority and whenever D7 is 1, regardless of other input values, the output will be 111. D6 will have the next higher priority, then D5 and so on.

Figure 1: Block diagram of 8:3 priority encoder

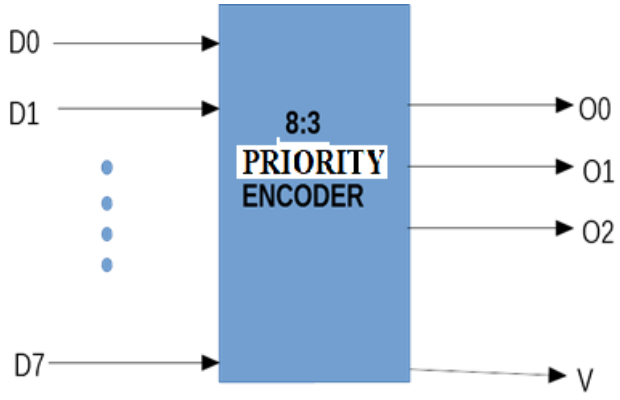


Table 1: Truth table of 8:3 **PRIORITY** encoder

INPUTS								OUTPUTS			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**O2**	**O1**	**O0**	**V**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**X**	**X**	**X**	**1**
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
0	**0**	**0**	**0**	**0**	**0**	**1**	**X**	**0**	**0**	**1**	**0**
0	**0**	**0**	**0**	**0**	**1**	**X**	**X**	**0**	**1**	**0**	**0**
0	**0**	**0**	**0**	**1**	**X**	**X**	**X**	**0**	**1**	**1**	**0**
0	**0**	**0**	**1**	**X**	**X**	**X**	**X**	**1**	**0**	**0**	**0**
0	**0**	**1**	**X**	**X**	**X**	**X**	**X**	**1**	**0**	**1**	**0**
0	**1**	**X**	**X**	**X**	**X**	**X**	**X**	**1**	**1**	**0**	**0**
1	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**1**	**1**	**1**	**0**

From the truth table shown in Table 1, we can write the *Boolean expression* for the four outputs in Product of Sum (POS) form as follows:

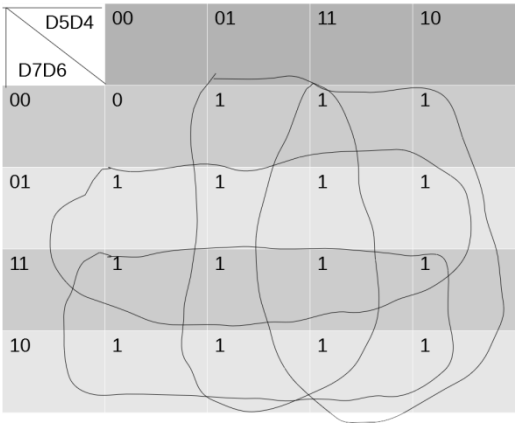
O0=$\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}\ \underline{D3}\ \underline{D2}$ D1 + $\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}$ D3 + $\underline{D7}\ \underline{D6}$ D5 + D7

O1=$\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}\ \underline{D3}$ D2+ $\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}$ D3 + $\underline{D7}$ D6+ D7

O2=$\underline{D7}\ \underline{D6}\ \underline{D5}$ D4+ $\underline{D7}\ \underline{D6}$ D5+ $\underline{D7}$ D6+ D7

V=$\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}\ \underline{D3}\ \underline{D2}\ \underline{D1}\ \underline{D0}$

K-Map for O2



O2=D7+D6+D5+D4

O1 Simplification:

O1=$\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}\ \underline{D3}$ D2+ $\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}$ D3 + $\underline{D7}$ D6+ D7

=$\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}\ \underline{D3}$ D2+ $\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}$ D3 + D6+ D7…….(A+$\underline{A}B = A + B$)

= $\underline{D6}\ \underline{D5}\ \underline{D4}\ \underline{D3}$ D2+ $\underline{D7}\ \underline{D5}\ \underline{D4}$ D3 + D6+ D7……. …….(A+$\underline{A}B = A + B$)

= $\underline{D5}\ \underline{D4}$ D2+ $\underline{D5}\ \underline{D4}$ D3 + D6+ D7

O1 = $\underline{D5}\ \underline{D4}$ **(D2+ D3) + D6+ D7**

O0 Simplification:

O0 =$\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}\ \underline{D3}\ \underline{D2}$ D1 + $\underline{D7}\ \underline{D6}\ \underline{D5}\ \underline{D4}$ D3 + $\underline{D7}\ \underline{D6}$ D5 + D7 …(A+$\underline{A}B = A + B$)

= $\underline{D6}\ \underline{D5}\ \underline{D4}\ \underline{D3}\ \underline{D2}$ D1 + $\underline{D6}\ \underline{D5}\ \underline{D4}$ D3 + $\underline{D6}$ D5 + D7

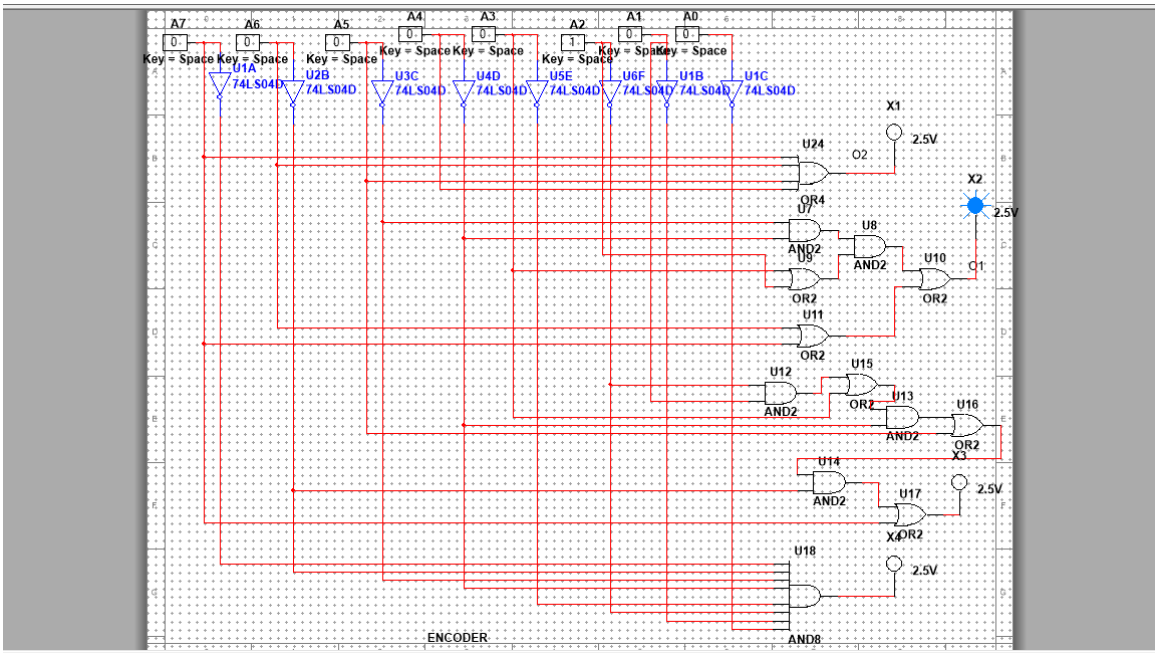
= $\underline{D6}$ ($\underline{D4}\ \underline{D3}\ \underline{D2}$ D1 + $\underline{D4}$ D3 + D5) + D7

O0 = $\underline{D6}$ ($\underline{D4}$ **(** $\underline{D2}$ **D1 + D3)+ D5)+ D7**

PROCEDURE:

1. Connect the circuit as shown in the logic diagram.
2. Before switching ON the power supply, make sure that the connections are correct.
3. Apply the input logic states as per truth table, in terms of +5 volts for state-1and 0 volts for state-0.
4. Observe the output states.
5. Verify the results with the truth table
6. Repeat steps from 3 to 5 for all possible combinations of input shown in the truth table.

CIRCUIT DIAGRAM:



OBSERVATION TABLE:

INPUTS								OUTPUTS			
D7	D6	D5	D4	D3	D2	D1	D0	O2	O1	O0	V
0	0	0	0	0	0	0	0	X	X	X	1
0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	1	X	0	0	1	0
0	0	0	0	0	1	X	X	0	1	0	0
0	0	0	0	1	X	X	X	0	1	1	0
0	0	0	1	X	X	X	X	1	0	0	0
0	0	1	X	X	X	X	X	1	0	1	0
0	1	X	X	X	X	X	X	1	1	0	0
1	X	X	X	X	X	X	X	1	1	1	0

CONCLUSION: We implemented the 8-3 Encoder the verified the truth table.

PRECAUTION:

a) Make the connections according to the IC pin diagram

b) The connection should be tight

EXPT - 7

ON
Design a 4 -bit magnitude comparator using combinational circuits

AIM: Design a 4 bit magnitude comparator using combinational circuits

Detailed objective of the experiment:

i. Make truth table for the 4-bit magnitude comparator
ii. Obtain the Boolean Expressions for the three outputs
iii. Implement using logic gates

APPARATUS REQUIRED:

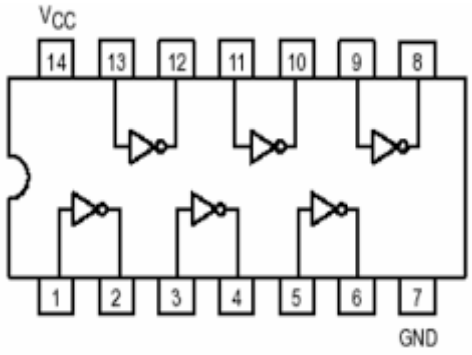
1. Trainer Kit (Micro LABORATORY Kit -II) or
   Wish board, Power supply

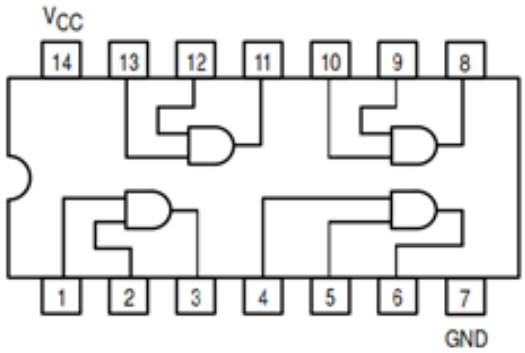
CIRCUIT COMPONENTS:

1. ICs: 7408,7402,7404 etc.
2. Connecting Wires
3. Connecting Wires

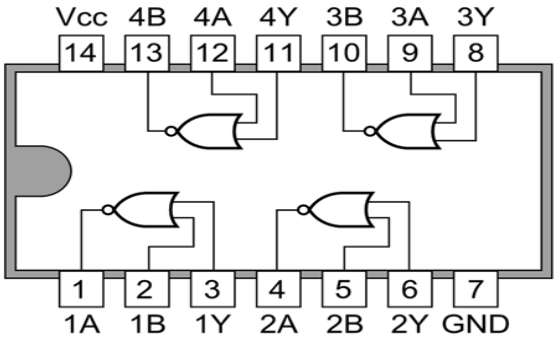
PIN DIAGRAM:

Pin Diagram of IC 7404 (HEX NOT GATES) & IC 7408 (QUAD 2-INPUT AND GATES)

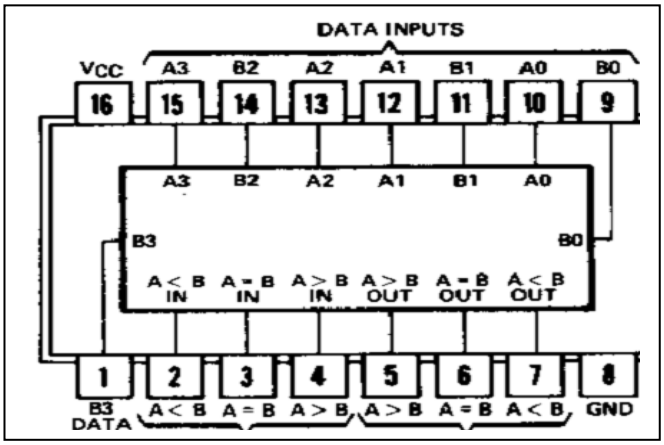




Pin Diagram of IC 7402 (QUAD 2-INPUT NOR GATES



Pin Diagram of IC 7485 (4-bit magnitude comparator)



THEORY:

Magnitude Comparator

The comparison of two numbers is an operation that determines whether one number is greater than, less than, or equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and Band determines their relative magnitudes. The outcome of the comparison is specified by three binary variables that indicate whether A>B, A=B, or A<B.

Inputs:

First n-bit number A ; Second n-bit number B

Outputs:

Three output signals (GT, EQ, LT), where:

1. GT = 1 IFF A > B 2. EQ = 1 IFF A = B 3. LT = 1 IFF A < B

One of these three outputs will be equal to 1, while the other 2 outputs will be 0's.

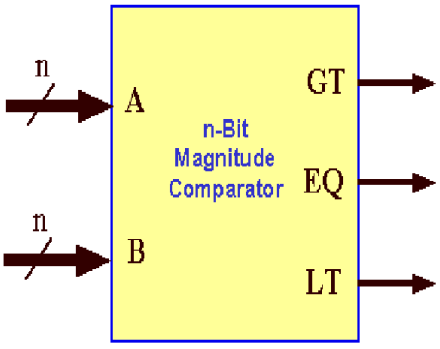


Figure 1. Block diagram of n-bit Magnitude Comparator

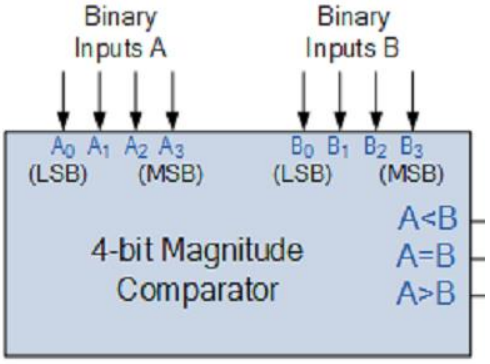


Figure 2. Block diagram of n-bit Magnitude Comparator

Design procedure of a 4-Bit Magnitude Comparator

Inputs: 8-bits (A ⇒4-bits, B ⇒4-bits)
A and B are two 4-bit numbers

- Let A = $A_3A_2A_1A_0$, and
- Let B = $B_3B_2B_1B_0$
- Inputs have 2^8(256) possible combinations
- Not easy to design using conventional techniques

The circuit possesses certain amount of regularity ⇒can be designed algorithmically.

a. Design of the EQ output (A = B) in 4-bit magnitude comparator

Each subscripted letter represents one of the digits in the number. The two numbers are equal if all pairs of significant digits are equal: $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$, and $A_0 = B_0$. When the numbers are binary, the digits are either 1 or 0.

The equality of each pair of bits can be expressed logically with an exclusive-NOR function as

$$X_i = A_iB_i + A'_iB'_i$$

Thus $X_i = 1$ IFF $A_i = B_i$; $X_i = 0$ IFF $A_i \neq B_i$ for i =0, 1, 2 and 3

Condition for A= B

EQ=1 (i.e., A=B) IFF

i. $A_3=B_3 \rightarrow (X_3= 1)$, and
ii. $A_2=B_2 \rightarrow (X_2= 1)$, and
iii. $A_1=B_1 \rightarrow (X_1= 1)$, and
iv. $A_0=B_0 \rightarrow (X_0= 1)$.

Thus, EQ=1 IFF $X_3X_2X_1X_0= 1$. In other words, EQ = $X_3X_2X_1X_0$

b. Design of the GT output (A >B) and LT output (A<B) in 4-bit magnitude Comparator

To determine whether A is greater or less than B

- we inspect the relative magnitudes of pairs of significant digits, starting from the most significant position.
- If the two digits of a pair are equal, we compare the next lower significant pair of digits. The comparison continues until a pair of unequal digits is reached.

- If the corresponding digit of A is 1 and that of B is 0, we conclude that A>B.
- If the corresponding digit of A is 0 and that of B is 1, we have A<B.

The sequential comparison can be expressed logically by the two Boolean functions

$$(A > B) = A_3B'_3 + x_3A_2B'_2 + x_3x_2A_1B'_1 + x_3x_2x_1A_0B'_0$$

$$(A < B) = A'_3B_3 + x_3A'_2B_2 + x_3x_2A'_1B_1 + x_3x_2x_1A'_0B_0$$

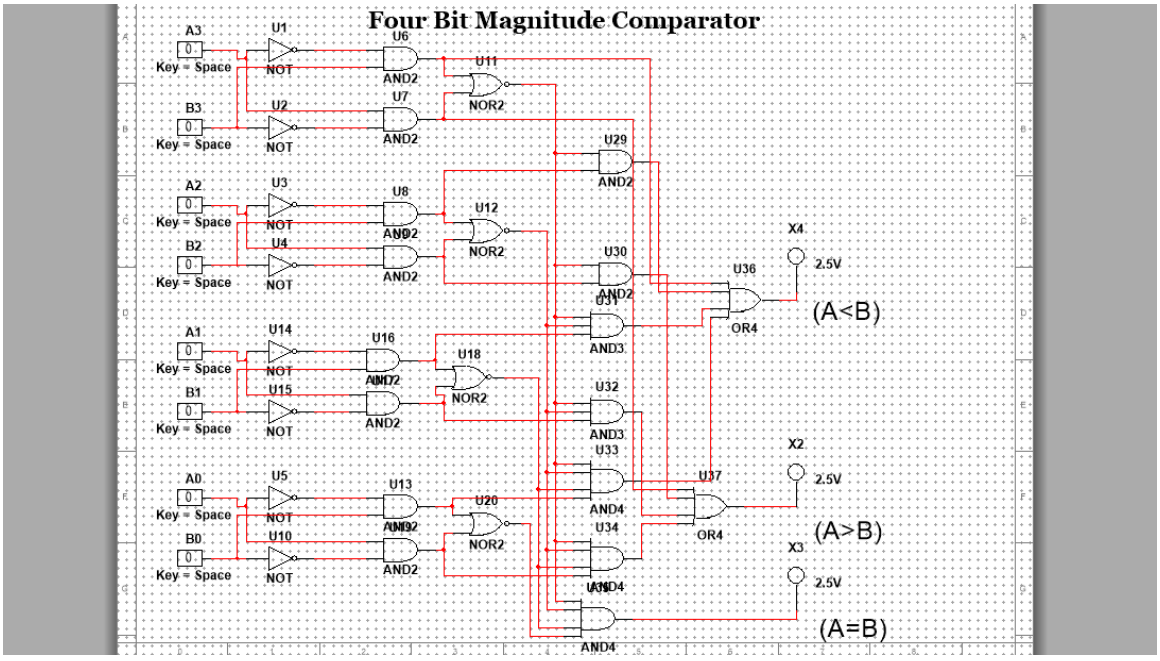
The symbols (A>B) and (A<B) are binary output variables that are equal to 1 when A>B and A>B, respectively.

- The logic diagram of the four-bit magnitude comparator is shown in Figure 2.
- The four x outputs are generated with exclusive-NOR circuits and are applied to an AND gate to give the output binary variable (A=B).
- The other two outputs use the x variables to generate the Boolean functions listed previously.

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Before switching ON power Supply, make sure that the connection are correct.
3. Apply the input logic as per Truth table in terms of +5 volts for state-1 and 0 volts for state-0.
4. Observe the Output state.
5. Verify the result of truthness.
6. Repeat steps from 3 to 5 for all possible combination.

CIRCUIT DIAGRAM:



OBSERVATION TABLE:

Sl. No.	A				B				A>B	A<B	A=B
	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0			
1	0	1	1	1	0	0	1	1	1	0	0
2	0	1	1	0	0	1	1	0	0	0	1
3	1	0	0	0	1	1	0	0	0	1	0
4	1	1	0	0	1	1	0	0	0	0	1
5	0	1	0	0	0	0	1	0	1	0	0
6	1	0	0	1	1	1	0	0	0	1	0
7	1	1	0	0	1	0	0	0	1	0	0

PRECAUTION:

a) Make the connections according to the IC pin diagram

b) The connection should be tight

EXPT - 8

ON

Design and implement 8:1 multiplexer and 1:4 demultiplexer

AIM: Design and implement 8:1 multiplexer and 1:4 demultiplexer.

APPARATUS REQUIRED:

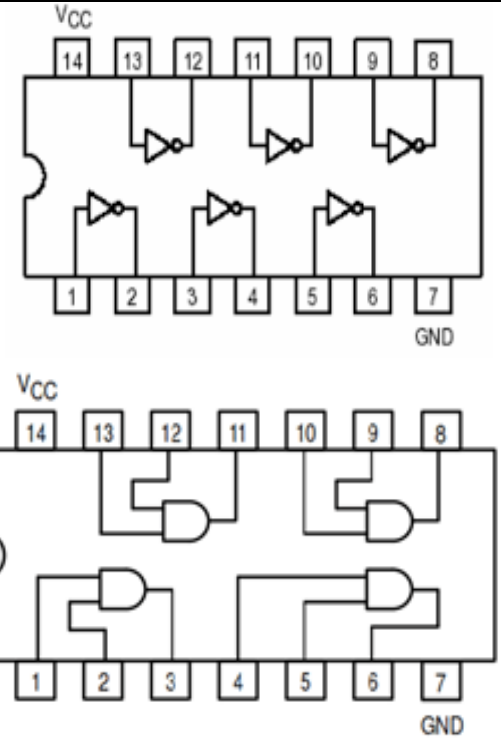
1. Trainer Kit (Micro LABORATORY Kit -II) or
   Wish board, Power supply

CIRCUIT COMPONENTS:

1. ICs: Four 7411, One 74HC4078, One 7432, Two 7404 etc.
2. Connecting Wires
3.

PIN DIAGRAM:

Pin Diagram of IC 7404 (HEX NOT GATES) &
Pin Diagram of IC 74LS32 (QUAD 2-INPUT AND GATES)



THEORY:

MULTIPLEXER:

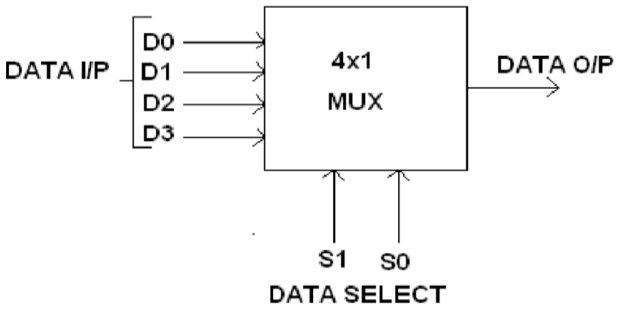
Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2n input line and n selection lines whose bit combination determine which input is selected.

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer. In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

A). 4:1 MILTIPLEXURE:

BLOCK DIAGRAM FOR 4:1 MULTIPLEXER



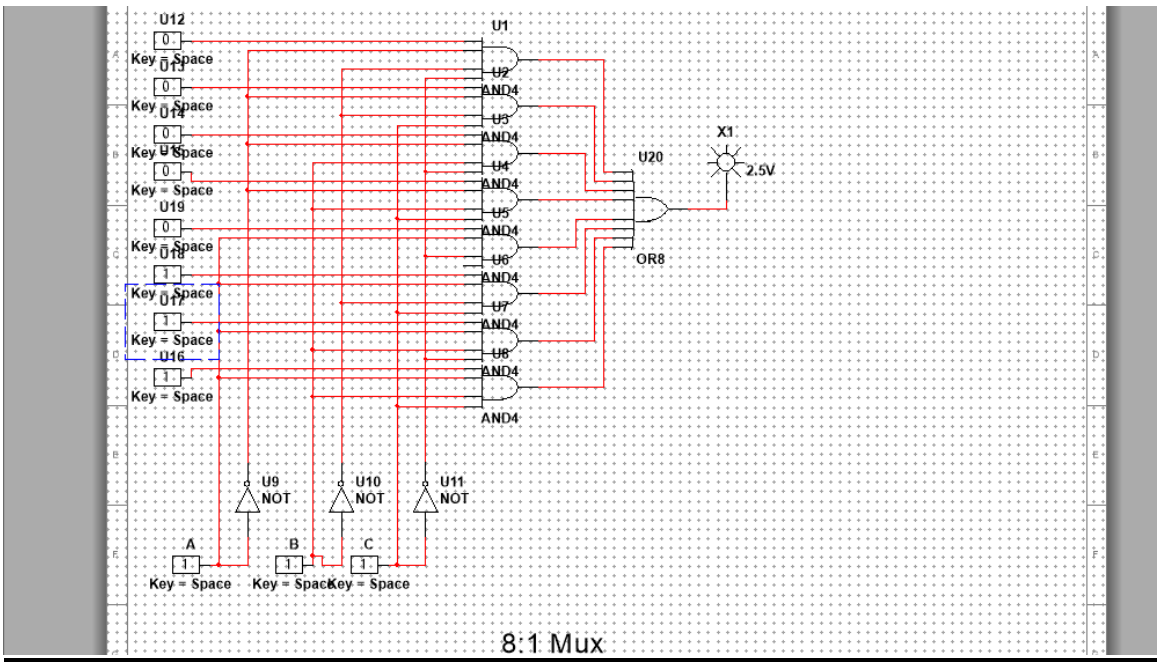
TRUTH TABL of 4:1 MILTIPLEXURE

S1	S0	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

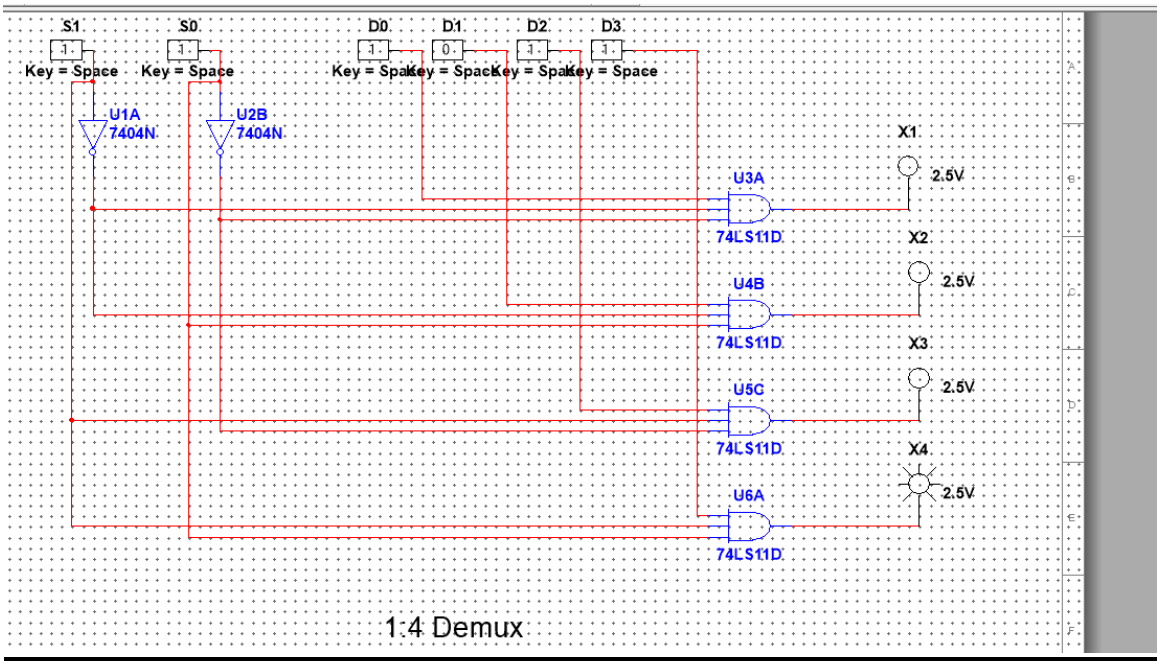
Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

CIRCUIT DIAGRAM:

CIRCUIT DIAGRAM FOR 8:1 MULTIPLEXER



CIRCUIT DIAGRAM FOR 1:4 DEMULTIPLEXER :



PROCEDURE:

1. Fix the IC's on the bread board & give the input supply.
2. Make connections according to the circuit.
3. Give select signal and strobe signal at respective pins.
4. Verify the truth table of multiplexer and demultiplexer for various inputs.

OBSERVAION TABLE

i) **Verification of the Truth Table**: ***8:1 MULTIPLEXER*** :

INPUT	OUTPUT

Enable	**S2**	**S1**	**S0**	
0	**x**	**x**	**x**	**X**
1	**0**	**0**	**0**	D0
1	**0**	**0**	**1**	D1
1	**0**	**1**	**0**	D2
1	**0**	**1**	**1**	D3
1	**1**	**0**	**0**	D4
1	**1**	**0**	**1**	D5
1	**1**	**1**	**0**	D6
1	**1**	**1**	**1**	D7

ii) Verification of the Truth Table: *1:4 De-MULTIPLEXER*:

INPUT			**OUTPUT**			
S1	**S0**	**I/P**	**D0**	**D1**	**D2**	**D3**
0	**0**	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**	**0**	**0**
0	**1**	**0**	**0**	**0**	**0**	**0**
0	**1**	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**0**	**0**	**0**
1	**0**	**1**	**0**	**0**	**1**	**0**
1	**1**	**0**	**0**	**0**	**0**	**0**
1	**1**	**1**	**0**	**0**	**0**	**1**

CONCLUSION: We implemented 8:1 Multiplexer and 1:4 Demultiplexer and verified the truth table.

PRECAUTION:

a) Make the connections according to the IC pin diagram

b) The connection should be tight

c) The V_{cc} and ground should be applied carefully at the specified pins only.

EXPT - 9

ON

Design a ALU with functions of ADD, SUB, INVERT, OR, AND, XOR, INC, DEC and CMP

AIM: Design a ALU with functions of ADD, SUB, INVERT, OR, AND, XOR, INC, DEC, and CMP

APPARATUS REQUIRED:

1. Wish Board
2. Microlab-II

CIRCUIT COMPONENTS:

1. IC 74181
2. LED with resistors
3. Connecting wires

PIN DIAGRAM:

Pin Diagram of IC 74LS181

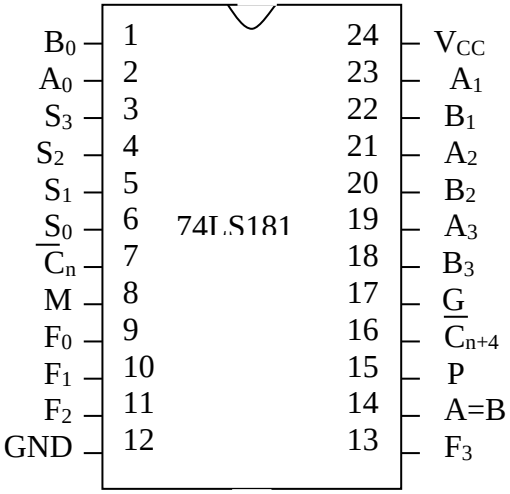


Fig. 2

THEORY:

ALU: The arithmetic and logic unit perform all the necessary arithmetic and logical operations. It requires one or two operands upon which it operates and produces a result. It is basically a multifunction combinational logic circuit. It provides select input to select the particular operation.

IC74LS181: It is a 4-bit Arithmetic Logic Unit (ALU). Its features are as given below:

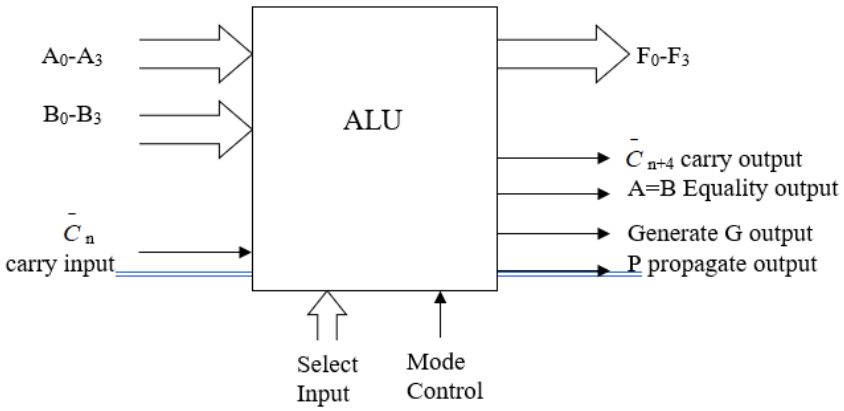
Features:

- Provides 16 arithmetic operations: add, subtract, compare, double, plus twelve other arithmetic operations.

- Provides all 16 logic operations of two variables: exclusive-OR, compare, AND, NAND, OR, NOR, Plus ten other logic operations.
- Full lookahead for high speed arithmetic operation on long words

Fig 1 and Fig. 2 show the block diagram and connection diagram for IC 74LS181. As shown in the Fig. 2, 74LS181 has two four bit operands ($A_0 – A_3$ and $B_0 – B_3$). Its mode select input selects one of the two modes : arithmetic or logic, and four function select inputs select a particular function from the selected mode. Table(1) gives the pin description for IC 74LS181.

Block Diagram: - **Fig 1**



Pin description of IC 74LS181

Pin Names	Description
A_0-A_3	Operand Inputs
B_0-B_3	Operand Inputs
S_0-S_3	Function Select Input
M	Mode Control Input
$\bar{C}_n$	Carry Input (Active LOW)
F_0-F_3	Function Output
A=B	Comparator Output
G	Carry Generate Output
P	Carry Propagate Output
$\bar{C}_{n+4}$	Carry Output (Active LOW)

Table (3) : Function Table-1 for IC 74LS181 (For $C_n = 1$)

Model Select Inputs				**Active HIGH Operands and F_n Outputs**	
S_3	**S_2**	**S_1**	**S_0**	**Logic (M=1)**	**Arithmetic (Note 2) (M=0)(C_n =1)**
0	0	0	0	F=A’	F=A
0	0	0	1	F=A’+B’	F=A+B
0	0	1	0	F=A’B	F=A+B’
0	0	1	1	F=Logic 0	F=minus 1
0	1	0	0	F=(AB)’	F=A plus AB’
0	1	0	1	F=B’	F=(A+B) plus AB’
0	1	1	0	F= $A \oplus B$	F=A minus B minus 1
0	1	1	1	F=AB’	F=AB minus 1

1	0	0	0	F=A'+B	F=A plus AB
1	0	0	1	F= $A' \oplus B'$	F=A plus B
1	0	1	0	F=B	F=(A+B') plus AB
1	0	1	1	F=AB	F=AB minus 1
1	1	0	0	F=logic 1	F=A plus A (Note 1)
1	1	0	1	F=A+B'	F=(A+B) plus A
1	1	1	0	F=A+B	F=(A+B') plus A
1	1	1	1	F=A	F=A minus 1

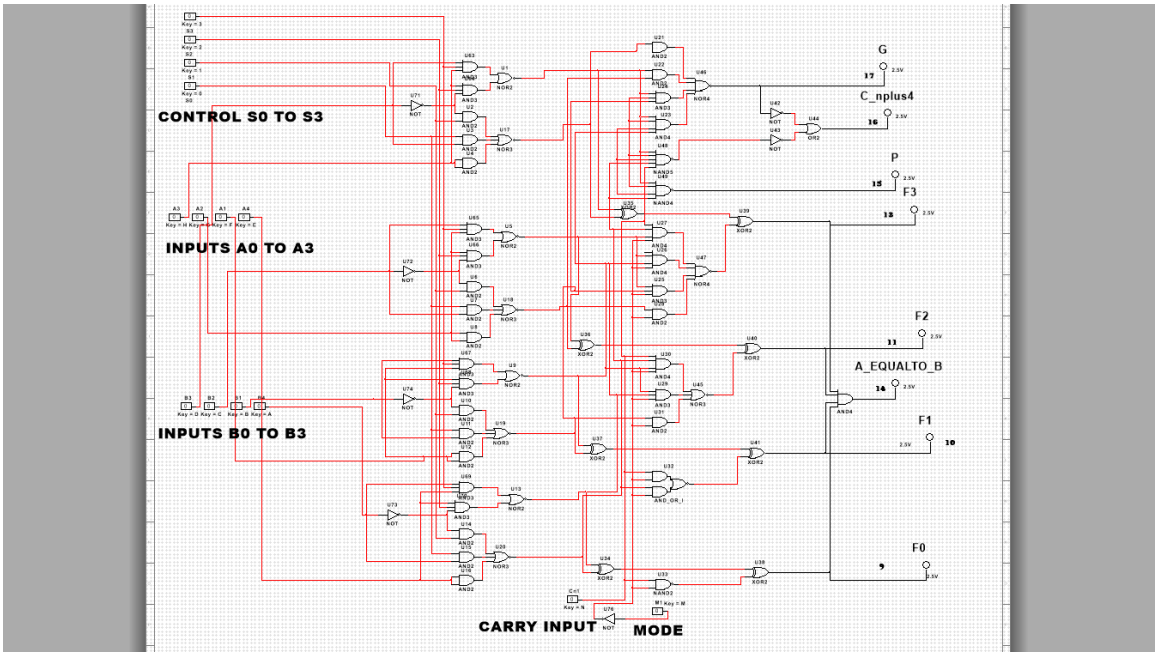
Table (3) Function Table-2 for IC 74LS181(For $C_n = 0$)

Model Select Inputs				**Active LOW Operands and F_n Outputs**	
S_3	**S_2**	**S_1**	**S_0**	**Logic (M=1)**	**Arithmetic (Note 2) (M=0) (C_n =0)**
0	0	0	0	F=A'	F=A minus 1
0	0	0	1	F=A'+B'	F=AB minus 1
0	0	1	0	F=A'B	F=AB' minus 1
0	0	1	1	F=Logic 1	F=minus 1
0	1	0	0	F=A'+B'	F=A plus (A+B')
0	1	0	1	F=B'	F=AB plus (A+B')
0	1	1	0	F= $A \oplus B$	F=A minus B minus 1
0	1	1	1	F=AB'	F=A+B'
1	0	0	0	F=A'+B	F=A plus (A+B)
1	0	0	1	F= $A' \oplus B'$	F=A plus B
1	0	1	0	F=B	F=AB' plus (A+B)
1	0	1	1	F=AB	F=A+B
1	1	0	0	F=Logic 1	F=A plus A (Note 1)
1	1	0	1	F=A+B'	F=AB plus A
1	1	1	0	F=A+B	F=AB' minus A
1	1	1	1	F=A	F=A

PROCEDURE:

1. Connect the circuit as shown in the circuit diagram.
2. Before switching ON power Supply, make sure that the connections are correct.
3. Apply the input logic as per Truth table in terms of +5 volts for state-1 and 0 volts for state-0.
4. Observe the Output state.
5. Verify the result of truthness.
6. Repeat steps from 3 to 5 for all possible combination.

CIRCUIT DIAGRAM:



OBSERVATION TABLE:

i). **ADDITION: A + B**

Mode Selection PIN Values =1011,M = 0., C_n = 0

S. No	Carry Input	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	S_3	S_2	S_1	S_0	Carry output
1	0	1	0	1	0	0	1	0	1	1	0	0	1	0
2	0	1	0	1	1	1	1	0	1	1	0	0	0	1
3	0	0	1	1	0	1	0	1	0	0	0	0	0	1
4	0	1	0	0	0	0	1	1	1	1	1	1	1	0
5	0	1	0	1	1	0	0	1	1	1	1	1	0	0
6	0	0	1	1	1	1	0	0	0	1	1	1	1	0
7	0	1	0	0	1	1	1	0	0	0	1	0	1	1

ii). **SUBSTRACTION: A - B**

Mode Selection PIN Values = 0110 M = 0., C_n = 0

S. No	Borrow Input	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	D_3	D_2	D_1	D_0	Borrow output
1	0	0	1	0	0	0	1	1	0	0	0	0	0	0
2	0	1	0	1	0	0	1	1	0	0	1	0	0	0
3	0	1	0	1	0	0	1	1	0	0	1	1	0	0
4	0	1	1	0	0	0	0	0	0	1	0	1	0	0
5	0	1	1	0	1	0	1	1	0	0	1	1	1	0

iii). **Inverter: A'**

Mode Selection PIN Values = 0000 M = 1 $C_n = 0$

S. No	INPUT				OUTPUT			
	A_3	A_2	A_1	A_0	A_3'	A'_2	A'_1	A'_0
1	0	1	0	1	1	0	1	0
2	1	0	0	0	0	1	1	1
3	0	1	1	0	1	0	0	1

iv). **OR: Logic A+B**

Mode Selection PIN Values = 1110 M =1 $C_n = 0$

S. No	INPUTS								OUTPUT			
	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	Y_3	Y_2	Y_1	Y_0
1	0	0	1	1	1	0	1	0	1	0	1	1
2	0	1	0	0	1	0	0	0	1	1	0	0
3	1	0	1	0	0	0	1	1	1	0	1	1

v). **AND: Logic A . B**

Mode Selection PIN Values = 0110 M =1, C_n =0

S. No	INPUTS								AND OUTPUT			
	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	Y_3	Y_2	Y_1	Y_0
1	1	0	1	0	1	1	1	0	1	0	1	0
2	1	0	1	1	0	0	1	1	0	0	1	1
3	0	1	1	1	0	1	1	0	0	1	0	0

vi). **XOR: Logic A XOR B**

Mode Selection PIN Values = 0110 M = 1 $C_n = 0$

S. No	INPUTS								XOR OUTPUT			
	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	Y_3	Y_2	Y_1	Y_0
1	1	0	0	1	0	0	1	0	0	0	1	1
2	1	1	0	1	0	1	1	0	1	0	1	1
3	0	1	0	1	1	0	1	0	1	1	1	1

vii). **INCREMENT: Logic A + 1**

Mode Selection PIN Values = 0011 M = 1 C_n = 0

S. No	INPUTS				OUTPUT			
	A_3	A_2	A_1	A_0	Y_3	Y_2	Y_1	Y_0
1	1	0	0	1	1	0	0	1
2	0	1	0	1	0	1	1	0
3	1	0	1	0	1	0	1	1

viii). **DECREMENT: Logic A - 1**

Mode Selection PIN Values = 0000 M =1 C_n = 0

S. No	INPUTS				OUTPUT			
	A_3	A_2	A_1	A_0	Y_3	Y_2	Y_1	Y_0
1	1	0	0	1	1	0	0	0
2	1	0	0	0	0	1	1	1
3	0	1	1	1	0	1	1	0

ix). **COMPARE:**

Mode Selection PIN Values = 0110 M = 1, C_n = 0

S. No	INPUTS								OUTPUT		
	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	LT	GT	EQ
1	0	0	0	1	0	0	1	1	1	0	0
2	0	1	0	1	0	1	0	0	0	1	0
3	1	0	0	0	1	0	0	0	0	0	1
4	0	1	1	1	1	0	0	1	0	1	0
5	1	0	1	0	1	1	0	0	1	0	0
6	0	1	1	0	0	1	1	0	0	0	1

CONCLUSION:

ALU can perform most of the necessary operations by providing select input to any particular function. Multiply and divide are not provided but can be performed in multiple steps using the shift and add or subtract function.

PRECAUTION:

a) Make the connections according to the IC pin diagram

b) The connection should be tight

c) The V_{cc} and ground should be applied carefully at the specified pins only.

EXPT - 10

ON

Design and Verify the Decade Counter

AIM: Design and Verify the Decade Counter.

Detailed objective of the experiment: To study the operation of J-K flip-flop and to design Modulo-10 asynchronous counter using J-K flip-flop.

APPARATUS REQUIRED:

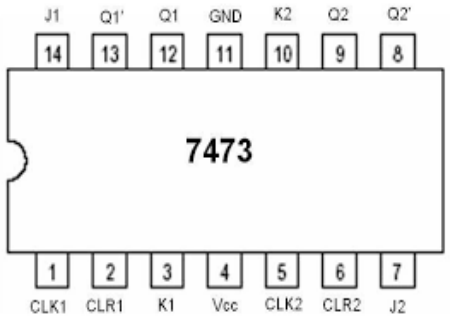
1. Wish board or Trainer Kit.
2. D.C. Power Supply
3. C.R.O.

CIRCUIT COMPONENTS:

4. IC 7400 - 1 NOs.
5. IC 7410 (3-input NAND gate IC) - 1 Nos
6. IC 74LS73D (Dual J-K Flip-flop-negative edge-triggered) - 2 NOs.

PIN DIAGRAM:

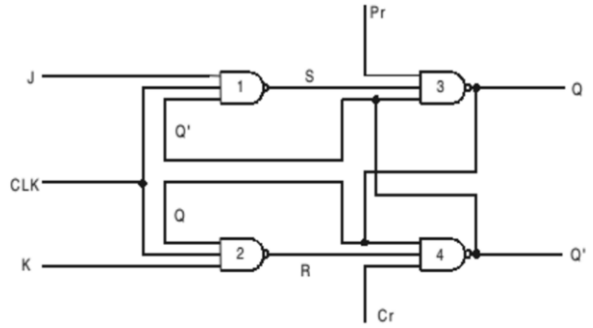
Pin Diagram of IC7473:



THEORY:

A) J-K flip-flop:

A J-K flip-flop has very similar characteristics to an S-R flip-flop. The only difference is that the undefined condition for an S-R flip-flop, i.e., S = R = 1 condition, is also included in this case. Inputs J and K behave like inputs S and R to set and reset the flip-flop respectively. When J = K = 1, the flip-flop is said to be in a toggle state, which means the output switches to its complementary state every time a clock passes. The inherent difficulty of an S-R flip-flop (i.e., S = R = 1) is eliminated by using the feedback connections from the outputs to the inputs of gate 1 and gate 2 as discussed in JK flip-flop. Truth tables JK flip-flop were formed with the assumption that the inputs do not change during the clock pulse (CLK = 1).



J-K Flip-flop Circuit Diagram

Flip-flop inputs		*Present output*	*Next output*
J	*K*	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J-K Flip-flop Characteristic Table

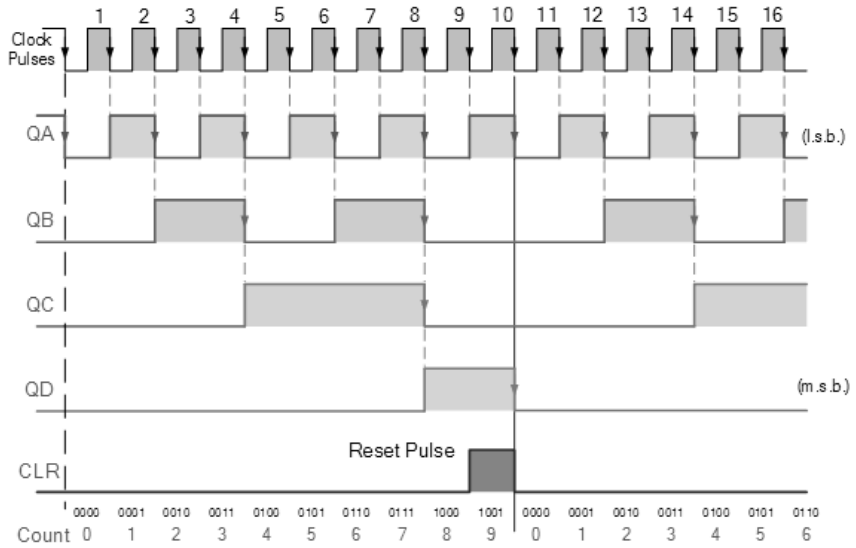
B) Synchronous and asynchronous counter:

Counters are circuits made using flip-flops. Synchronous counter, as the name suggests, have all the flip-flops working in sync with clock pulse as well as each other. Here clock pulse is applied to every flip flop. Whereas in Asynchronous counter clock pulse is applied only to the initial flip flop whose value would be considered as LSB. Instead of the clock pulse, the output of first flip-flop acts as a clock pulse to the next flip flop, whose output is used as a clock to the next in line flip-flop and so on. Thus, in Asynchronous counter after the transition of the previous flip flop, the transition of the next flip flop takes place, not at the same time as seen in Synchronous counter.

The truth table, circuit diagram and timing diagram of the asynchronous decade (MOD-10) counter are shown below.

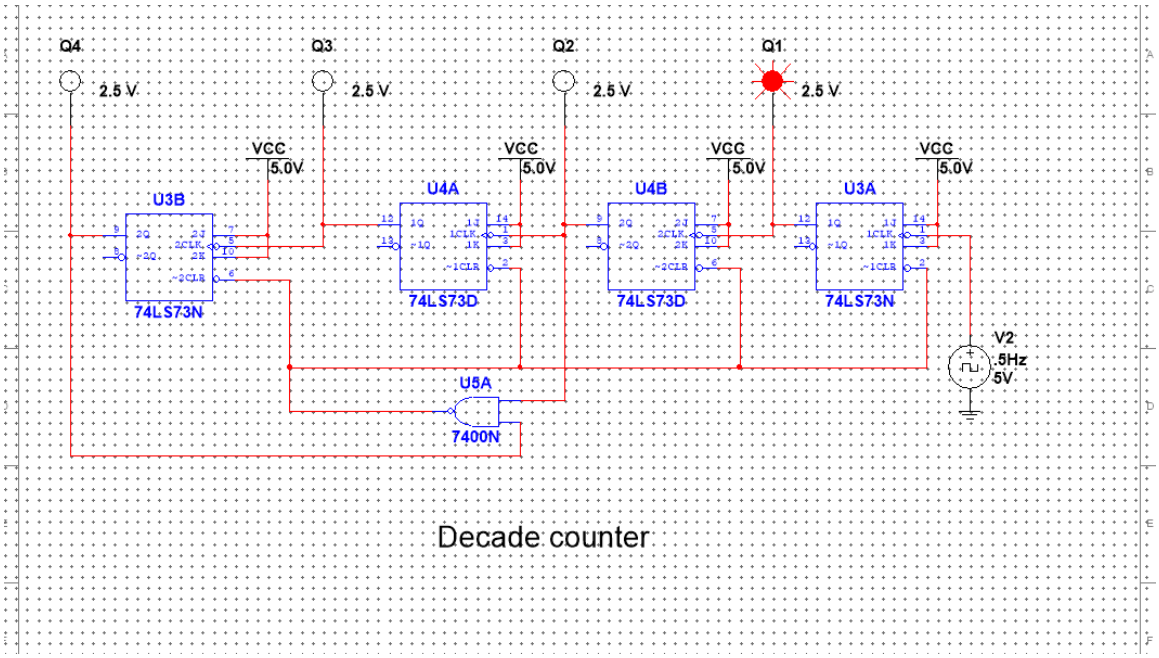
Clock Count	**Q_D**	**Q_C**	**Q_B**	**Q_A**	**Decimal Value**
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	Counter Resets its Outputs back to Zero				

Decade Counter Timing Diagram:



CIRCUIT DIAGRAM:

Circuit Diagram of Decade counter using IC-74LS73



PROCEDURE:

1. Fix the IC's on the bread board & give the input supply.
2. Make connections according to the circuit.
3. Give the external Clock signal and observe the Q1, Q2, Q3, Q4
4. Check the recounting and verify the truth table of the decade counter

OBSERVATION TABLE:

Clock Count	Q_4	Q_3	Q_2	Q_1	Decimal Value
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	0	0	0	0	0

PRECAUTION:

a) Make the connections according to the IC pin diagram

b) The connection should be tight

c) The V_{cc} and ground should be applied carefully at the specified pins only.

EXPT - 11

ON

Design a ROM (8X4) using a decoder, gates and diodes

AIM: Design a ROM (8X4) using a decoder, gates and diodes.

APPARATUS REQUIRED:

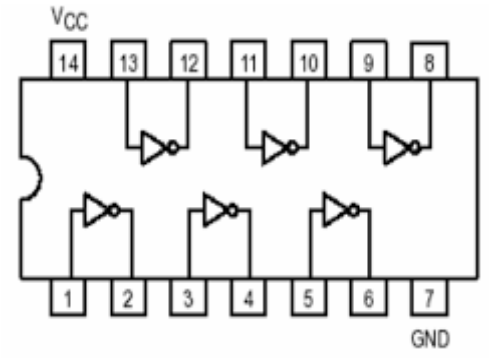
1. Wish board or Trainer Kit.
2. D.C. Power Supply
3. C.R.O.

CIRCUIT COMPONENTS:

1. Decoder IC 74LS138 (1 No.)
2. Hex Inverter IC 74LS04 (2 Nos.)
3. Diodes 1N4007 (20 Nos.)
4. LED (4 Nos.)
5. Resistors (1Kohm, 4 Nos.)

PIN DIAGRAM:

Pin Diagram of IC 7404 (HEX NOT GATES)

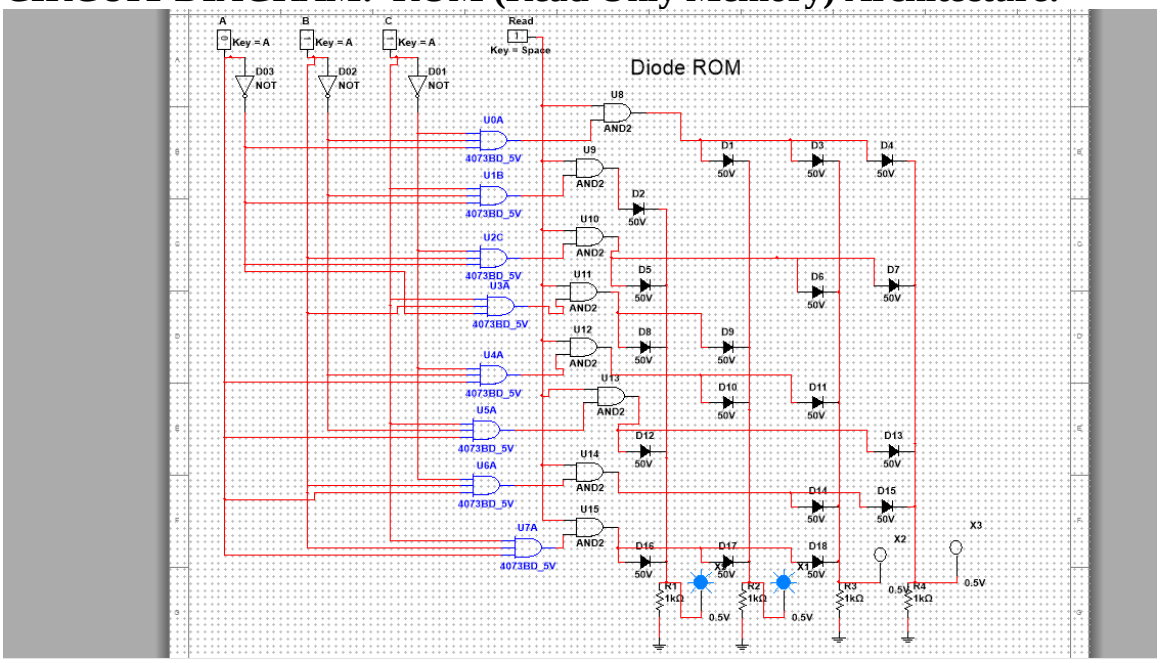


THEORY:

ROM (Read Only Memory)

ROM is used for storing programs that are permanently resident in the computer and for tables of constants that do not change in value once the production of the computer is completed. In this experiment you will design a 8X4 ROM for storing 4 bit data/code at 8 different memory locations using diodes and then you will read data/code from any of the 8 locations by sending three bit address via a address decoder circuit.

CIRCUIT DIAGRAM: ROM (Read Only Memory) Architecture:



PROCEDURE:

1. Fix the Decoder IC's on the bread board & give the input supply.
2. Make connections according to the circuit.
3. observe the output
4. Check the recounting and verify the truth table of the decade counter

OBSERVATION TABLE:

Address bits			Location	Output bits				O/P In Hex
A_2	A_1	A_0		Y_3	Y_2	Y_1	Y_0	
0	0	0	1^{st}	0	1	1	1	7
0	0	1	2^{nd}	1	0	0	0	8
0	1	0	3^{rd}	1	0	1	1	B
0	1	1	4^{th}	1	1	0	0	C
1	0	0	5^{th}	0	1	1	0	6
1	0	1	6^{th}	1	0	0	1	9
1	1	0	7^{th}	0	0	1	1	3
1	1	1	8^{th}	1	1	1	0	E

CONCLUSION: Here we understood that Diode Rom Matrix which we used can covert BCD to decimal readout.

PRECAUTION:

a) Make the connections according to the IC pin diagram

b) The connection should be tight

c) The Vcc and ground should be applied carefully at the specified pins only.

EXPT - 12

ON

Design a pre settable up and down counter

AIM: Design a pre settable up and down counter

Detailed objective of the experiment:

1) Design a binary up and down counter using IC
2) Design a pre settable up and down counter for any random preset value

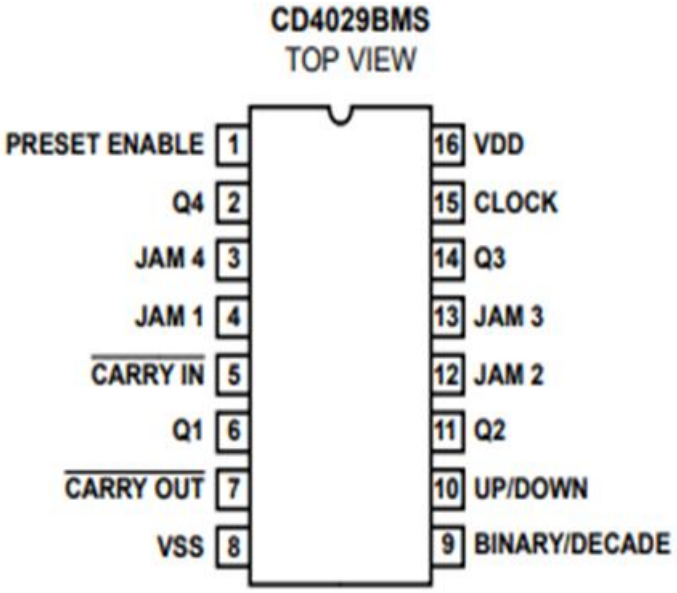
APPARATUS REQUIRED:

1. Wish board or Trainer Kit.
2. D.C. Power Supply
3. C.R.O.

CIRCUIT COMPONENTS:

1. CD4029 Decade counter IC4029

PIN DIAGRAM:



THEORY:

Up-Down Counter. **Counters** are used in many different applications. Some **count up** from zero and provide a change in state of output upon reaching a predetermined value; others **count down** from a preset value to zero to provide an output state change. The **counters** are synchronous, but they are asynchronously pre settable. In this experiment you will use IC CD 4029 and implement following counter configurations.

i. 4 bit Binary UP Counter

ii. 4 bit Binary DOWN Counter

iii. 4 bit Binary UP Counter with preset value

iv. 4 bit Binary Down Counter with preset value

Description of IC 4029

CD4029BMS consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, $\overline{\text{CARRY-IN}}$ ($\overline{\text{CLOCK ENABLE}}$), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a $\overline{\text{CARRY OUT}}$ signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the $\overline{\text{CARRY-IN}}$ and PRE-SET ENABLE signals are low. Advancement is inhibited when the $\overline{\text{CARRY-IN}}$ or PRESET ENABLE signals are high. The $\overline{\text{CARRY-OUT}}$ signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the $\overline{\text{CARRY-IN}}$ signal is low. The $\overline{\text{CARRY-IN}}$ signal in the low state can thus be considered a $\overline{\text{CLOCK ENABLE}}$. The $\overline{\text{CARRY-IN}}$ terminal must be connected to VSS when not in use.

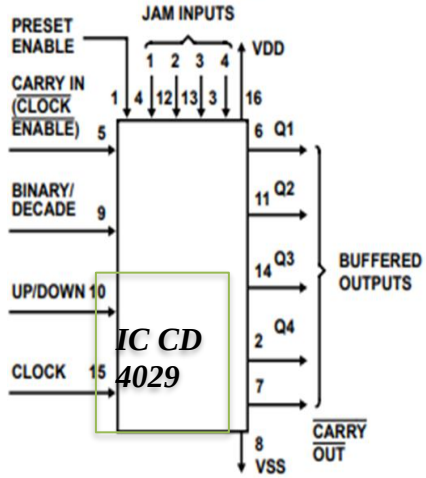
Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts up when the UP/DOWN input is high, and down when the UP/DOWN input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Figure 17.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

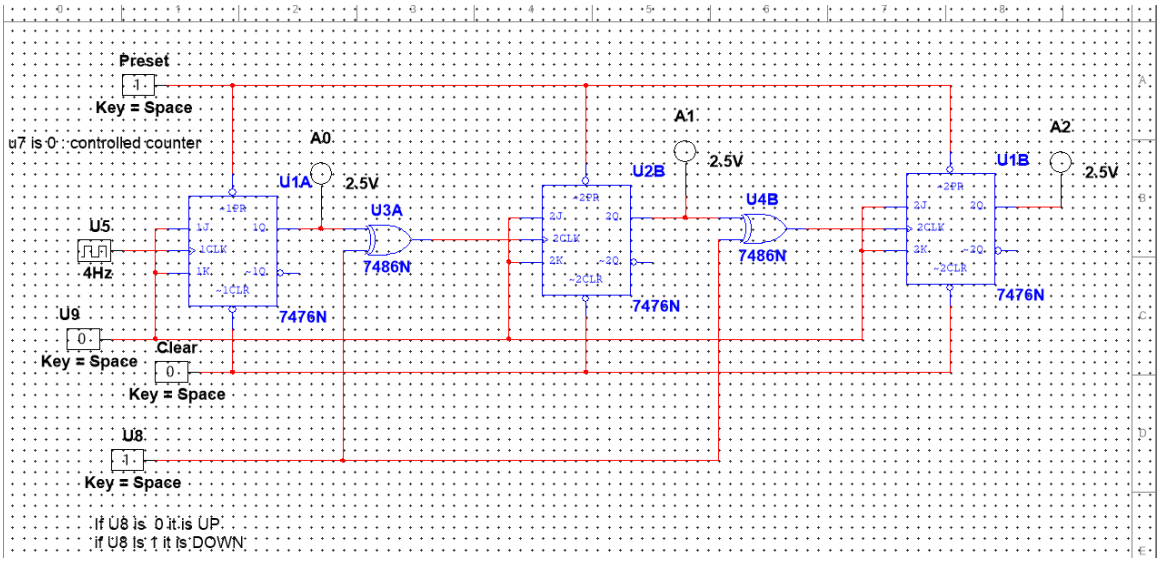
The CD4029BMS is supplied in these 16-lead outline packages:

Braze Seal DIP	H4X
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Functional Diagram



CIRCUIT DIAGRAM:



PROCEDURE:

1. Fix the IC's on the bread board.
2. Make connections according to the circuit.
3. Give the external Clock signal
4. Make Binary/ Decade input (pin9) of the IC4029 HIGH for binary counting.

For binary UP Counter

5. Make UP/ Down input (pin10) of the IC4029 HIGH for UP-Counting.
6. Observe the output Q1, Q2, Q3, Q4.
7. Verify the truth table of the binary UP-Counter

For binary DOWN Counter

8. Make UP/ Down input (pin10) of the IC4029 LOW for DOWN-Counting.
9. Observe the output Q1, Q2, Q3, Q4.
10. Verify the truth table of the binary DOWN-Counter

For Pre-settable binary UP/DOWN Counter

11. Make Preset input of the IC4029 HIGH.
12. For presetting, apply any random value to the JAM inputs (pin 4, 12, 13, 3).
13. Repeat steps 5 -7 for up counting.
14. Repeat steps 8 -10 for down counting.

OBSERVATION TABLE:

A. Binary UP Counter (Pin 9 & 10 are connected to 5V)

a. Truth table for /UP/DOWN Counter

Clock				
	Q4	Q3	Q2	Q1
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0

12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

B. Truth table for Pre-settable DOWN Counter

Clock				
	Q4	Q3	Q2	Q1
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1

PRECAUTION:

a) Make the connections according to the IC pin diagram
b) The connection should be tight
c) The V_{cc} and ground should be applied carefully at the specified pins only.