CONTENT OF JOURNAL

- Measurement of voltage, time period and frequency of different signals on CRO. Measurement of frequency and phase of two different signals using Lissajous pattern.
- To determine the forward and reverse bias characteristics of PN junction diode.
- To determine the reverse bias characteristics of Zener diode and its application as a voltage regulator.
- Measurement of rectification efficiency and ripple factor of Half-wave and Full-wave rectifier circuits with and without C-Filter.
- To determine the frequency response of CE transistor amplifier and finding its gain Bandwidth product.
- To determine the output and transfer characteristics of JFET and measurement of its voltage gain.
- Design of RC phase shift oscillator using IC-741 Op-Amp and finding its frequency of oscillation.
- Design of Inverting and Non-inverting amplifier using IC 741 OP-AMP and finding its frequency response.
- Realization of Basic logic gates (AND, OR, NOT) using NAND Gate (IC-7400).
- Implementation of Boolean expression F = (A.B.C + D.E) using AND Gate(IC 7408) and OR Gate (IC 7432).
- Generation of Amplitude modulated wave and calculation of percentage of modulation using standard setup.
- Generation of FM-wave and its detection using standard setup.

EXPERIMENT – 1

AIM(A): Measurement of the following using Cathode Ray Oscilloscope (CRO):

a. DC Voltage
b. Peak & RMS Value of AC Voltage
c. Time Period & Frequency of Periodic Signals (Sine Wave, Square Wave, Triangular Wave)

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Power Supply
- CRO
- Function Generator

THEORY:

Cathode ray oscilloscope is one of the most useful electronic equipment, which gives a visual representation of electrical quantities, such as voltage and current waveforms in an electrical circuit. It utilizes the properties of cathode rays of being deflected by an electric and magnetic field and of producing scintillations on a fluorescent screen. Since the inertia of cathode rays is very small, they are able to follow the alterations of very high frequency fields and thus electron beam serves as a practically inertia less pointer. When a varying potential difference is established across two plates between which the beam is passing, it is deflected and moves in accordance with the variation of potential difference. When this electron beam impinges upon a fluorescent screen, a bright luminous spot is produced there which shows and follows faithfully the variation of potential difference. From the trace of the signal several measurements can be made.

Measurement of DC Voltage: Deflection on a CRO screen is directly proportional to the voltage applied to the deflecting plates. Therefore, if the screen is first calibrated in terms of known voltage. i.e., the deflection sensitivity is determined, the direct voltage can be measured by applying it between a pair of deflecting plates. The amount of deflection so produced multiplied by the deflection sensitivity, gives the value of direct voltage.

V = (No. of Divisions) x (Volts / Division)

Measurement of A.C voltage: To measure the alternating voltage of sinusoidal waveform, The AC signal, from the signal generator, is applied across the y –plates. The voltage (deflection) sensitivity band switch (Y-Plates) and time base band switch (X-Plates) are adjusted such that a steady picture of the waveform is obtained on the screen. The vertical height (l) i.e. peak-to-peak height is measured. When this peak-to-peak height (l) is multiplied by the voltage (deflection) sensitivity (n) i.e., volt/div, we get the peak-to-peak voltage (2Vp). From this we get the peak voltage (Vp). The rms voltage Vrms is equal to $\sqrt{2}/$. This rms voltage Vrms is verified with rms voltage value, measured by the multi-meter.

Measurement of Frequency: An unknown frequency source (signal generator) is connected to y-plates of C.R.O. Time base signal is connected to x –plates (internally connected). We get a sinusoidal wave on the screen, after the adjustment of voltage sensitivity band switch (Y-plates) and time base band switch (X-plates). To calculate the frequency of the observed signal, one has to measure the period, i.e., the time taken for 1 complete cycle, using the calibrated sweep scale.

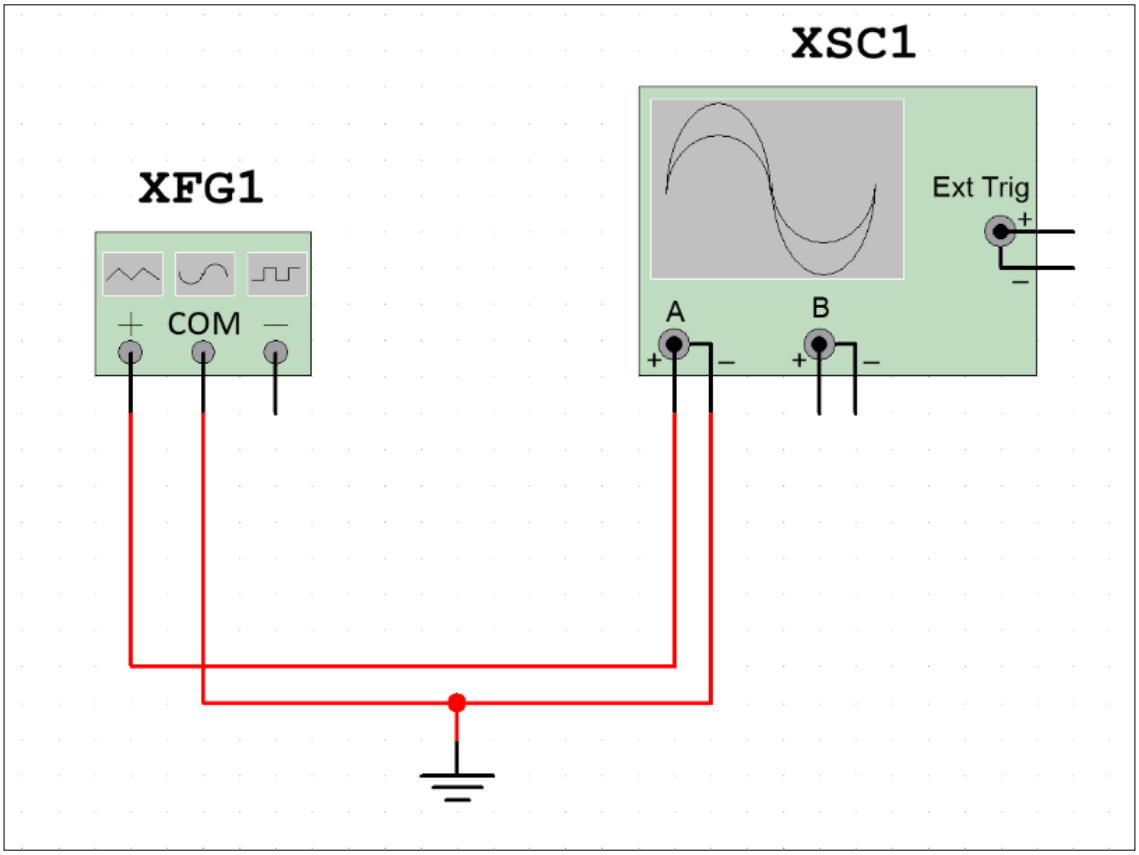
The period could be calculated by:

T = (No. of Divisions) x (Time / Division)

Once the period T is known, the frequency is given by:

f (Hz)= 1/T(sec)

EXPERIMENTAL SETUP:



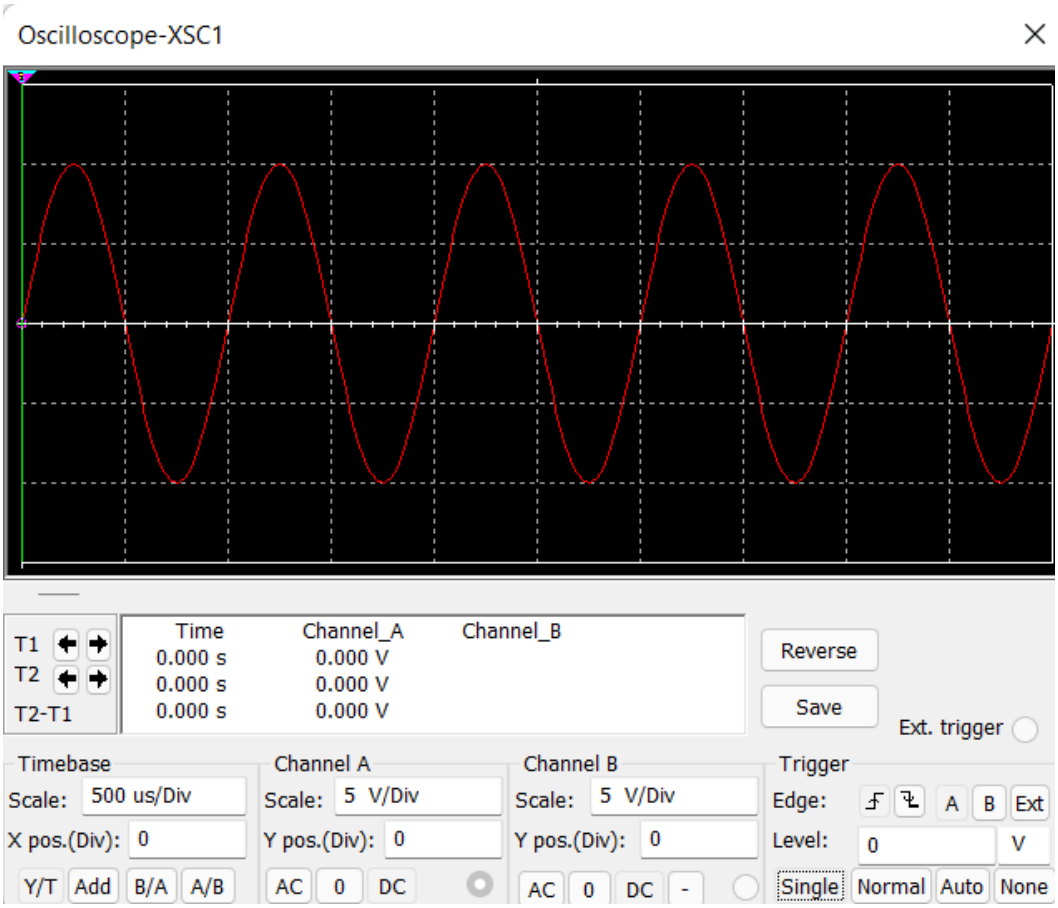
(Circuit diagram for the measurement of Voltage, Time Period, Frequency)

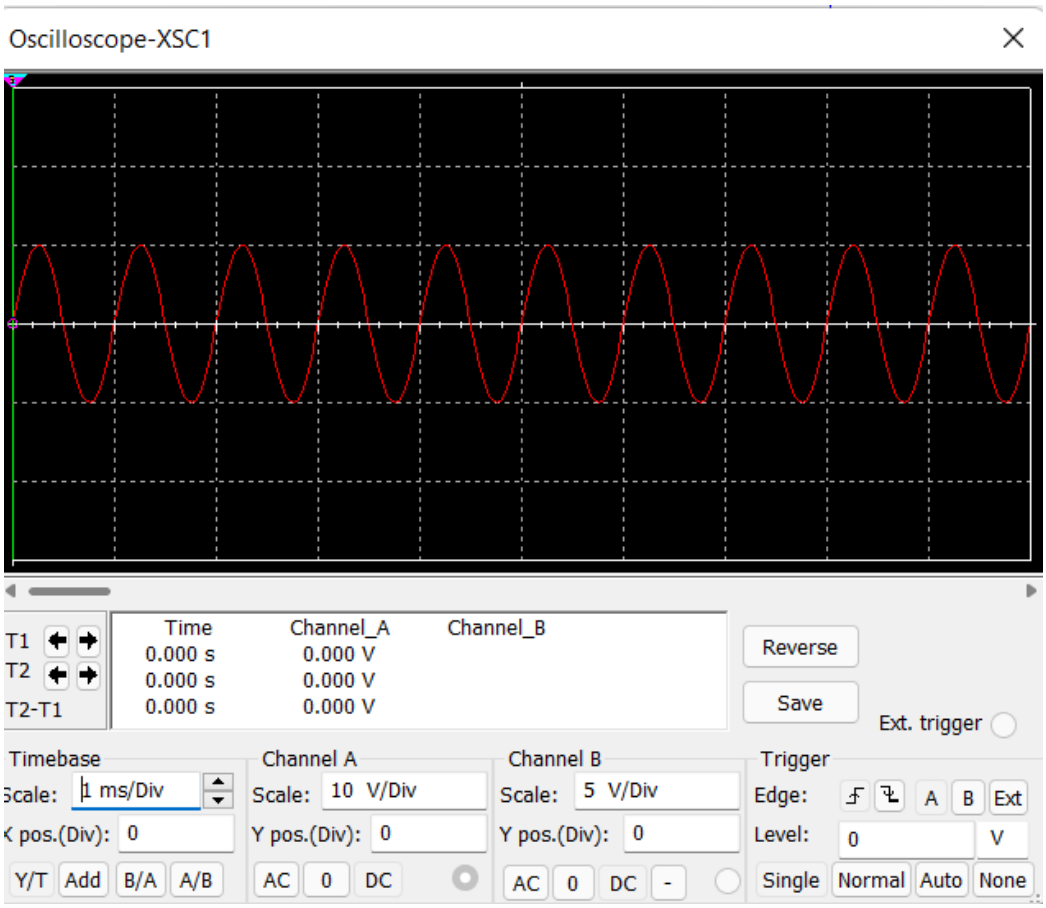
OBSERVATION:

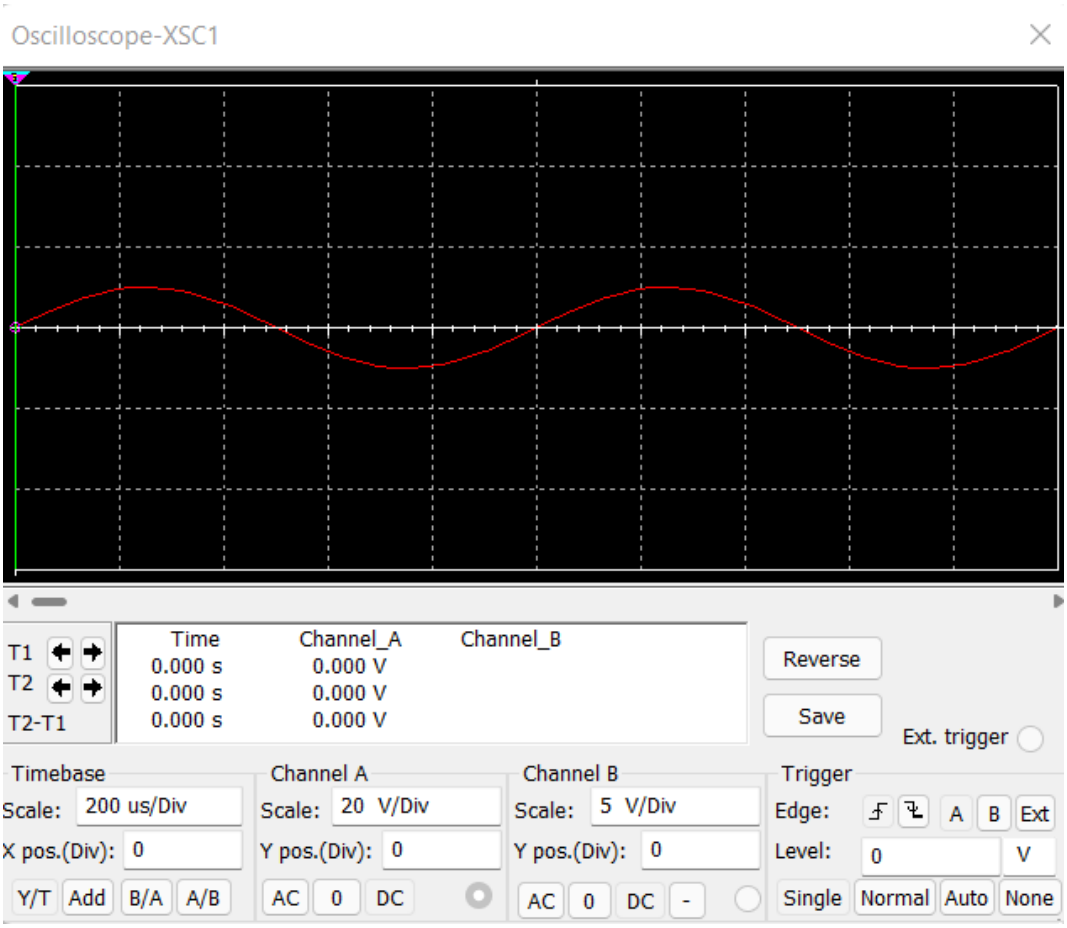
- **For Sine Wave Measurement:**
  1. From Function Generator:
     Input Voltage: 10 Volts
     Input Frequency: 1000 Hz
  2. From CRO:

S No.	Scale on Volts/Div. (V)	Scale on Time/Div. (msec)	No. of division for Peak Voltage (V_p)	No. of division for Time Period (T)	Peak Voltage (V_p)	Rms Voltage $V_{rms}=V_p/\sqrt{2}$ (V)	Time Period (T) (msec)	Measured Frequency (f) (Hz)
1.	5 Volts/Div.	0.5 msec/div.	2 Div.	2 Div.	10 Volts	7.07 Volts	1 msec	1000 Hz
2.	10 Volts/Div.	1 msec/div.	1 Div.	1 Div.	10 Volts	7.07 Volts	1 msec	1000 Hz
3.	20 Volts/Div.	0.2 msec/div.	0.5 Div.	5 Div.	10 Volts	7.07 Volts	1 msec	1000 Hz

Graph For Sine Wave Measurement:





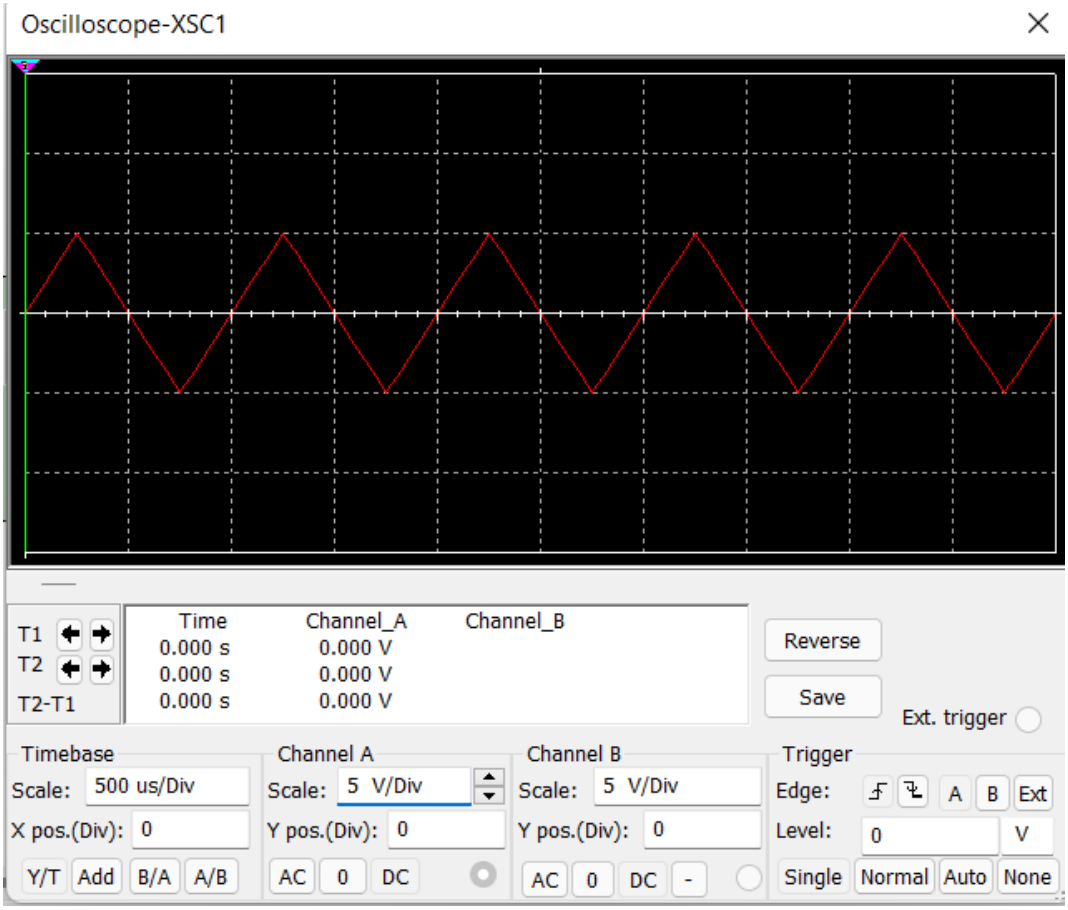


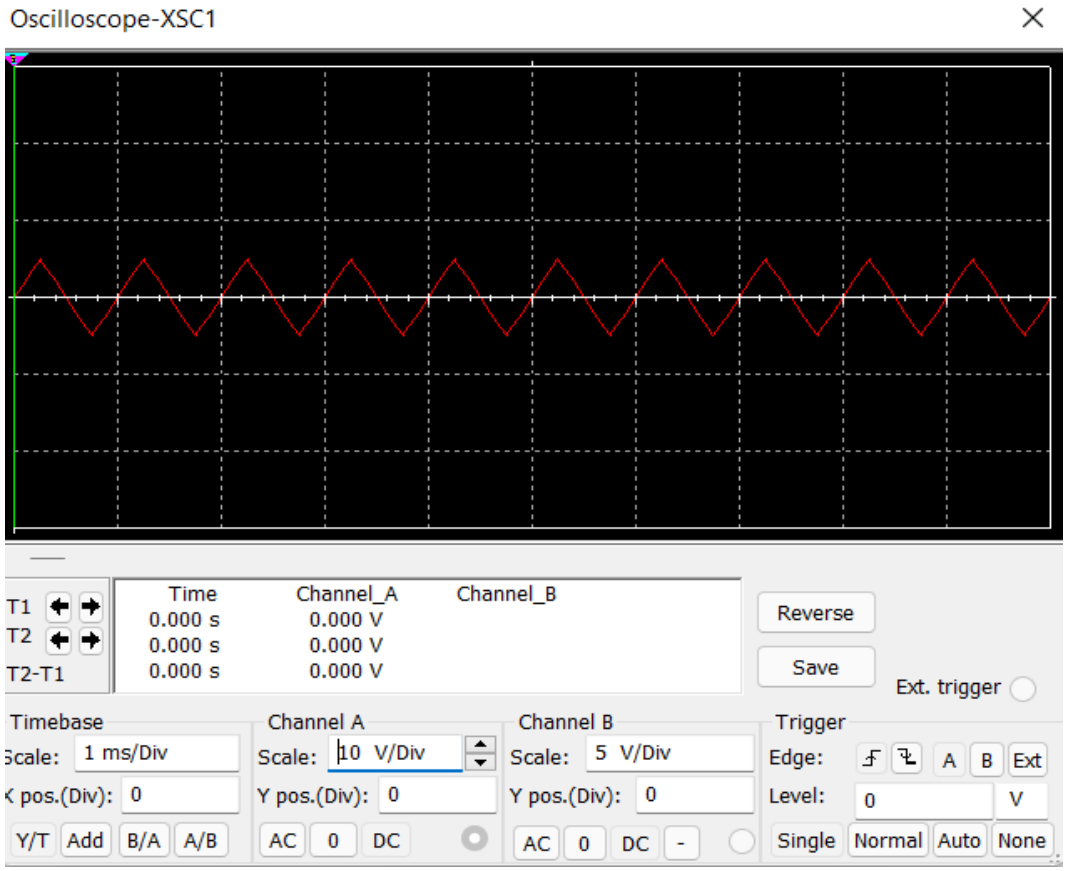
➢ **For Triangular Wave Measurement:**

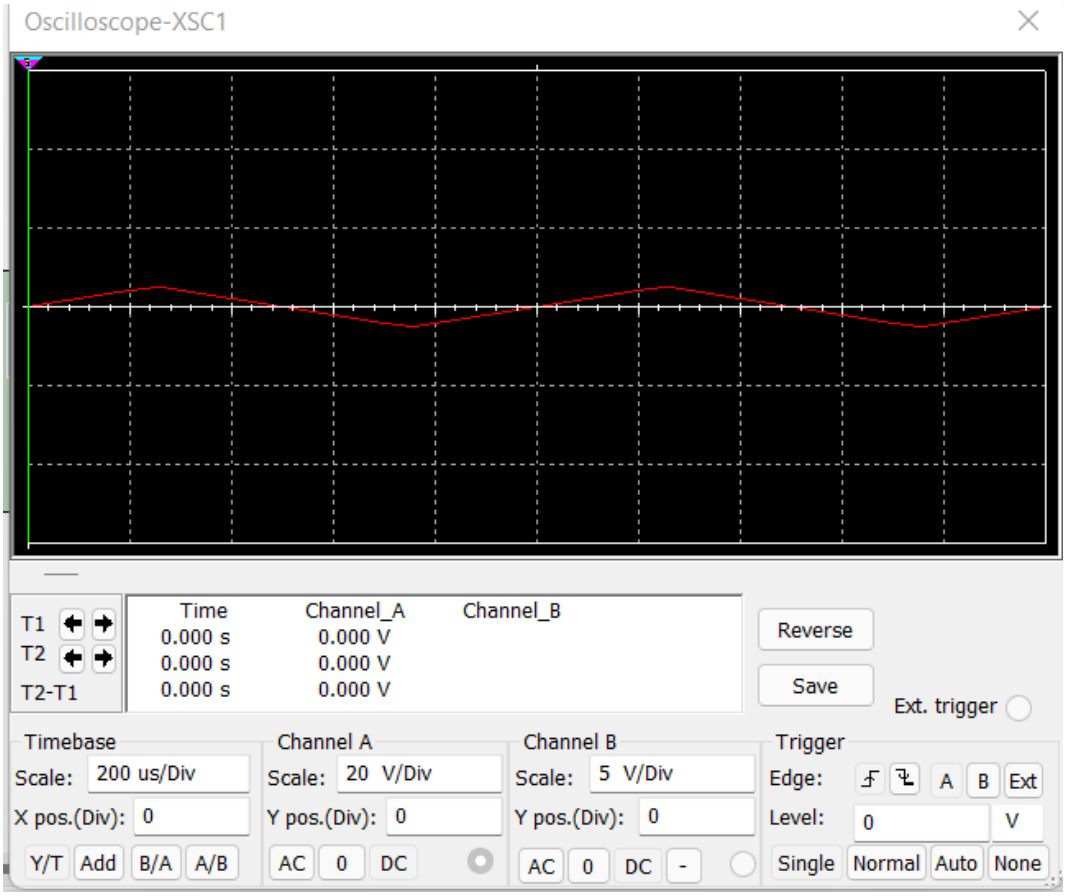
1. From Function Generator:
   Input Voltage: 5 Volts
   Input Frequency: 1000 Hz
2. From CRO:

S No.	Scale on Volts/Div. (V)	Scale on Time/Div. (msec)	No. of division for Peak Voltage (V_p)	No. of division for Time Period (T)	Peak Voltage (V_p)	Rms Voltage $V_{rms}=V_p/\sqrt{3}$ (V)	Time Period (T) (msec)	Measured Frequency (f) (Hz)
1.	5 Volts/Div.	0.5 msec/div.	1 Div.	2 Div.	5 Volts	2.88 Volts	1 msec	1000 Hz
2.	10 Volts/Div.	1 msec/div.	0.5 Div.	1 Div.	5 Volts	2.88 Volts	1 msec	1000 Hz
3.	20 Volts/Div.	0.2 msec/div.	0.25 Div.	5 Div.	5 Volts	2.88 Volts	1 msec	1000 Hz

Graph For Triangular Wave Measurement:



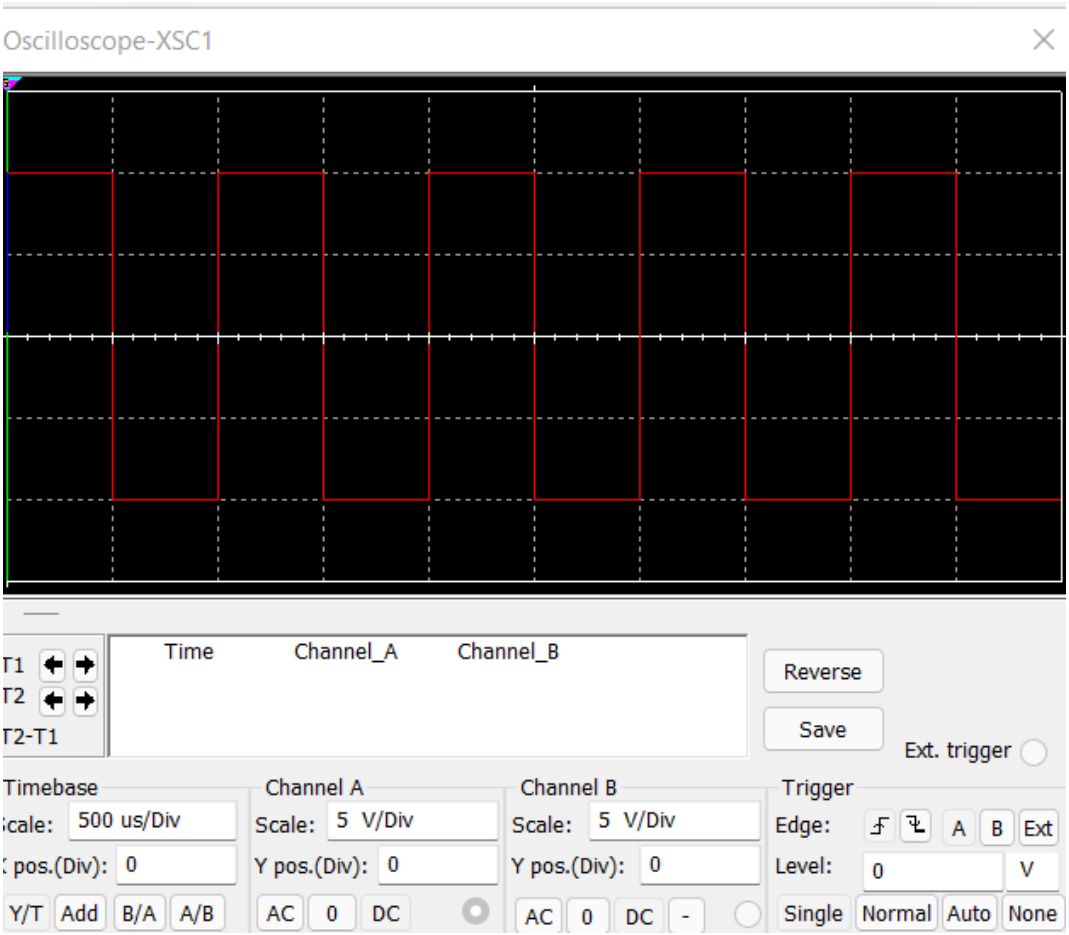


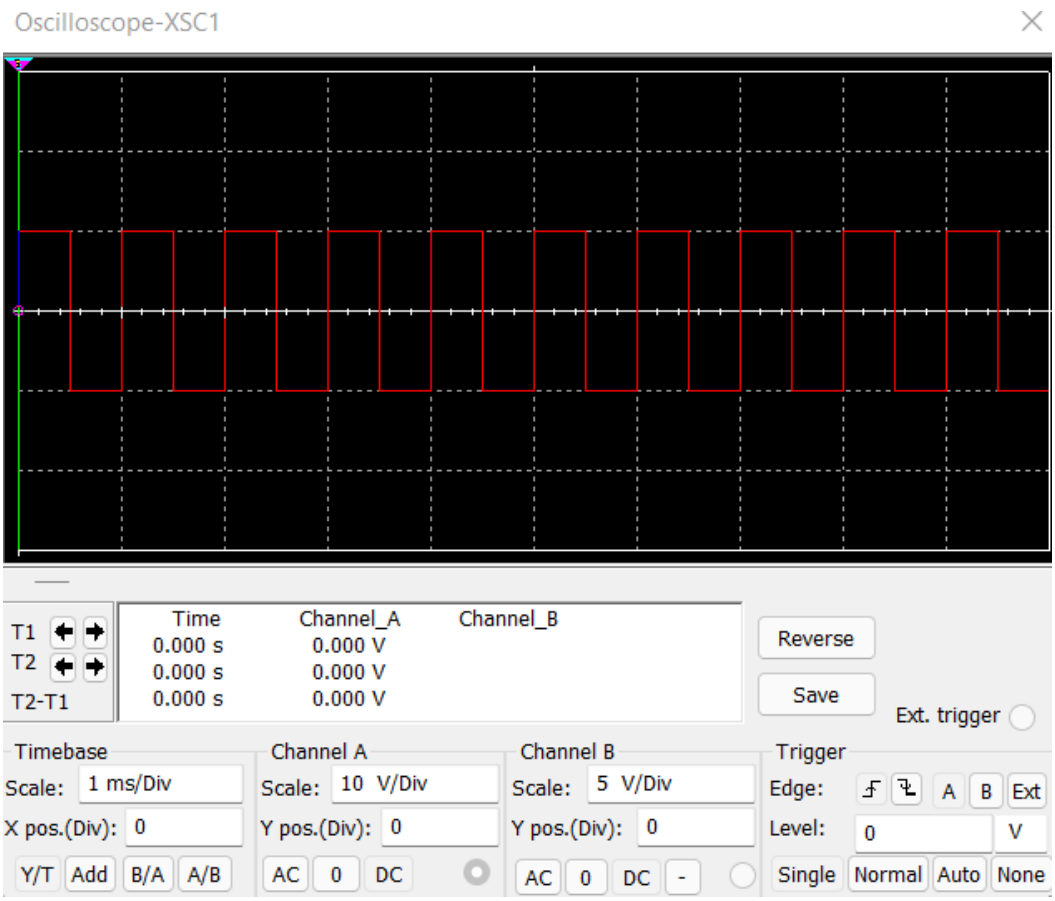


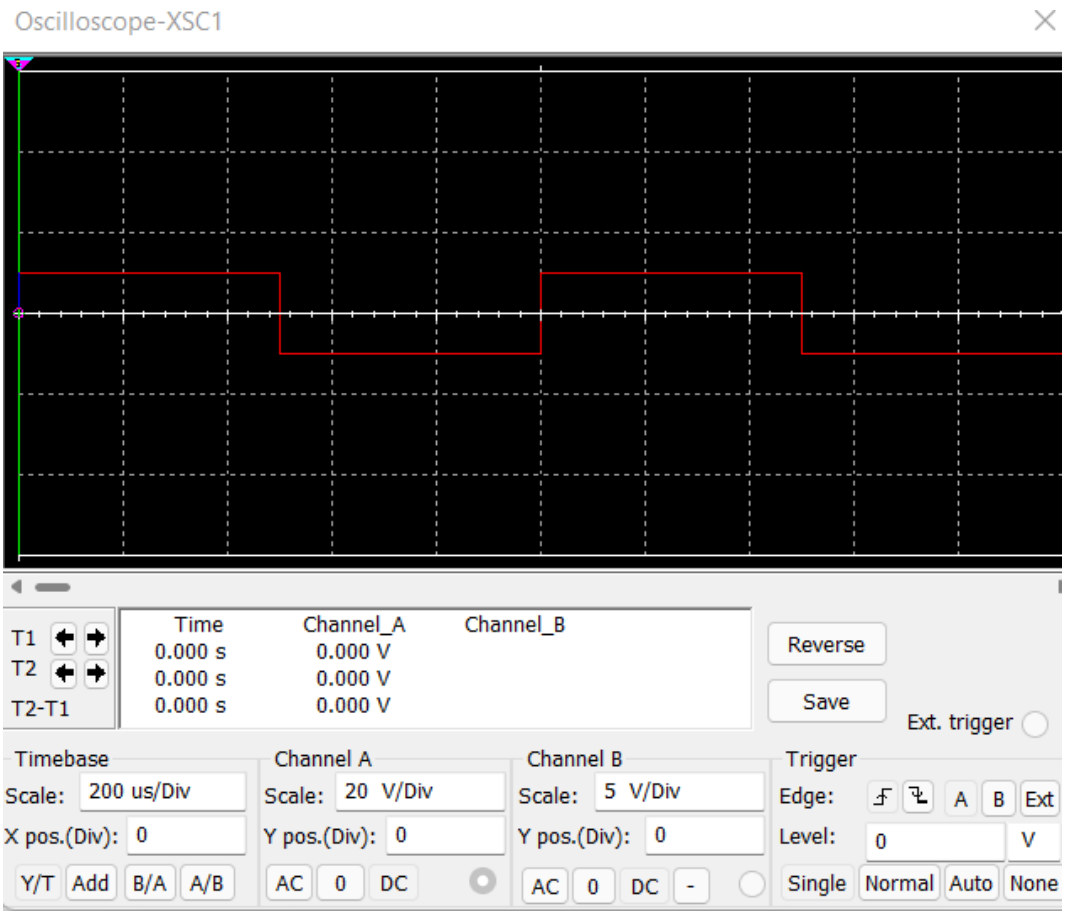
- **For Square Wave Measurement:**
  1. From Function Generator:
     Input Voltage: 10 Volts
     Input Frequency: 1000 Hz
  2. From CRO:

S No.	Scale on Volts/Div. (V)	Scale on Time/Div. (msec)	No. of division for Peak Voltage (V_p)	No. of division for Time Period (T)	Peak Voltage (V_p)	Rms Voltage $V_{rms}=V_p$ (V)	Time Period (T) (msec)	Measured Frequency (f) (Hz)
1.	5 Volts/Div.	0.5 msec/div.	2 Div.	2 Div.	10 Volts	10 Volts	1 msec	1000 Hz
2.	10 Volts/Div.	1 msec/div.	1 Div.	1 Div.	10 Volts	10 Volts	1 msec	1000 Hz
3.	20 Volts/Div.	0.2 msec/div.	0.5 Div.	5 Div.	10 Volts	10 Volts	1 msec	1000 Hz

Graph For Square Wave Measurement:







RESULT :

1. **For Sine Wave:**
    - Peak Voltage: 10 Volts
    - Rms Voltage: 7.07 Volts
    - Time Period: 1 msec
    - Frequency: 1000 Hz
2. **For Triangular Wave:**
    - Peak Voltage: 5 Volts
    - Rms Voltage: 2.88 Volts
    - Time Period: 1 msec
    - Frequency: 1000 Hz
3. **For Square Wave:**
    - Peak Voltage: 10 Volts
    - Rms Voltage: 10 volts
    - Time Period: 1 msec
    - Frequency: 1000 Hz

CONCLUSION:

- The oscilloscope measures the peak voltage as exactly the input voltage provided in the function generator. The frequency of the waveforms produced by the oscilloscope is the same as the input frequency in the function generator.

AIM(B): Measurement of Unknown Frequencies Using Lissajous Pattern

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Power Supply
- CRO
- Function Generator

THEORY:

Two super - position of the two harmonic functions such as sine wave produce a Lissajous Pattern on the CRO screen. Lissajous pattern may be a straight line, an ellipse or a circle depending on the frequency, phase and amplitude of the two signals.

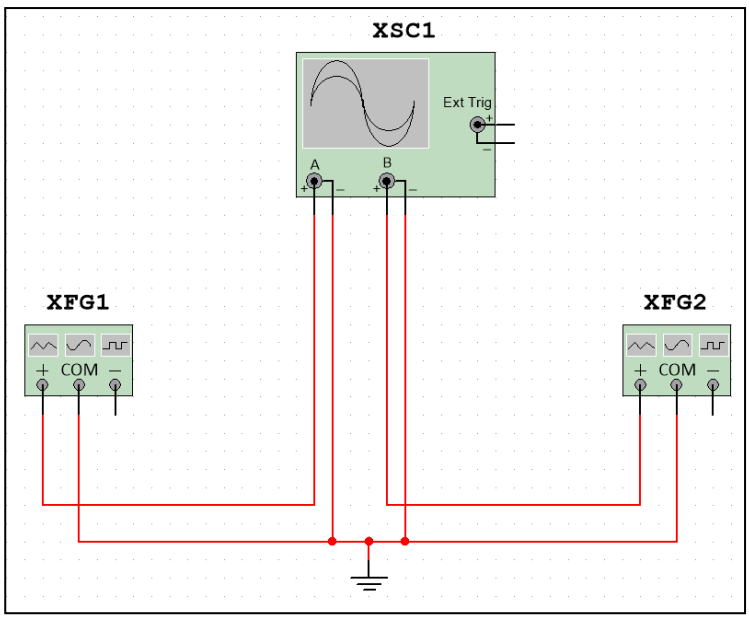
A straight-line result when the two waves are in phase or exactly 180° out of phase with each other. A circle is displayed when the phase difference is 90° and the signals are equal in amplitude. If f_y corresponds to the frequency of vertical deflection voltage and f_x corresponds to the horizontal deflection voltage then,

f_y / f_x = No. of horizontal tangencies (HT) / No. of vertical tangencies (VT)

Where, Horizontal Tangency (HT): It is the no of times, a factitious straight line taken at any one Horizontal side of the Lissajous pattern (Up/Down) serves as a tangent to the Lissajous pattern.

Vertical Tangency (VT) is the no of times, a factitious straight line taken at any one Vertical side of the Lissajous pattern (Up/Down) serves as a tangent to the Lissajous pattern. Hence f_y can be found if f_x is known.

EXPERIMENTAL SETUP:

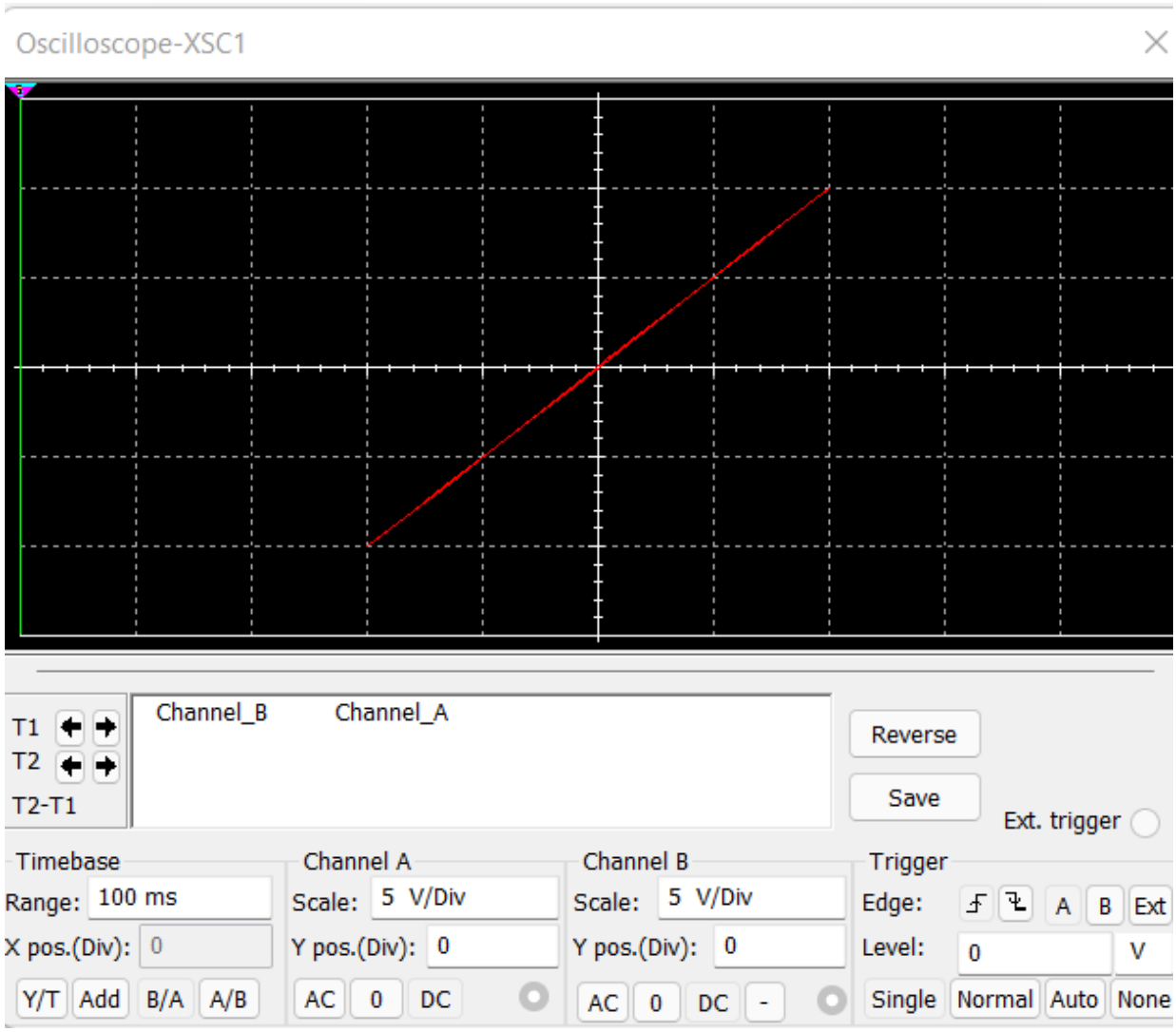


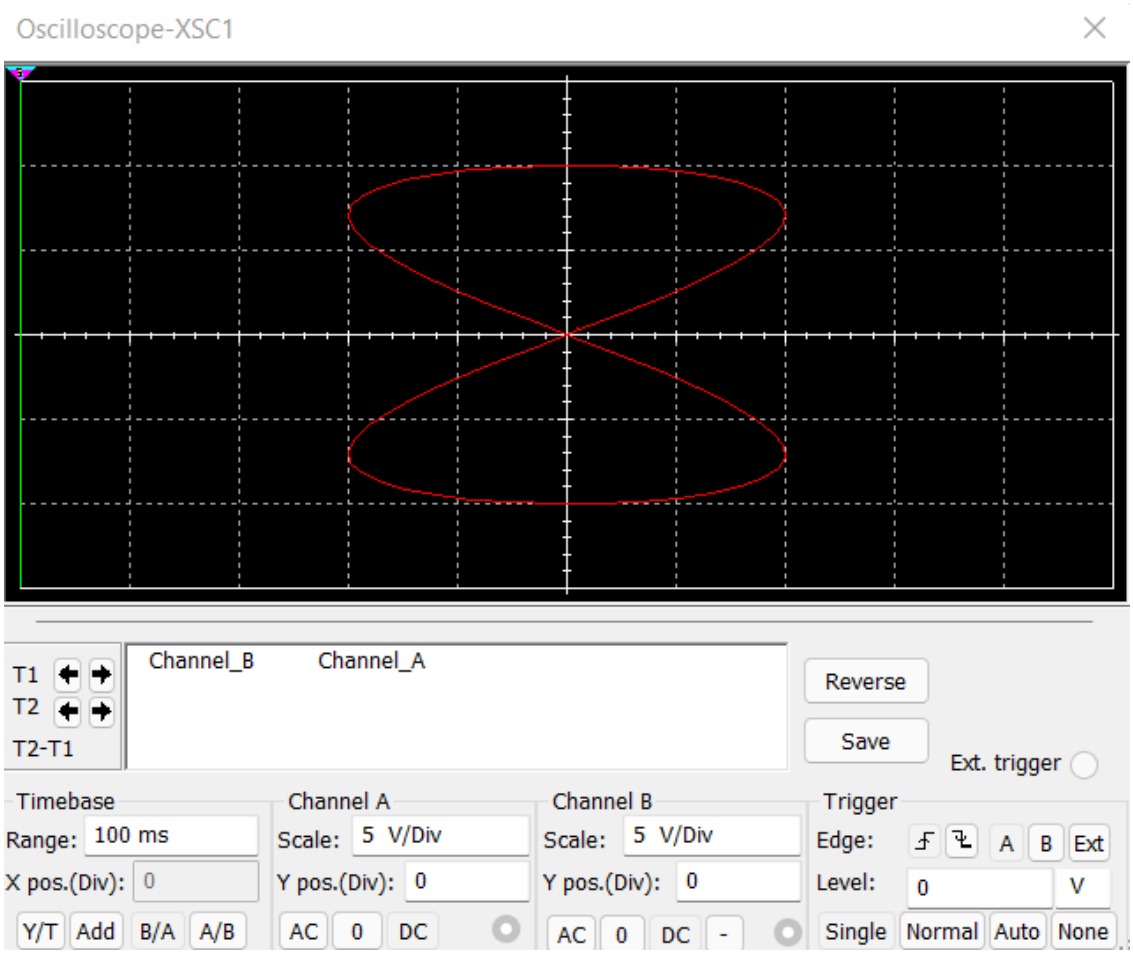
(Circuit diagram for the measurement of unknown Frequency using Lissajous Pattern)

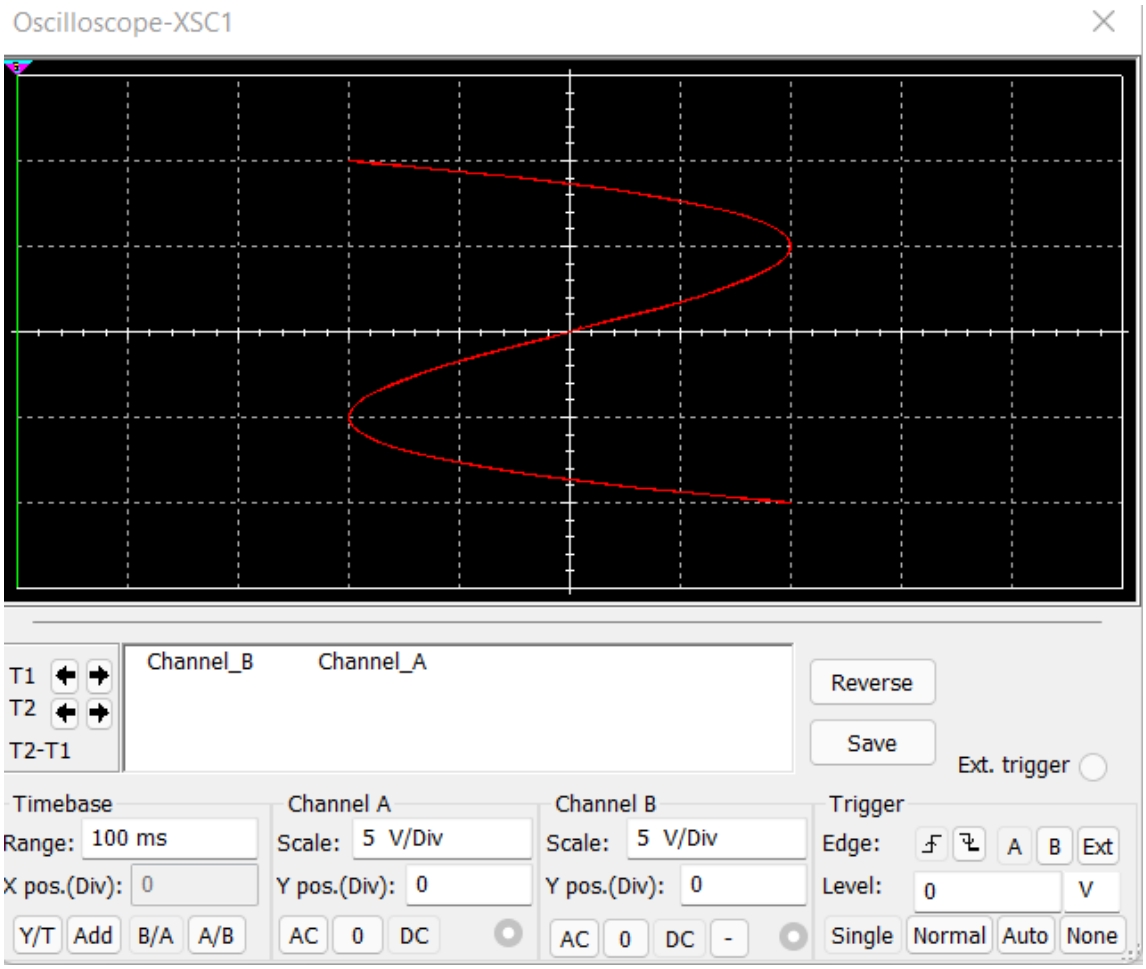
OBSERVATION:

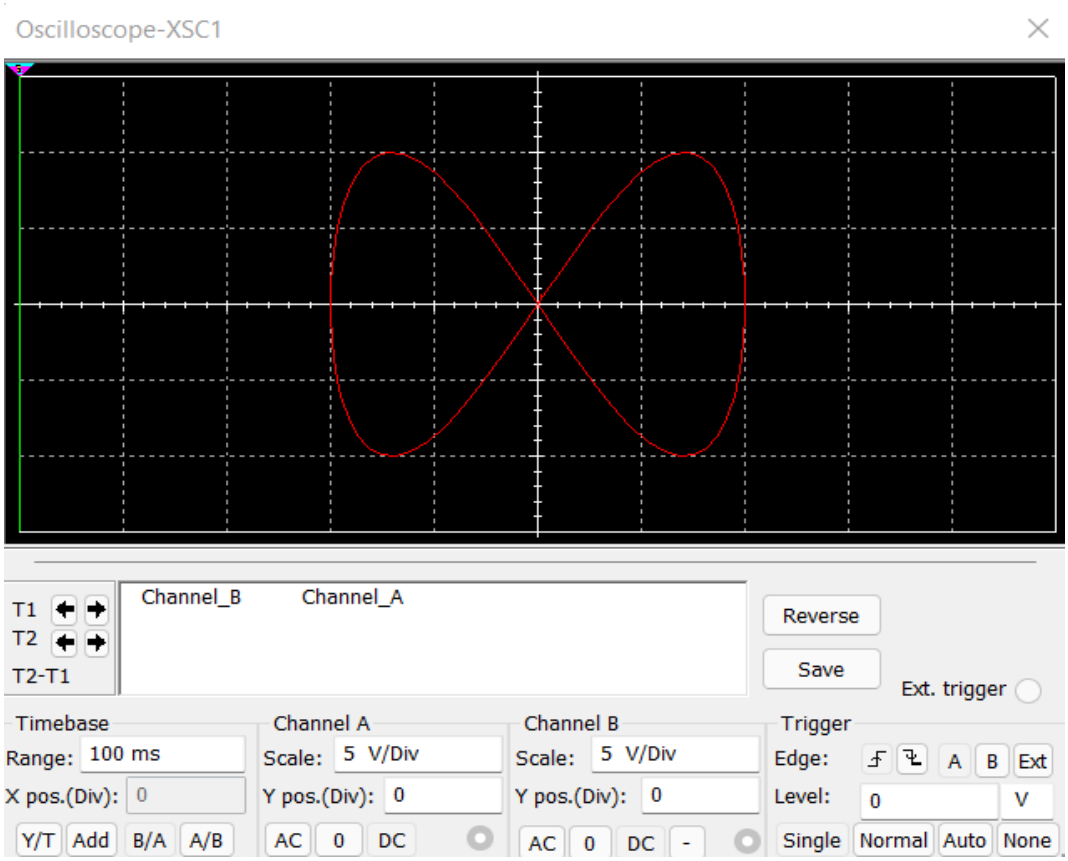
S No.	f_x (Hz)	Horizontal Tangency (HT)	Vertical Tangency (VT)	$f_y = (HT/VT) * f_x$ (Hz)
1.	100 Hz	1	1	100 Hz
2.	200 Hz	2	4	100 Hz
3.	300 Hz	1	3	100 Hz
4.	400 Hz	4	2	800 Hz
5.	600 Hz	4	6	400 Hz

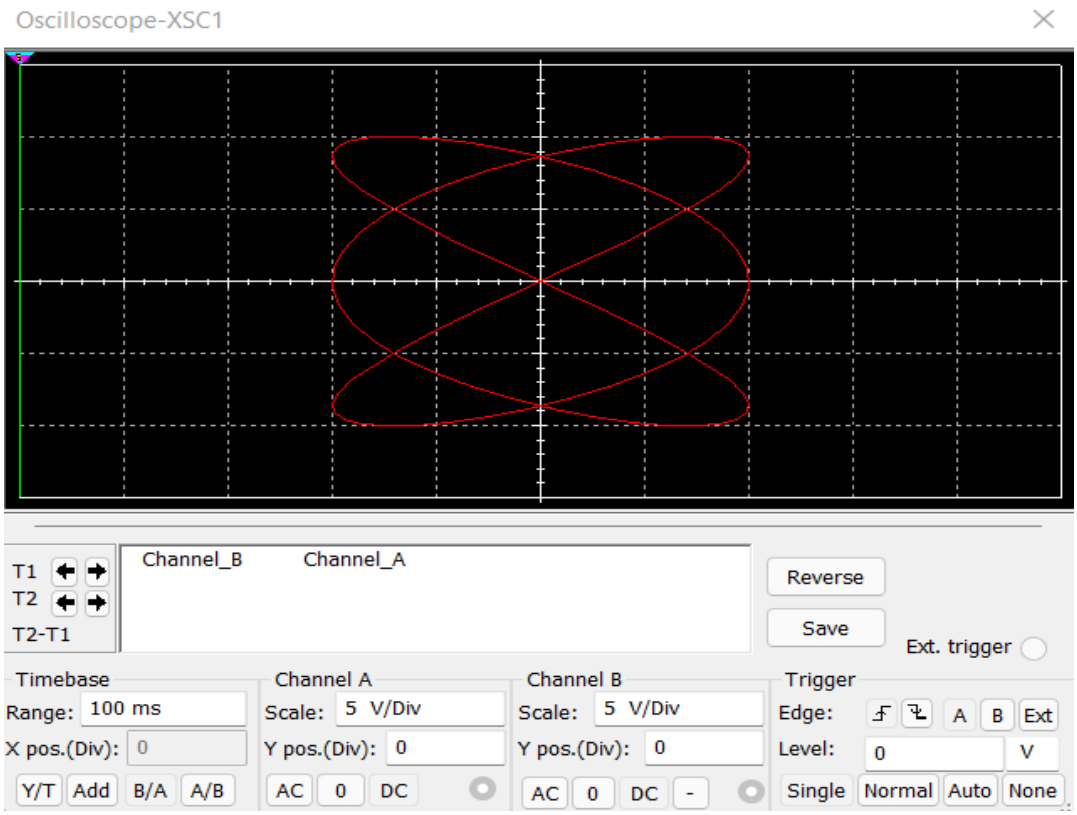
GRAPH OF LISSAJOUS PATTERN:




Oscilloscope-XSC1
T1
T2
T2-T1
Channel_B
Channel_A
Reverse
Save
Ext. trigger
Timebase
Range: 100 ms
X pos.(Div): 0
Y/T
Add
B/A
A/B
Channel A
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
-
Trigger
Edge:
A
B
Ext
Level: 0 V
Single
Normal
Auto
None


Oscilloscope-XSC1
T1
T2
T2-T1
Channel_B
Channel_A
Reverse
Save
Ext. trigger
Timebase
Range: 100 ms
X pos.(Div): 0
Y/T
Add
B/A
A/B
Channel A
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
-
Trigger
Edge:
A
B
Ext
Level: 0 V
Single
Normal
Auto
None





RESULT:

f_y / f_x = No. of Horizontal Tangencies (HT) / No. of Vertical Tangencies (VT)

CONCLUSION:

- The unknown frequency is very accurately calculated by the observing the Lissajous Patter on the CRO screen and knowing the horizontal and the vertical tangencies of the patterns.

AIM(C): Measurement of the Phase Angle Between Two Signals of the same Frequency using CRO

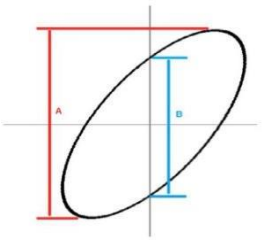
SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Power Supply
- CRO
- Function Generator

THEORY:

When two Sinusoidal signals of different amplitudes and equal frequencies are applied to Y-input and X-input of the CRO an ellipse is obtained.



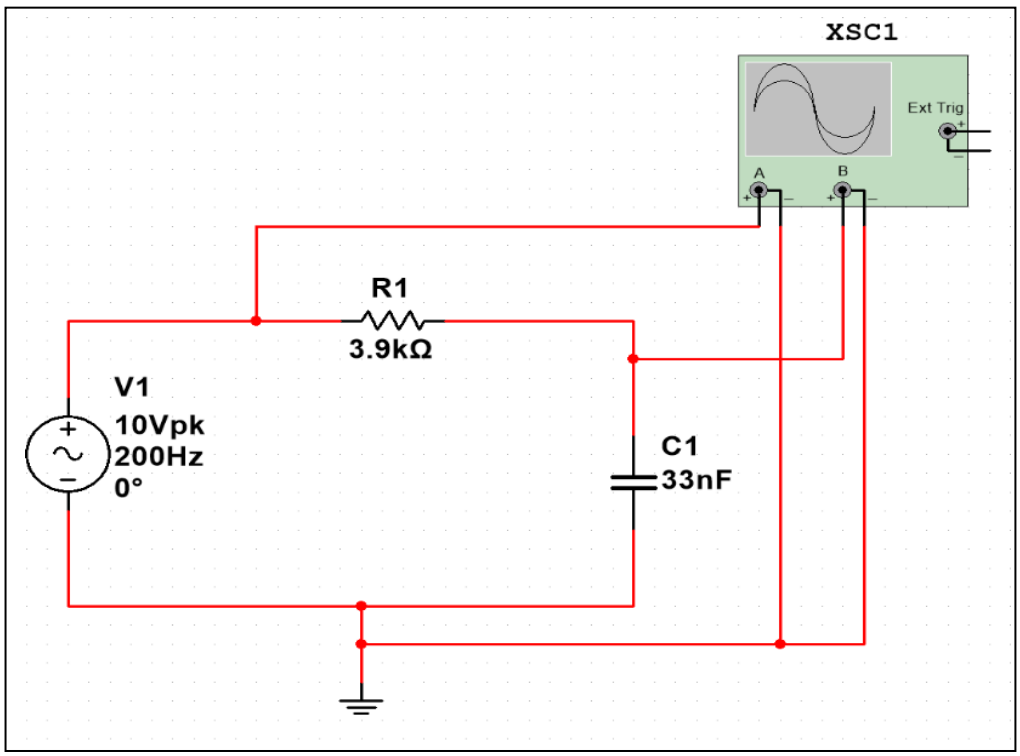
$$\sin \Phi = \frac{B}{A}$$

$$\Phi = \text{Phase A}$$

Theoretical $\phi = \tan^{-1}(\omega RC)$

Experimental $\phi = \sin^{-1}[\text{Y-intercept (B)} / \text{Y-peak (A)}]$

EXPERIMENTAL SETUP:



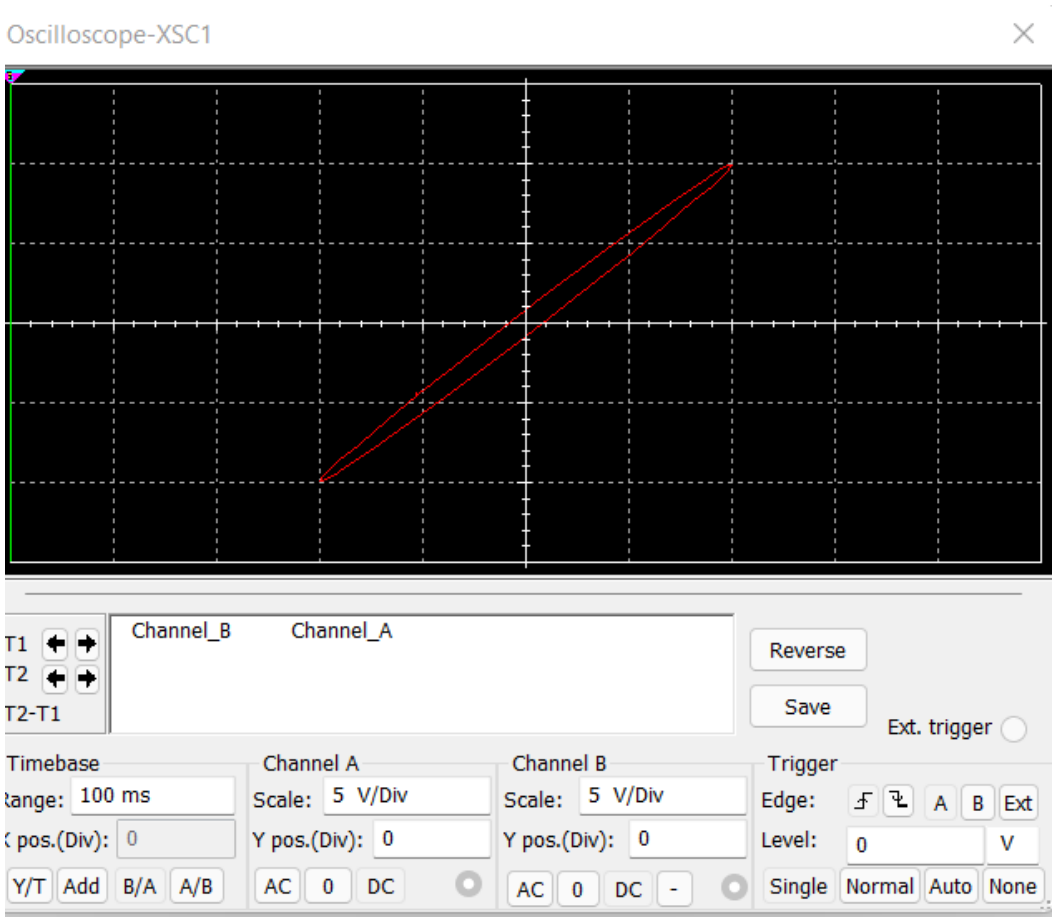
(Circuit diagram for the measurement of Phase Angle)

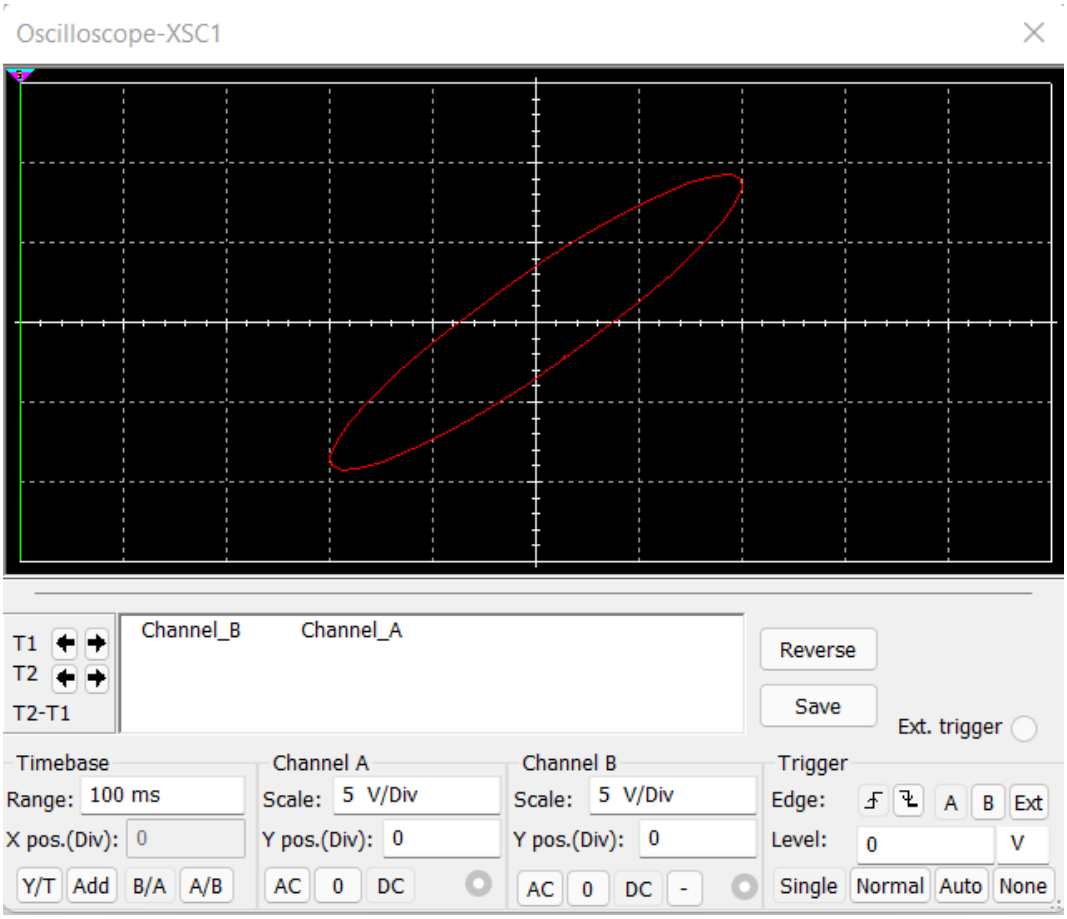
OBSERVATION:

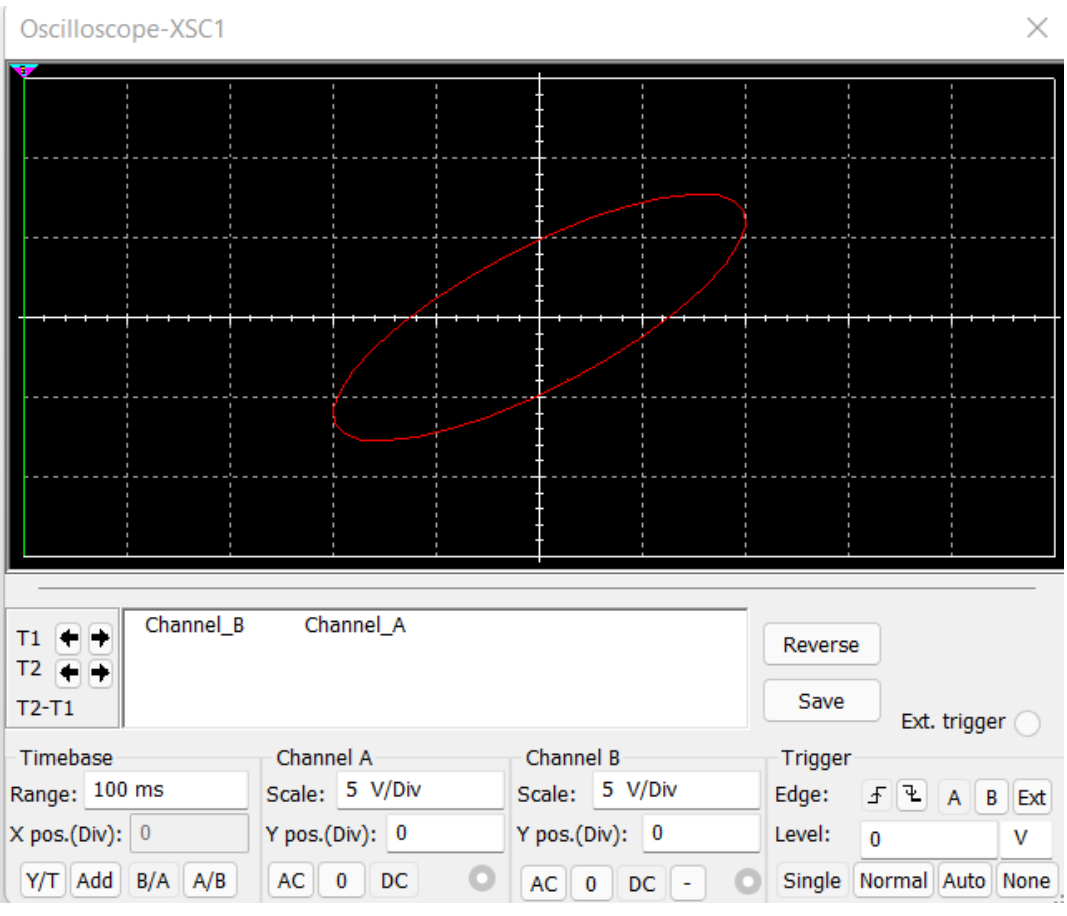
R = 3.9kΩ, C = 33nF

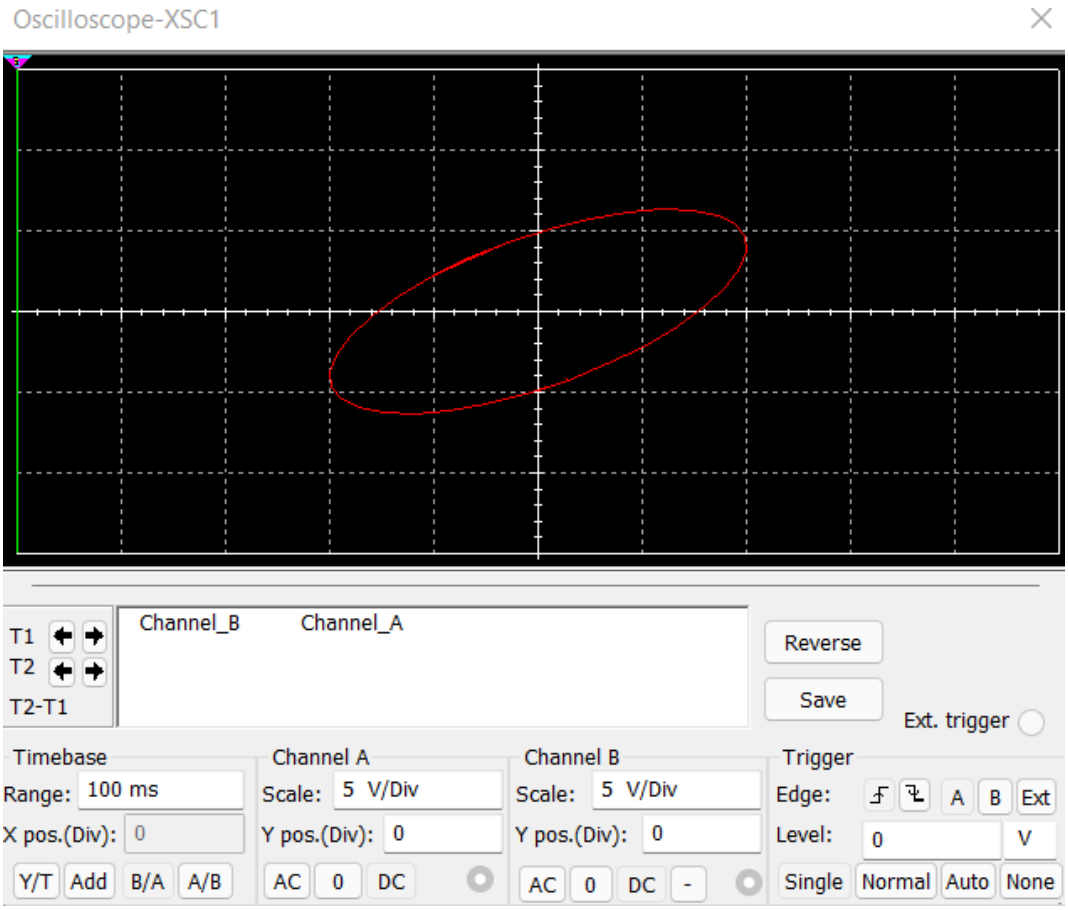
Frequency of applied signal (Hz)	(θ_1) $\phi = \tan^{-1}(\omega RC)$	(B) Y - Intercept	(A) Y - Peak	(θ_2) $\sin^{-1}(B/A)$	Error ($\theta_1 - \theta_2$)
100 Hz	4.57°	2	20	5.73°	-1.16
500 Hz	21.80°	7	18	22.83°	-1.03
1000 Hz	38.65°	10	16	38.68°	-0.03
1500 Hz	50.47°	10	13	50.26°	0.21
2000 Hz	58.25°	9	10.5	58.21°	0.04

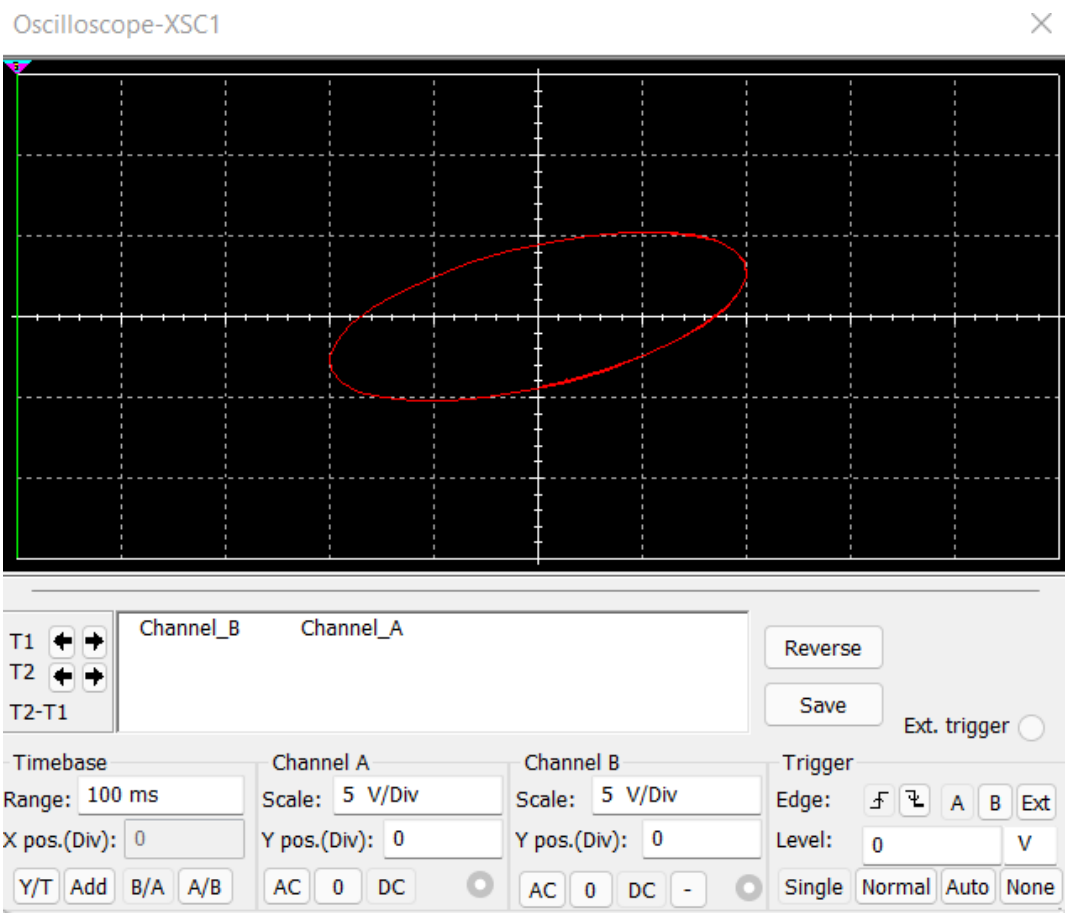
GRAPH:




Oscilloscope-XSC1
T1
T2
T2-T1
Channel_B
Channel_A
Reverse
Save
Ext. trigger
Timebase
Range: 100 ms
X pos.(Div): 0
Y/T
Add
B/A
A/B
Channel A
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
-
Trigger
Edge:
A
B
Ext
Level: 0
V
Single
Normal
Auto
None


Oscilloscope-XSC1
T1
T2
T2-T1
Channel_B
Channel_A
Reverse
Save
Ext. trigger
Timebase
Range: 100 ms
X pos.(Div): 0
Y/T
Add
B/A
A/B
Channel A
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
Channel B
Scale: 5 V/Div
Y pos.(Div): 0
AC
0
DC
-
Trigger
Edge:
A
B
Ext
Level: 0
V
Single
Normal
Auto
None





CONCLUSION:

- A negative error in the observed phase angle and the theoretically calculated phase angle is observed for ome of the applied signal of the different frequency.

Reference Links: https://youtu.be/kh-oIlf4e3Y

EXPERIMENT – 2

AIM(A): To determine the Forward and Reverse Bias Characteristics of PN Junction Diode

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Power Supply
- Millimetre
- Micro Ammeter
- Voltmeter

CIRCUIT COMPONENTS:

- Diode (1N4001)
- Resistance (100Ω)

THEORY:

In a piece of semiconductor material, if one half is doped by P-type impurity and the other half is doped by N-type impurity, a PN junction is formed. The plane dividing the two halves or zones is called PN junction. The N-type material has high concentration of free electrons, while P-type material has high concentration of holes. Therefore, at the junction there is a tendency for the free electrons to diffuse over the P-side and holes the N-side. This process is called diffusion. As the free electron moves across the junction from N-type to P-type, the donor irons become positively charged. Hence a positive charge is built on the N-side of the junction. The free electrons that cross the junction uncover the negative acceptor ions by filling in the holes. Therefore, a net negative charge is established on the P-side of the junction. This net negative charge on the P-side prevents further diffusion of electron in to the P-side. Similarly, the net positive charge on the N-side repels the holes crossing from P-side to N-side. Thus, a barrier is set-up near the junction which prevents further movement of charge carriers. As the consequence of the induced electric field across the depletion layer, an electrostatic potential difference is established between P and N region, which is called the potential barrier, junction barrier, diffusion potential, or contact potential, VO. The magnitude of the contact potential Ovaries with doping levels and temperature. V_0 is 0.3 V for germanium and 0.72 V for silicon.

FORWARD BIAS:

When positive terminal of the battery is connected to the P-type and negative terminal to the N-type of the PN diode, the bias is known as forward bias. Under the forward bias condition, the applied positive potential repels the holes in P-type region so that the holes move towards the junction and the applied negative potential repels the electron in the N-type region and the electron move towards the junction. Eventually, when the applied potential is more than the internal barrier potential the depletion region and internal potential barrier disappear. A feature worth to be noted in the forward characteristics is the cut in or threshold voltage V_γ below which the current is very small. It is 0.3 V for GE and 0.7 V for Si respectively. At the cut in voltage, the potential is overcome and the current through the junction starts to increase rapidly.

REVERSE BIAS:

When the negative terminal of the battery is connected to the P-type and positive terminal of the battery is connected to the N-type of the PN junction, the bias applied is known as reverse bias. Under applied reverse bias, holes which form the majority carriers or the P-side moves towards the negative terminal of the battery and electron which form the majority carrier of the N-side are attracted towards the positive terminal of the battery. Hence, the width of the depletion region which is depleted of the mobile charge carriers increases. Thus, the electric field produced by applied reverse bias, is in the same direction as the electric field of the potential barrier. Hence, the resultant potential barrier is increased which prevents the flow of majority carriers in both the directions. Therefore, theoretically no current should flow in the external circuit. But in practice, a very small current of the order of a few microamperes flows

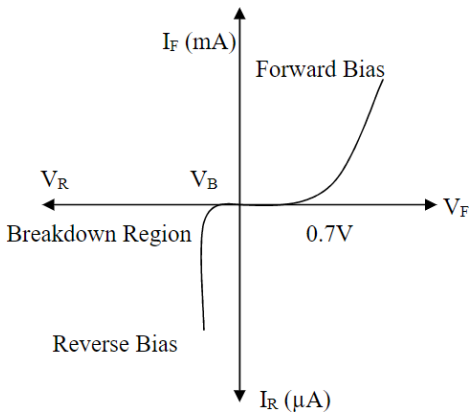
under reverse bias. Electron forming covalent bonds of the semiconductor atoms in the P and N-type regions may absorb sufficient energy from heat and light to cause breaking of some covalent bonds. Hence electron-hole pairs are continually produced in both the regions. Under the reverse bias condition, the thermally generated holes in the P-region are attracted towards the negative terminal of the battery and the electrons in the N-region are attracted towards the positive terminal of the battery. Consequently, the minority carriers, electron on the P-region and holes in the N-region, wander over to the junction and flow towards their majority carrier side giving rise to a small reverse current. This current is known as reverse saturation current, IO. The magnitude of reverse current depends upon the junction temperature because the major source of minority carriers is thermally broken covalent bonds. For large applied reverse bias, the free electrons from the N-type moving towards the positive terminal of the battery acquire sufficient energy to move with high velocity to dislodge valence electron from semiconductor atoms in the crystal. These newly liberated electrons, in turn, acquire sufficient energy to dislodge other parent electrons. Thus, a large number of free electrons are formed which is commonly called as an avalanche of free electrons. This leads to the breakdown of the junction leading to very large reverse current. The reverse voltage at which the junction breakdown occurs is known as breakdown voltage, VBD. PN diode applications

An ideal PN diode is a two terminal polarity sensitive device that has zero resistance when it is forward biased and infinite resistance when it is reverse biased. Due to this characteristic the diode finds number of applications as given below:

1. Rectifier
2. Switch
3. Clamper
4. Clipper
5. Demodulation detector circuits

The graph of voltage applied across the diode (V) versus the current (I) flowing thru it is called its V-I characteristic. A typical V-I characteristic of a p-n junction diode is as shown.

- Static Forward Resistance (R_{DC}) = $(V_F/I_F)\ \Omega$
- Dynamic Forward Resistance (R_{AC}) = $(\Delta V_F/\Delta I_F)\ \Omega$



EXPERIMENTAL SETUP:

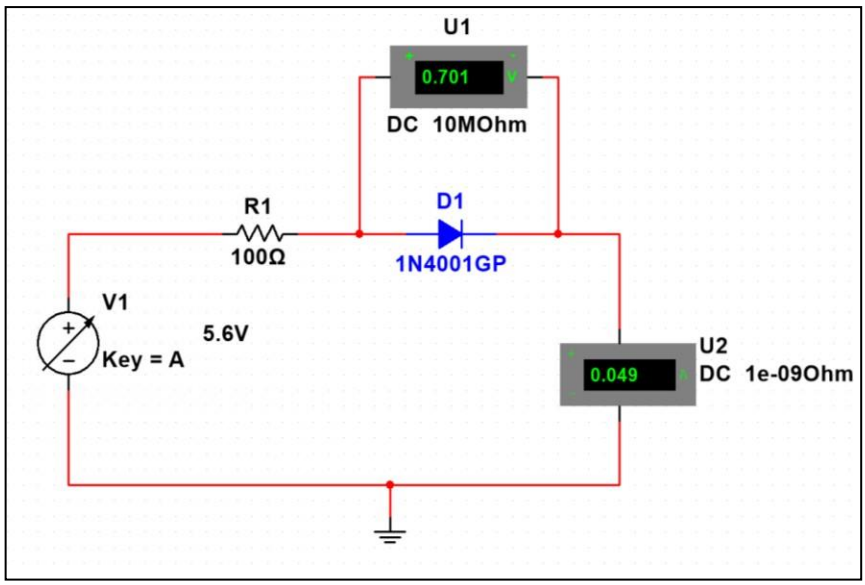


Fig.–1 (Circuit diagram for Forward Bias PN Diode)

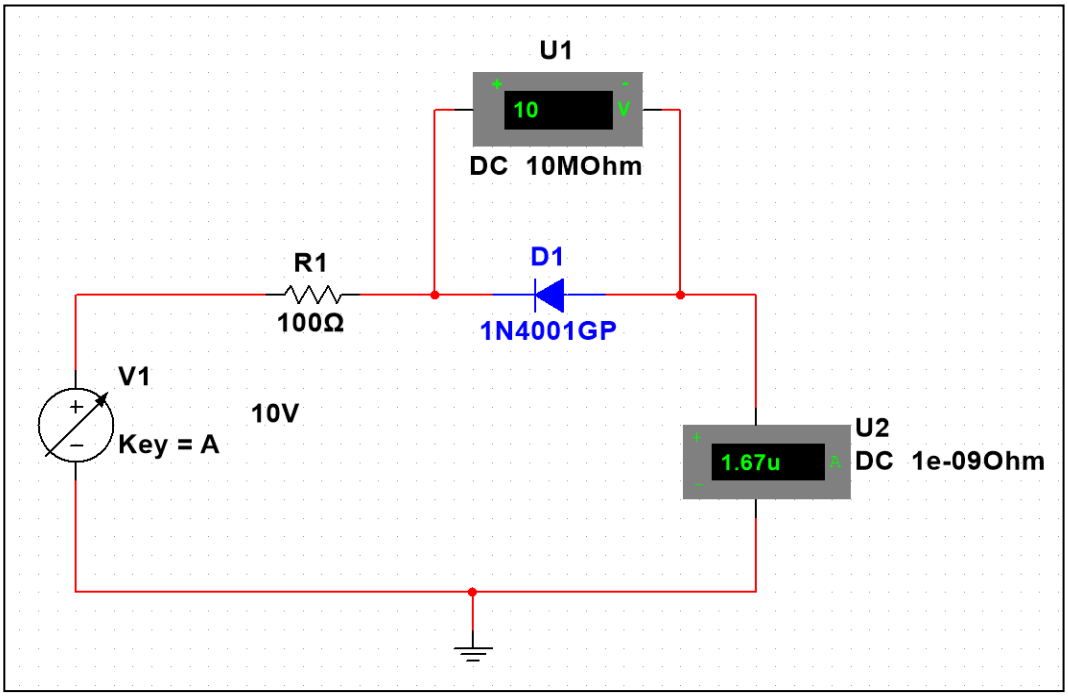


Fig.-2 (Circuit diagram for Reverse Bias PN Diode)

OBSERVATION:

Table-1: Reading for the Forward Bias Diode

S No.	V_{in} (Volts)	V_f (Volts)	I_f (mA)
1.	0.1 Volts	0.1 Volts	0.002653 mA
2.	0.2 Volts	0.198 Volts	0.015 mA
3.	0.3 Volts	0.293 Volts	0.072 mA
4.	0.4 Volts	0.373 Volts	0.266 mA
5.	0.5 Volts	0.432 Volts	0.68 mA
6.	0.6 Volts	0.472 Volts	1.284 mA
7.	0.7 Volts	0.499 Volts	2.005 mA
8.	0.8 Volts	0.52 Volts	2.798 mA
9.	0.9 Volts	0.537 Volts	3.634 mA
10.	1.0 Volts	0.55 Volts	4.5 mA
11.	1.5 Volts	0.594 Volts	9.062 mA
12.	2.0 Volts	0.620 Volts	14 mA
13.	2.5 Volts	0.639 Volts	19 mA

14.	3.0 Volts	0.654 Volts	23 mA
15.	3.5 Volts	0.666 Volts	28 mA
16.	4.0 Volts	0.676 Volts	33 mA
17.	4.5 Volts	0.685 Volts	38 mA
18.	5.0 Volts	0.693 Volts	43 mA
19.	5.5 Volts	0.699 Volts	48 mA
20.	6.0 Volts	0.706 Volts	53 mA
21.	6.5 Volts	0.712 Volts	58 mA
22.	7.0 Volts	0.717 Volts	63 mA
23.	7.5 Volts	0.722 Volts	68 mA
24.	8.0 Volts	0.726 Volts	73 mA
25.	8.5 Volts	0.731 Volts	78 mA
26.	9.0 Volts	0.735 Volts	83 mA
27.	9.5 Volts	0.739 Volts	88 mA
28.	10 Volts	0.742 Volts	93 mA
29.	12 Volts	0.755 Volts	112 mA
30.	14 Volts	0.766 Volts	132 mA
31.	16 Volts	0.776 Volts	152 mA
32.	18 Volts	0.784 Volts	172 mA
33.	20 Volts	0.792 Volts	192 mA
34.	22 Volts	0.799 Volts	212 mA
35.	24 Volts	0.806 Volts	232 mA
36.	26 Volts	0.812 Volts	252 mA
37.	28 Volts	0.817 Volts	272 mA
38.	30 Volts	0.822 Volts	292 mA
39.	35 Volts	0.834 Volts	342 mA
40.	40 Volts	0.845 Volts	392 mA
41.	45 Volts	0.855 Volts	441 mA
42.	50 Volts	0.863 Volts	491 mA
43.	55 Volts	0.872 Volts	541 mA
44.	60 Volts	0.879 Volts	591 mA
45.	65 Volts	0.886 Volts	641 mA
46.	70 Volts	0.893 Volts	691 mA
47.	75 Volts	0.900 Volts	741 mA
48.	80 Volts	0.906 Volts	791 mA
49.	85 Volts	0.912 Volts	841 mA
50.	90 Volts	0.918 Volts	891 mA

Graph-1: For Forward Bias Diode

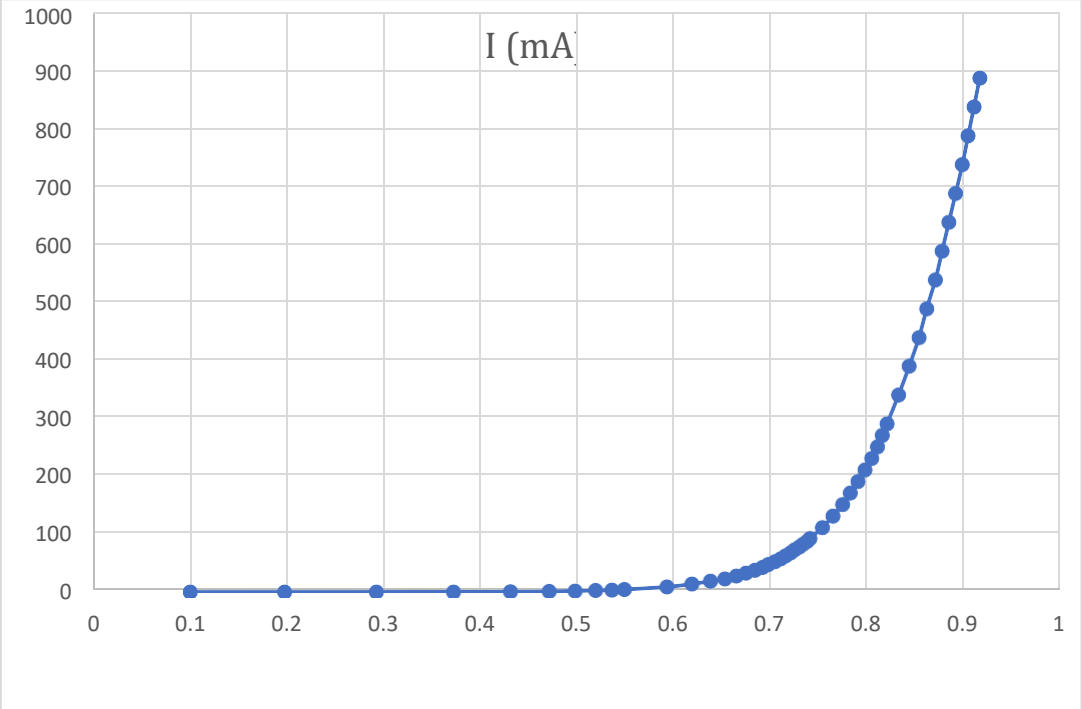
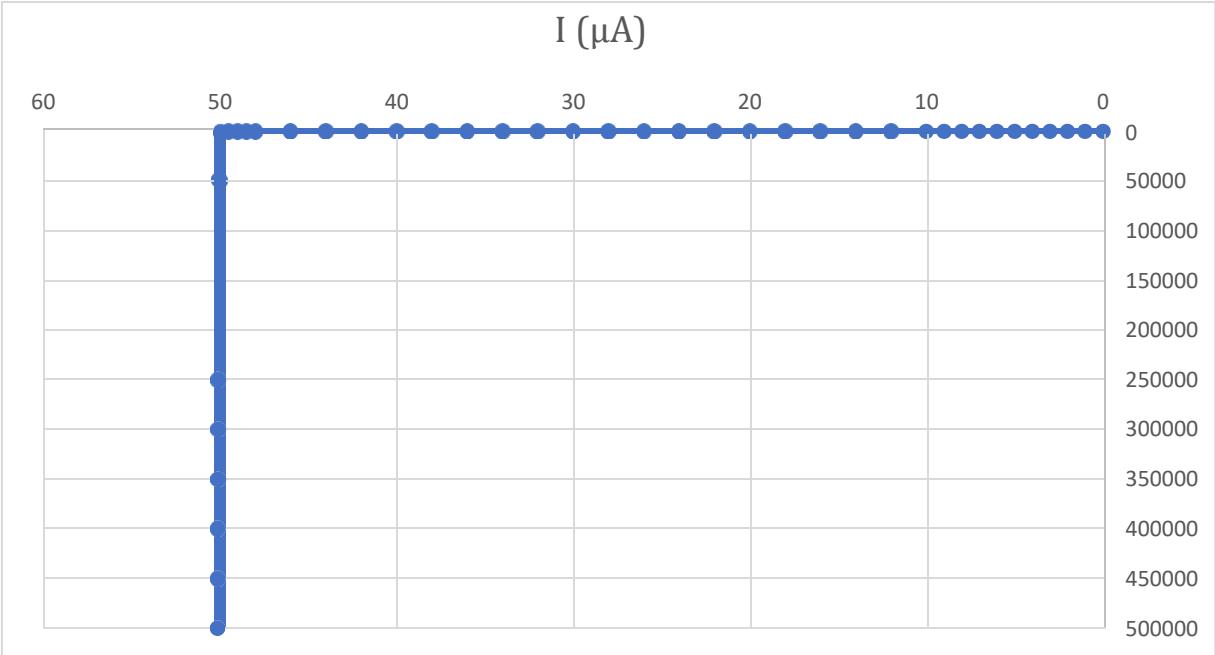


Table-2: Reading for the Reverse Bias Diode

S No.	V_{in} (Volts)	V_r (Volts)	I_r (µA)
1.	0 Volts	0 Volts	0 µA
2.	1 Volts	1 Volts	0.77 µA
3.	2 Volts	2 Volts	0.87 µA
4.	3 Volts	3 Volts	0.97 µA
5.	4 Volts	4 Volts	1.07 µA
6.	5 Volts	5 Volts	1.17 µA
7.	6 Volts	6 Volts	1.27 µA
8.	7 Volts	7 Volts	1.37 µA
9.	8 Volts	8 Volts	1.47 µA
10.	9 Volts	9 Volts	1.57 µA
11.	10 Volts	10 Volts	1.67 µA
12.	12 Volts	12 Volts	1.87 µA
13.	14 Volts	14 Volts	2.07 µA
14.	16 Volts	16 Volts	2.27 µA
15.	18 Volts	18 Volts	2.47 µA
16.	20 Volts	20 Volts	2.67 µA
17.	22 Volts	22 Volts	2.87 µA
18.	24 Volts	24 Volts	3.07 µA
19.	26 Volts	26 Volts	3.27 µA
20.	28 Volts	28 Volts	3.47 µA
21.	30 Volts	30 Volts	3.67 µA

22.	32 Volts	32 Volts	3.87 µA
23.	34 Volts	34 Volts	4.07 µA
24.	36 Volts	36 Volts	4.27 µA
25.	38 Volts	38 Volts	4.47 µA
26.	40 Volts	40 Volts	4.67 µA
27.	42 Volts	42 Volts	4.87 µA
28.	44 Volts	43.999 Volts	5.07 µA
29.	46 Volts	45.999 Volts	5.27 µA
30.	48 Volts	47.999 Volts	5.47 µA
31.	48.5 Volts	48.499 Volts	5.52 µA
32.	49 Volts	48.999 Volts	5.57 µA
33.	49.5 Volts	49.499 Volts	5.62 µA
34.	50 Volts	49.943 Volts	572 µA
35.	50.5 Volts	49.999 Volts	50007 µA
36.	55 Volts	50.06 Volts	49000 µA
37.	60 Volts	50.081 Volts	99000 µA
38.	65 Volts	50.093 Volts	149000 µA
39.	70 Volts	50.103 Volts	199000 µA
40.	75 Volts	50.111 Volts	249000 µA
41.	80 Volts	50.118 Volts	299000 µA
42.	85 Volts	50.124 Volts	349000 µA
43.	90 Volts	50.129 Volts	399000 µA
44.	95 Volts	50.134 Volts	449000 µA
45.	100 Volts	50.139 Volts	499000 µA

Graph-2: For Reverse Bias Diode



RESULT:

- While operating the PN Junction Diode in forward biased the current was of the order of milliampere while operating same diode in reverse biased the current was found to be in the order of microampere and almost saturated.
- In forward biased after a particular voltage [cut-in voltage] there is significant increase in the current for the small change in the diode voltage. In reverse biased too after crossing a particular voltage, the diode current increased significantly and we say that the diode is in breakdown.
- The graph obtained by the experimental observation was found to be consistent with the actual PN Junction characteristic curve of the diode.

CONCLUSION:

- When the forward bias is applied in the diode the current is observed in the order of the milliamperes. After a particular value of the voltage (cut- in voltage), a significant increase in the current is observed for a small change in the diode voltage.
- When the reverse bias is applied in the diode, the current is observed in the order of the micro amperes. However, after a particular value of the voltage (breakdown voltage), the reverse current increase significantly for a very small change in diode voltage. Thus, the graph obtained by the experimental observation was found to be consistent with the I-V characteristic of the PN Junction Diode.

Reference Links: **https://youtu.be/Gp4dnjN8kGw**

EXPERIMENT – 3

AIM: To determine the Reverse Bias Characteristics of the Zener Diode and its application as Voltage Regulator

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Power Supply
- DC Ammeter
- DC Voltmeter

CIRCUIT COMPONENTS:

- Resistors- 470Ω, 1.5kΩ, 2.2kΩ, 3.3kΩ, 5.6kΩ, 12kΩ
- Zener- 1Z12

THEORY:

Zener Diode: A Zener Diode is a silicon PN Junction device that is designed for operation in the reverse-breakdown region. The breakdown voltage of a Zener Diode is set by carefully controlling the doping level during manufacture. When a diode reaches reverse breakdown, its voltage remains almost constant even though the current changes drastically, and this is the key to Zener Diode operation. This volt-ampere characteristic is shown again in Figure-1with the normal operating region for Zener Diodes shown as a shaded area.

Zener Breakdown: Zener Diodes are designed to operate in reverse breakdown. Two types of reverse breakdown in a Zener Diode are avalanche and Zener. The avalanche effect, occurs in both rectifier and Zener Diodes at a sufficiently high reverse voltage. Zener breakdown occurs in a Zener Diode at low reverse voltages. A Zener Diode is heavily doped to reduce the breakdown voltage. This causes a very thin depletion region. As a result, an intense electric field exists within the depletion region. Near the Zener breakdown voltage (VZ), the field is intense enough to pull electrons from their valence bands and create current. Zener diodes with breakdown voltages of less than approximately 5 V operate predominately in Zener breakdown. Those with breakdown voltages greater than approximately 5 V operate predominately in avalanche breakdown. Both types, however, are called Zener Diodes. Zener's are commercially available with breakdown voltages from less than 1 V to more than 250 V with specified tolerances from 1% to 20%.

Zener Regulation: Figure-2 shows the reverse portion of a Zener Diode's characteristic curve. Notice that as the reverse voltage (VR) is increased, the reverse current (IR) remains extremely small up to the "knee" of the curve. The reverse current is also called the Zener current, IZ. At this point, the breakdown effect begins; the internal Zener resistance, also called Zener impedance (ZZ), begins to decrease as the reverse current increases rapidly. From the bottom of the knee, the Zener breakdown voltage (VZ) remains essentially constant although it increases slightly as the Zener current, IZ, increases. Zener Regulation is the ability to keep the reverse voltage across its terminals essentially constant is the key feature of the Zener Diode. A Zener Diode operating in breakdown acts as a voltage regulator because it maintains a nearly constant voltage across its terminals over a specified range of reverse-current values. A minimum value of reverse current, IZK, must be maintained in order to keep the diode in breakdown for voltage regulation. When the reverse current is reduced below the knee of the curve, the voltage decreases drastically and regulation is lost. Also, there is a maximum current, IZM, above which the diode may be damaged due to excessive power dissipation. So, basically, the Zener Diode maintains a nearly constant voltage across its terminals for values of reverse current ranging from IZK to IZM. A nominal Zener voltage, VZ, is usually specified on a datasheet at a value of reverse current called the Zener test current.

To prevent high current through the Zener (for it may be damaged), a series resistor is included. After breakdown the voltage across the Zener remains constant even if the input voltage varies or the load current changes.

Characteristic Graphs:

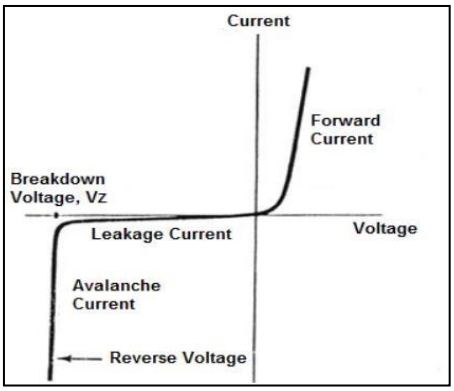


Fig.-1

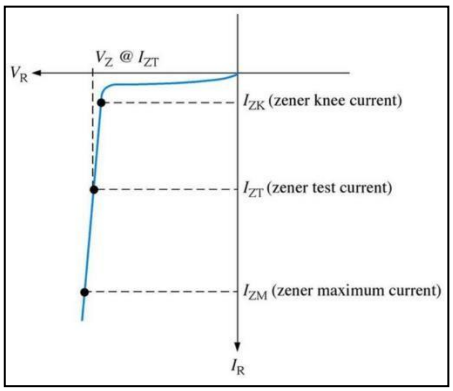
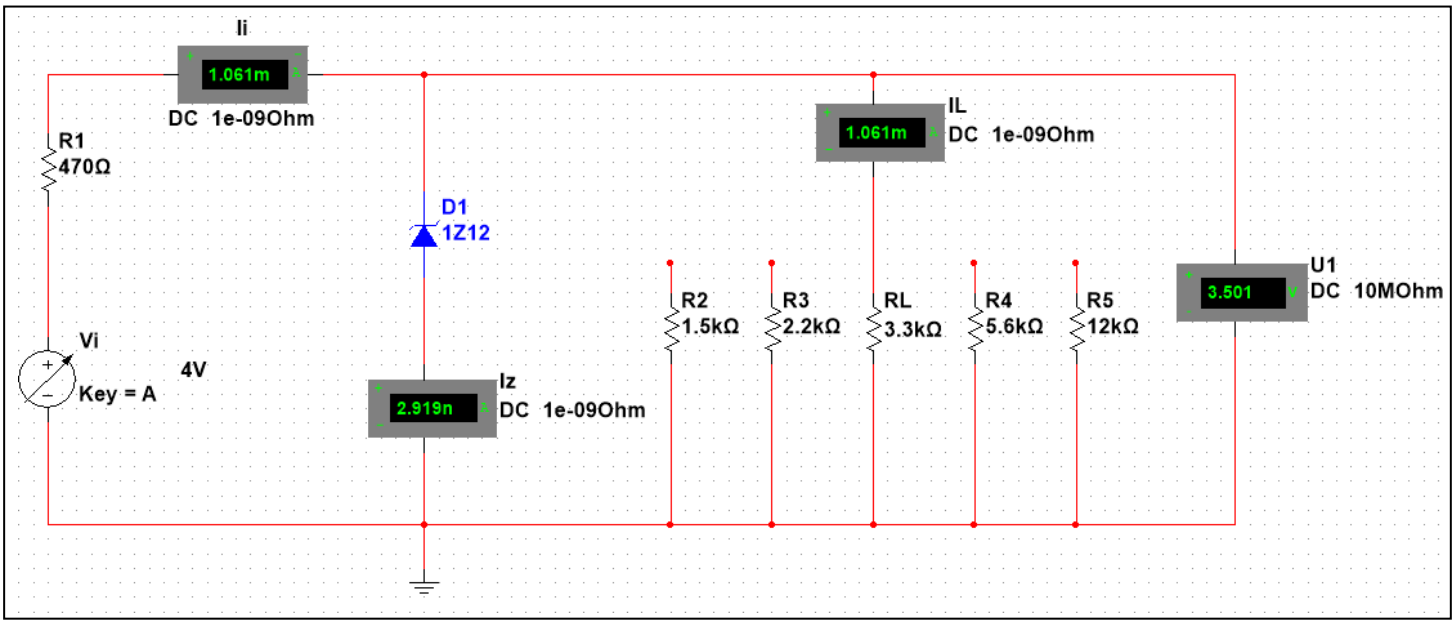


Fig.-2

EXPERIMENTAL SETUP:



(Circuit Diagram to find Zener Diode Characteristics)

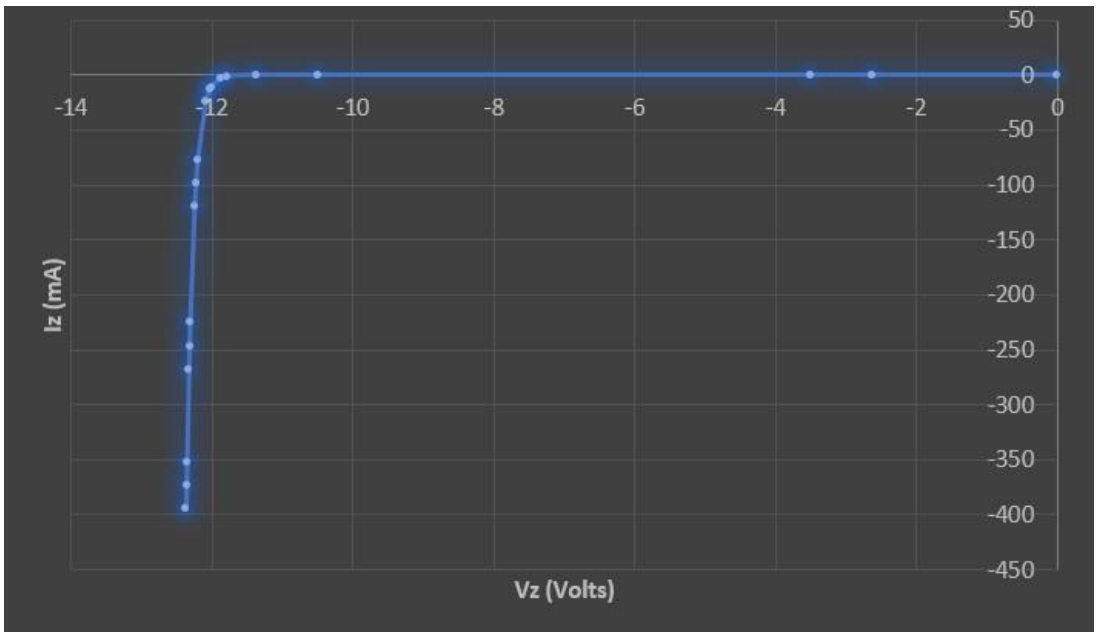
OBSERVATION:

-

Vi (Volts)	Ii (mA)	Iz (mA)	IL (mA)	Vz/Vdc (Volts)
1 V	0.265 mA	0.73 nA	0.265 mA	0.875 V
2 V	0.531 mA	1.46 nA	0.530 mA	1.751 V
3 V	0.796 mA	2.189 nA	0.796 mA	2.626 V
4 V	1.061 mA	2.919 nA	1.061 mA	3.501 V
5 V	1.327 mA	3.648 nA	1.326 mA	4.376 V
6 V	1.593 mA	4.378 nA	1.592 mA	5.252 V
7 V	1.858 mA	5.107 nA	1.856 mA	6.127 V
8 V	2.123 mA	5.837 nA	2.122 mA	7.002 V
9 V	2.388 mA	6.566 nA	2.387 mA	7.878 V

10 V	2.654 mA	7.296 nA	2.652 mA	8.753 V
11 V	2.919 mA	8.026 nA	2.917 mA	9.268 V
12 V	3.185 mA	0.012 µA	3.183 mA	10.504 V
13 V	3.467 mA	0.019 mA	3.444 mA	11.371 V
14 V	4.717 mA	1.143 mA	3.570 mA	11.783 V
15 V	6.637 mA	3.034 mA	3.599 mA	11.881 V
16 V	8.657 mA	5.038 mA	3.615 mA	11.931 V
17 V	11 mA	7.083 mA	3.626 mA	11.966 V
18 V	13 mA	9.149 mA	3.633 mA	11.991 V
19 V	15 mA	11 mA	3.640 mA	12.012 V
20 V	17 mA	13 mA	3.645 mA	12.029 V
25 V	27 mA	24 mA	3.663 mA	12.087 V
30 V	38 mA	34 mA	3.674 mA	12.123 V
35 V	49 mA	45 mA	3.681 mA	12.15 V
40 V	59 mA	56 mA	3.688 mA	12.172 V
45 V	70 mA	66 mA	3.693 mA	12.189 V
50 V	80 mA	77 mA	3.698 mA	12.204 V
60 V	102 mA	98 mA	3.705 mA	12.228 V
70 V	123 mA	119 mA	3.711 mA	12.248 V
80 V	144 mA	140 mA	3.716 mA	12.264 V
90 V	165 mA	162 mA	3.720 mA	12.278 V
100 V	187 mA	183 mA	3.723 mA	12.291 V
110 V	208 mA	204 mA	3.727 mA	12.302 V
120 V	229 mA	225 mA	3.730 mA	12.312 V
130 V	250 mA	247 mA	3.732 mA	12.321 V
140 V	272 mA	268 mA	3.736 mA	12.329 V
150 V	293 mA	289 mA	3.737 mA	12.336 V
160 V	314 mA	310 mA	3.739 mA	12.344 V
170 V	335 mA	332 mA	3.741 mA	12.350 V
180 V	357 mA	353 mA	3.745 mA	12.356 V
190 V	378 mA	374 mA	3.746 mA	12.362 V
200 V	399 mA	395 mA	3.746 mA	12.368 V

GRAPH:

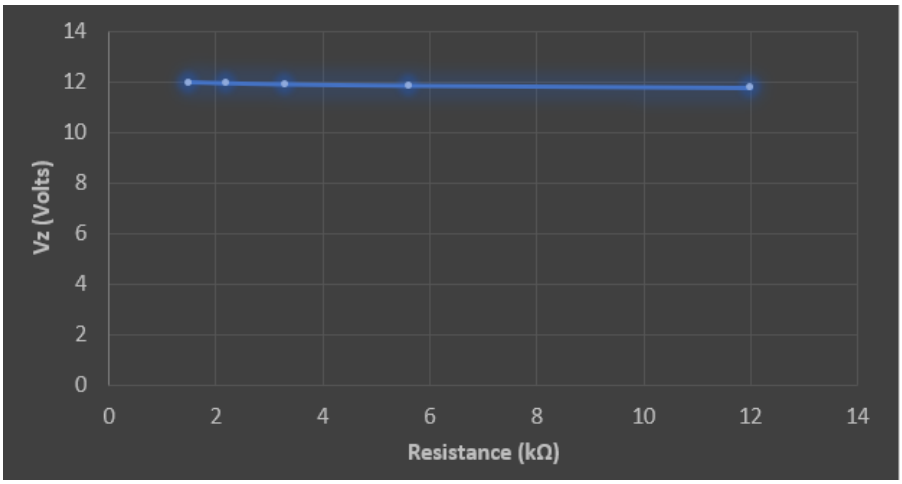


(Graph of I_z v/s V_z)

OBSERVATION:

R_L (kΩ)	I_i (mA)	I_z (mA)	I_L (mA)	V_z/V_{dc} (Volts)
1.5 kΩ	16 mA	8.02 mA	7.985 mA	11.978 V
2.2 kΩ	11 mA	5.547 mA	5.429 mA	11.941 V
3.3 kΩ	7.237 mA	3.631 mA	3.604 mA	11.899 V
5.6 kΩ	4.361 mA	2.244 mA	2.116 mA	11.851 V
12 kΩ	1.980 mA	0.999 mA	0.981 mA	11.770 V

GRAPH:



RESULT:

- After breakdown the voltage across the Zener remains constant even if the input voltage varies or the load current changes.
- The voltage across the Zener will remain approximately constant at its break down voltage Vz for all values of the load resistance.
- Average Zener Voltage (Vz) = 11.8874 Volts

Reference Links: https://youtu.be/s3JU0e2A3l4

EXPERIMENT – 4

AIM: Measurement of Rectification Efficiency and Ripple Factor of Half-Wave Rectifier and Full-Wave Rectifier Circuits with and without C-Filter

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Power Supply
- CRO
- Multimeter

CIRCUIT COMPONENTS:

- Resistors (R_L) –1kΩ
- Capacitor (C) – 100μF

THEORY:

Because of the ability to conduct current in one direction and block current in the other direction, diodes are used in circuits called rectifiers that convert AC Voltage into DC Voltage. Rectifiers are found in all DC power supplies that operate from an AC Voltage source. A power supply is an essential part of each electronic system from the simplest to the most complex.

Half Wave Rectifier: During positive half cycle of the input voltage, the diode D1 is in the forward bias and conducts through the load resistor R_L. Hence the current produces an output voltage across the load resistor R_L, which has the same shape as the +ve half cycle of the input voltage.

During the -ve half cycle of the input voltage, the diode is in reverse biased and there is no current in the circuit i.e., the voltage across the load resistor R_L is zero. The net result is only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified output voltage is the value measured on DC voltmeter.

Full Wave Rectifier: The circuit of a centre tapped full wave rectifier uses two diodes D1 and D2. During the positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2 is reverse biased. The diode D1 conducts and current flows through the load resistor RL. During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flows through the load resistor RL in the same direction. There is a continuous current flow through the load resistor RL, during both the half cycles and will get unidirectional current flow.

The difference between full wave and half wave rectification is that, a full wave rectifier allows unidirectional current to the load during the entire 360 degrees of the input signal and half wave rectifier allows this only during one half cycle i.e.,180 degrees.

For practical circuits, transformer coupling is usually provided for two reasons:

1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus, preventing shock hazards in the secondary circuit.

A filter ideally eliminates the fluctuations in the output voltage of a halfwave or full-wave rectifier and produces a constant-level dc voltage. Filtering is necessary because electronic circuits require a constant source of dc voltage and current to provide power and biasing for proper operation.

Ripple Factor: The output of a rectifier consists of a DC component and an AC component (also known as ripple). The AC component is undesirable and accounts for the pulsations in the rectifier output. The effectiveness of a rectifier depends upon the magnitude of AC component in the output; the smaller this component, the more effective is the rectifier.

The ratio of RMS value of AC component to the DC component in the rectifier output is known as ripple factor i.e.

Ripple factor (r) is defined as;

$$r = \frac{rms\ value\ of\ the\ a.c.component}{d.c.value\ of\ the\ rectifier\ wave} = \frac{I_{ac,rms}}{I_{dc}}$$

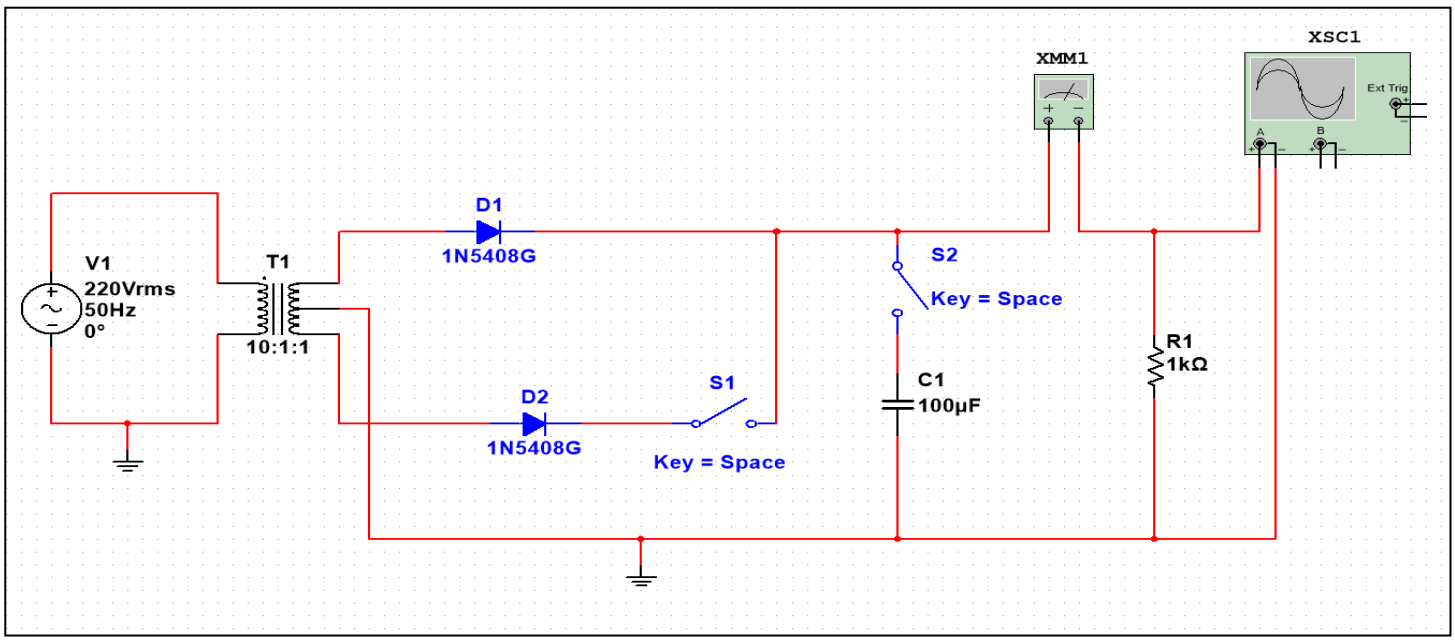
Therefore, ripple factor is very important in deciding the effectiveness of a rectifier. The smaller the ripple factor, the lesser the effective AC component and hence more effective is the rectifier.

Rectification Efficiency: The ratio of DC power output to the applied input AC power is known as Rectification Efficiency.

Rectification Efficiency or Ratio of Rectification (η) is defined as;

$$\eta = \frac{d.c.\ power\ delivered\ to\ load}{a.c.\ input\ power\ from\ the\ Transformer} = \frac{P_{dc}}{P_{ac}}$$

EXPERIMENTAL SETUP:



(Circuit Diagram of Half-Wave and Full-Wave Diode Rectifier)

OBSERVATION:

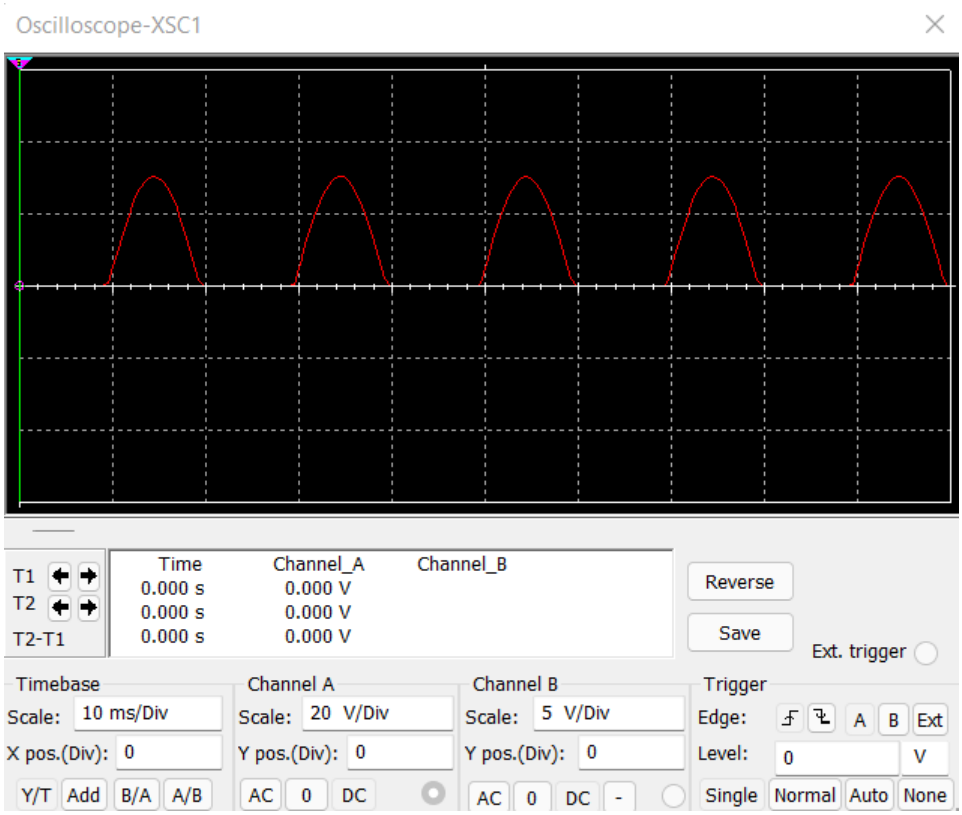
Type Of Rectification	$I_{AC,rms}$ (mA)	I_{dc} (mA)	I_{rms} (mA)	Ripple Factor (r)	Rectification Efficiency (η)
Half-Wave Rectifier (without C- Filter)	11.688 mA	9.557 mA	15.097 mA	1.223	40.06 %
Half-Wave Rectifier (with C- Filter)	1.504 mA	27.909 mA	27.949 mA	0.053	99.6 %
Full-Wave Rectifier (without C- Filter)	9.484 mA	19.126 mA	21.34 mA	0.495	80.28 %
Full-Wave Rectifier (with C- Filter)	0.773 mA	29.31 mA	29.32 mA	0.026	99.80 %

NOTE:

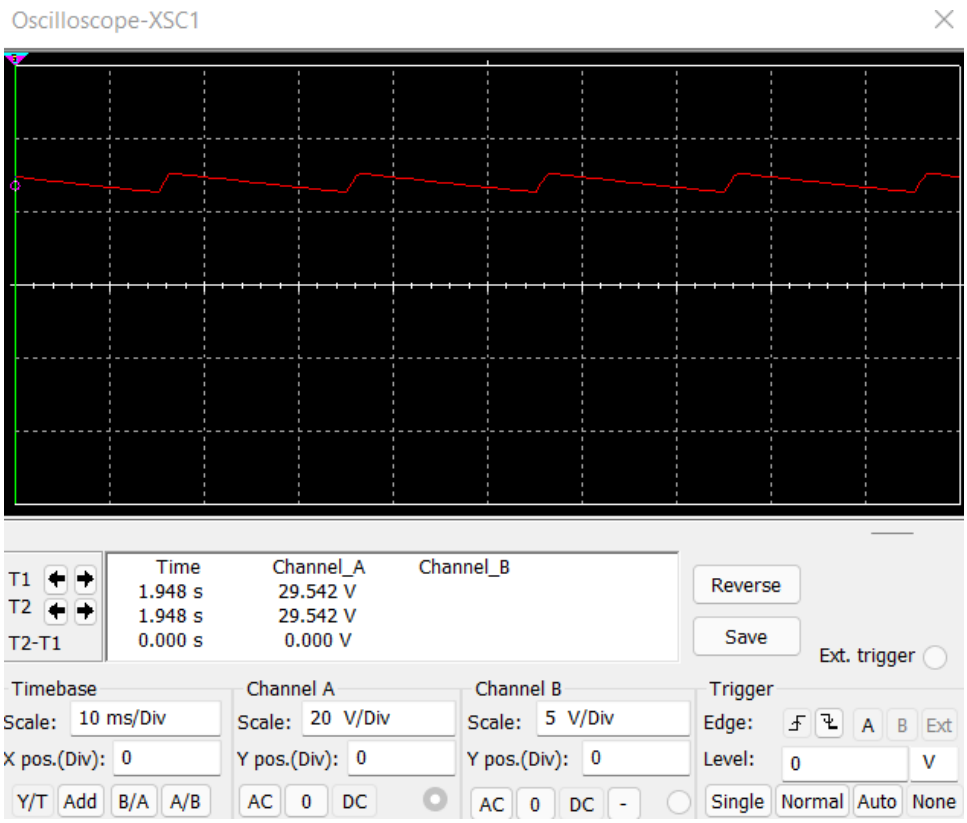
$$I_{rms} = \sqrt{(I_{ac,rms}^2 + I_{dc}^2)}$$

$$\eta = \frac{P_{dc}}{P_{ac}} = \left(\frac{I_{dc}}{I_{rms}}\right)^2 \cdot \left(\frac{R_L}{R_f + R_L}\right) \approx \left(\frac{I_{dc}}{I_{rms}}\right)^2 ; \quad for\ R_f \ll R_L$$

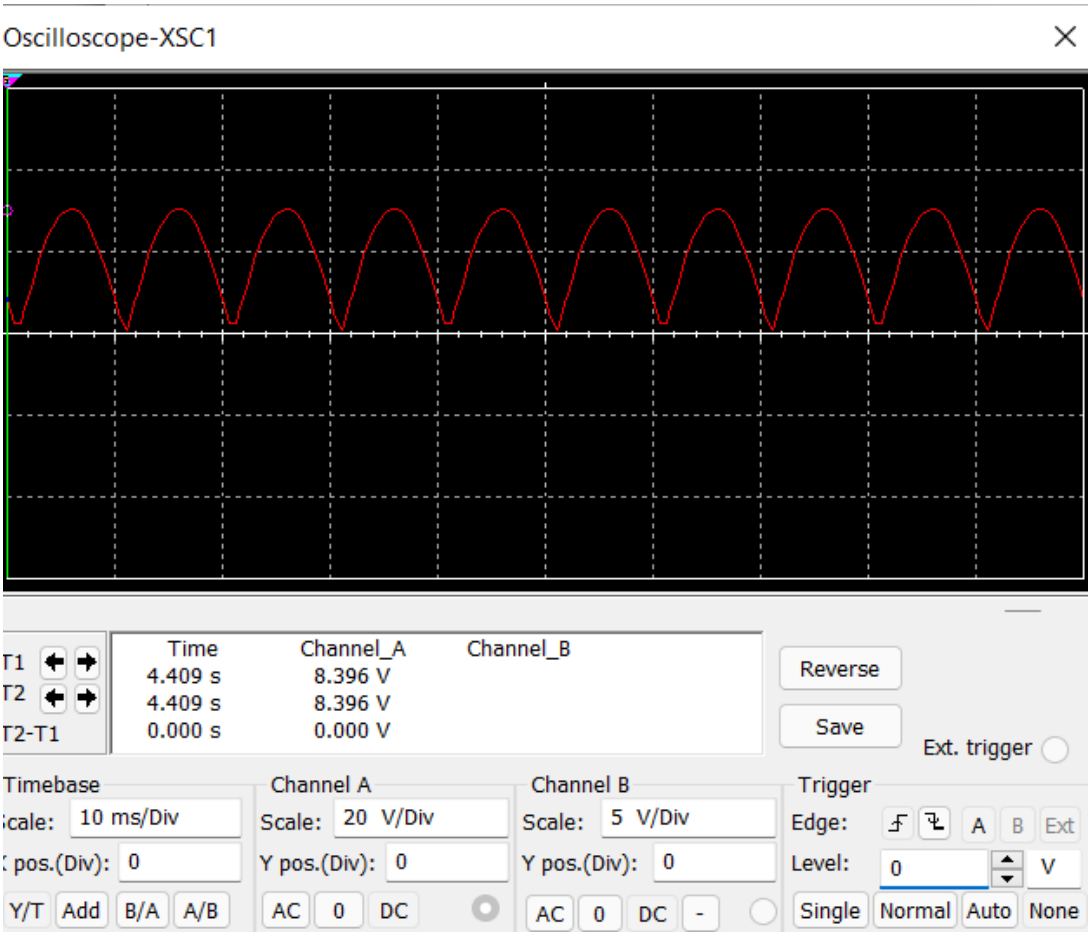
GRAPH:



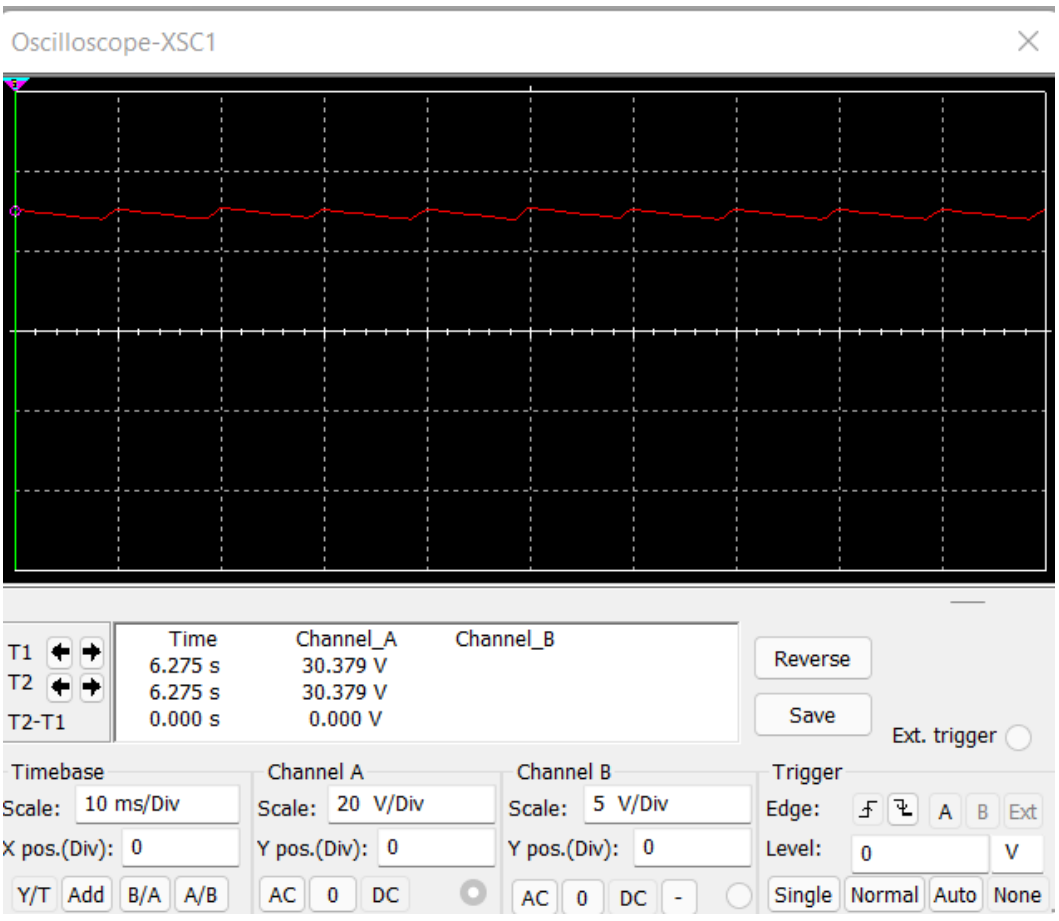
(Half-Wave Rectifier without C-Filter - Waveform)



(Half-Wave Rectifier with C-Filter - Waveform)



(Full-Wave Rectifier without C-Filter - Waveform)



(Full-Wave Rectifier with C-Filter - Waveform)

RESULT:

- Half-Wave Rectifier (without C- Filter):

  Rectification Efficiency (η) = 40.06%
  Ripple Factor (r) = 1.223

- Half-Wave Rectifier (with C- Filter):

  Rectification Efficiency (η) = 99.6%
  Ripple Factor (r) = 0.053

- Full-Wave Rectifier (without C- Filter):

  Rectification Efficiency (η) = 80.28%
  Ripple Factor (r) = 0.495

- Full-Wave Rectifier (with C- Filter):

  Rectification Efficiency (η) = 99.80%
  Ripple Factor (r) = 0.026

CONCLUSION:

From the experiment we can conclude that for Half-Wave and Full-Wave Rectifier without c-filter the efficiency is low.

Reference Links: **https://youtu.be/QGawHsg4NpQ , https://youtu.be/syZgyPLHyp8**

EXPERIMENT – 5

AIM: To Determine the Frequency Response of CE Transistor Amplifier and Finding its Gain-Bandwidth Product.

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Power Supply
- AC Milli Voltmeter
- Function Generator
- Common Emitter Amplifier Transistor Circuit

CIRCUIT COMPONENTS:

- Capacitors = C_1 - 50µF, C_2 - 50µF, C_3 - 250µF
- Resistance = R_1 – 1KΩ , R_2 – 8.2KΩ , R_3 – 1.5KΩ , R_4 – 1KΩ , R_5 – 470Ω , R_6 – 1KΩ

THEORY:

The Amplifier is an electronic circuit that is used to increase the strength of a weak input signal in terms of voltage, current, or power. The process of increasing the strength of a weak signal is known as Amplification. One most important constraint during the amplification is that only the magnitude of the signal should increase and there should be no changes in original signal shape. The transistor (BJT,FET) is a major component in an amplifier system. When a transistor is used as an amplifier, the first step is to choose an appropriate configuration, in which device is to be used. Then, the transistor should be biased to get the desired Q-point. The signal is applied to the amplifier input and output gain is achieved. In this article, we will discuss common emitter amplifier analysis.

Common Emitter Amplifier Configuration: In Common Emitter Amplifier Configuration, the Emitter of a BJT is common to both the input and output signal as shown below. The arrangement is the same for a NPN transistor, but bias will be opposite w.r.t PNP transistor.

Operation of Common Emitter Amplifier: When a signal is applied across the emitter-base junction, the forward bias across this junction increases during the upper half cycle. This leads to increase the flow of electrons from the emitter to a collector through the base, hence increases the collector current. The increasing collector current makes more voltage drops across the collector load resistor RC=R3.The negative half cycle decreases the forward bias voltage across the emitter-base junction. The decreasing collector-base voltage decreases the collector current in the whole collector resistor R3. Thus, the amplified load resistor appears across the collector resistor. It is seen that there is a 180-degree phase shift between the input and output waveforms.

Common Emitter Amplifier Circuit Elements and Their Functions:

Biasing Circuit/Voltage Divider: The resistances R2, R4and R5 used to form the voltage biasing and stabilisation circuit. The biasing circuit needs to establish a proper operating Q-point otherwise, a part of the negative half cycle of the signal may be cut-off in the output.

Input Capacitor (C1):
The capacitor C1 is used to couple the signal to the base terminal of the BJT. If it is not there, the signal source resistance, R1 will come across R4and hence, it will change the bias. C1 allows only the AC signal to flow but isolates the signal source from R4.

Emitter Bypass Capacitor(C3):
An Emitter bypass capacitor C3 is used parallel with R5to provide a low reactance path to the amplified AC signal. If it is not used, then the amplified AC signal following through R5will cause a voltage drop across it, thereby dropping the output voltage.

Coupling Capacitor(C2):
The coupling capacitor C2 couples one stage of amplification to the next stage. This technique used to isolate the DC bias settings of the two coupled circuits.

Base Current: $i_B = I_B + I_b$

Where,

I_B = DC base current when no signal is applied

I_b = AC base when AC signal is applied

i_B = Total Base Current

Collector Current: $i_C = I_C + i_c$

Where,

i_C = Total Collector Current

I_C = Zero Signal Collector Current

I_c = AC Collector Current when AC Signal is applied

Emitter Current: $i_E = I_E + i_e$

Where,

I_E = Zero Signal Emitter Current

I_e = AC Emitter Current when AC Signal is applied

I_E = Total Emitter Current

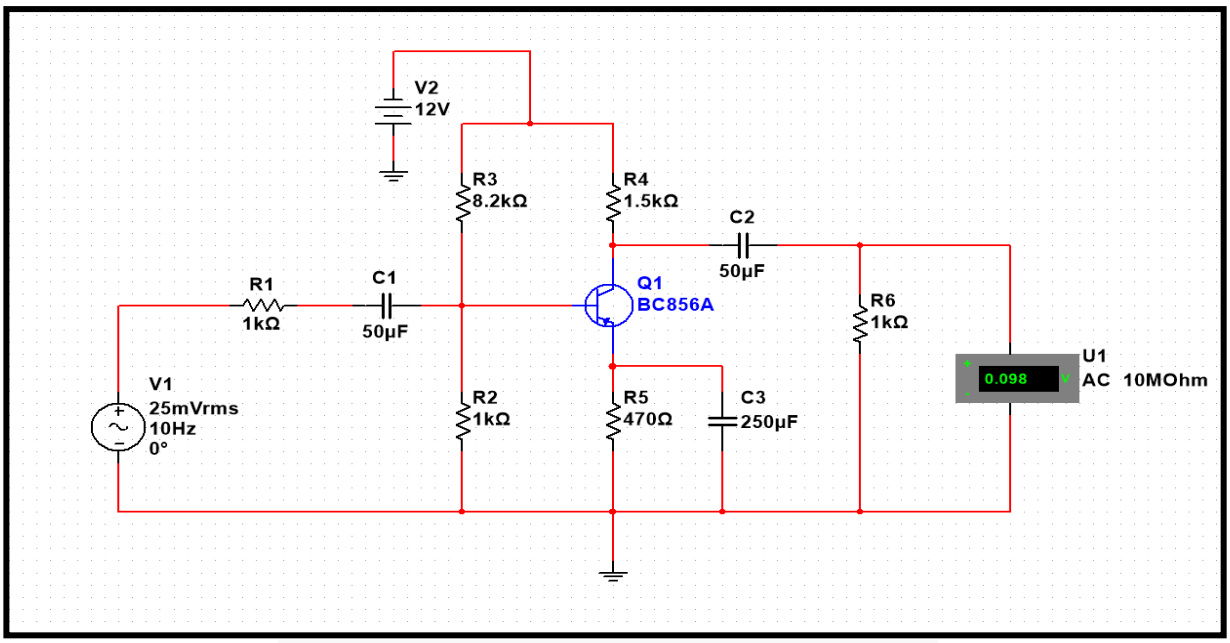
CE Amplifier Frequency Response: The voltage gain of a CE amplifier varies with signal frequency. It is because reactance of capacitors in the circuit changes with signal frequency and hence affects the output voltage. The curve drawn between voltage gain and the signal frequency of an amplifier is known as frequency response. Below model graph shows the frequency response of a typical CE amplifier.

At low frequencies (<FL):The reactance of coupling capacitor C_2 is relatively high and hence very small part of the signal will pass from amplifier stage to the load. Moreover, C_3 cannot shunt the R_5 effectively because of its large reactance at low frequencies. These two factors cause a drop off of voltage gain at low frequencies.

At high frequencies (>FH):The reactance of coupling capacitor C_2 is very small and it behaves as a short circuit. This increases the loading effect of the amplifier stage and serves to reduce the voltage gain. Moreover, at high frequencies, the capacitive reactance of base-emitters junction is low which increases the base current. This frequency reduces the current amplification factor β. Due to these two reasons, the voltage gain drops off at high frequency.

At mid frequencies (FL to FH):The voltage gain of the amplifier is constant. The effect of the coupling capacitor C_2 in this frequency range is such as to maintain a constant voltage gain. Thus, as the frequency increases in this range, the reactance of C_2 decreases, which tend to increase the gain. However, at the same time, lower reactance means higher almost cancel each other, resulting in a uniform fair at mid-frequency.

EXPERIMENTAL SETUP:



(Circuit diagram for Common Emitter Amplifier)

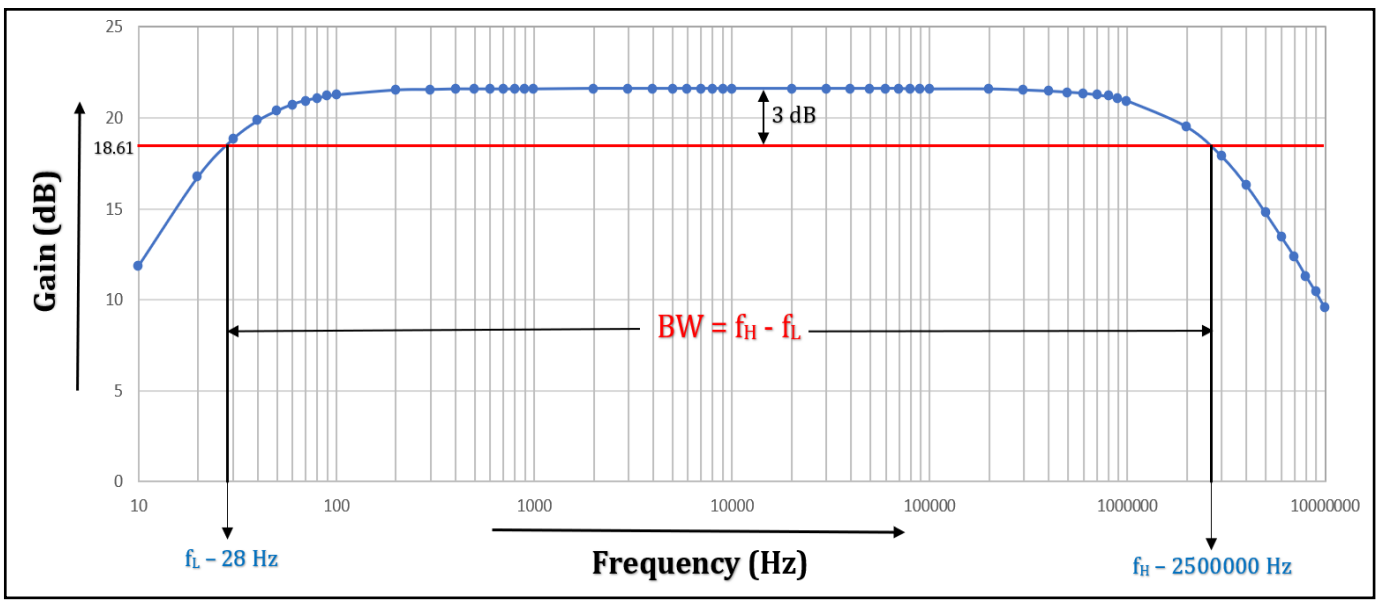
OBSERVATION:

- Input Voltage (fixed) = 25mV

Frequency (Hz)	**Output Voltage** (Volt)	**Voltage Gain** (V_{out}/V_{in})	**Gain** **[20 $\log_{10}(V_{out}/V_{in})$]** (dB)
10 Hz	0.098 Volt	3.92	11.86 dB
20 Hz	0.172 Volt	6.88	16.75 dB
30 Hz	0.218 Volt	8.72	18.81 dB
40 Hz	0.245 Volt	9.8	19.82 dB
50 Hz	0.261 Volt	10.44	20.37 dB
60 Hz	0.272 Volt	10.88	20.73 dB
70 Hz	0.279 Volt	11.16	20.95 dB
80 Hz	0.283 Volt	11.32	21.07 dB
90 Hz	0.287 Volt	11.48	21.19 dB
100 Hz	0.289 Volt	11.56	21.25 dB
200 Hz	0.298 Volt	11.92	21.52 dB
300 Hz	0.299 Volt	11.96	21.55 dB
400 Hz	0.300 Volt	12	21.58 dB
500 Hz	0.300 Volt	12	21.58 dB
600 Hz	0.300 Volt	12	21.58 dB
700 Hz	0.300 Volt	12	21.58 dB
800 Hz	0.300 Volt	12	21.58 dB
900 Hz	0.300 Volt	12	21.58 dB
1000 Hz	0.300 Volt	12	21.58 dB
2000 Hz	0.301 Volt	12.04	21.61 dB
3000 Hz	0.301 Volt	12.04	21.61 dB
4000 Hz	0.301 Volt	12.04	21.61 dB
5000 Hz	0.301 Volt	12.04	21.61 dB
6000 Hz	0.301 Volt	12.04	21.61 dB
7000 Hz	0.301 Volt	12.04	21.61 dB
8000 Hz	0.301 Volt	12.04	21.61 dB
9000 Hz	0.301 Volt	12.04	21.61 dB
10k Hz	0.301 Volt	12.04	21.61 dB
20k Hz	0.301 Volt	12.04	21.61 dB
30k Hz	0.301 Volt	12.04	21.61 dB
40k Hz	0.301 Volt	12.04	21.61 dB
50k Hz	0.301 Volt	12.04	21.61 dB
60k Hz	0.301 Volt	12.04	21.61 dB

70k Hz	0.301 Volt	12.04	21.61 dB
80k Hz	0.300 Volt	12	21.58 dB
90k Hz	0.300 Volt	12	21.58 dB
100k Hz	0.300 Volt	12	21.58 dB
200k Hz	0.300 Volt	12	21.58 dB
300k Hz	0.298 Volt	11.92	21.52 dB
400k Hz	0.296 Volt	11.84	21.46 dB
500k Hz	0.294 Volt	11.76	21.40 dB
600k Hz	0.292 Volt	11.68	21.34 dB
700k Hz	0.289 Volt	11.56	21.25 dB
800k Hz	0.286 Volt	11.44	21.16 dB
900k Hz	0.282 Volt	11.28	21.04 dB
1M Hz	0.278 Volt	11.12	20.92 dB
2M Hz	0.236 Volt	9.44	19.49 dB
3M Hz	0.196 Volt	7.84	17.88 dB
4M Hz	0.163 Volt	6.52	16.28 dB
5M Hz	0.137 Volt	5.48	14.77 dB
6M Hz	0.118 Volt	4.72	13.47 dB
7M Hz	0.104 Volt	4.16	12.38 dB
8M Hz	0.092 Volt	3.68	11.31 dB
9M Hz	0.083 Volt	3.32	10.42 dB
10M Hz	0.075 Volt	3.0	9.54 dB

GRAPH:



(Frequency Response of Common Emitter Amplifier)

RESULT:

- Maximum Gain = 21.61 dB
- 3 dB Gain = 18.61 dB
- 3 dB Lower Cut Off Frequency (f_L) = 28 Hz
- 3 dB Higher Cut Off Frequency (f_H) = 2500 kHz
- 3 dB Bandwidth (BW) = $f_H - f_L$ = 2499.927 kHz
- Gain Bandwidth Product = Bandwidth X Maximum Gain = 2499.927 * 21.61 = 54023.42252 kHz
- Max voltage Gain = 12.04

CONCLUSION:

From this experiment we can understand that the frequency response of any given circuit is the variation in its behavior with changes in the input signal frequency as it shows the band of frequencies over which the output (and the gain) remains fairly constant. The range of frequencies either big or small between f_L and f_H is called the circuits bandwidth. So, from this we are able to determine at a glance the voltage gain (in dB) for any sinusoidal input within a given frequency range.

Reference Links: https://youtu.be/5RbWfuuX8gk

EXPERIMENT – 6

AIM: To Determine the Output and Transfer Characteristics of JFET and Measurement of its Voltage Gain.

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Power Supply
- Millimetre
- Electronic Multimeter

CIRCUIT COMPONENTS:

- JEFT – BFW 10/112
- Resistance = R_S – 1KΩ , R_L – 1KΩ

THEORY:

A field effect transistor is a three-terminal unipolar device. Its input impedance is very high. A field effect transistor can be either a JFET or MOSFET. A JFET, MOSFET both can be either have N-channel or P-channel. An N-channel JFET has an N-type Semiconductor bar, the two ends of which make the drain and source terminals. On the other two sides of this N-type Semiconductor bar, two P type regions are made. These P-regions form gates. Usually, these two Gates are connected together to form a single gate. The gate is given a negative bias with respect to the source. The drain is given positive potential with respect to the source. In case of a P-channel JFET, the terminals of all the batteries are reversed.

JFET is a voltage controlled current device so its characteristics are the curves which represent relationship between different dc currents and voltages. These are helpful in studying different region of operation of a Field effect transistor when connected in a circuit. The two important characteristics of a Field Effect Transistor are:

1. Output /Drain characteristic
2. Transfer characteristic

Output / Drain Characteristics: It is the curve plotted between output drain current I_D verses output drain to source voltage V_{DS} for constant values of input Gate to source voltage V_{GS} as shown in Fig 1.

Ohmic region OA: This part of the characteristic is linear indicating that for low values of V_{DS}, current varies directly with voltage following Ohm's Law. It means that JFET behaves like an ordinary resistor till point A (called knee) is reached.

Curve AB: In this region, I_D increases at inverse square law rate up to point B which is called Pinch-off point. This progressive fall in the rate of increase of I_D is caused by the square law increase in the depletion region at each gate up to point B where the two regions are closest without touching each other. The drain to source voltage V_{DS} corresponding to point B is called pinch-off voltage V_{PO}.

Pinch-off region BC: It is also known as saturation region or 'amplifier' region. Here, JFET operates as a constant-current device because I_D is relatively independent of V_{DS}. It is due to the fact that as V_{DS} increases channel resistance also increases proportionally thereby keeping I_D practically constant at I_{DSS}. Drain current in this region is given by Shockley's equation;

$$I_D = I_{DSS} [1 - (V_{GS} / V_{PO})^2] = I_{DSS} [- (V_{GS} / V_{GS\,(off)})^2]$$

It is the normal operating region of the JFET when used as an amplifier.

Breakdown Region: If V_{DS} is increased beyond its value corresponding to point C (called avalanche breakdown voltage), JFET enters the breakdown region where I_D increases to an extensive value. This happens because the reversed biased gate channel PN junction undergoes avalanche breakdown when small change in V_{DS} produce very large change in I_D.

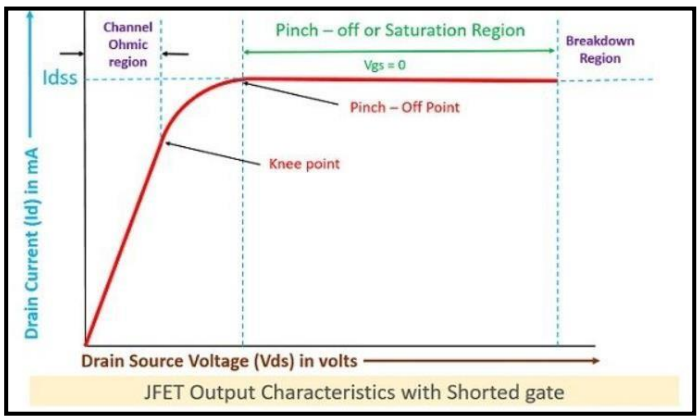


Fig - 1

JFET characteristics with External Bias: Fig 2 shows a family of I_D verses V_{DS} curves for different values of V_{GS}. It is seen that as the negative gate bias voltage is increased: Pinch-off voltage V_P is reached at a lower value of V_{DS} than V_{GS}= 0. Value of V_{DS} for breakdown is decreased.

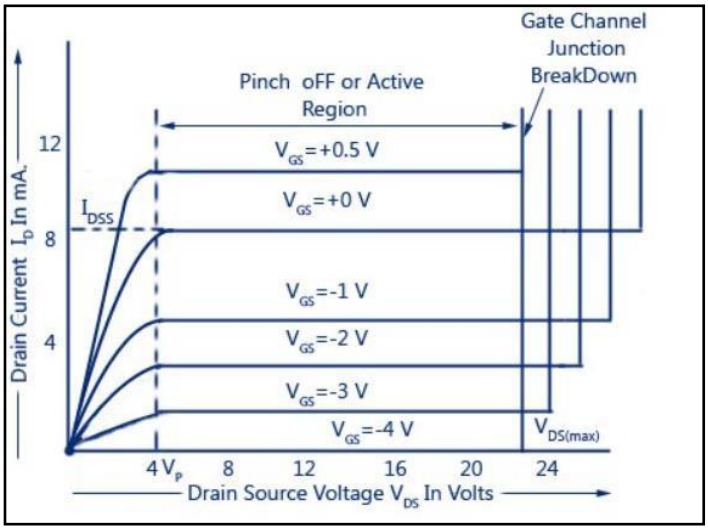


Fig - 2

Transfer Characteristic: It is the curve plotted between output drain current versus input Gate to source voltage for constant values of output drain to source voltage as shown in Fig 3.

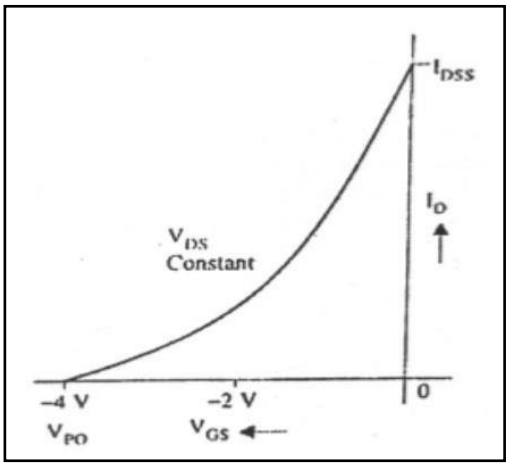


Fig - 3

It is similar to the transconductance characteristics of a vacuum tube or a transistor. It is shows that when V_{GS}= 0, I_D= I_{DSS} and when I_D= 0, V_{GS}= V_{PO}. The transfer characteristic approximately follows the equation.

$$I_D = I_{DSS}\left[1 - (V_{GS} / V_{PO})^2\right] = I_{DSS}\left[-(V_{GS} / V_{GS\,(off)})^2\right]$$

The above equation can be written as $V_{GS} = V_{GS(off)} [1 - (I_D / I_{DSS})^{1/2}]$. These characteristics can also be obtained from the drain/output characteristics by reading off V_{GS} and I_{DSS} values for different values of V_{DS}. The various parameters of a JFET can be obtained from its two characteristics.

The main parameters of a JFET when connected in common source mode are:

1.AC Drain Resistance, r_d :It is the AC resistance between drain and source terminals when JFET is operating in the pinch-off region. It is given by;

$$r_d = \frac{Change\ in\ V_{DS}}{Change\ in\ I_D} \quad ; \text{ At } V_{GS} \text{ constant}$$

An alternative name is dynamic drain resistance. It is given by the slope of the drain characteristics in the pinch off region. It is sometimes written as r_{ds} emphasizing the fact that it is the resistance from drain to source. Since r_d is usually the output resistance of a JFET, it may also be expressed as an output admittance Y_{ds}. Obviously, $Y_{ds} = 1/r_d$. It has a very high value.

2. Transconductance, g_m: It is simply the slope of transfer characteristics;

$$g_m = \frac{Change\ in\ I_D}{Change\ in\ V_{GS}} \quad ; \text{ At } V_{DS} \text{ constant}$$

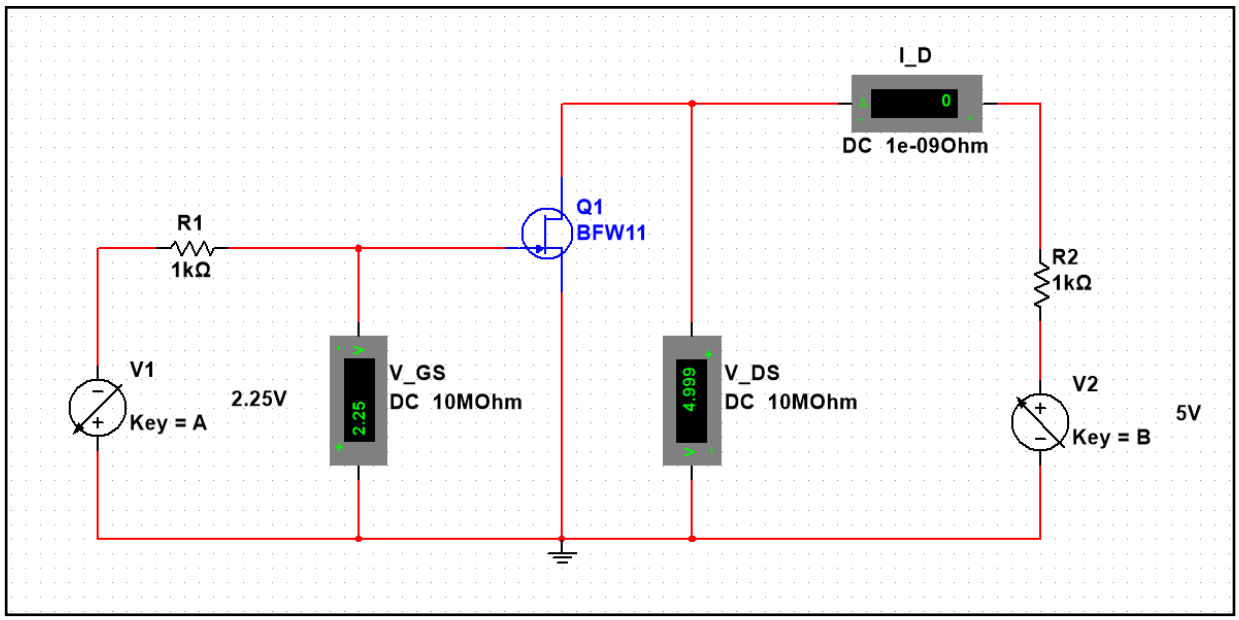
Its unit is siemens (S) /mho. It is also called forward transconductance (g_{fs}) or forward transadmittance Y_{fs}. The transconductance measured at I_{DSS} is written as g_{mo}. Mathematically;

$$g_m = g_{mo} [1 - (V_{GS} / V_P)]$$

FORMULAE USED:

- Drain Resistance $(r_d) = \Delta V_{DS} / \Delta I_d \mid V_{GS} = \text{Constant}$
- Train Conductance $(g_m) = \Delta I_D / \Delta V_{GS} \mid V_{DS} = \text{Constant}$
- Amplification / Intrinsic Factor of JFET $= \mu = r_d \times g_m = \Delta V_{DS} / \Delta V_{GS} \mid I_D = \text{Constant}$

EXPERIMENTAL SETUP:



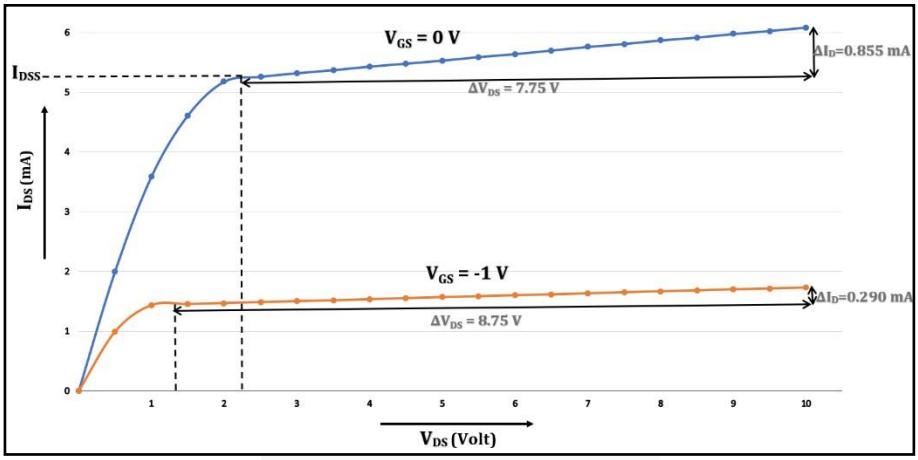
(Circuit diagram for the Measurement of Output and Transfer Characteristics of JEFT)

OBSERVATION:

- **Output Characteristics:**

S No.	V_{DS} (0 V to 10 V) In Steps Of 0.5 Volt (Volt)	V_{GS} = 0 V	V_{GS} = -1 V
		I_D (mA)	I_D (mA)
1.	0 Volt	0 mA	0.287 pA
2.	0.5 Volt	2 mA	0.993 mA
3.	1 Volt	3.587 mA	1.436 mA
4.	1.5 Volt	4.609 mA	1.454 mA
5.	2 Volt	5.175 mA	1.470 mA
6.	2.5 Volt	5.258 mA	1.486 mA
7.	3 Volt	5.318 mA	1.502 mA
8.	3.5 Volt	5.369 mA	1.518 mA
9.	4 Volt	5.429 mA	1.534 mA
10.	4.5 Volt	5.478 mA	1.553 mA
11.	5 Volt	5.529 mA	1.569 mA
12.	5.5 Volt	5.588 mA	1.585 mA
13.	6 Volt	5.638 mA	1.60 mA
14.	6.5 Volt	5.698 mA	1.616 mA
15.	7 Volt	5.758 mA	1.632 mA
16.	7.5 Volt	5.807 mA	1.651 mA
17.	8 Volt	5.867 mA	1.668 mA
18.	8.5 Volt	5.915 mA	1.682 mA
19.	9 Volt	5.974 mA	1.70 mA
20.	9.5 Volt	6.025 mA	1.714 mA
21.	10 Volt	6.082 mA	1.730 mA

- **GRAPH:**

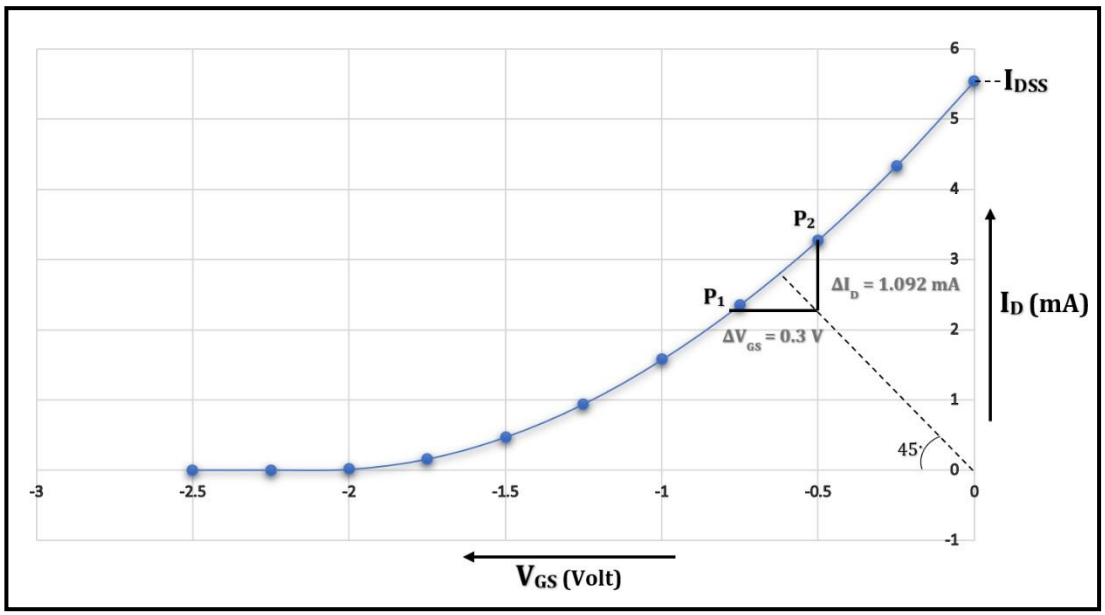


(Drain Characteristics Curve)

- **Transfer Characteristics:**

S No.	V_{GS} (0 V to -5 V) In Steps Of 0.25 Volt (Volt)	V_{DS} (Constant) = 5 V
		I_D (mA)
1.	0 Volt	5.539 mA
2.	-0.25 Volt	4.331 mA
3.	-0.50 Volt	3.271 mA
4.	-0.75 Volt	2.349 mA
5.	-1.00 Volt	1.569 mA
6.	-1.25 Volt	0.939 mA
7.	-1.50 Volt	0.467 mA
8.	-1.75 Volt	0.155 mA
9.	-2.00 Volt	9.77 µA
10.	-2.25 Volt	0 mA
11.	-2.5 Volt	0 mA

- **GRAPH:**



(Transfer Characteristics Curve)

RESULT:

1. Drain Resistance (r_d):

- V_{GS} = 0 Volt
  r_d = 9.06 kΩ
- V_{GS} = -1 Volt
  r_d = 30.17 kΩ

2. Trans Conductance (g_m):- $3.64 \times 10^{-3}\ \Omega^{-1}$

3. Amplification Factor (μ):

- V_{GS} = 0 Volt
  $\mu = (9.06\ k\Omega) \times (3.64 \times 10^{-3}\ \Omega^{-1}) = 32.978$
- V_{GS} = -1 Volt
  $\mu = (30.17\ k\Omega) \times (3.64 \times 10^{-3}\ \Omega^{-1}) = 109.818$

CONCLUSION:

From this experiment we can analyse the Drain and Transfer Characteristics of JFET in Common Source Configuration. JFET is a field effect transistor which is a voltage controlled current source having extremely high input impedance unlike BJT it is a unipolar junction transistor which is used in many electronic devices as an amplifier. This experiment effectively exemplified how one can use a Junction Field-Effect Transistor in a common-source amplifier configuration, which is the most widely used JFET amplifier design.

Reference Links: **https://youtu.be/TQ0B_n3gEvw**

EXPERIMENT – 7

AIM: Design of RC Phase Shift Oscillator using IC 741 OP-AMP and Finding its Frequency of Oscillation

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Dual DC Power Supply
- CRO

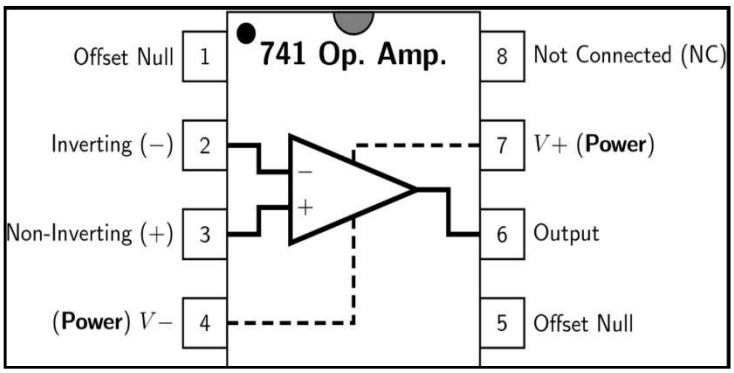
CIRCUIT COMPONENTS:

- Capacitors = C_1 – 0.1µF, C_2 – 0.1µF, C_3 – 0.1µF
- Resistance = R_1 – 10KΩ , R_2 – 470KΩ , R_3 – 10KΩ , R_4 – 10KΩ , R_5 – 10KΩ , R_6 – 33KΩ
- IC 741

THEORY:

- About OP – AMP IC 741:

The 741 is the godfather of all operational amplifiers (amplifiers on a chip). Although most up-to-date designs beat it for speed, low noise, etc., it still works well as a general-purpose device. One of its advantages is that it is *compensated* (its frequency response is tailored) to ensure that under most circumstances it won't produce unwanted spurious oscillations. This means it is easy to use, but the down-side of this is the poor speed/gain performance as compared to the modern OP – AMPs.



(741 IC in 8-Pin DIL-Dual in Line Pack)

The 741 is usually supplied in an 8-pin 'DIL' (Dual in Line) or 'DIP' (Dual Inline Package, or sometimes Dual Inline Plastic) package with a pinout shown above. This has proved so popular that many other competing op-amps have adopted the same package/pinout. Hence for many applications the various op-amps are 'drop in' replacements or upgrades for one another. These days there is a large family of 741 type devices, made by various manufacturers. Sometimes one manufacturer will make different versions, which work better than others in some respect. Each has a slightly different part number, but it generally has "741" in it somewhere!

The values given below are 'typical' for an ordinary 741, better versions may give better results...

```
Typical values of Basic Parameters:
Rail voltages : +/- 15V dc (+/- 5V min, +/- 18V max)
Input impedance: Around 2MegOhms
Low Frequency voltage gain: approx 200,000
Input bias current: 80nA
Slew rate: 0.5V per microsecond
Maximum output current: 20mA
Recommended output load: not less than 2kilOhms
```

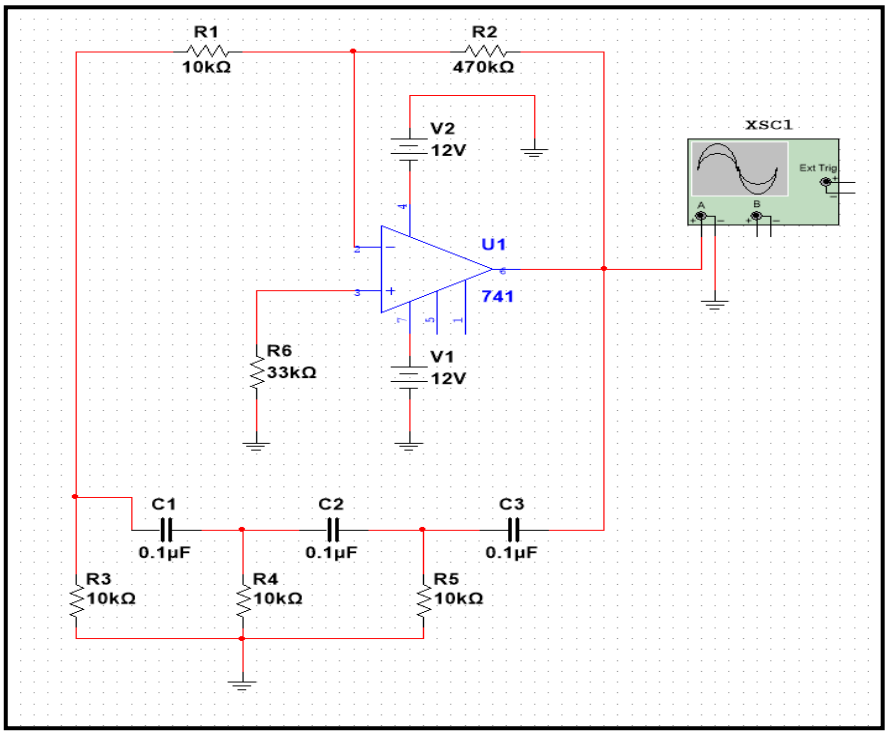
Note:- Due to frequency compensation, the 741 Voltage Gain fall rapidly with increasing signal frequency. We can say that the 741 has a gain bandwidth product of around one million.

RC Phase Shift Oscillator: The RC phase shift oscillator consists of an OP-AMP as amplifier and 3 RC cascade networks as the feedback circuit. The OP-AMP is used in the inverting mode, so output signal will be 180° out of phase. The feedback RC network provides the exactly 180° phase shift. So, the total phase shift is 0°. The gain of the amplifier is also kept large to produce oscillation.

The frequency of oscillation is given by;

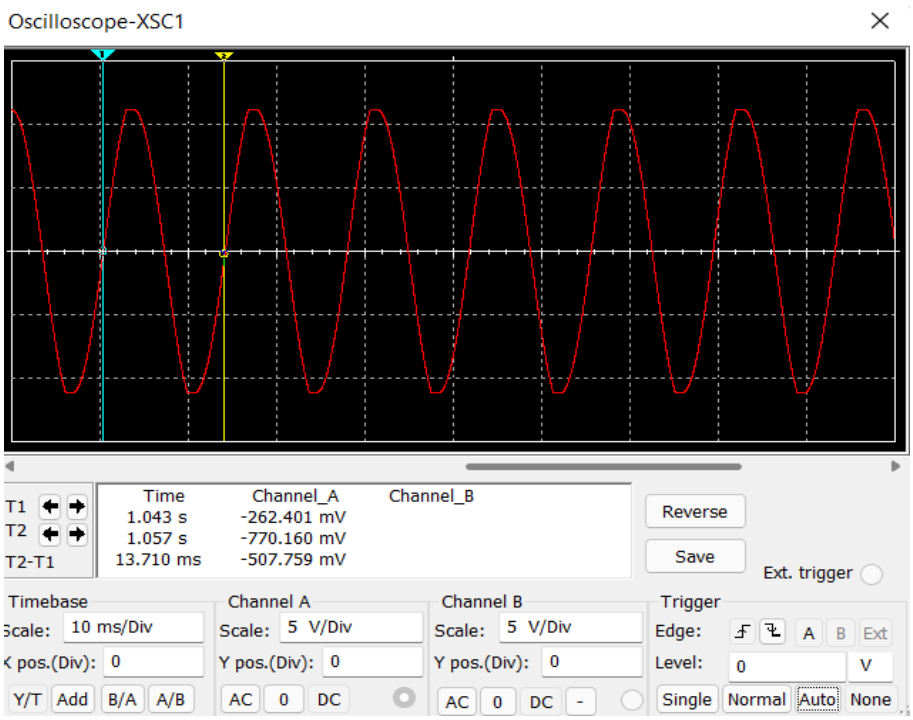
$$f = 0.065/RC$$

EXPERIMENTAL SETUP:



(Circuit diagram for RC Phase Shift Oscillator using IC 741 OP-AMP)

GRAPH:



(Output Waveform From CRO)

RESULT:

- Time Period = 13.710 millisecond
- Obtained Frequency = 72.93 Hz
- Calculated Frequency = 65.01 Hz
- Difference in Obtained and Calculated Frequency = 7.929 Hz
- Percentage Error = 12.182%

CONCLUSION:

From this experiment we can understand that the C phase shift oscillator is a sinusoidal oscillator used to produce sustained well shaped sine wave oscillations. It is used for different applications such as local oscillator for synchronous receivers, musical instruments, study purposes etc. This oscillator circuit designing is easy with basic components like resistors as well as capacitors. This circuit is not expensive and gives excellent frequency stability.

Reference Links: https://youtu.be/N_ijKNR4ar0

EXPERIMENT – 8

AIM(A): Design of Inverting Amplifier Using IC 741 OP – AMP and Finding its Frequency Response

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Power Supply
- AC Milli Voltmeter
- Function Generator

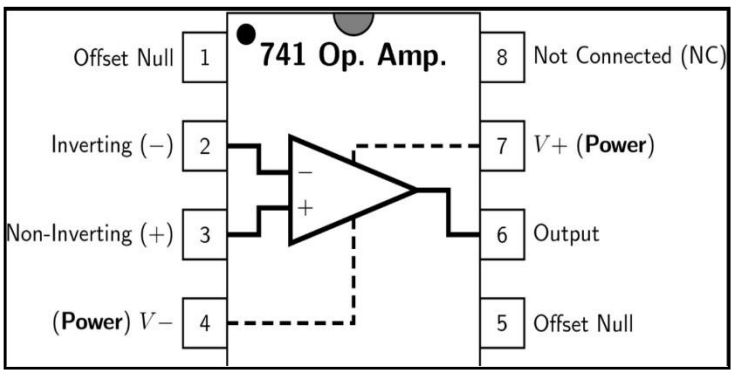
CIRCUIT COMPONENTS:

- IC 741
- Resistance = 47KΩ , 470KΩ , 4.7KΩ

THEORY:

- About OP – AMP IC 741:

The 741 is the godfather of all operational amplifiers (amplifiers on a chip). Although most up-to-date designs beat it for speed, low noise, etc., it still works well as a general-purpose device. One of its advantages is that it is *compensated* (its frequency response is tailored) to ensure that under most circumstances it won't produce unwanted spurious oscillations. This means it is easy to use, but the down-side of this is the poor speed/gain performance as compared to the modern OP – AMPs.



(741 IC in 8-Pin DIL-Dual in Line Pack)

The 741 is usually supplied in an 8-pin 'DIL' (Dual in Line) or 'DIP' (Dual Inline Package, or sometimes Dual Inline Plastic) package with a pinout shown above. This has proved so popular that many other competing op-amps have adopted the same package/pinout. Hence for many applications the various op-amps are 'drop in' replacements or upgrades for one another. These days there is a large family of 741 type devices, made by various manufacturers. Sometimes one manufacturer will make different versions, which work better than others in some respect. Each has a slightly different part number, but it generally has "741" in it somewhere!

The values given below are 'typical' for an ordinary 741, better versions may give better results...

```
Typical values of Basic Parameters:
Rail voltages : +/- 15V dc (+/- 5V min, +/- 18V max)
Input impedance: Around 2MegOhms
Low Frequency voltage gain: approx 200,000
Input bias current: 80nA
Slew rate: 0.5V per microsecond
Maximum output current: 20mA
Recommended output load: not less than 2kilOhms
```

Note:- Due to frequency compensation, the 741 Voltage Gain fall rapidly with increasing signal frequency. We can say that the 741 has a gain bandwidth product of around one million.

- Inverting Operational Amplifier Configuration:

In this Inverting Amplifier circuit, the operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are: "No current flows into the input terminal" and that "V2 always equals V3". However, in real world op-amp circuits both of these rules are slightly broken.

This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a "Virtual Earth/Ground". Because of this virtual earth node, the input resistance of the amplifier is equal to the value of the input resistor,R1and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

We said above that there are two very important rules to remember about Inverting Amplifiers or any operational amplifier for that matter and these are

- No Current Flows into the Input Terminals
- The Differential Input Voltage is Zero as $V_3 = V_2 = 0$(Virtual Earth)

The basic circuit of Inverting amplifier is shown below. In this mode of operation, the positive input terminal of the amplifier is grounded and the input signal Vin is applied to the negative input terminal via resistor R1.The feedback applied through Rf = R2 from the input terminal, is negative. This helps to in maintaining gain stable. The inverting operation performed by circuit is determined by Rf = R2 & R1.Note that the resistor R2 provides the negative feedback. Since the input signal is applied to the inverting input (–), the output will be inverted (i.e., 180° out of phase) as compared to the input. Hence the name inverting amplifier.

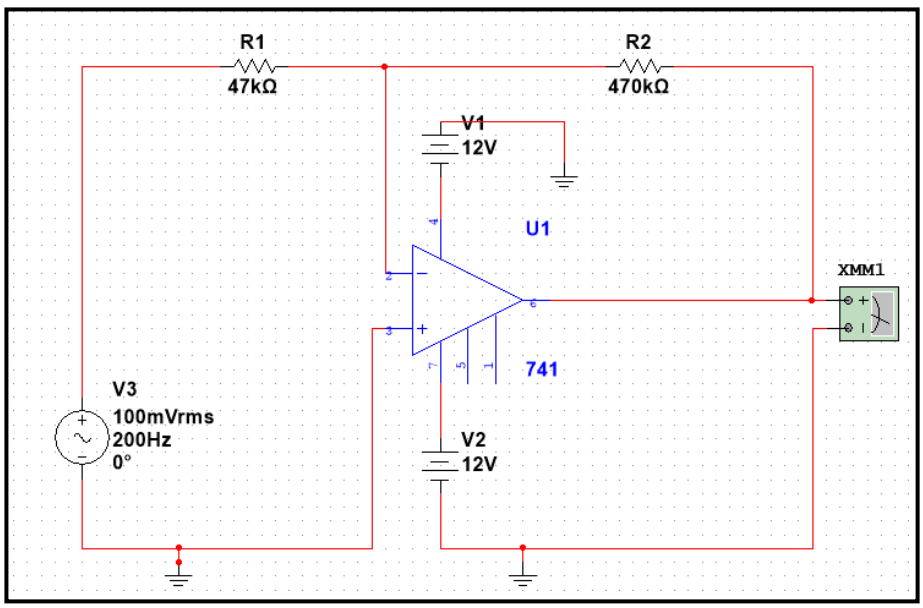
The current to the inverting input is zero. Therefore, current I_{in} flowing through R1entirely flows through feedback resistor R2. In other words, If= I_{in}.

$$\text{Thus, } I_{in} = \frac{V_{in}-0}{R1} = I_f = \frac{0-V_{out}}{R2}$$

$$\text{Since, } I_{in} = I_f \Longrightarrow \frac{V_{in}}{R1} = \frac{-V_{out}}{R2}$$

$$\text{Thus, the Closed-loop voltage gain } A_{CL} = \frac{V_{out}}{V_{in}} = -\frac{R2}{R1}$$

EXPERIMENTAL SETUP:



(Circuit diagram for Inverting Amplifier using IC – 741 OP - AMP)

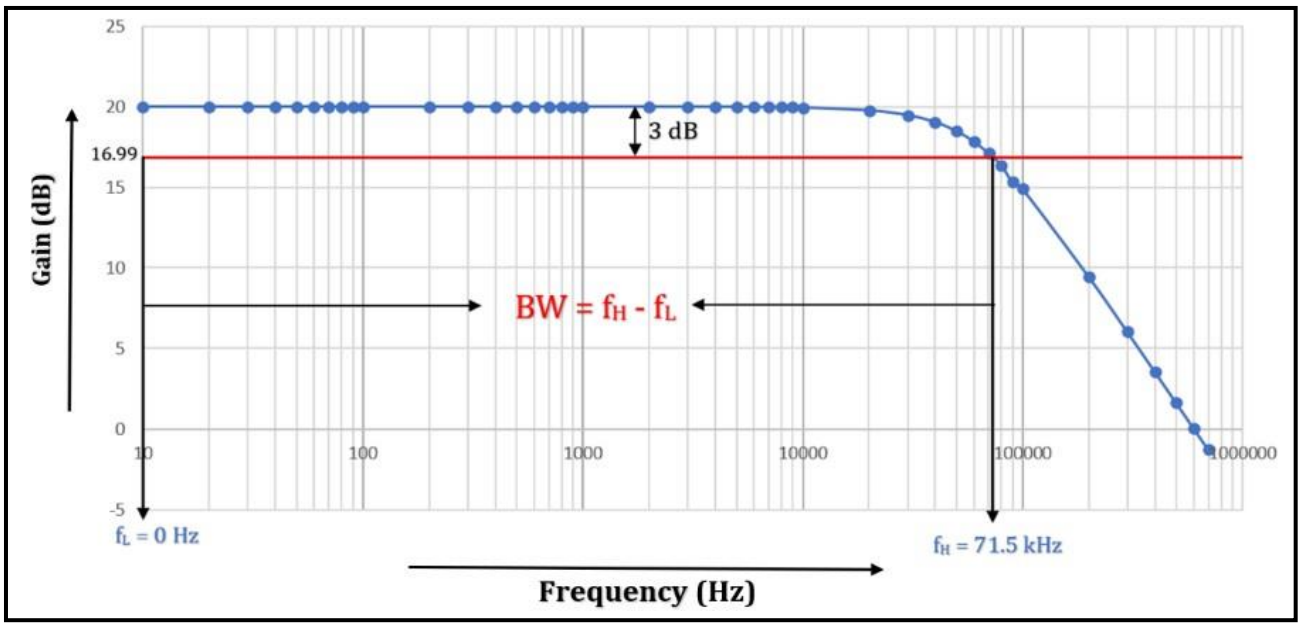
OBSERVATION:

- Input Voltage (fixed) = 100mV
- Case 1 :
  When R_1 = 47kΩ

Frequency (Hz)	**Output Voltage** (V_{out}) (Milli Volt)	**Voltage Gain** (V_{out}/V_{in})	**Gain** **[20 $\log_{10}(V_{out}/V_{in})$]** (dB)
10 Hz	999.932 mV	9.999	19.999 dB
20 Hz	999.932 mV	9.999	19.999 dB
30 Hz	999.932 mV	9.999	19.999 dB
40 Hz	999.931 mV	9.999	19.999 dB
50 Hz	999.931 mV	9.999	19.999 dB
60 Hz	999.931 mV	9.999	19.999 dB
70 Hz	999.930 mV	9.999	19.999 dB
80 Hz	999.928 mV	9.999	19.999 dB
90 Hz	999.941 mV	9.999	19.999 dB
100 Hz	999.939 mV	9.999	19.999 dB
200 Hz	999.930 mV	9.999	19.999 dB
300 Hz	999.925 mV	9.999	19.999 dB
400 Hz	999.919 mV	9.999	19.999 dB
500 Hz	999.913 mV	9.999	19.999 dB
600 Hz	999.904 mV	9.999	19.999 dB
700 Hz	999.910 mV	9.999	19.999 dB
800 Hz	999.900 mV	9.999	19.999 dB
900 Hz	999.889 mV	9.998	19.998 dB
1000 Hz	999.876 mV	9.998	19.998 dB
2000 Hz	999.665 mV	9.996	19.996 dB
3000 Hz	999.350 mV	9.993	19.993 dB
4000 Hz	998.888 mV	9.988	19.989 dB
5000 Hz	998.281 mV	9.982	19.984 dB
6000 Hz	997.557 mV	9.975	19.978 dB
7000 Hz	996.703 mV	9.967	19.971 dB
8000 Hz	995.714 mV	9.957	19.962 dB
9000 Hz	994.593 mV	9.945	19.952 dB
10k Hz	993.341 mV	9.933	19.941 dB
20k Hz	973.585 mV	9.735	19.766 dB
30k Hz	940.759 mV	9.407	19.469 dB
40k Hz	895.621 mV	8.956	19.042 dB
50k Hz	840.621 mV	8.403	18.488 dB

60k Hz	779.052 mV	7.790	17.830 dB
70k Hz	716.820 mV	7.168	17.107 dB
80k Hz	657.620 mV	6.576	16.359 dB
90k Hz	603.702 mV	6.037	15.616 dB
100k Hz	555.710 mV	5.557	14.896 dB
200k Hz	296.790 mV	2.967	9.446 dB
300k Hz	200.002 mV	2.000	6.020 dB
400k Hz	150.550 mV	1.505	3.550 dB
500k Hz	120.645 mV	1.206	1.626 dB
600k Hz	100.634 mV	1.006	0.052 dB
700k Hz	86.307 mV	0.863	-1.279 dB

GRAPH:



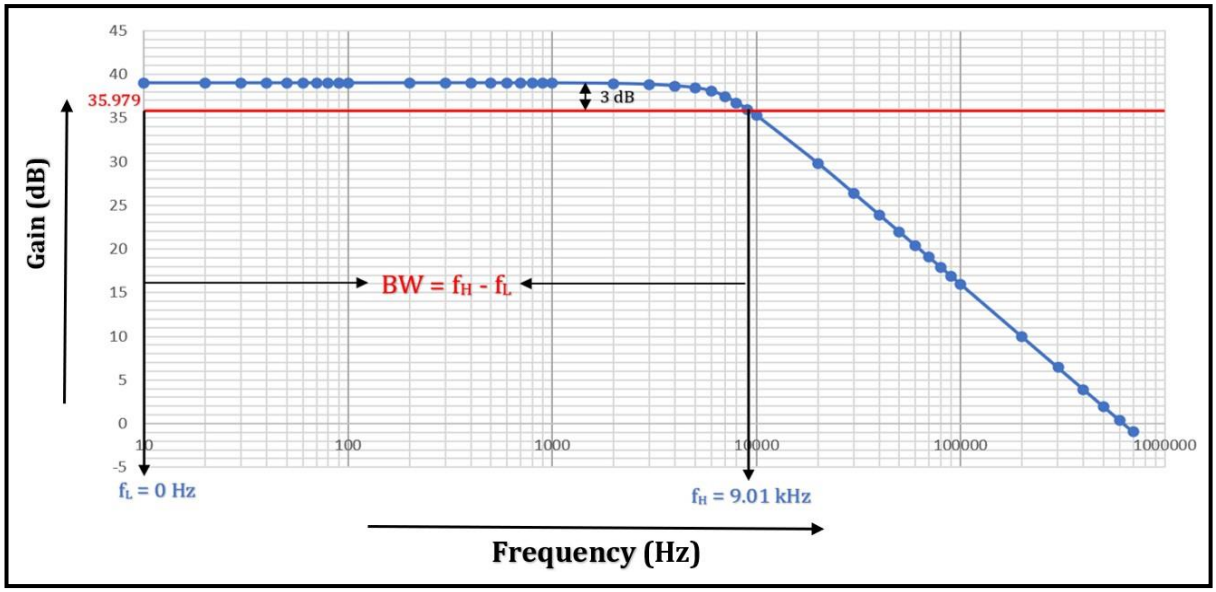
(Frequency Response of Inverting Amplifier for R_1 = 47kΩ)

- Case 2 :
  When R_1 = 4.7kΩ

Frequency (Hz)	**Output Voltage** (V_{out}) (Milli Volt)	**Voltage Gain** (V_{out}/V_{in})	**Gain** **[20 $\log_{10}(V_{out}/V_{in})$]** (dB)
10 Hz	8891 mV	88.91	38.979 dB
20 Hz	8891 mV	88.91	38.979 dB
30 Hz	8891 mV	88.91	38.979 dB
40 Hz	8891 mV	88.91	38.979 dB
50 Hz	8891 mV	88.91	38.979 dB
60 Hz	8892 mV	88.92	38.979 dB

70 Hz	8892 mV	88.92	38.979 dB
80 Hz	8893 mV	88.93	38.980 dB
90 Hz	8893 mV	88.93	38.980 dB
100 Hz	8893 mV	88.93	38.980 dB
200 Hz	8895 mV	88.95	38.982 dB
300 Hz	8897 mV	88.97	38.984 dB
400 Hz	8900 mV	89.00	38.987 dB
500 Hz	8898 mV	88.98	38.985 dB
600 Hz	8896 mV	88.96	38.983 dB
700 Hz	8894 mV	88.94	38.981 dB
800 Hz	8892 mV	88.92	38.979 dB
900 Hz	8890 mV	88.90	38.978 dB
1000 Hz	8887 mV	88.87	38.975 dB
2000 Hz	8830 mV	88.30	38.919 dB
3000 Hz	8718 mV	87.18	38.808 dB
4000 Hz	8557 mV	85.57	38.646 dB
5000 Hz	8347 mV	83.47	38.430 dB
6000 Hz	8023 mV	80.23	38.086 dB
7000 Hz	7457 mV	74.57	37.451 dB
8000 Hz	6857 mV	68.57	36.722 dB
9000 Hz	6300 mV	63.00	35.986 dB
10k Hz	5800 mV	58.00	35.268 dB
20k Hz	3088 mV	30.88	29.793 dB
30k Hz	2078 mV	20.78	26.352 dB
40k Hz	1564 mV	15.64	23.884 dB
50k Hz	1253 mV	12.53	21.959 dB
60k Hz	1045 mV	10.45	20.382 dB
70k Hz	896.181 mV	8.961	19.047 dB
80k Hz	784.400 mV	7.844	17.890 dB
90k Hz	697.367 mV	6.973	16.868 dB
100k Hz	627.722 mV	6.277	15.955 dB
200k Hz	314.012 mV	3.140	9.938 dB
300k Hz	209.373 mV	2.093	6.415 dB
400k Hz	157.039 mV	1.570	3.917 dB
500k Hz	125.634 mV	1.256	1.979 dB
600k Hz	104.700 mV	1.047	0.398 dB
700k Hz	89.746 mV	0.897	-0.944 dB

GRAPH:



(Frequency Response of Inverting Amplifier for R_1 = 4.7kΩ)

RESULT:

➢ Case 1 :
When R_1 = 47kΩ

- Maximum Gain = 19.999 dB
- 3 dB Gain = 16.999 dB
- Max voltage Gain = 9.999
- 3 dB Lower Cut Off Frequency (f_L) = 0 Hz
- 3 dB Higher Cut Off Frequency (f_H) = 71.5 kHz
- 3 dB Bandwidth (BW) = $f_H - f_L$ = 71.5 kHz
- Gain Bandwidth Product = Bandwidth X Maximum Gain = 19.999 * 71.5 kHz = 1429.928 kHz

➢ Case 2:
When R_1 = 4.7kΩ

- Maximum Gain = 38.979 dB
- 3 dB Gain = 35.979 dB
- Max voltage Gain = 88.91
- 3 dB Lower Cut Off Frequency (f_L) = 0 Hz
- 3 dB Higher Cut Off Frequency (f_H) = 9.01 kHz
- 3 dB Bandwidth (BW) = $f_H - f_L$ = 9.01 kHz
- Gain Bandwidth Product = Bandwidth X Maximum Gain = 38.979 * 9.01 kHz = 351.200 kHz

CONCLUSION:

We were able to design inverting amplifier using IC 741 OP-AMP. From this experiment we can understand that the frequency response of any given circuit is the variation in its behaviour with changes in the input signal frequency as it shows the band of frequencies over which the output (and the gain) remains fairly constant. The range of frequencies either big or small between f_L and f_H is called the circuits bandwidth. So, from this we are able to determine at a glance the voltage gain (in dB) for any sinusoidal input within a given frequency range.

AIM(B): Design of Non-Inverting Amplifier Using IC 741 OP – AMP and Finding its Frequency Response

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- Power Supply
- AC Milli Voltmeter
- Function Generator

CIRCUIT COMPONENTS:

- IC 741
- Resistance = 47KΩ , 470KΩ

THEORY:

- Non-Inverting Operational Amplifier:

It is called as Non-Inverting Amplifier because input is applied at pin no.3 i.e., non-inverting input. So, we get output-signal in phase with input signal. In this case the input-signal is applied directly to the non-inverting (+ve) input-terminal of the amplifier & the feedback resistor 'R_2=R_f' is connected between the output-terminal & negative input-terminal. The 'R_1' is connected between the inverting terminal & ground. Note that Vin is not equal to zero in this case, meaning that non-inverting circuit has to virtual ground at one of its input-terminals. Thus, the closed loop gain of a non-inverting amplifier is always greater than or equal to unity & it is determined by R_1 & R_f.

- Voltage Gain:

If we assume that we are not at saturation, the potential at point X is the same as Vin. Since the input impedance of OP-AMP is very high, all of the current that flows through R_2, also flows through R1. Thus, we have,

Voltage across R_1 = Vin – 0
Voltage across R_2 = Vout - Vin

Now, current through R_1 = Current Through R_2

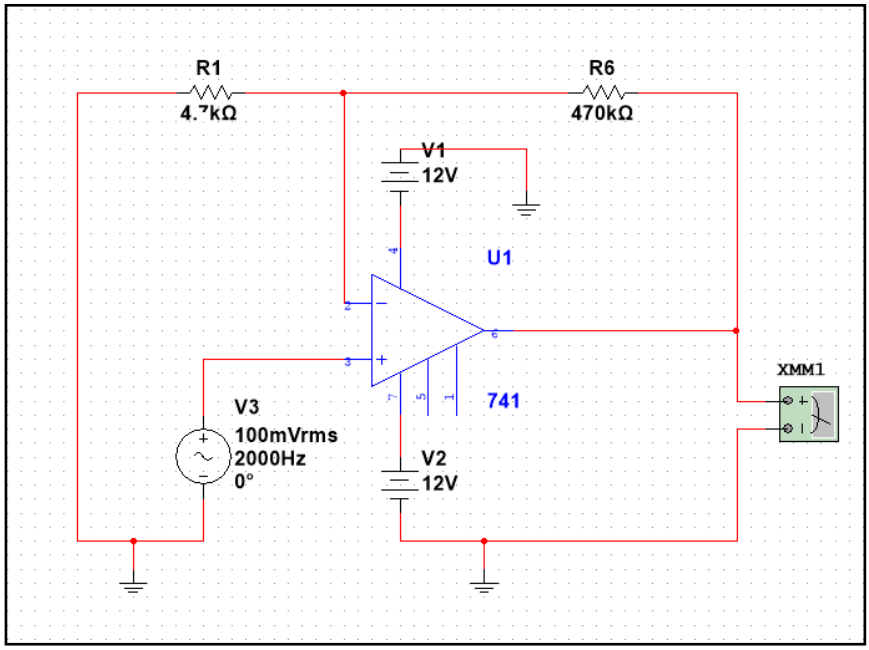
$$\therefore \quad \frac{V_{in} - 0}{R1} = \frac{V_{out} - V_{in}}{R2}$$

$$\Rightarrow \quad V_{in}.R2 = V_{out}.R1 - V_{in}.R1$$

Thus, the Closed-loop voltage-gain $A_{CL} = \frac{V_{out}}{V_{in}} = \frac{R2 + R1}{R1} = 1 + \frac{R2}{R1}$

Feedback control of the non-inverting operational amplifier is achieved by applying a small part of the output voltage signal back to the inverting (–) input terminal via a R_2 –R_1 voltage divider network, again producing negative feedback. This closed-loop configuration produces a non-inverting amplifier circuit with very good stability, a very high input impedance, Rin approaching infinity, as no current flows into the positive input terminal, (ideal conditions) and a low output impedance, Rout.

EXPERIMENTAL SETUP:



(Circuit diagram for Non-Inverting Amplifier using IC – 741 OP - AMP)

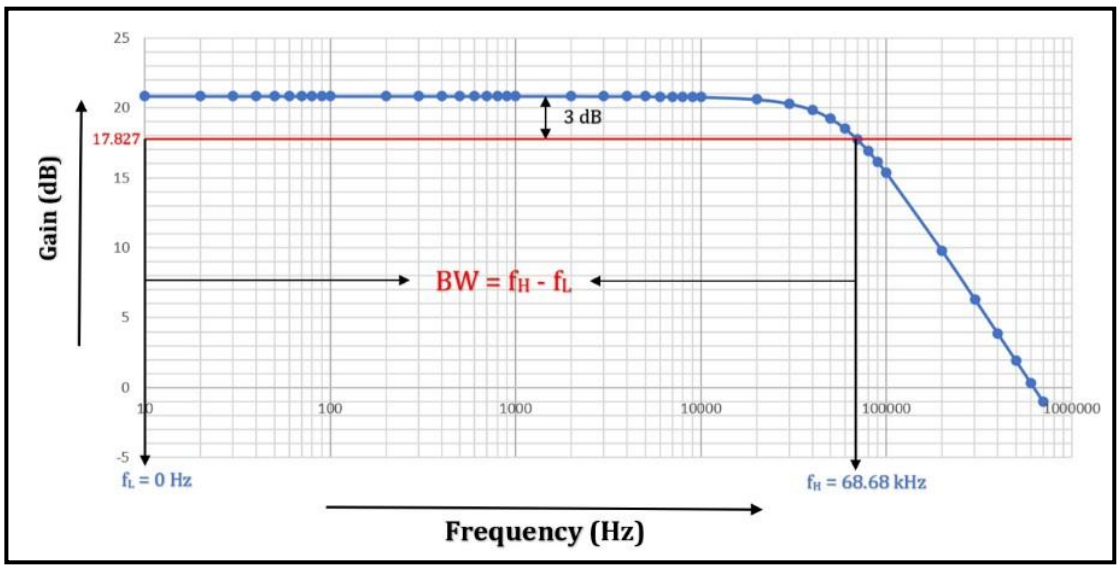
OBSERVATION:

- Input Voltage (fixed) = 100mV

Frequency (Hz)	**Output Voltage** (V_{out}) (Milli Volt)	**Voltage Gain** (V_{out}/V_{in})	**Gain** **[20 $\log_{10}(V_{out}/V_{in})$]** (dB)
10 Hz	1100 mV	11	20.827 dB
20 Hz	1100 mV	11	20.827 dB
30 Hz	1100 mV	11	20.827 dB
40 Hz	1100 mV	11	20.827 dB
50 Hz	1100 mV	11	20.827 dB
60 Hz	1100 mV	11	20.827 dB
70 Hz	1100 mV	11	20.827 dB
80 Hz	1100 mV	11	20.827 dB
90 Hz	1100 mV	11	20.827 dB
100 Hz	1100 mV	11	20.827 dB
200 Hz	1100 mV	11	20.827 dB
300 Hz	1100 mV	11	20.827 dB
400 Hz	1100 mV	11	20.827 dB
500 Hz	1100 mV	11	20.827 dB
600 Hz	1100 mV	11	20.827 dB
700 Hz	1100 mV	11	20.827 dB
800 Hz	1100 mV	11	20.827 dB

900 Hz	1100 mV	11	20.827 dB
1000 Hz	1100 mV	11	20.827 dB
2000 Hz	1100 mV	11	20.827 dB
3000 Hz	1099 mV	10.99	20.819 dB
4000 Hz	1099 mV	10.99	20.819 dB
5000 Hz	1098 mV	10.98	20.812 dB
6000 Hz	1097 mV	10.97	20.804 dB
7000 Hz	1096 mV	10.96	20.796 dB
8000 Hz	1095 mV	10.95	20.788 dB
9000 Hz	1094 mV	10.94	20.780 dB
10k Hz	1093 mV	10.93	20.772 dB
20k Hz	1071 mV	10.71	20.595 dB
30k Hz	1034 mV	10.34	20.290 dB
40k Hz	981.188 mV	9.811	19.835 dB
50k Hz	915.681 mV	9.156	19.234 dB
60k Hz	842.622 mV	8.426	18.512 dB
70k Hz	769.146 mV	7.691	17.720 dB
80k Hz	700.612 mV	7.006	16.909 dB
90k Hz	639.430 mV	6.394	16.115 dB
100k Hz	585.946 mV	5.859	15.357 dB
200k Hz	308.180 mV	3.081	9.776 dB
300k Hz	207.107 mV	2.071	6.323 dB
400k Hz	155.754 mV	1.557	3.848 dB
500k Hz	124.761 mV	1.247	1.921 dB
600k Hz	104.040 mV	1.040	0.344 dB
700k Hz	89.221 mV	0.892	-0.990 dB

GRAPH:



(Frequency Response of Non-Inverting Amplifier)

RESULT:

- Maximum Gain = 20.827 dB
- 3 dB Gain = 17.827 dB
- Max voltage Gain = 11
- 3 dB Lower Cut Off Frequency (f_L) = 0 Hz
- 3 dB Higher Cut Off Frequency (f_H) = 68.68 kHz
- 3 dB Bandwidth (BW) = $f_H - f_L$ = 68.68 kHz
- Gain Bandwidth Product = Bandwidth X Maximum Gain = 20.827 * 68.68 kHz = 1430.398 kHz

CONCLUSION:

We were able to design non-inverting amplifier using IC 741 OP-AMP. From this experiment we can understand that the frequency response of any given circuit is the variation in its behaviour with changes in the input signal frequency as it shows the band of frequencies over which the output (and the gain) remains fairly constant. The range of frequencies either big or small between f_L and f_H is called the circuits bandwidth. So, from this we are able to determine at a glance the voltage gain (in dB) for any sinusoidal input within a given frequency range.

Reference Links: https://youtu.be/ImTzh3kgnvA

EXPERIMENT – 9

AIM: Realization of Basic Logic Gates (AND, OR, NOT) Using NAND Gate (IC 7400)

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- DC Power Supply

CIRCUIT COMPONENTS:

- IC 7400

THEORY:

The NAND gate is said to be a universal gate because any all-other gates as well as any digital system can be implemented with it. Combinational circuits and sequential circuits as well can be constructed with this gate because the flip-flop circuit can be constructed from two NAND gates connected back-to-back.

The NAND (Not–AND) gate has an output that is normally at logic level "1" and only goes "LOW" to logic level "0" when all of its inputs are at logic level "1". The Logic NAND Gate is the reverse or "Complementary" form of the AND gate. The logic or Boolean expression given for a logic NAND gate is that for Logical Addition, which is the opposite to the AND gate, and which it performs on the complements of the inputs. The Boolean expression for a logic NAND gate is denoted by a single dot or full stop symbol, (.) with a line or Overline, (¯) over the expression to signify the NOT or logical negation of the NAND gate giving us the Boolean expression of: A . B = Q.

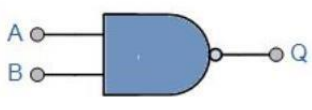
Then we can define the operation of a 2-input digital logic NAND gate as being:

"If either A or B are NOT true, then Q is true"

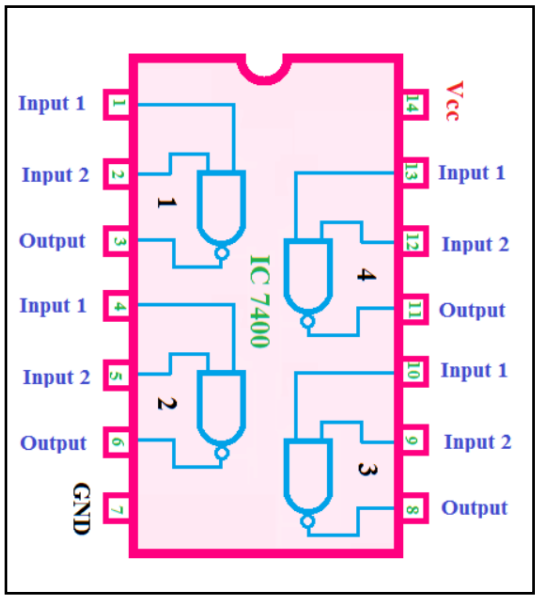
Logic NAND Gates are available using digital circuits to produce the desired logical function and is given a symbol whose shape is that of a standard AND gate with a circle, sometimes called an "inversion bubble" at its output to represent the NOT gate symbol with the logical operation of the NAND gate given as.

The implementation of the AND, OR, and NOT operation with NAND gate is shown in Fig. The NOT operation is obtained from a one-input NAND gate. The AND operation requires two NAND gates. The first produces the inverted AND and the second acts as an inverter to produce the normal output. The OR operation is achieved through a NAND gate with additional inverters in each input.

- 2-Input Logic NAND Gate

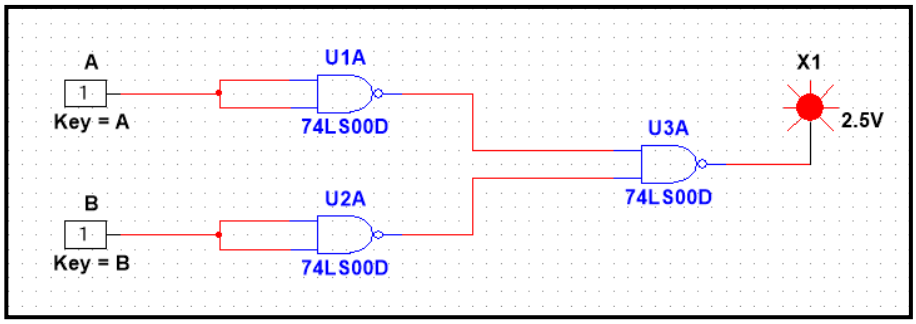
Symbol	Truth Table		
 2-input NAND Gate	B	A	Q
	0	0	1
	0	1	1
	1	0	1
	1	1	0
Boolean Expression $Q = \overline{A.B}$	Read as A AND B gives NOT Q		

IC PIN DIAGRAM:

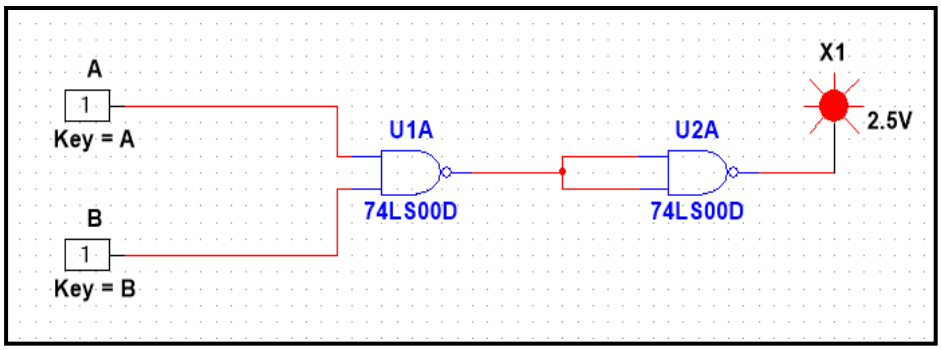


(IC 7400 Pin Diagram with Internal Gate Connections)

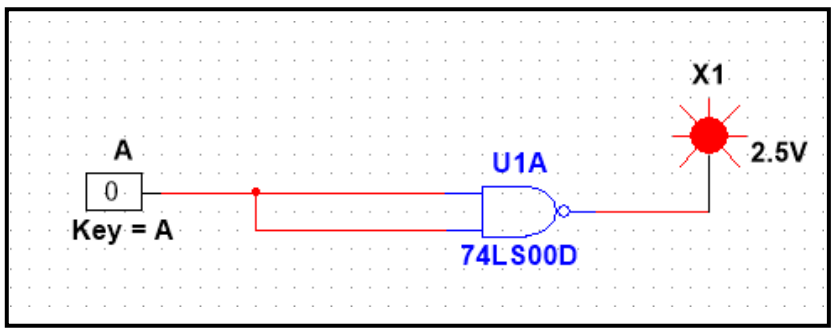
EXPERIMANETAL SETUP:



(OR GATE)



(AND GATE)



(NOT GATE)

OBSERVATION:

- Verifying Truth Table of AND Gate:

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

- Verifying Truth Table of OR Gate:

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

- Verifying Truth Table of NOT Gate:

INPUT	OUTPUT
A	Y
0	1
1	0

RESULT:

- For AND GATE:
  As it can be observed from the truth table, the output of the AND GATE is 1 only when both the inputs are 1. The output of other input is 0.

- For OR GATE:
  As it can be observed from the truth table, the output of the OR GATE is 0 only when both the inputs are 0. The output of other input is 1.

- For NOT GATE:
  As it can be observed from the truth table, the output of the NOT GATE is 0 when the input is 1 and the output is 1 when the input is 0.

CONCLUSION:

The results obtained from the experiment were found to be consistent with the theory.

Reference Links: https://youtu.be/fPxxv7qahY4

EXPERIMENT – 10

AIM: Implementation of The Boolean Expression F = (A.B.C + D.E) Using AND GATE (IC – 7408) And OR GATE (IC 7432)

SOFTWARE USED: NI Multisim 14.2 Software

APPARATUS REQUIRED:

- DC Power Supply

CIRCUIT COMPONENTS:

- IC 7408
- IC 7432

THEORY:

- AND Gate

The output state of a "Logic AND Gate" only returns "LOW" again when any of its inputs are at a logic level "0". In other word for a logic AND gate, any LOW input will give a LOW output. The logic or Boolean expression given for a digital logic AND gate is that for Logical Multiplication which is denoted by a single dot or full stop symbol, (.) giving us the Boolean expression of : A . B = Q .

Then we can define the operation of a 2-input logic AND gate as being:

"If both A and B are true, then Q is true"

Logic AND Gates are available using digital circuits to produce the desired logical function and is given a symbol whose shape represents the logical operation of the AND gate.

- The 2 – Input Logic AND Gate:

Symbol	Truth Table		
	B	A	Q
 2-input AND Gate	0	0	0
	0	1	0
	1	0	0
	1	1	1
Boolean Expression **Q = A.B**	Read as A **AND** B gives Q		

- OR Gate

The output, Q of a "Logic OR Gate" only returns "LOW" again when all of its inputs are at a logic level "0". In other word for a logic OR gate, any "HIGH" input will give a "HIGH", logic level "1" output.

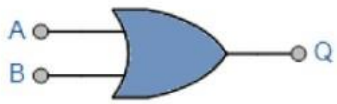
The logic or Boolean expression given for a digital logic OR gate is that for Logical Addition which is denoted by a plus sign, (+) giving us the Boolean expression of: A + B = Q .

Thus, a logic OR gate can be correctly described as an "Inclusive OR gate" because the output is true when both of its inputs are true (HIGH). Then we can define the operation of a 2-input logic OR gate as being:

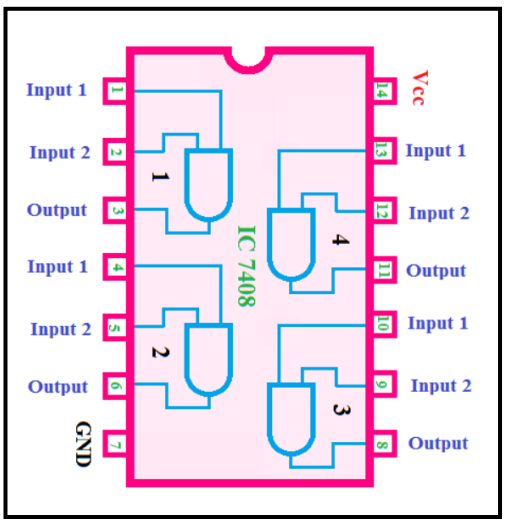
"If either A or B is true, then Q is true"

Logic OR Gates are available using digital circuits to produce the desired logical function and is given a symbol whose shape represents the logical operation of the OR gate.

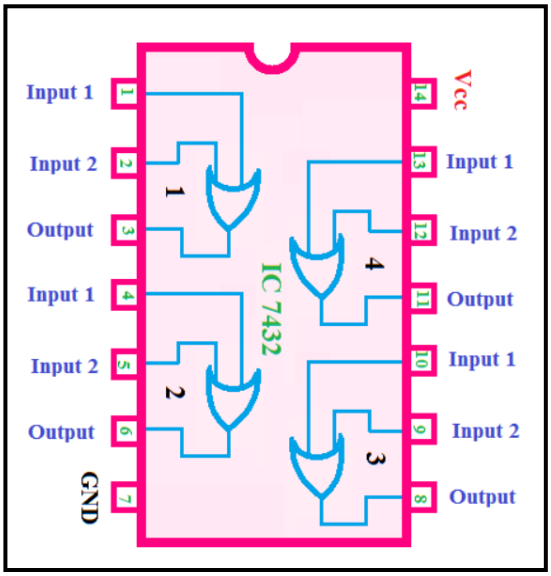
- The 2 – Input Logic OR Gate:

Symbol	Truth Table		
 2-input OR Gate	B	A	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	1
Boolean Expression **Q = A+B**	Read as A **OR** B gives Q		

IC PIN DIAGRAM:

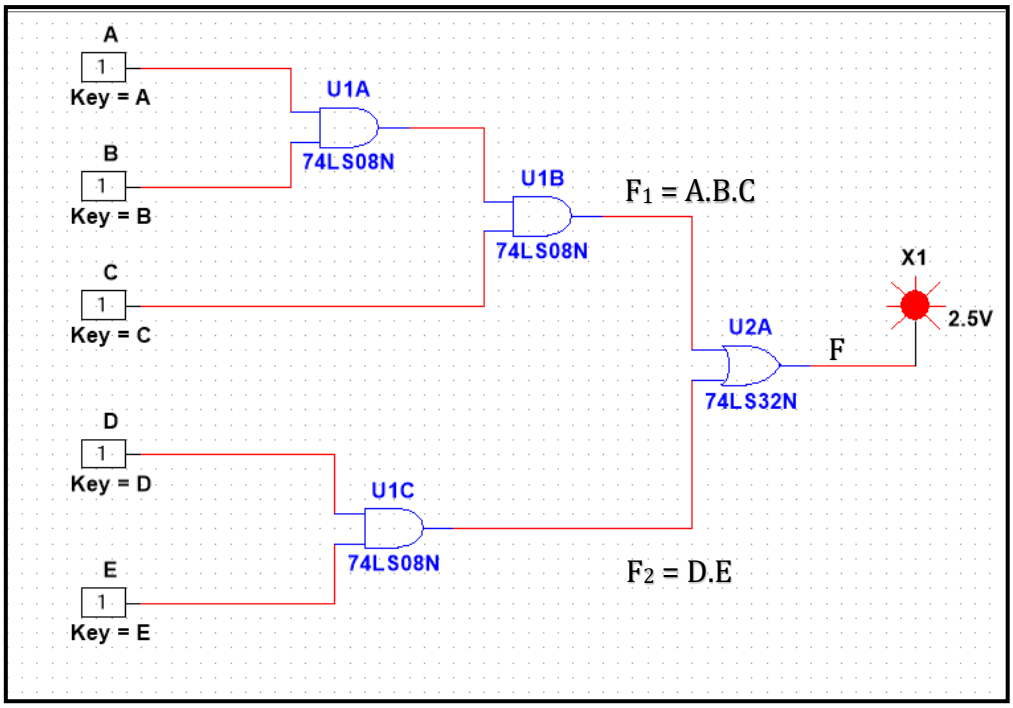


(IC 7408 Pin Diagram with Internal Gate Connections)



(IC 7432 Pin Diagram with Internal Gate Connections)

EXPERIMENTAL SETUP:



FUNCTION TABLE:

Inputs					Intermediate Functions		Final Output
A	B	C	D	E	F1 = A.B.C	F2 = D.E	F = A.B.C + D.E
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0
1	1	0	1	1	0	1	1
0	0	1	0	0	0	0	0
1	0	0	1	1	0	1	1
1	1	1	0	0	1	0	1
1	0	1	0	1	0	0	0
1	1	0	1	0	0	0	0
1	1	1	1	0	1	0	1
1	1	1	1	1	1	1	1

RESULT:

- For Function F_1 :

  As it can be observed from the truth table, the output of the AND GATE is 1 only when all the three inputs are 1. The output of other input is 0.

- For Function F_2 :

  As it can be observed from the truth table, the output of the AND GATE is 1 only when both the inputs are 1. The output of other input is 0.

- For Function F :

  As it can be observed from the truth table, the output of the OR GATE is 0 only when both the input of F_1 and F_2 are 0. The output of the other inputs is 1.

CONCLUSION:

The results obtained from the experiment were found to be consistent with the theory.

Reference Links: **https://youtu.be/uTnlOBETwxc**

https://youtu.be/BI6SoAjBazU

EXPERIMENT – 11

AIM: Generation of Amplitude Modulated Wave and Calculation of Percentage of Modulation Using The Standard Setup

SOFTWARE USED: Solid Thinking Embed 2017.2

THEORY:

Amplitude Modulation is defined as a process in which the amplitude of the carrier wave C(t) is varied linearly with the instantaneous amplitude of the message signal m(t).The standard form of an amplitude modulated (AM) wave is defined by;

$$S(t) = A_C[1 + K_a m(t)] \cos 2\pi f_C t$$

Where Ka is a constant called the amplitude sensitivity of the modulator.

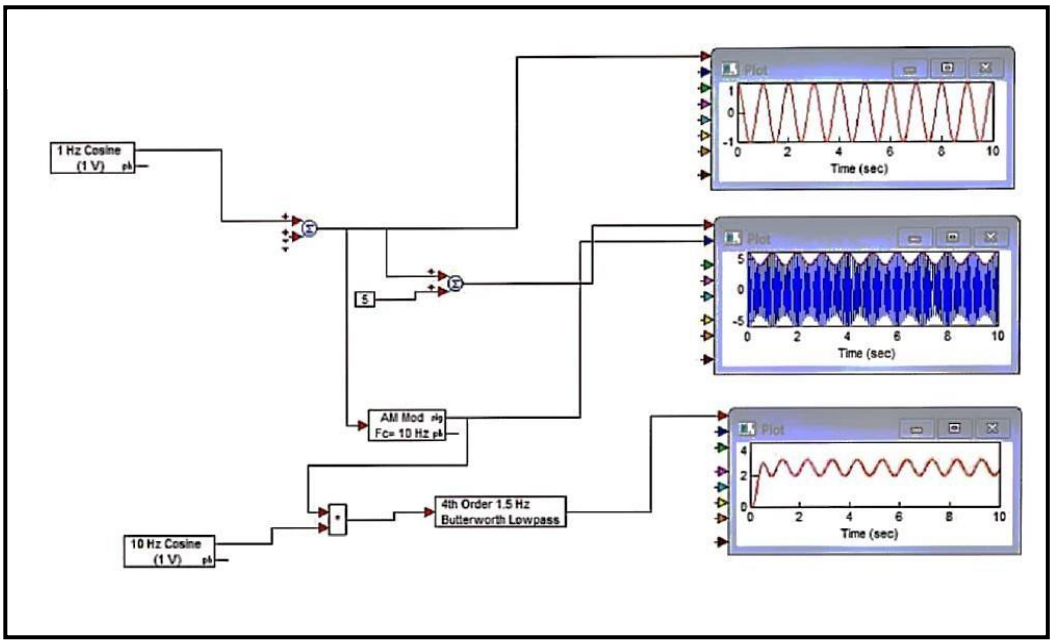
The demodulation circuit is used to recover the message signal from the incoming AM wave at the receiver. An envelope detector is a simple and yet highly effective device that is well suited for the demodulation of AM wave, for which the percentage modulation is less than 100%. Ideally, an envelope detector produces an output signal that follows the envelop of the input signal wave form exactly; hence, the name. Some version of this circuit is used in almost all commercial AM radio receivers.

The Modulation Index is defined as,

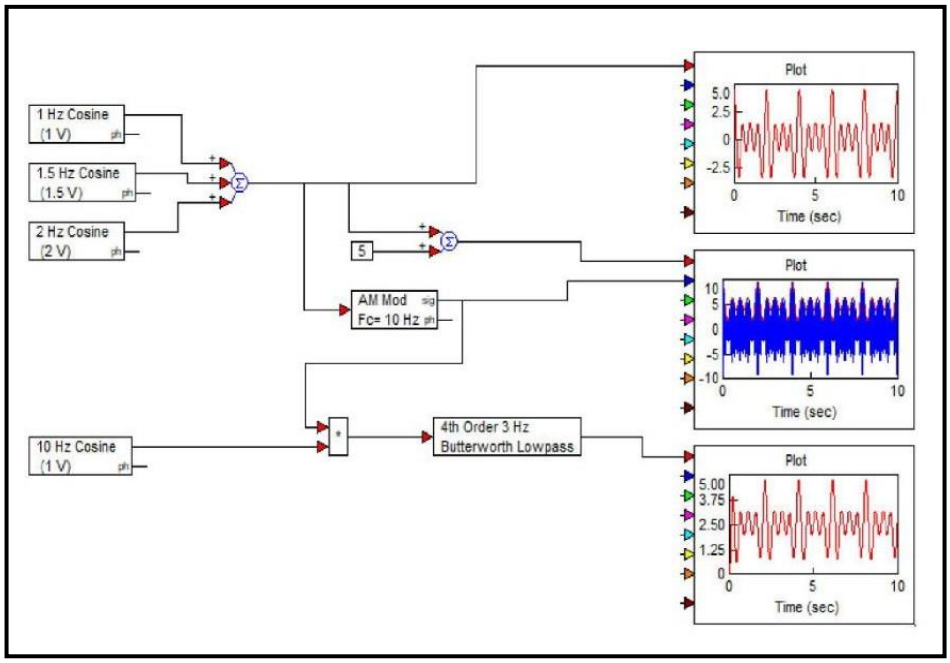
$$m = \frac{E_{max} - E_{min}}{E_{max} + E_{min}}$$

Where Emax and Emin are the maximum and minimum amplitudes of the modulated wave.

EXPERIMENTAL SETUP FOR SINGLE SIGNAL:



EXPERIMENTAL SETUP FOR MULTI TONE SIGNAL:

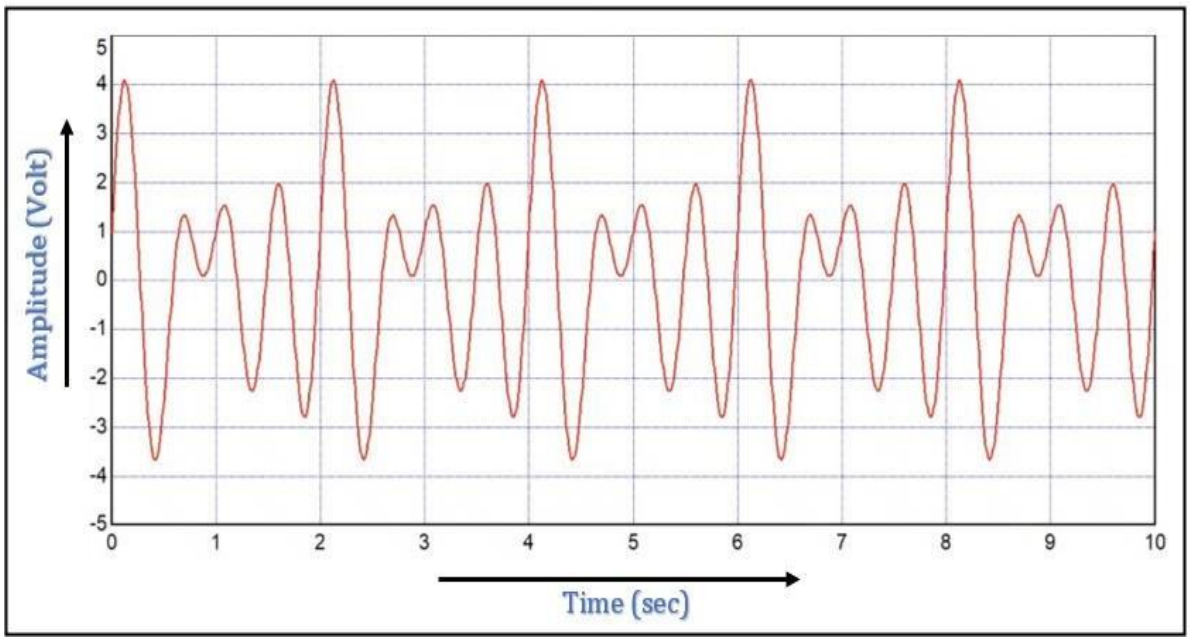


OBSERVATION:

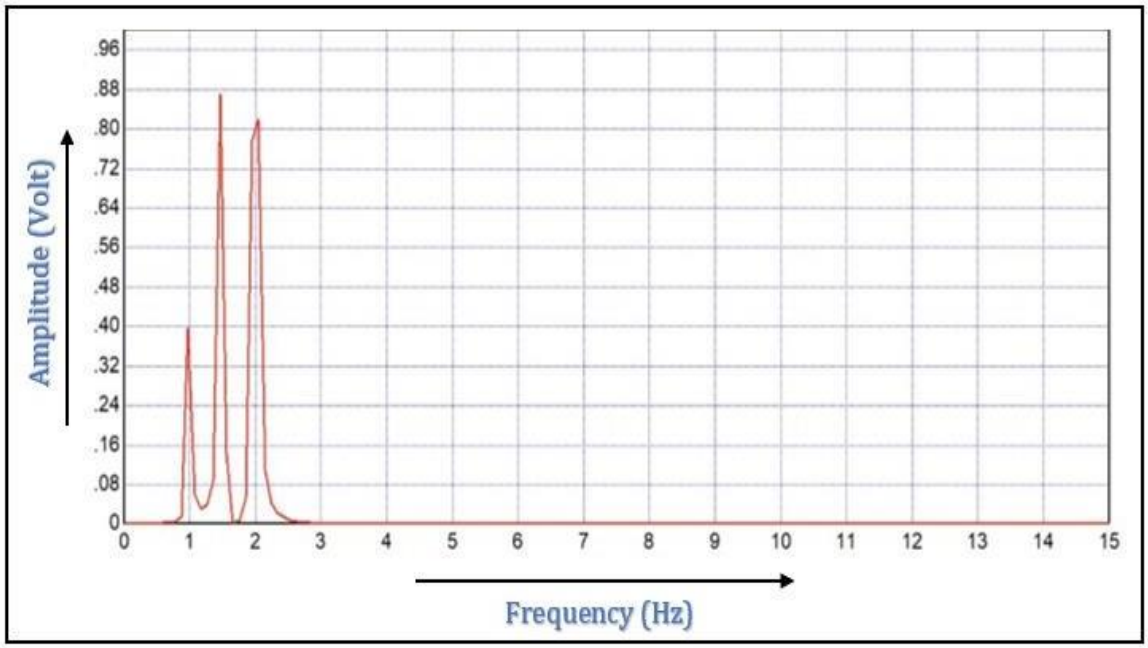
S No.	A_m (V)	Emax (V)	Emin (V)	Percentage of Modulation (m)
1.	1 Volt	4 Volt	2 Volt	33.33 %
2.	1.5 Volt	4.5 Volt	1.5 Volt	50 %
3.	2 Volt	5 Volt	1 Volt	66.66 %

GRAPH FOR MULTI TONE SIGNAL:

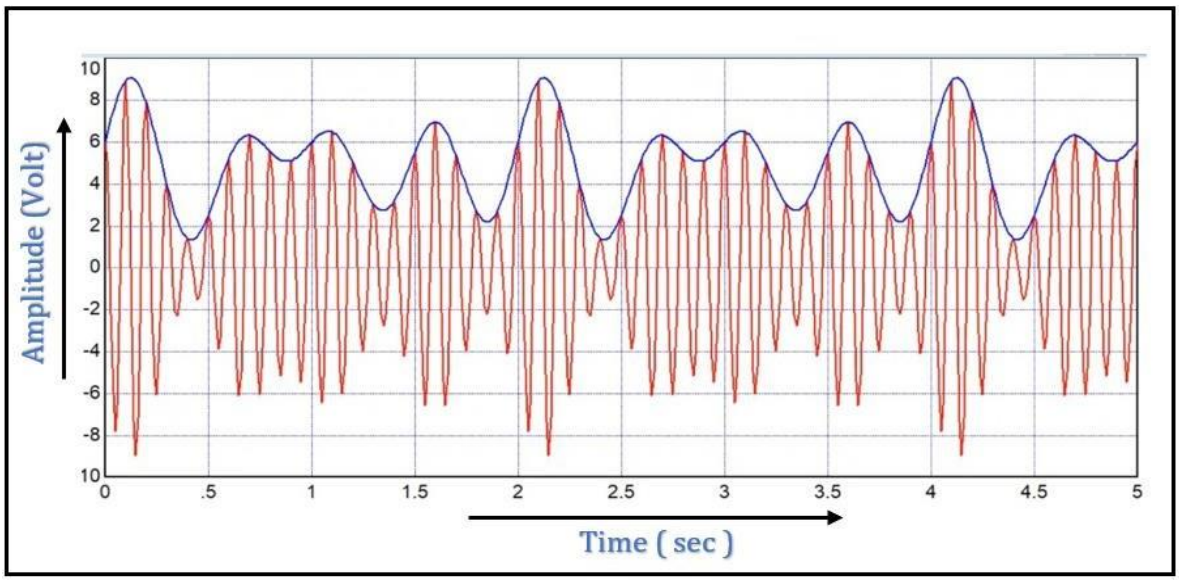
- Time Domain Message Signal



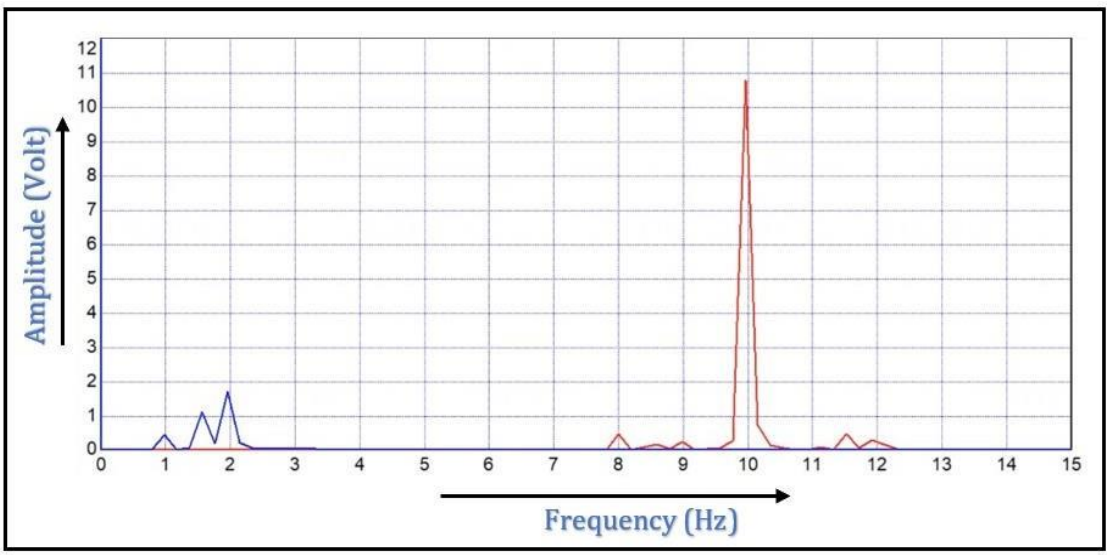
- Frequency Domain Message Signal



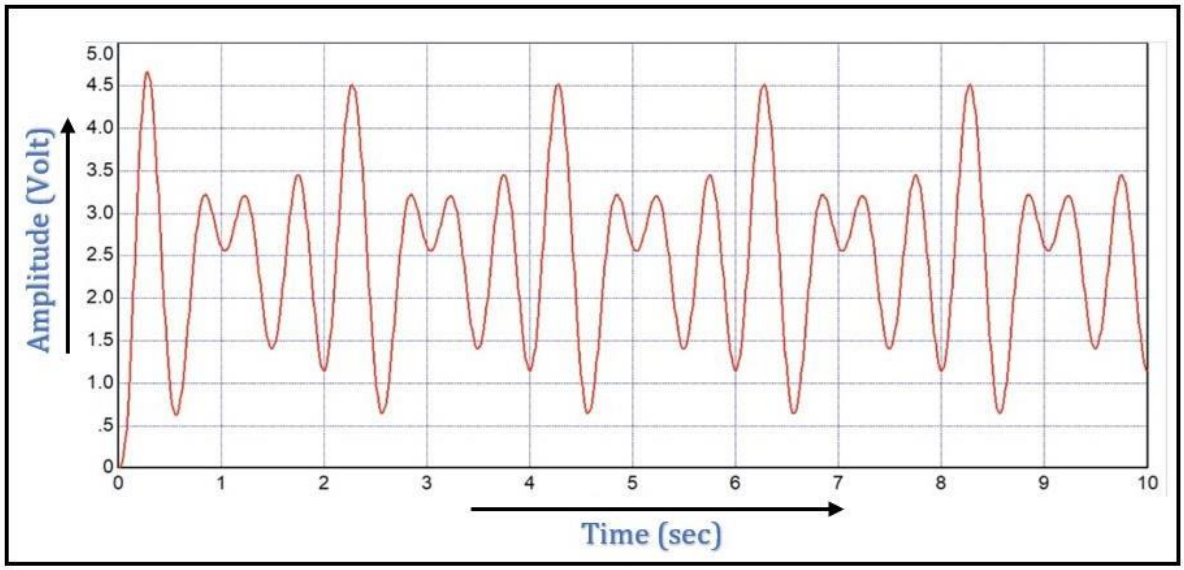
- Time Domain Modulated



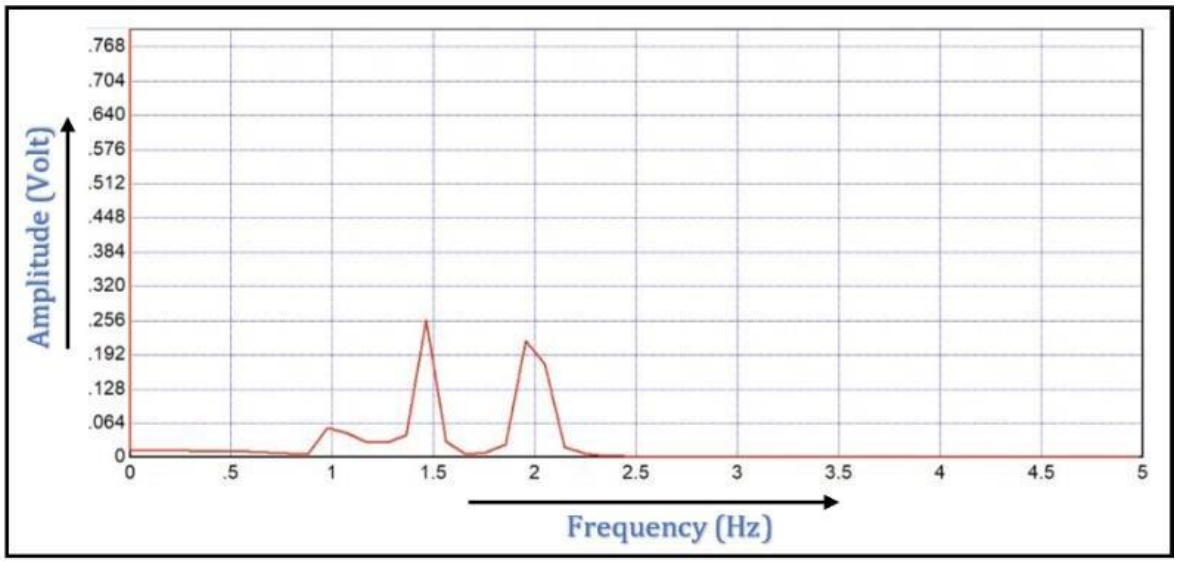
- Frequency Domain Modulated



- Time Domain Demodulated



- Frequency Domain Demodulated



RESULT:

- Percentage of Modulation
  1. For A_m = 1V, m = 33.33 %
  2. For A_m = 1.5V, m = 50%
  3. For A_m = 2V, m = 66.66%
- It can be observed that as the amplitude of the modulating signal is increased keeping the frequency and amplitude of carrier signal constant, the percentage of modulation increases.

CONCLUSION:

The results obtained from the experiment were found to be consistent with the theory.

Reference Links: https://youtu.be/sa3smGqnwEE

EXPERIMENT – 12

AIM: Generation of FM Wave and Its Detection Using Standard Setup

SOFTWARE USED: Solid Thinking Embed 2017.2

THEORY:

The process, in which the frequency of the carrier is varied in accordance with the instantaneous amplitude of the modulating signal, is called "Frequency Modulation". The FM signal is expressed as;

$$S(t) = A_C \cos[2\pi f_c t + \beta \sin(2\pi f_m t)]$$

Where A_C is amplitude of the carrier signal, f_C is the carrier frequency β is the modulation index of the FM wave. Where,

- Carrier signal, $C(t)=A_c \cos(2\pi f_c t)$
- Modulating signal, $m(t)= A_m \cos(2\pi f_m t)$

The instantaneous frequency of the resulting FM wave is,

$$\begin{aligned} f_i(t) &= f_c + K_f\, m(t) \\ &= f_c + K_f\, A_m \cos(2\pi f_m t) \\ &= f_c + \Delta f \cos(2\pi f_m t) \end{aligned}$$

Where, $\Delta f = K_f A_m$ = frequency deviation. It is the maximum departure of the instantaneous frequency of the FM wave from the carrier frequency f_c. A fundamental characteristic of FM wave is that the Δf is proportional to the amplitude of the modulating signal.

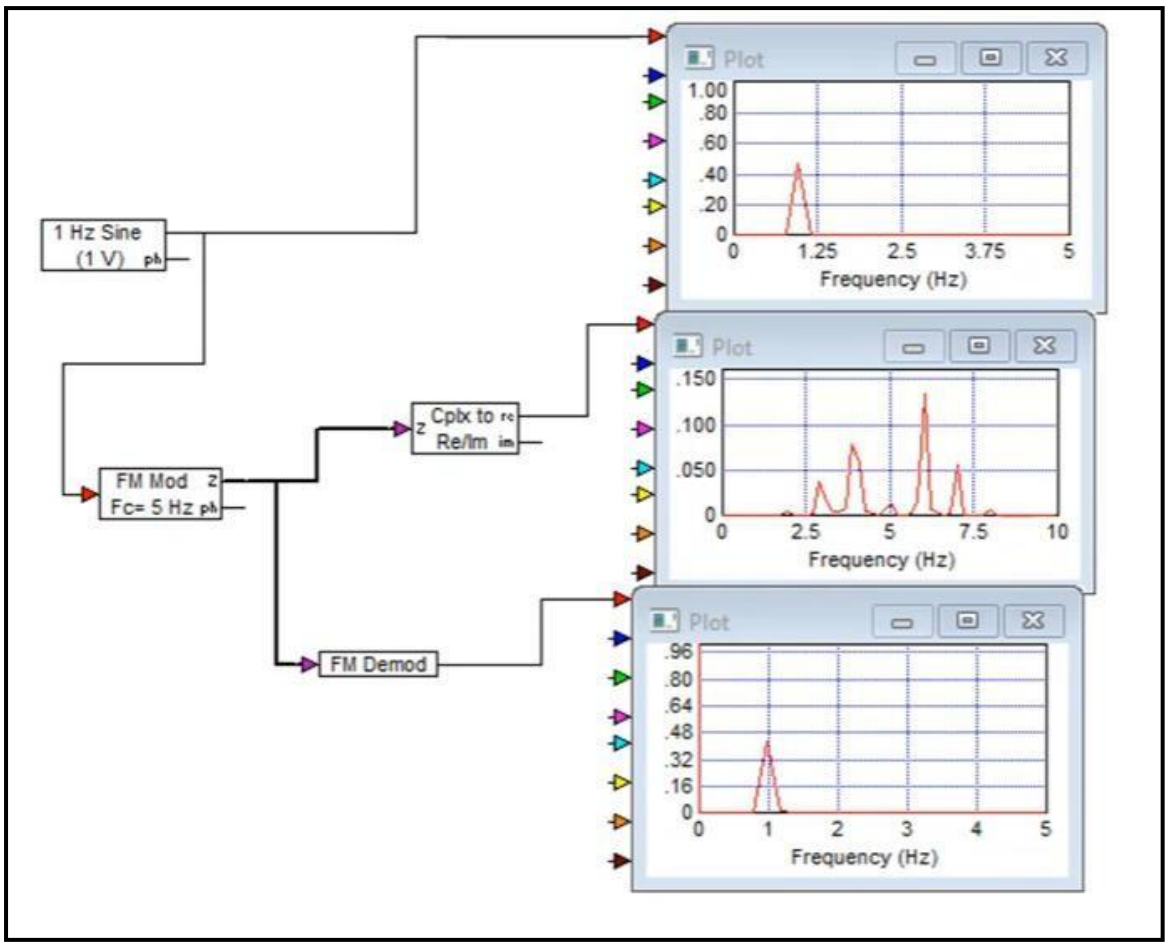
The constant term f_c represents the frequency of the unmodulated carrier; the constant K_f represents the frequency-sensitivity factor of the modulator, expressed in hertz per volt on the assumption that is a voltage waveform. Integrating Eq.-$f_i(t)$ with respect to time and multiplying the result by 2π we get-

$$\begin{aligned} \theta_i(t) &= 2\pi \int_0^t f_i(t).dt \\ &= 2\pi f_C t + 2\pi K_f \int_0^t m(t).dt \\ &= 2\pi f_C t + \frac{\Delta f}{f_m} \sin(2\pi f_m t) \\ &= 2\pi f_C t + \beta \sin(2\pi f_m t) \end{aligned}$$

The parameter β= modulation index $= \frac{\Delta f}{fm}$, represents the phase deviation of the FM wave that is the maximum departure of the angle $\theta_i(t)$ from the angle $2\pi f_c t$ of the unmodulated carrier. Depending on the β - value, there are two cases;

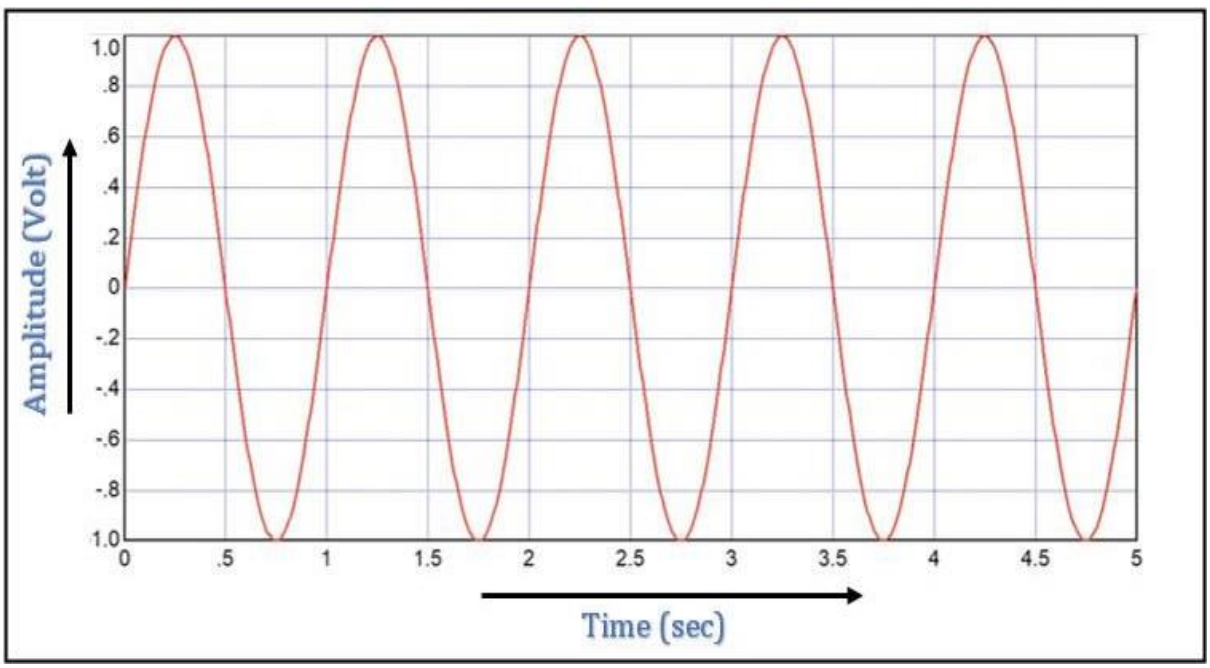
- Narrow-Band FM(for β very small value)
- Wide-Band FM(for β very large value)

EXPERIMENTAL SETUP:

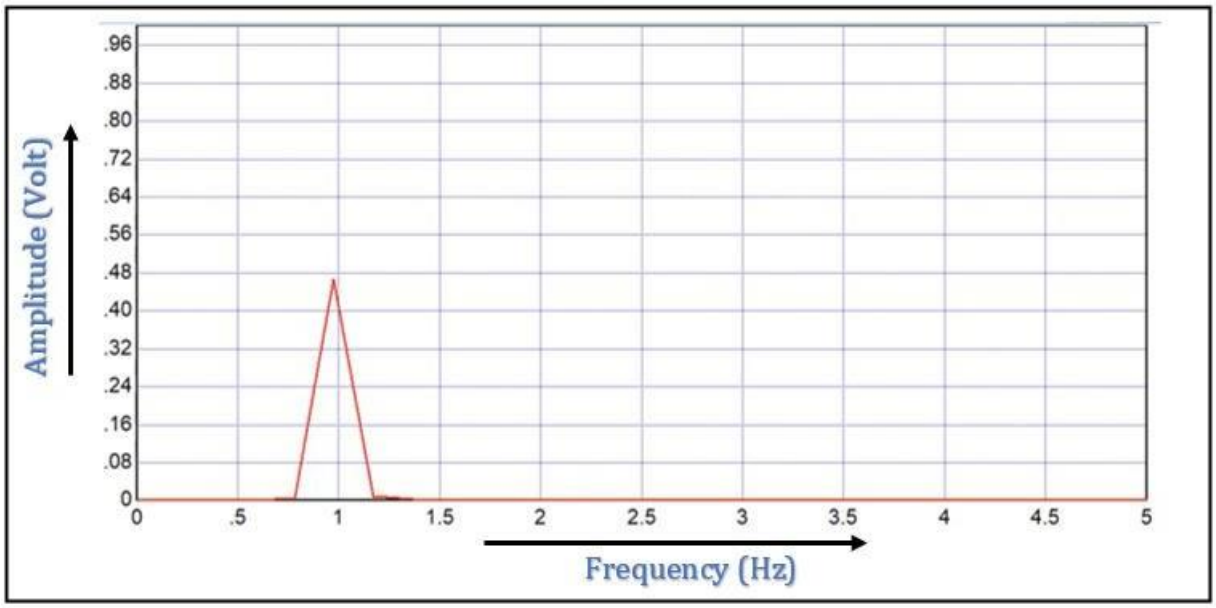


GRAPH:

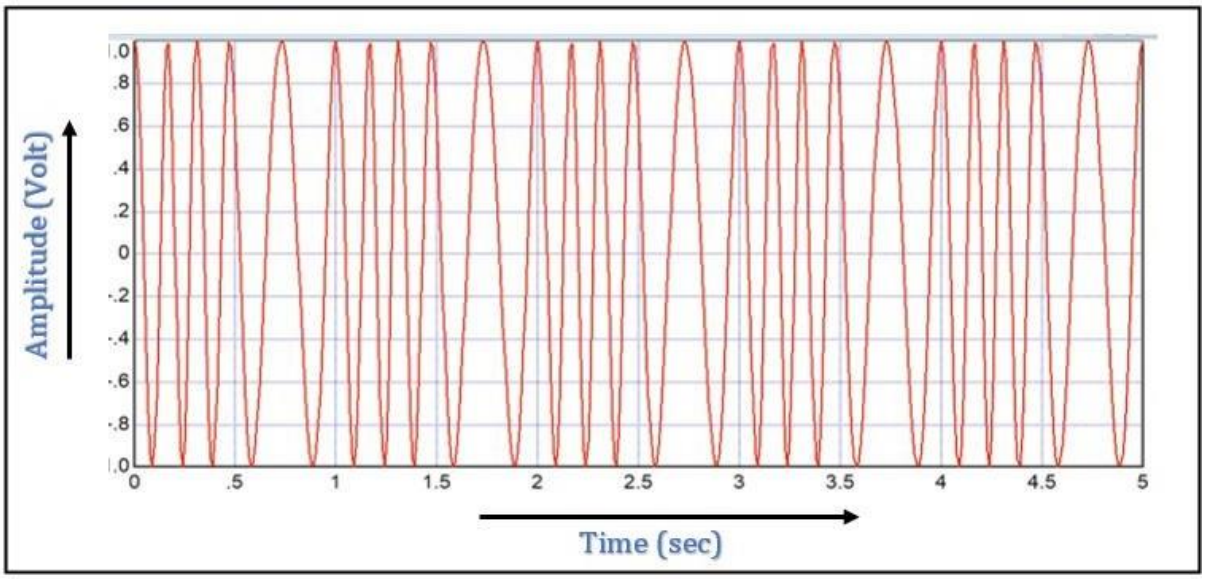
- Time Domain Message Signal



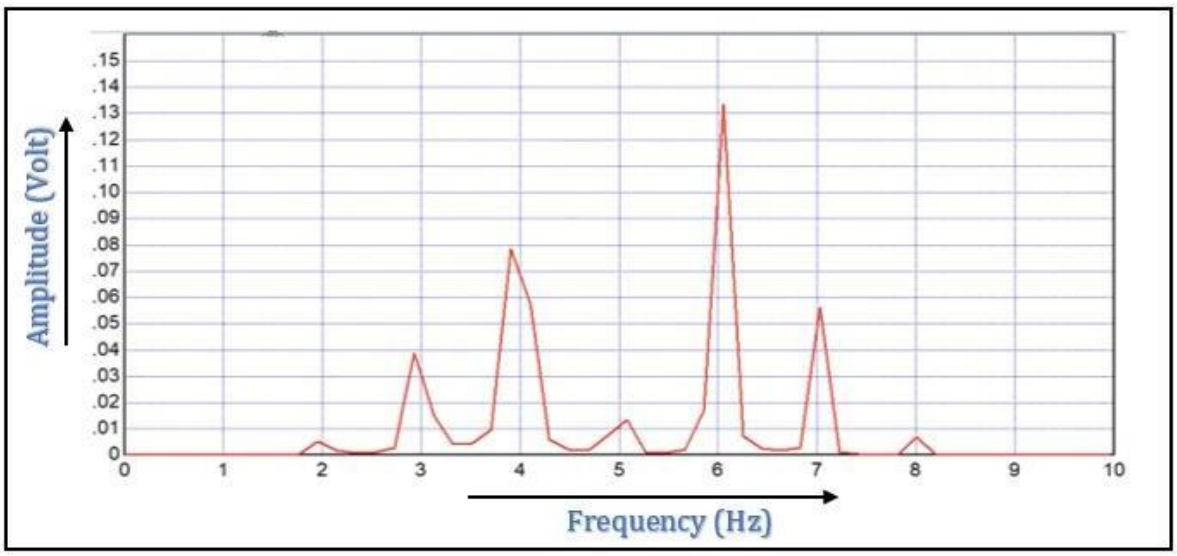
- Frequency Domain Message Signal



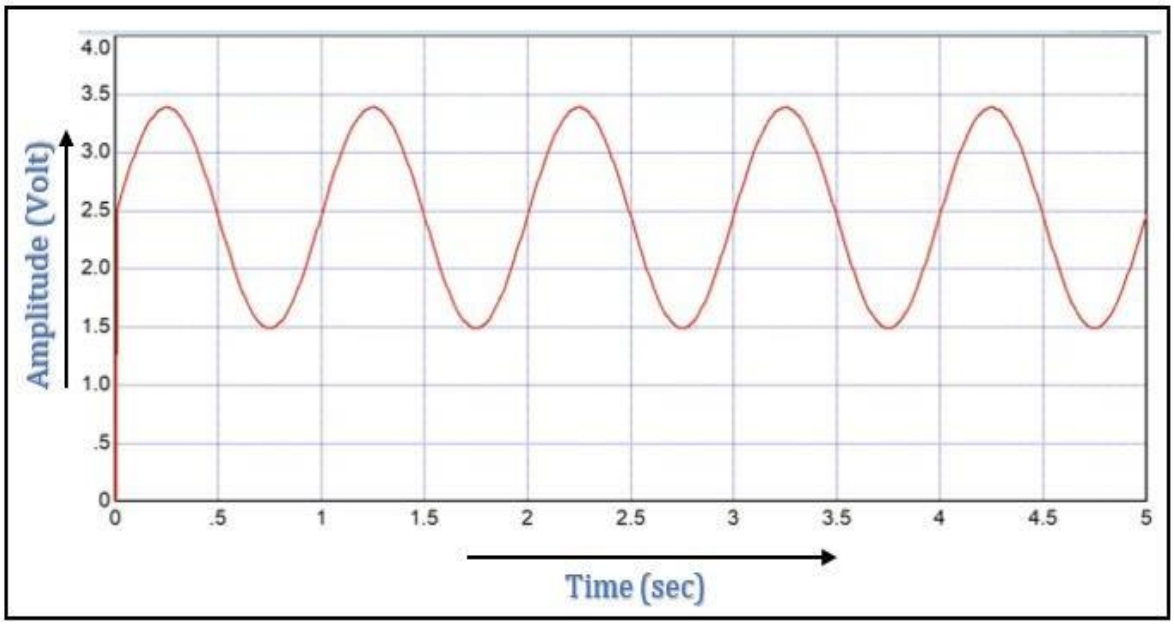
- Time Domain Modulated



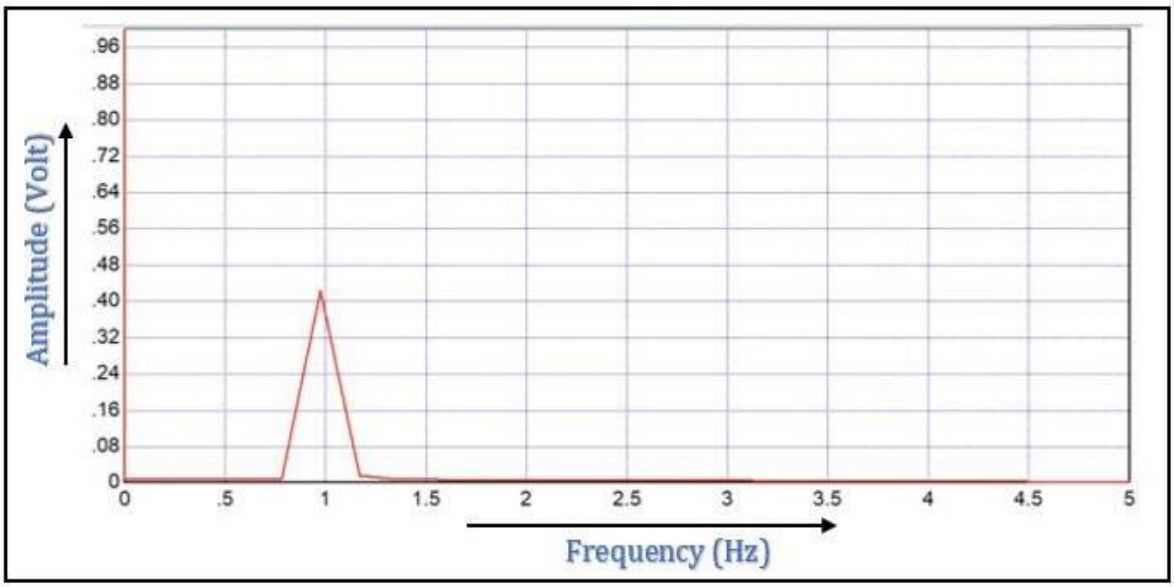
- Frequency Domain Modulated



- Time Domain Demodulated



- Frequency Domain Demodulated



RESULT:

- It can be observed from the graph that the frequency of the FM is less when the amplitude of the message signal is negative and the frequency of the FM is more when the amplitude of the message signal is positive i.e., the frequency of FM changes with time.

- The amplitude of FM remains constant with time.

CONCLUSION:

The results obtained from the experiment were found to be consistent with the theory.

Reference Links: **https://youtu.be/D5Se6hQdWQA**