

**DEPARTMENT
OF
ELECTRONICS AND COMMUNICATION ENGINEERING**



**BIRLA INSTITUTE OF TECHNOLOGY
MESRA RANCHI**

**EC254
ANALOG CIRCUITS LAB SESSIONAL RECORD**

**NAME: BHEEMREDDY PRAVEEN KUMAR REDDY
ROLL NO. : BTECH/10539/19
BRANCH : ECE - B (SEM - 4)
SESSION : 2020-21**

EXPERIMENT 1

NAME OF THE EXPERIMENT: Determine the h-parameters h_{ie} and h_{fe} of a transistor.

AIM: Design a CE Transistor circuit to evaluate the h_{ie} and h_{fe} .

SOFTWARE USED: NI Multisim 14.1

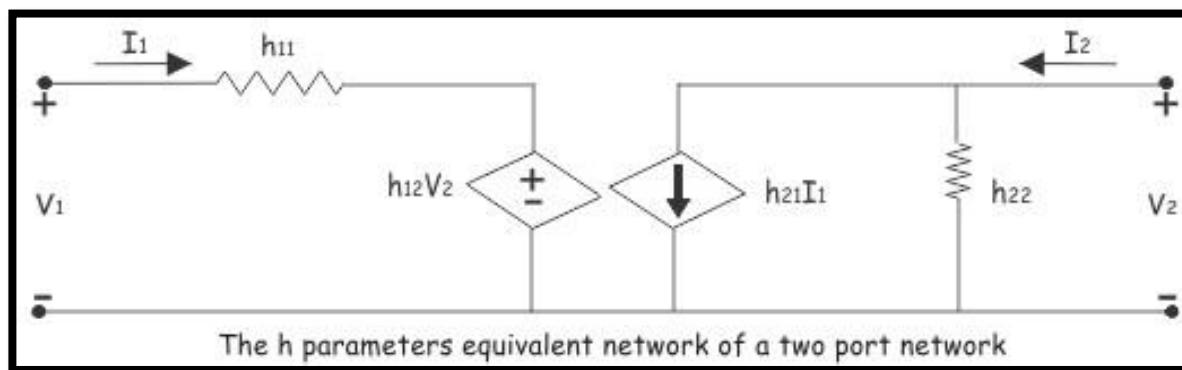
THEORY :

The hybrid model has four h- parameters. The h stands for a hybrid because the parameters are a mix of impedance, admittance and dimensionless unit. In common emitter the parameters are:

- h_{ie} : input impedance (ohm)
- h_{re} : reverse voltage ratio (dimensionless)
- h_{fe} : forward current transfer ratio (dimensionless)
- h_{oe} : output admittance (siemen)

The lower case suffixes indicate small-signal values and last suffix indicate the mode. So H_{ie} is input impedance in the common emitter. The hybrid model is suitable for small signals at mid-band and describes the action of the transistor.

- *Equivalent Circuit:*



Formulae :

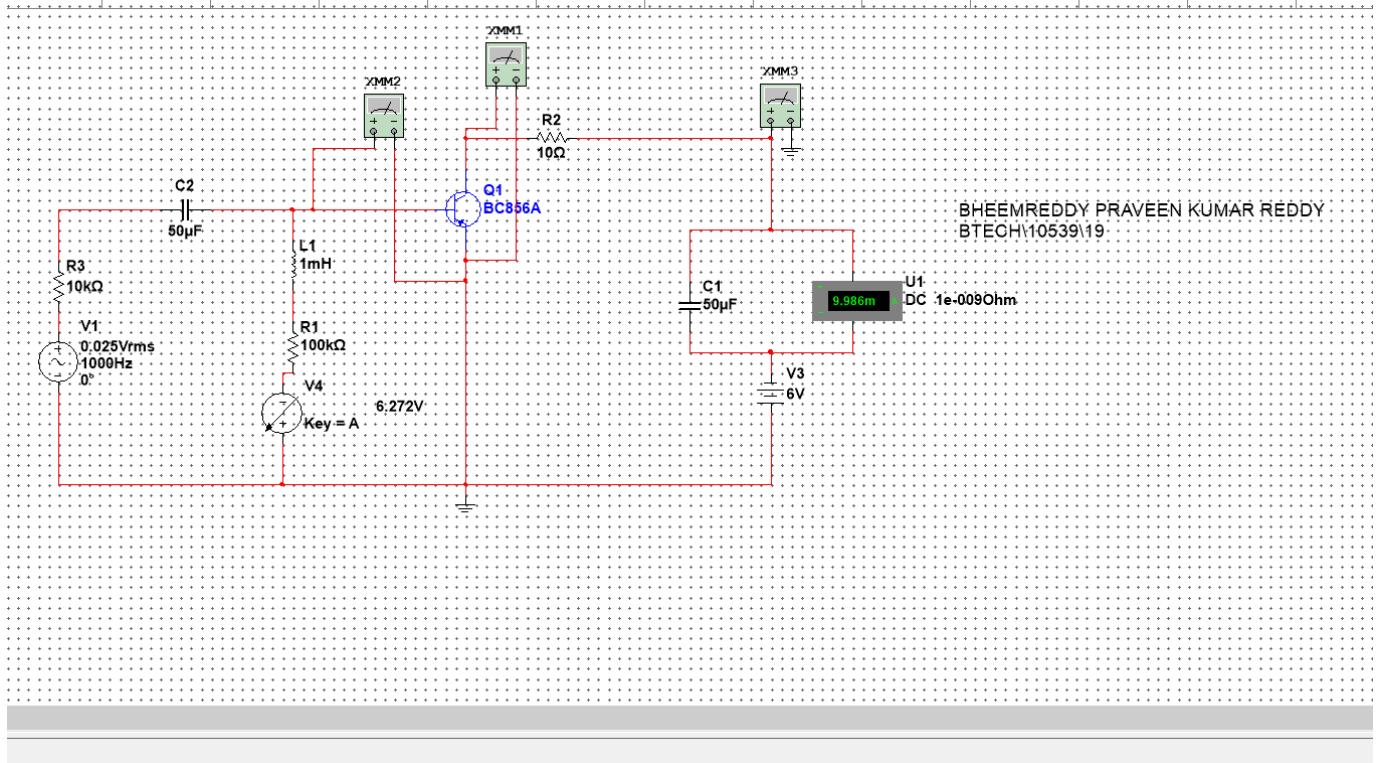
- $h_{ie} = V_{be}/I_b$ input impedance in ce configuration
- $h_{fe} = I_c/I_b$ forward current gain in ce configuration

PROCEDURE :

1. Connect the circuit as shown in the figure.
2. Apply V_{in} as 25 mV and 1 kHz from the function generator.
3. Fix collector voltage V_{cc} at 6 V.

4. Vary I_{CQ} by varying V_{EE} .
5. Measure V_{be} , V_{ce} and V_{cr} for various collector currents (I_c).
6. Tabulate the readings and calculate h_{ie} and h_{fe} .

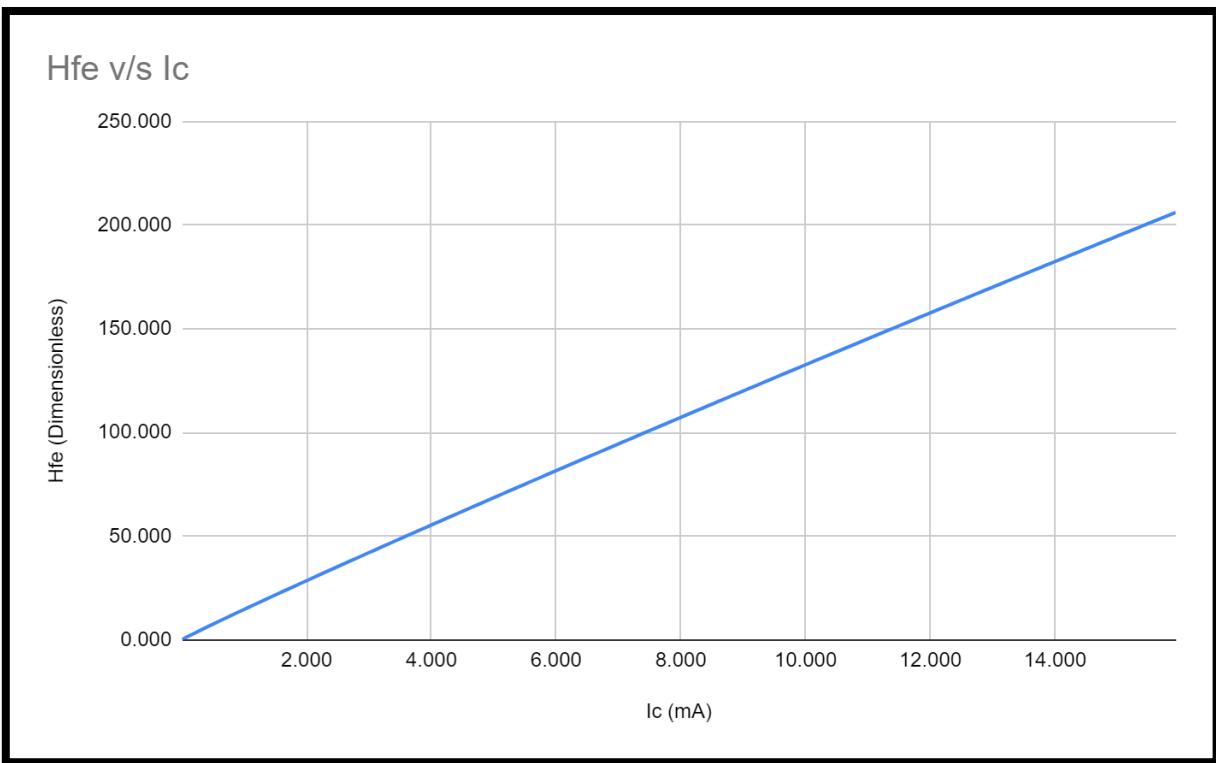
CIRCUIT DIAGRAM :



OBSERVATIONS :

I (mA)	V_3 (V)	V_{be} (V)	V_{ce} (V)	V_{cr} (V)	$I_{lb} = (V_{in} - V_{be}) / 10k\Omega$ (mA)	$I_c = (V_{ce} - V_{cr}) / 10$ (mA)	$H_{ie} = V_{be} / I_{lb}$ (kΩ)	$H_{fe} = I_c / I_b$ (dimensionless)
1	1.2	-0.64	-5.989	-6	0.068	1.062	9.416	15.522
2	1.75	-0.66	-5.979	-6	0.070	2.068	9.431	29.409
3	2.3	-0.67	-5.969	-6	0.071	3.072	9.440	42.982
4	2.85	-0.68	-5.959	-6	0.072	4.067	9.447	56.229
5	3.4	-0.69	-5.949	-6	0.073	5.051	9.452	69.169
6	3.95	-0.70	-5.940	-6	0.074	6.022	9.457	81.822
7	4.55	-0.70	-5.929	-6	0.074	7.067	9.461	95.320
8	5.1	-0.71	-5.920	-6	0.075	8.013	9.464	107.430
9	5.7	-0.71	-5.910	-6	0.075	9.030	9.467	120.372
10	6.3	-0.71	-5.900	-6	0.075	10.033	9.470	133.049

PLOTS:



RESULT :

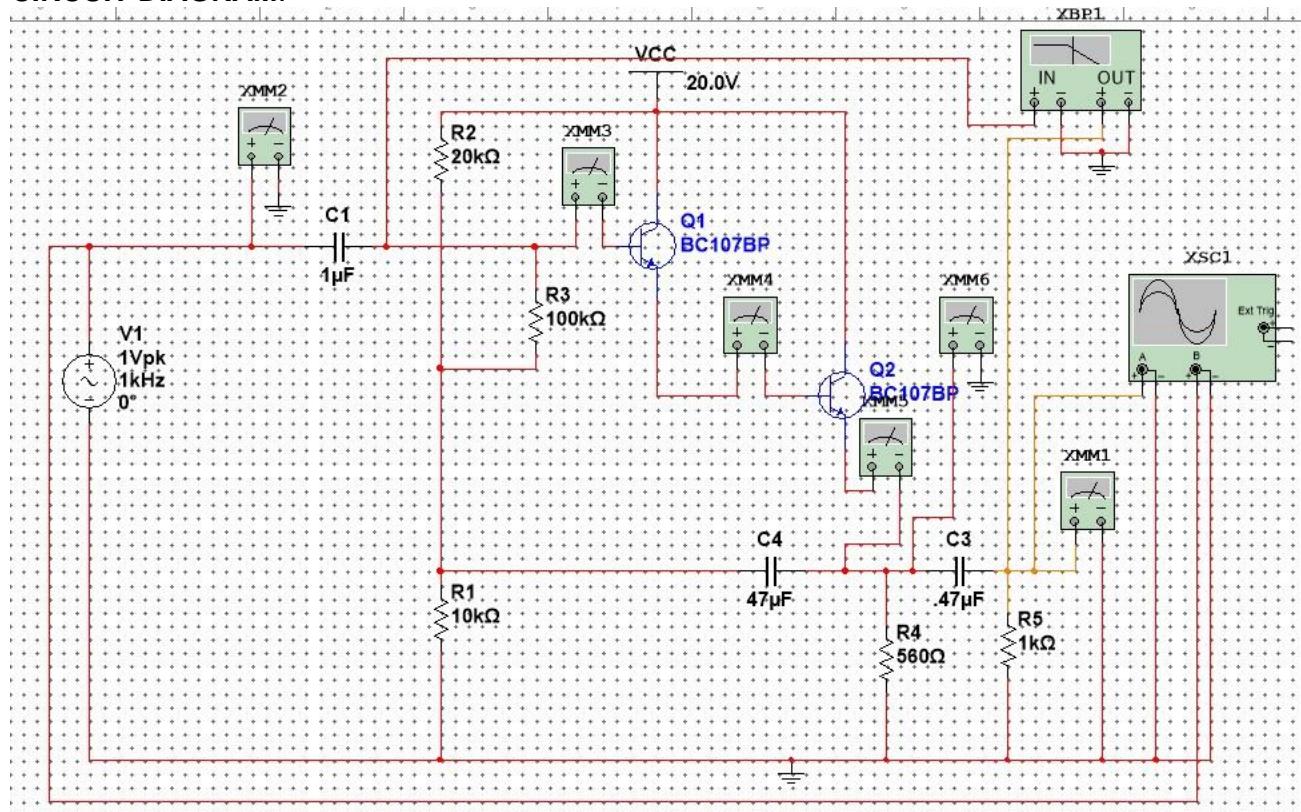
H_{fe} varies linearly with I_c with constant slope $1/I_b$. H_{ie} has a fixed average value of **9.352 kOhm**

EXPERIMENT 2

AIM: Design a Darlington pair amplifier and obtain its frequency response characteristics.

SOFTWARE USED: NI Multisim 14.1

CIRCUIT DIAGRAM:



OBSERVATIONS:

1. Frequency Response with BootStrap and RL =1kΩ:

Sl.No.	Frequency (Hz)	Gain Av	dB Gain A = 20log ₁₀ (V _o /V _{in})
1	1.00	0.003	-50.1
2	2.00	0.004	-44.95
3	5.0	0.018	-36.44
4	10.00	0.03	-29.65
5	20.00	0.059	-25.71
6	50.12	0.14	-16.81
7	100.00	0.28	-11.08
8	199.53	0.50	-8.03
9	500.0	0.81	-1.80
10	1.0K	0.93	-0.45
11	2.0K	0.97	-0.29
12	5.0K	0.98	-0.18
13	10.0K	0.98	-0.18
14	20.0K	0.98	-0.18
15	50.1K	0.98	-0.18
16	100.0K	0.98	-0.18
17	199.5K	0.98	-0.18
18	501.2K	0.98	-0.16
19	1.0M	0.97	-0.18
20	2.0M	0.95	-0.24
21	5.0M	0.94	-0.53
22	10.0M	0.89	-0.97
23	20.0M	0.86	-1.31
24	50.1M	0.84	-1.44
25	100.0M	0.85	-1.37
26	200.0M	0.87	-1.14
27	501.2M	0.90	-0.80
28	1000.0M	0.93	-0.69

2. Frequency Response without BootStrap and $RL = 1k\Omega$:

Sl.No.	Frequency (Hz)	Gain A_V	dB Gain $A = 20\log_{10}(V_o/V_{in})$
1	1.00	1.63×10^{-9}	-175.715
2	2.00	5.82×10^{-9}	-164.7
3	5.01	2.50×10^{-8}	-152.01
4	10.00	5.82×10^{-8}	-144.7
5	20.00	1.24×10^{-7}	-138.1
6	50.00	3.42×10^{-7}	-129.3
7	100.00	8.41×10^{-7}	-121.5
8	505.00	7.02×10^{-6}	-103.07
9	1.0K	1.49×10^{-6}	-96.512
10	10.15K	0.00015	-76.4
11	51.2K	0.00076	-62.35
12	100.9K	0.0015	-56.45
13	508.9K	0.0075	-42.4
14	1.003M	0.0149	-36.5
15	10.2M	0.15	-16.4
16	50.2M	0.57	-4.76
17	101.7M	0.77	-2.16
18	512.8M	0.9032	-0.884
19	1.01G	0.9078	-0.84
20	2.04G	0.9087	-0.831
21	5.09G	0.9067	-0.85
22	10.04G	0.8983	-0.931
23	20.3G	0.8659	-1.25
24	50.6G	0.7064	-3.018
25	102.4G	0.4608	-6.728
26	503.5G	0.0922	-20.7
27	1.019T	0.0602	-24.4
28	5.004T	0.0491	-26.175
29	10.1T	0.0488	-26.23
30	50.00T	0.0486	-26.26
31	100.00T	0.0486	-26.26
32	500.00T	0.0486	-26.26
33	1.00P	0.0486	-26.26

RESULTS:

Parameter	Frequency	Avm = Vo/Vin	Db Gain	Ie	Ib	Ai
With Bootstrap	5kHz	0.97	-0.184	2.034mA	44.205nA	46012.89
Without Bootstrap	3Ghz	0.90	-0.838	1.8mA	30.8mA	17.134

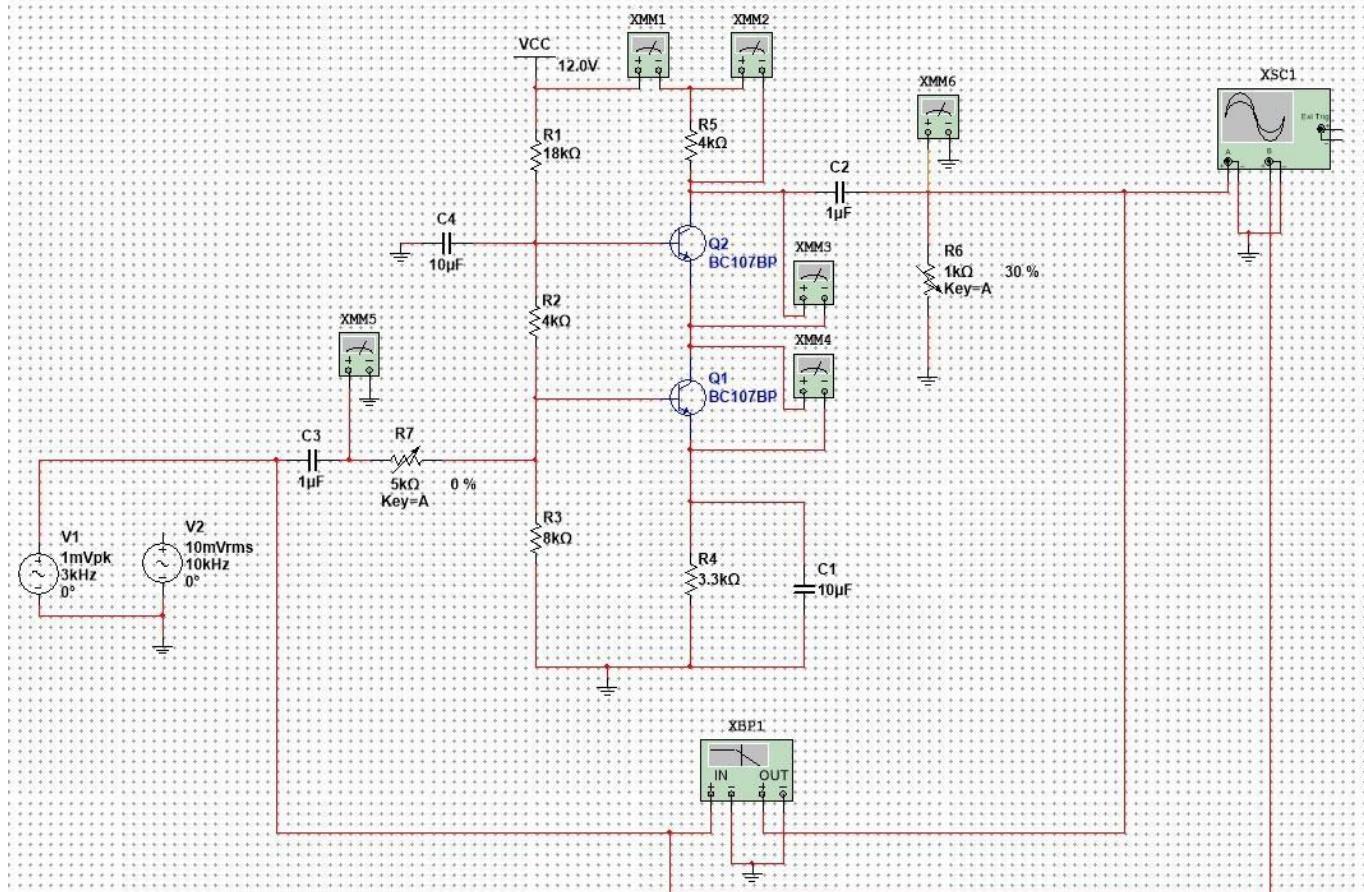
Parameter	Input Impedance	Output Impedance
With Bootstrap	4.42 MΩ	0.861 Ω
Without Bootstrap	35.51 Ω	6.42 Ω

EXPERIMENT 3

AIM: Find the frequency response of a Cascode Amplifier. Find its voltage gain, input resistance and output resistance.

SOFTWARE USED: NI Multisim 14.1

CIRCUIT DIAGRAM:



Theory:

Cascade amplifier is a cascade connection of a common emitter and common base amplifiers. It is used for amplifying the input signals. The common application of Cascode amplifiers is for impedance matching. The low impedance of CE is matched with the medium of the CB stage.

The major advantage of this circuit arrangement stems from the placement of the upper FET as the load of the input (lower) FET output terminals (drain). Because at operating frequencies the upper FET's (output terminal). The upper FET exhibits a low input resistance to the lower FET, making the voltage gain of the lower FET very small, which dramatically reduces the

Miller effect feedback capacitance from the lower FET's drain to gate. This loss of voltage gain is recovered by the upper FET. The upper transistor permits the lower FET to operate with minimal negative feedback, improving its band

OBSERVATIONS:

Frequency Response ($V_{in} = 10\text{mV}$ (rms) and RL open)

SI.No.	Frequency (Hz)	Gain $A_v = V_o/V_{in}$	Gain in dB $A_v = 20\log_{10}(V_o/V_{in})$
1	50.12	23.88	28.97
2	100.00	53.29	33.37
3	200.00	108.64	39.72
4	501.00	200.59	45.003
5	1.0K	240.71	46.63
6	2.5K	257.62	48.22
7	5.0K	260.31	48.31
8	10.0K	260.91	48.33
9	20.0K	261.21	48.34
10	50.1K	261.21	48.34
11	100.0K	261.21	48.34
12	501.2K	261.21	48.34
13	1.0M	261.21	48.34
14	2.0M	261.24	48.34
15	5.8M	257.31	48.208
16	10.0M	244.34	47.76
17	20.2M	172.58	44.74
18	50.5M	56.62	35.06
19	100M	26.36	28.42
20	507M	5.87	14.19
21	1G	3.44	9.25

RESULTS :

(At $V_{in} = 10\text{mV}$ (rms) and Frequency = 50 kHz and RL Open) :

1. Maximum Gain in dB = 48.34dB

2. 3dB Frequency Bandwidth = 5.79MHz

3. Input Impedance = 1.4 KΩ

4. Output Impedance = 4 kΩ

Parameter	Frequency (Hz)	Gain $A_v = V_o/V_{in}$	Gain in dB $A_v = 20\log_{10}(V_o/V_{in})$
With RL = 1 kΩ	50 kHz	51	35.32
Without RL	50 kHz	255	49.81

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EXPERIMENT 4

AIM:

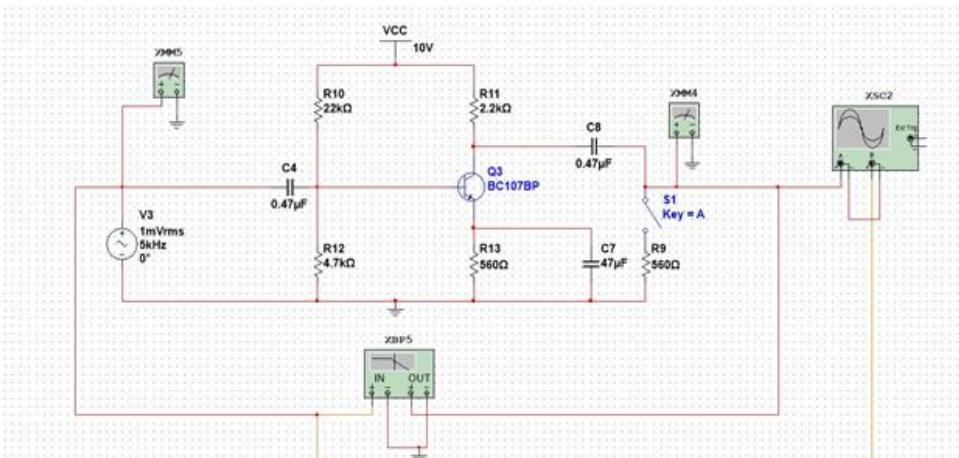
Find the frequency response of single-stage and multistage amplifiers.

Determine the mid band gain and bandwidth of the amplifiers.

SOFTWARE USED: NI Multisim 14.1

OBJECTIVE-(A): To Design Common Emitter or Single Stage RC Coupled Amplifier Using BJT

CIRCUIT DIAGRAM:



OBSERVATIONS: With $V_{in} = 1\text{mV(rms)}$ and 5kHz .

Frequency (Hz)	Av - Gain (Without Load)	dBGain (Without Load)	Av - Gain (With 1kOhm Load)	dBGain (With 1kOhm Load)
1	0.04	-27.2	0.0001	-77.725
10	0.81	-1.76	0.02	-32.37
50	13.35	22.51	1.87	5.47

100	35.80	31.08	7.63	17.66
200	71.77	37.12	20.27	26.14

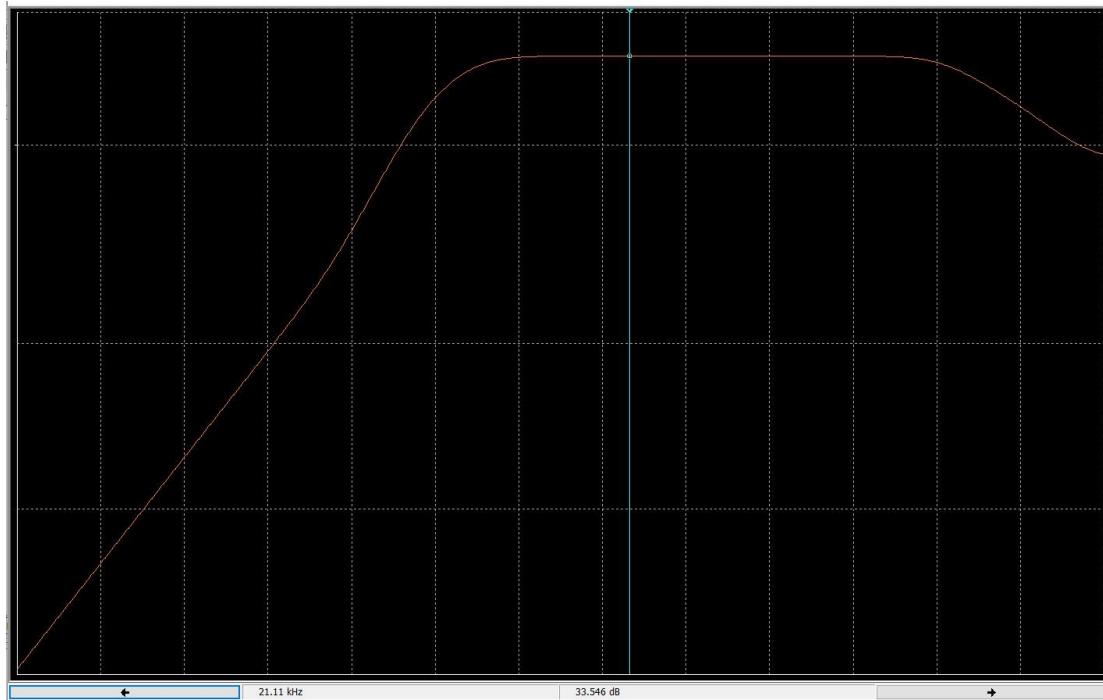
344.7	103.99	40.34	31.44	29.95
385.2	110.02	40.83	33.65	30.54
500	121.33	41.68	38.06	31.61
1.0K	139.31	42.88	44.71	33.01
5.0K	146.72	43.33	47.42	33.52
10.1K	146.9	43.34	47.53	33.54
50.0K	146.9	43.34	47.53	33.54
100.0K	146.9	43.34	47.53	33.54
200.0K	146.9	43.34	47.53	33.54
500.0K	146.9	43.34	47.53	33.54
1.0M	146.9	43.34	47.53	33.54
5.0M	145.88	43.28	47.53	33.54
10.0M	141.90	43.04	47.36	33.51
37.1M	103.99	40.34	45.23	33.11
50.0M	87.49	38.84	43.51	32.78
100.0M	50.06	34.06	35.56	31.02
114.03M	45.49	33.16	33.65	30.54
500.0M	10.61	20.52	10.37	20.32
1.0G	5.20	14.33	5.16	14.26

5.0G	0.98	-0.175	0.97	-0.18
10.0G	0.65	-3.65	0.65	-3.66

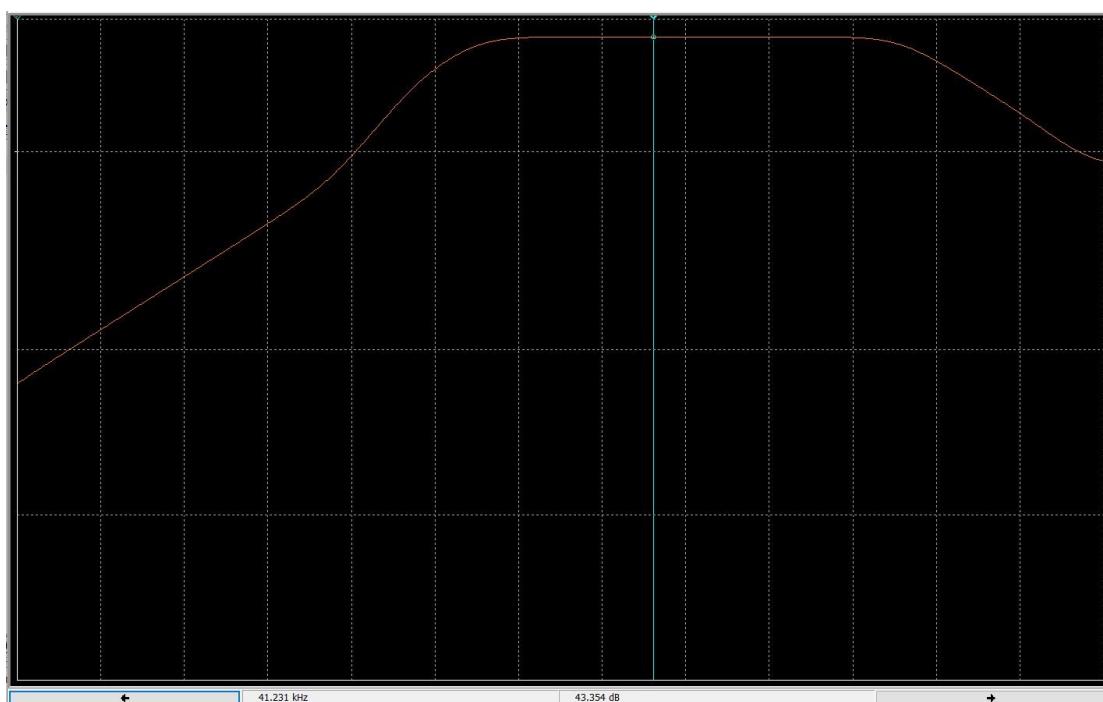
(All highlighted portions are the 3dB Frequency Range for respective conditions.)

BODE PLOTTER:

With $V_{in} = 1\text{mV(rms)}$ and 5kHz and Load Resistance $1\text{k}\Omega$.



With $V_{in} = 1\text{mV(rms)}$ and 5kHz and Without Load Resistance.



RESULTS AND CONCLUSION: With $V_{in} = 1\text{mV(rms)}$ and 5kHz.

Parameter	With Load Resistance (1 kΩ)	Without Load Resistance
Gain	47.5	146.9
Gain in dB	33.54	43.34
R _i (Input Impedance)	2.08 kΩ	2.08 kΩ
R _o (Output Impedance)	675 Ω	2.1 kΩ
3dB Frequency Bandwidth (B _w)	385.2 Hz - 114.03 MHz (B _w = 114.03 MHz)	344.7 Hz - 37.1 MHz (B _w = 37.1 MHz)

From this experiment we observed that for single stage, at $V_{in} = 1\text{mV(rms)}$ and frequency 5kHz:

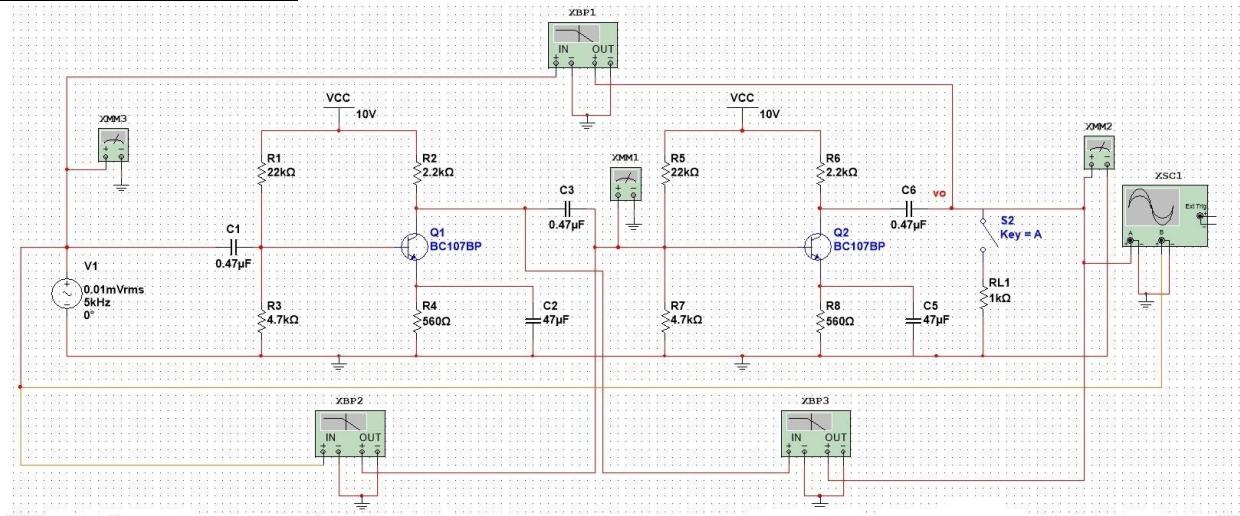
With Load: The gain is 33.54dB and 3dB Bandwidth is 114.03 MHz.

Without Load: The gain is 43.34dB and 3dB Bandwidth is 37.1 MHz.

Hence, without load resistance the gain increased, 3dB bandwidth has decreased, R_i remained almost constant and R_o also increased.

OBJECTIVE-(B): To Design multistage RC Coupled Amplifier Using BJT.

CIRCUIT DIAGRAM:



OBSERVATIONS:

With Vin = 0.01mV(rms) and 5kHz and without load resistance.

Frequency (Hz)	Av (1st Stage)	dB gain (1st Stage)	Av (2nd Stage)	dB gain (2nd Stage)
1	0.0005	-65.9	0.04	-27.28
10	0.08	-21.01	0.82	-1.62
100	17.25	24.74	36.81	31.32
200	36.34	31.21	72.52	37.21
338.8	51.76	34.28	103.15	40.27
346.5	52.17	34.35	104.11	40.35
500	60.60	35.65	121.47	41.69
1.0K	69.42	36.83	139.15	42.87
5.0K	73.02	37.27	146.72	43.33
10.0K	73.11	37.28	147.06	43.35
50.0K	72.69	37.23	147.06	43.35
100.0K	71.20	37.05	147.06	43.35
200.0K	65.99	36.39	147.06	43.35

369.6K	51.76	34.28	147.06	43.35
500.0K	47.04	33.45	147.06	43.35
1.0M	28.37	29.06	147.06	43.35
5.0M	6.23	15.89	145.71	43.27
10.0M	3.16	10.01	141.90	43.04
37.3M	1.16	1.29	104.11	40.35
50.0M	1.01	0.09	86.09	38.7
100.0M	0.80	-1.92	50.00	33.98
500.0M	0.32	-9.65	10.71	20.60

(All highlighted portions are the 3dB Frequency Range for respective conditions.)

With Vin = 0.01mV(rms) and 5kHz and without load resistance.

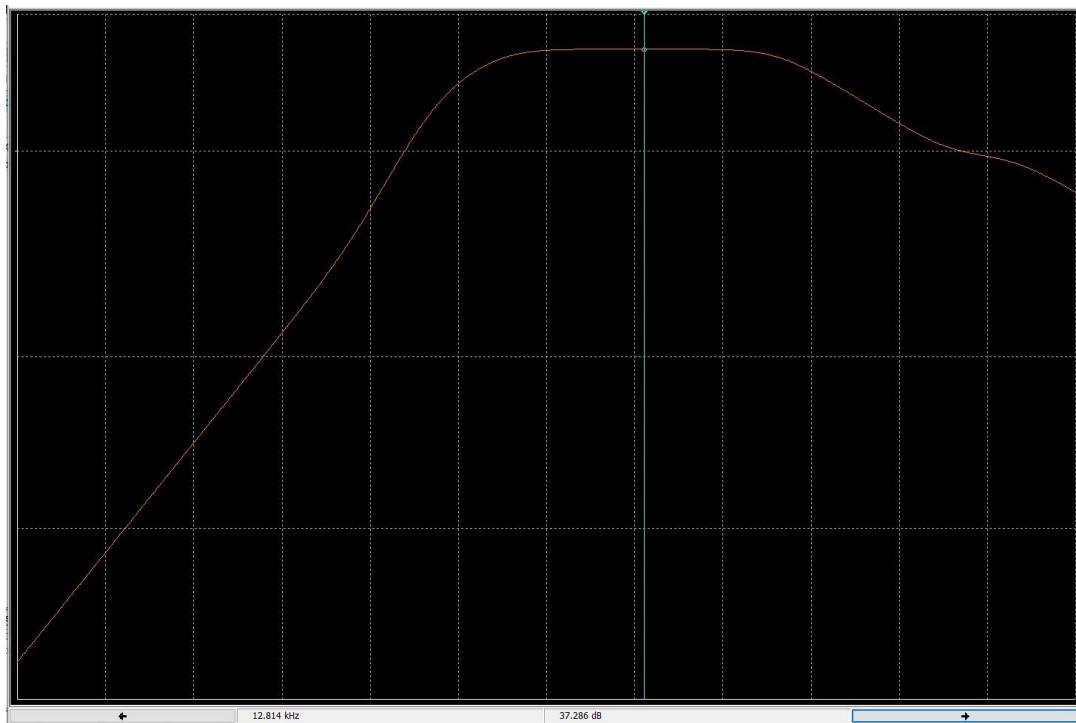
Frequency (Hz)	Av (Combined Stage)	dB gain (Combined Stage)
1	0.0019	-54.29
10	0.65	-3.67
100	993.11	59.94
200	3475.36	70.82
448.1	7603.26	77.62
500	8090.95	78.16
1.0K	9942.60	79.95
5.0K	10739.89	80.62
10.0K	10739.89	80.62
50.0K	10702.86	80.59
100.0K	10483.34	80.41
200.0K	9749.89	79.78

422.5 k	7603.26	77.62
500.0K	6966.26	76.86
1.0M	4202.42	72.47
5.0M	909.91	59.18
10.0M	455.51	53.17
50.0M	38.97	38.97
100.0M	41.16	32.29
500.0M	3.51	10.93

(All highlighted portions are the 3dB Frequency Range for respective conditions.)

BODE PLOTTER:

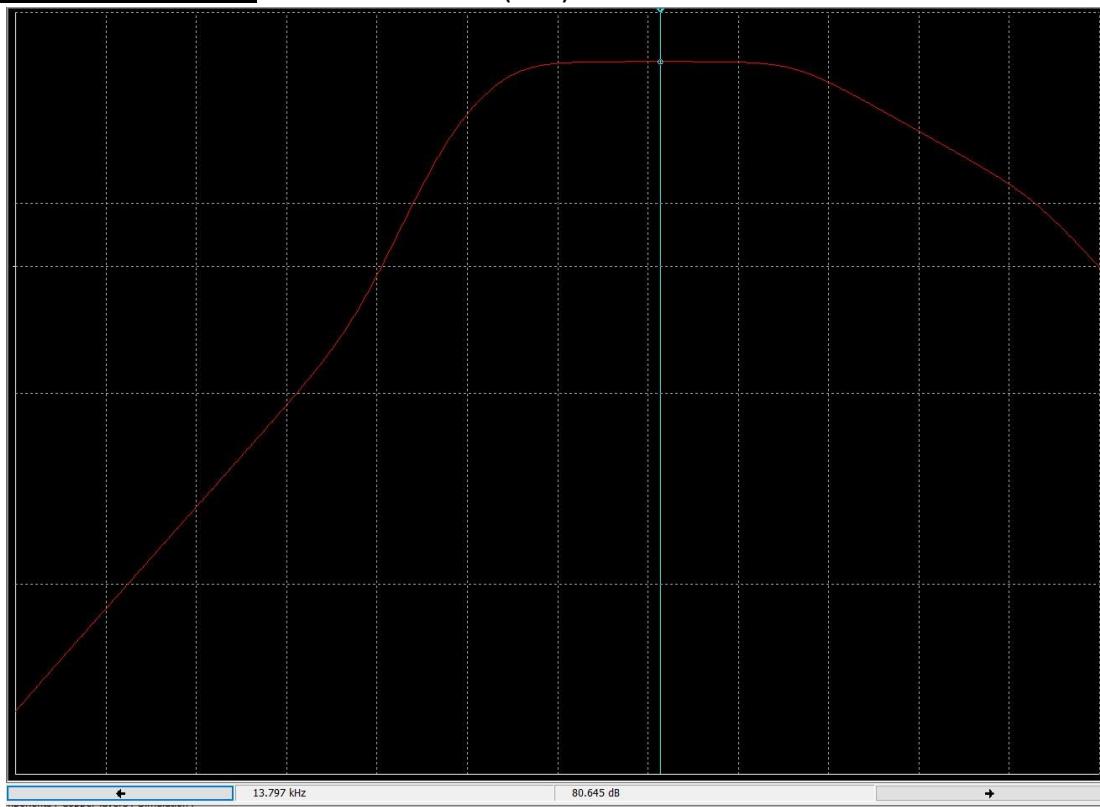
For Stage 1 : with $V_{in} = 0.01\text{mV(rms)}$ and 5kHz and without Load Resistance.



For Stage 2 : with $V_{in} = 0.01\text{mV(rms)}$ and 5kHz and without Load Resistance.



For Combined Stage: with $V_{in} = 0.01\text{mV(rms)}$ and 5kHz and without Load Resistance.



RESULTS:

For Multi-Stage Amplifier with $V_{in} = 0.01\text{mV(rms)}$ and frequency 5kHz :

Parameter	With Load Resistance (1 kΩ)	Without Load Resistance
Gain	70.84	80.645
Gain in dB	3483.37	10745.9
Ri (Input Impedance)	2.08 kΩ	2.08 kΩ
Ro (Output Impedance)	682Ω	2.09 kΩ
3dB Frequency Bandwidth (Bw)	477.8 Hz - 932.8 kHz (Bw = 932.4 kHz)	448.1 Hz - 422.5 kHz (Bw = 422.1 kHz)

For Multi-Stage amplifier, it is observed that at $V_{in} = 0.01\text{mV(rms)}$ and frequency 5kHz:

With Load: The gain is 70.84dB and 3dB Bandwidth is 932.4 kHz.

Without Load: The gain is 80.64dB and 3dB Bandwidth is 422.1 kHz.

Hence, without load resistance the gain increased, 3dB bandwidth has decreased, Ri remained almost constant and also Ro increased.

$V_{in} = 0.01\text{mV(rms)}$ and frequency 5kHz and without load resistance:

Parameter	Stage 1	Stage 2	Combined Stage
Gain	73.11	147.06	10745.9
Gain in dB	37.28	43.35	80.64
3dB Frequency Bandwidth (Bw)	338.8 Hz - 369.6 kHz (Bw = 369.6 kHz)	346.5 Hz - 37.3 MHz (Bw = 37.3 MHz)	448.1 Hz - 422.5 kHz (Bw = 422.1 kHz)

Also comparing the results from Stage 1, Stage 2 and Combined Stage (with $V_{in} = 0.01\text{mV(rms)}$ and frequency 5kHz and without load resistance), it can be verified that the gain of Combined Stage is the product of gain of Stage 1 and Stage 2 (i.e. $73.11 \times 147.06 = 10752.13$).

CONCLUSION:

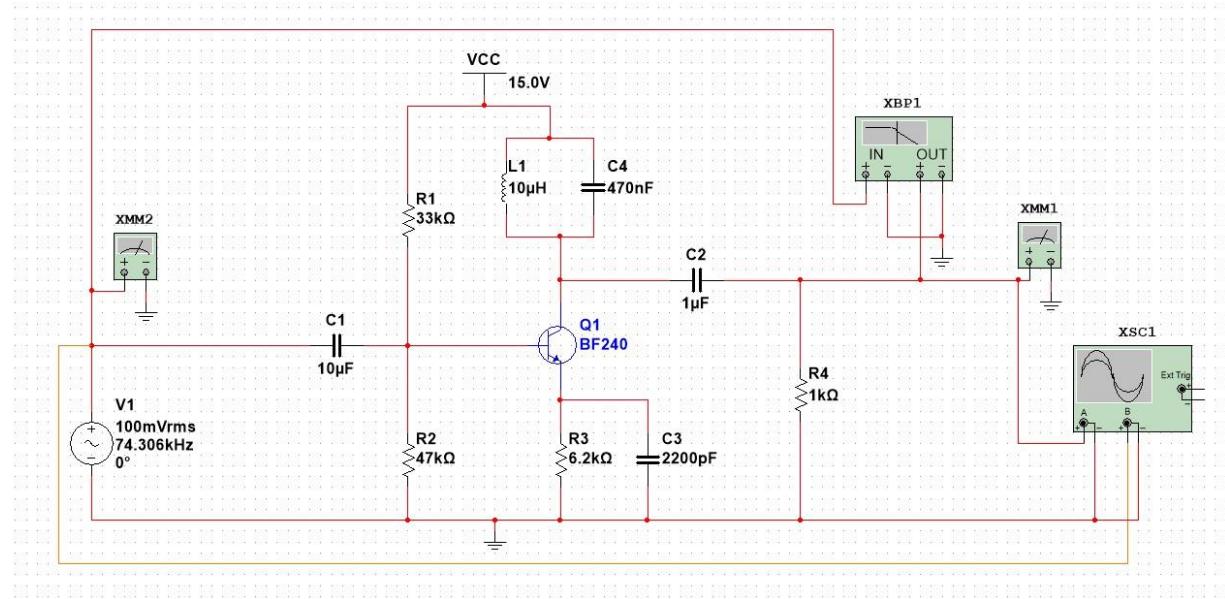
It can be observed that the gain has increased drastically from single stage to multistage amplifier (i.e. from 43.34dB (gain=147.06) to 80.64dB (gain=10745.9) without load resistance and from 33.54dB to 70.84dB with load resistance) and 3dB bandwidth has decreased.

EXPERIMENT 5

AIM: Design a BJT based tuned amplifier and find its frequency response.

SOFTWARE USED: NI Multisim 14.1

CIRCUIT DIAGRAM:



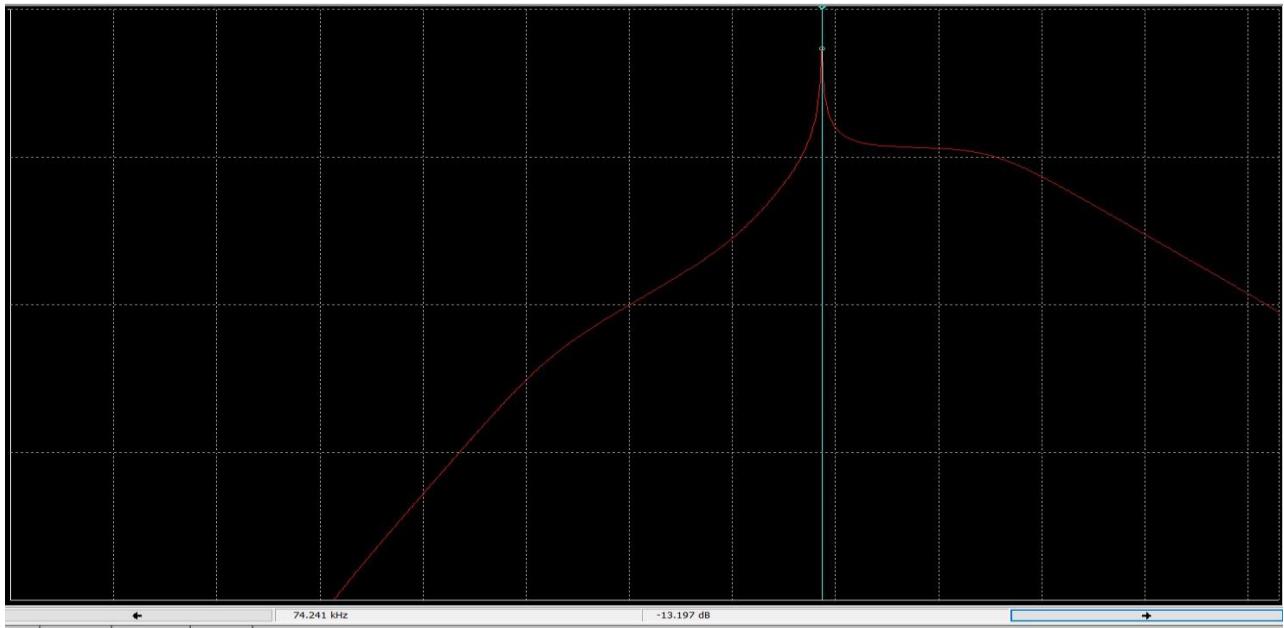
OBSERVATION:

$V_{in} = 100\text{mV}$ (rms Value) ; $L = 10 \mu\text{H}$; $C = 470\text{nF}$ with BJT BF240 and $R_I = 1\text{k}\Omega$.

Frequency	Av	Av in db
5 Hz	1.577×10^{-9}	-176.04
10.2 Hz	6.404×10^{-8}	-163.87
101 Hz	5.420×10^{-7}	-125.32
1k Hz	4.802×10^{-6}	-106.37
5k Hz	5.578×10^{-5}	-85.07
10k Hz	0.0001	-77.39

50k Hz	0.0041	-47.72
70k Hz	0.0536	-25.41
72k Hz	0.1967	-14.12
73.18k Hz	1.014	0.12
75k Hz	0.0989	-20.09
80k Hz	0.0300	-30.45
100k Hz	0.0099	-40.05
500k Hz	0.0046	-46.60
1M Hz	0.0042	-47.34
5M Hz	0.0025	-51.74
10M Hz	0.0014	-56.72
100M Hz	0.0001	-76.23
500M Hz	3.104×10^{-5}	-90.16

BODE PLOTTER:



RESULTS AND CONCLUSION:

Parameter	With RI (1kOhm)	Without RI
Resonant Frequency (fr)	73.18 kHz	73.17 kHz
Gain	1.014	3.91
Gain in dB	0.12	31.59
Ri	18.84 kΩ	18.8 kΩ
Ro	95 Ω	147.2 Ω
3dB Frequency Bandwidth (Bw)	75.5 KHz - 72.5 KHz (3.1 KHz)	75.3 KHz - 72.25 KHz (3.05 KHz)
Q factor (fr/Bw)	23.606	23.99

The gain was found maximum at the resonant frequency fr (73.18 kHz as highlighted in the observation table) i.e. 0.12 dB gain (with RI = 1 kΩ) and 31.59 dB gain (without RI) and observed that it is decreasing on the either sides of the resonant frequency.

The 3dB Frequency Bandwidth was 3.1KHz (with load) and 3.05KHz (without load).

The Q factor was 23.606(with load) and 23.99 (without load).

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Experiment- 6

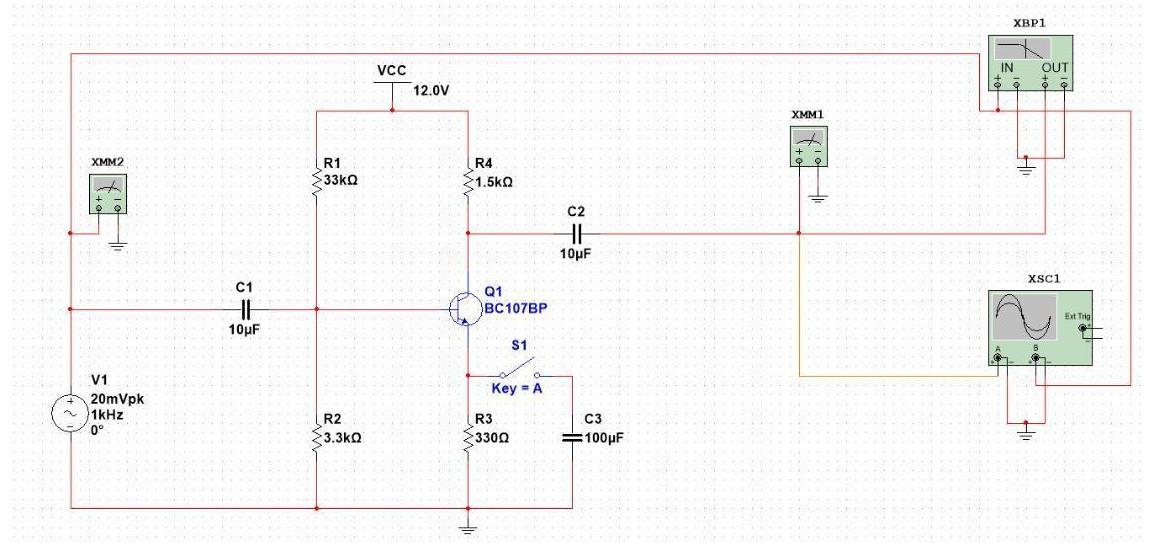
Aim- Design and test the current-series and voltage-shunt feedback amplifier and to calculate the following parameters with and without feedback:

- a) Mid-band gain
- b) Bandwidth and cut-off frequencies
- c) Input and output impedance.

Objective(A)- To calculate the following parameters of Current - Series Feedback Amplifier with and without feedback:

- a) Mid-band gain
- b) Bandwidth and cut-off frequencies
- c) Input and output impedance.

Circuit Diagram:



Switch S1: ON(Closed) = Without Current Series Feedback
 Switch S1: OFF(Open) = With Current Series Feedback

OBSERVATION:

(At $V_{in} = 1\text{mV}$ (Vp-p) ; Frequency = 1 kHz ; Without any Load Resistance)

Frequency (Hz)	Gain (Without Feedback)	Gain (dB) (Without Feedback)	Gain (With Feedback)	Gain (With Feedback)
1.0	0.79	-1.96	0.78	-2.14
5.0	4.14	12.36	2.90	9.26
5.42	4.44	12.95	3.01	9.58
10.1	8.45	18.54	3.74	11.48
83.34	50.75	34.11	4.24	12.56
100.0	55.08	34.82	4.25	12.57
200.0	66.14	36.41	4.25	12.58
500.0	70.71	36.99	4.25	12.58
1.0K	71.44	37.08	4.25	12.58
10.0K	71.69	37.11	4.25	12.58
50.0K	71.69	37.11	4.25	12.58
100.0K	71.69	37.11	4.25	12.58
500.0K	71.69	37.11	4.25	12.58

1.0M	71.69	37.11	4.25	12.58
10.0M	71.12	37.04	4.21	12.5
50.0M	57.54	35.20	3.48	10.85
67.81M	50.75	34.11	3.14	9.95
73.51M	48.75	33.76	3.01	9.58
100.0M	40.13	32.07	2.55	8.16
200.0M	23.01	27.24	1.70	4.63
500.0M	9.60	19.65	1.15	1.27
1.0G	4.83	13.68	1.04	0.35

(All highlighted portions are the 3dB Frequency Range for respective conditions.)

RESULTS AND CONCLUSION:

(At Vin = 1mV (Vp-p); Frequency = 1 kHz; Without any Load Resistance)

Parameter	Without Feedback	With Feedback
Gain	71.48	4.26
Gain in dB	37.08	12.58
Ri (Input Impedance)	2.205 kOhm	2.925 kOhm
Ro (Output Impedance)	1.47 kOhm	1.496 kOhm

3dB Frequency Bandwidth (Bw)	83.34 Hz - 67.81 MHz (Bw = 67.81 MHz)	5.42 Hz - 73.51 MHz (Bw = 73.51 MHz)
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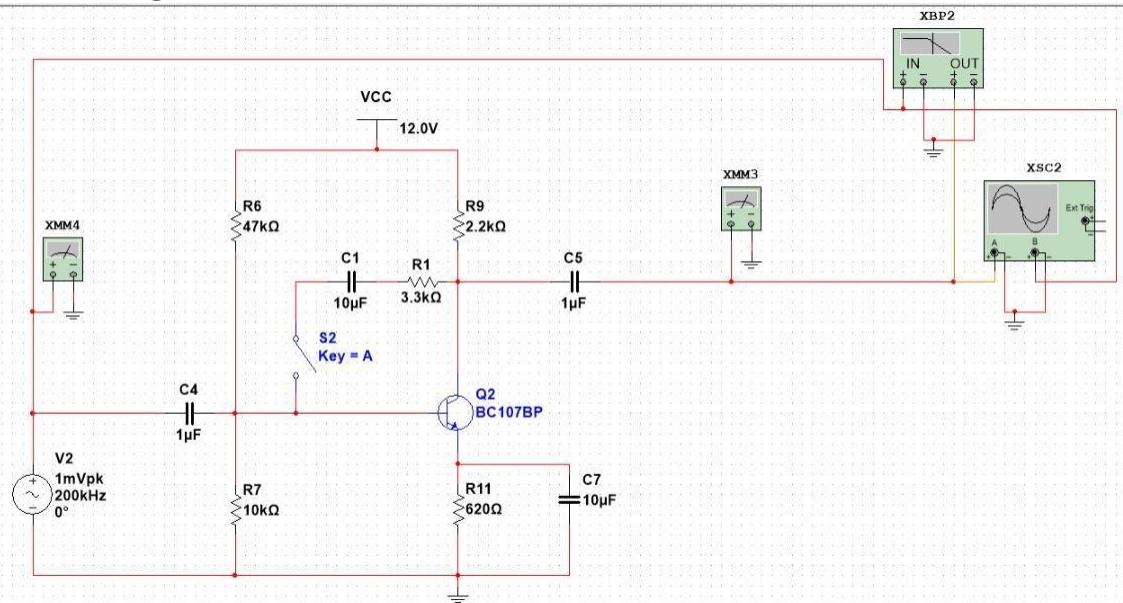
Performing the experiment, it can be concluded and verified that after applying the Current Series feedback in a circuit using the S1 switch at $V_{in} = 1\text{mV}$ (Vp-p), Frequency = 1 kHz and without any Load Resistance the:

- Gain = Decreases
- R_i (Input Impedance) = Increases
- R_o (Output Impedance) = Increases
- 3dB Frequency Bandwidth (Bw) = Increases.

Objective(B)- To calculate the following parameters of voltage shunt feedback amplifier with and without feedback:

- a) Mid-band gain
- b) Bandwidth and cut-off frequencies
- c) Input and output impedance.

Circuit Diagram:



OBSERVATION:

(At $V_{in} = 1\text{mV}$ (Vp-p) ; Frequency = 200 kHz ; Without any Load Resistance)

Frequency(Hz)	Gain (Without FB)	Gain (dB)	Gain (With FB)	Gain (in dB)
1.0	0.17	-15.10	0.0631	-23.99
5.0	0.84	-1.42	0.085	-21.35
10.1	1.65	4.38	0.13	-17.57
100.0	13.39	22.54	1.58	4.00
200.0	26.06	28.32	3.25	10.24
500.0	61.09	35.72	8.14	18.22
1.0K	104.11	40.35	16.31	24.25
1.29K	118.85	41.50	20.44	26.21
6.34K	164.62	44.33	72.61	37.22
10.0K	166.53	44.43	86.89	38.78
50.0K	167.88	44.50	101.85	40.16
100.0K	167.88	44.50	102.44	40.21
500.0K	167.88	44.50	102.56	40.22
1.0M	167.88	44.50	102.56	40.22
10.0M	162.74	44.23	101.39	40.12
39.30M	118.85	41.50	87.19	38.81
50.0M	103.99	40.34	81.00	38.17
64.06M	87.59	38.85	72.61	37.22
100.0M	61.09	35.72	55.08	34.82
200.0M	32.54	30.25	31.69	30.02
500.0M	12.89	22.21	13.01	22.29
1.0G	6.23	15.90	6.20	15.86

(All highlighted portions are the 3dB Frequency Range for respective conditions.)

RESULTS AND CONCLUSION:

(At $V_{in} = 1\text{mV (Vp-p)}$; Frequency = 200 kHz ; Without any Load Resistance)

Parameter	Without Feedback	With Feedback
Gain	167.97	102.61
Gain in dB	44.50	40.22
R_i (Input Impedance)	$2.0375 \text{ k}\Omega$	31.5Ω
R_o (Output Impedance)	$2.07 \text{ k}\Omega$	$1.275 \text{ k}\Omega$
3dB Frequency Bandwidth (Bw)	1.29 kHz - 39.30 MHz (Bw = 39.30 Mhz)	6.34 kHz - 64.06 Mhz (Bw = 64.06 Mhz)

Performing the experiment, it can be concluded and verified that after applying the Voltage Shunt feedback in a circuit using the S2 switch at $V_{in} = 1\text{mV (Vp-p)}$, Frequency = 200 kHz and without any Load Resistance the:

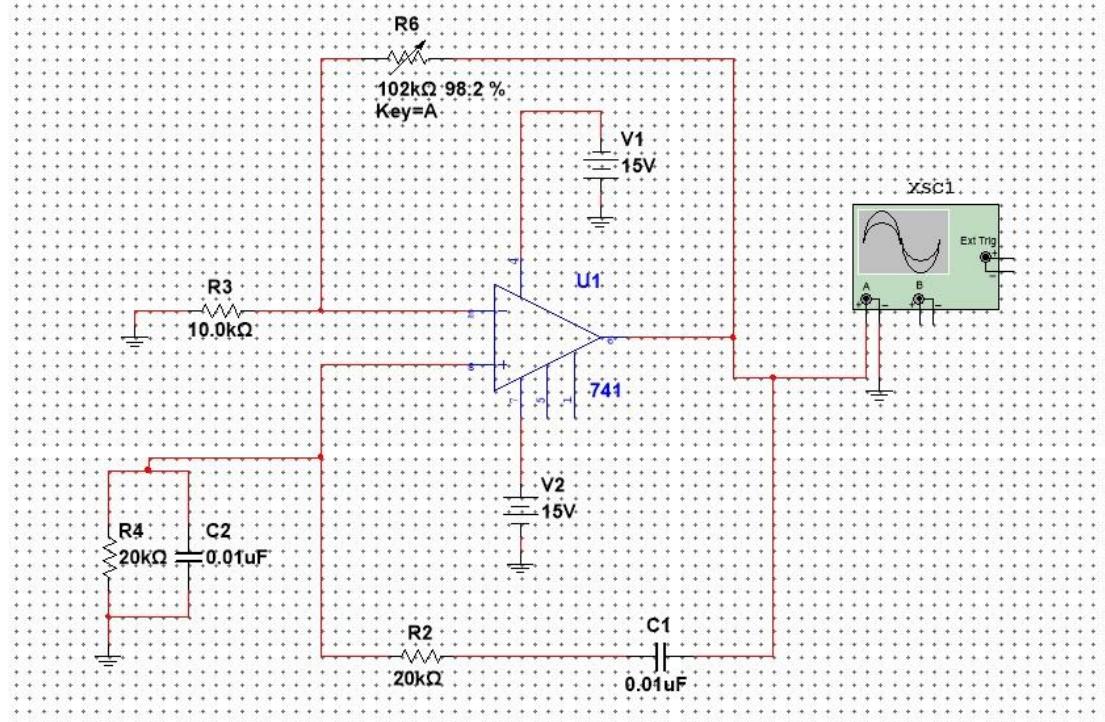
- Gain = Decreases
- R_i (Input Impedance) = Decreases
- R_o (Output Impedance) =Decreases
- 3dB Frequency Bandwidth (Bw) = Increases.

EXPERIMENT - 7

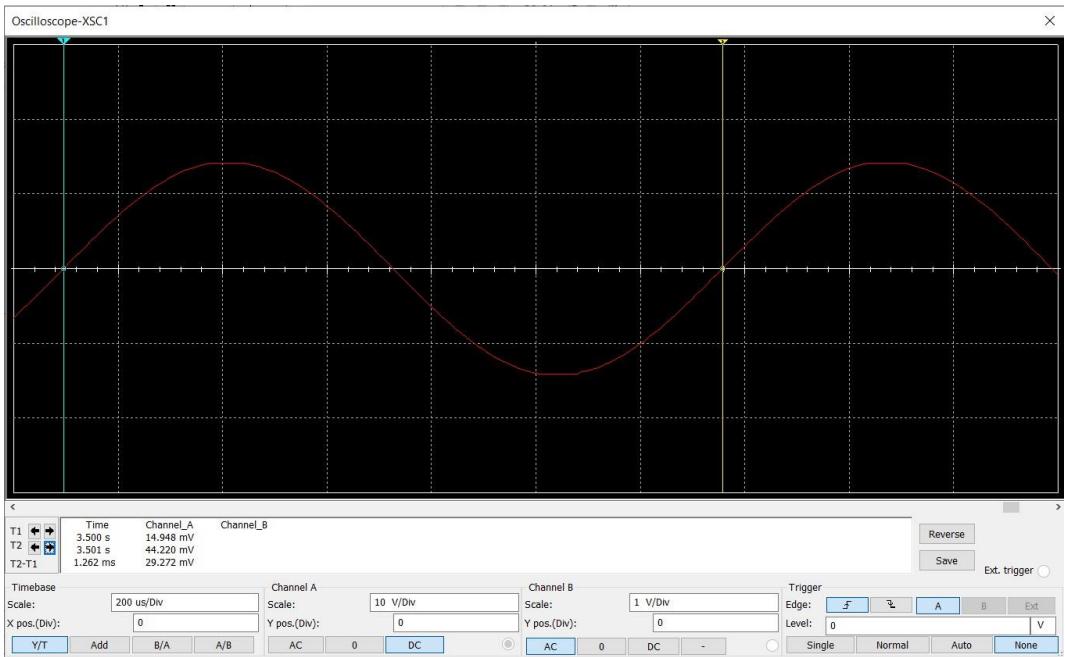
AIM: Design a Wein's bridge oscillator using BJT/OP-AMP and calculate the theoretical gain of the main amplifier. Observe and plot its output waveform.

SOFTWARE USED: NI Multisim 14.1

CIRCUIT DIAGRAM:



BODE PLOTTER:



RESULTS AND CONCLUSION:

CALCULATIONS :

According to the theory of Wein's Bridge Oscillator:

- ★ Using the formula, the Theoretical value of Time Period of the oscillator for R = 20 kOhm and C = 0.01uF is:

$$T = \frac{1}{f_0} = 2\pi rc = 2\pi(20\text{ k}\Omega)(0.01\mu\text{F}) = 1.25663\text{ms.}$$

- ★ The measured value of Time Period of the oscillator using Oscilloscope for R = 20 kΩ and C = 0.01μF; R5 = 10 kΩ and R6 = 20.042 kΩ is **1.262ms**.

Note:

(The simulation results were taken after trans time 2.5s or 2.5min at stable and unrectified output in oscilloscope)

$$\text{Error} = \frac{(\text{Theoretical Value} - \text{Measured Value})}{\text{Theoretical Value}} \times 100 = \frac{(1.2566 - 1.262)}{1.2566} \times 100 = 0.4297\%$$

CONCLUSION :

Performing the experiment and doing the calculations it can be successfully verified with the theory of Wein's Bridge Oscillator, that the Theoretical value (i.e. **1.2566ms**) and Measured Value (i.e.**1.262ms**) of Time Period of the oscillator (for R = 20 kΩ and C = 0.01μF) are found to be approximately same with an Error of **0.4297%**.

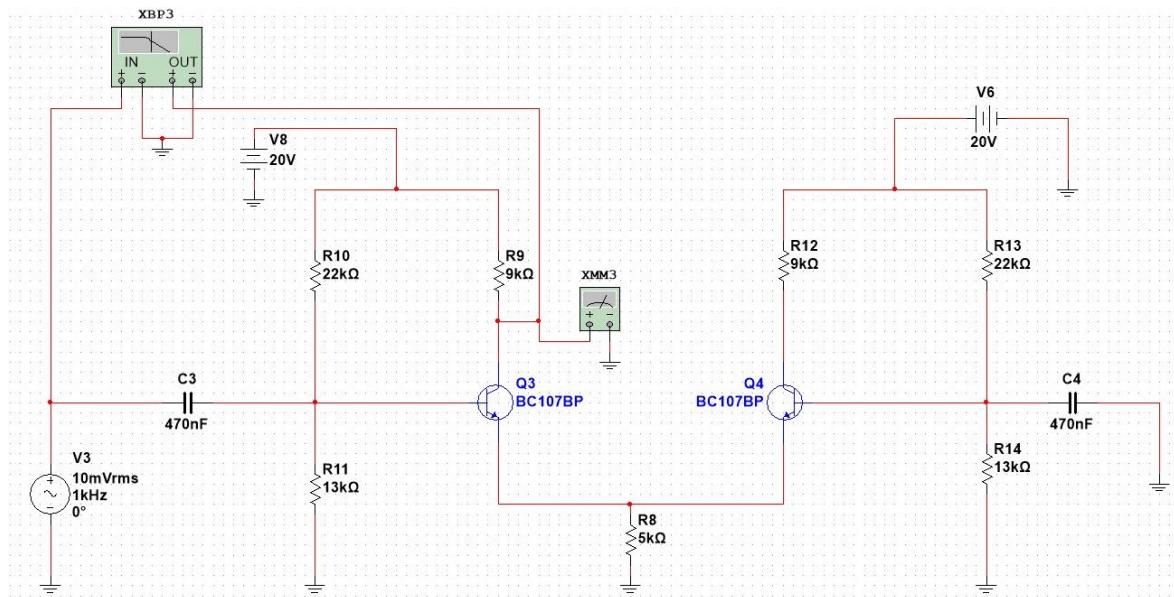
EXPERIMENT 8

AIM: Design a differential amplifier using BJT and determine the common-mode gain at different frequencies. Find the CMRR.

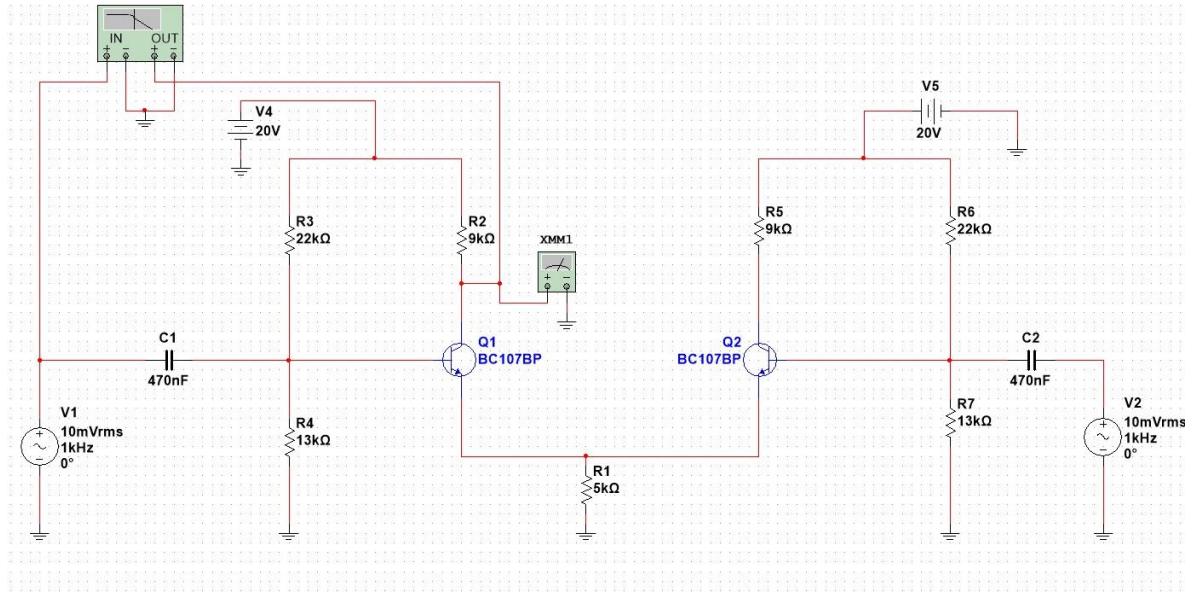
SOFTWARE USED: NI Multisim 14.1

CIRCUIT DIAGRAM:

Differential Mode:



Common Mode:



OBSERVATIONS:

- ★ Differential Mode Frequency Response: ($V1 = 10\text{mVrms}$ and $V2 = 0\text{Vrms}$)

Frequency (Hz)	Voltage Gain (Ad)	Gain in dB
1	1.48	4.121
10	18.250	24.835
100	88.787	39.867
1k	107.755	40.659
10k	108.01	40.660
100k	108.01	40.671
1M	106.535	40.631
10M	79.158	35.37
100M	10.678	21.221
1G	1.638	4.252

- ★ Common Mode Frequency Response: ($V1 = 10\text{mVrms}$ and $V2 = 10\text{mVrms}$)

Frequency (Hz)	Voltage Gain (Ac)	Gain in dB
1	0.021	-33.206
10	0.211	-13.506
100	0.824	-1.671
1k	0.892	-0.996
10k	0.892	-0.987
100k	0.892	-0.987
1M	0.894	-0.968
10M	0.984	-0.132
100M	1.04	0.344
1G	1.00	0.007

CONCLUSIONS AND RESULTS:

Performing the experiment it can be concluded that:

- ★ The Differential Mode Gain (at V1 = 10mVrms and V2 = 0Vrms and 1 kHz Frequency) is **Ad = 107.755** (in dB = 40.659).

The Common Mode Gain (at V1 = 10mVrms and V2 = 10mVrms and 1 kHz Frequency) is **Ac = 0.892** (in dB = -0.996).

- ★ Observing the Frequency Response it can be verified from the theory that:

For Differential Mode, the gain first increases then becomes constant at 49.659dB (frequency range = 69.5 Hz - 10.8 Mhz) and then again decreases.

For Common mode, the gain first increases then becomes constant around Zero(0 dB) after 50Hz frequency.

- ★ The theoretical formula of output voltage (Vo) has been successfully verified:

$$\text{Formula for } V_o: V_o = A_d(V_1 - V_2) + A_c \left(\frac{V_1 + V_2}{2} \right)$$

At frequency = 1kHz; V1 = 10mVrms; V2 = 5mVrms.

$$\begin{aligned}\text{According to formula : } V_o &= 107.755 \times (10mV - 5mV) + 0.892 \times ((10mV + 5mV)/2) \\ &= \mathbf{0.544V}.\end{aligned}$$

Measured value : $V_o = \mathbf{0.545 V}$. (Measured using Multimeter)

The value of output voltage V_o using the theoretical formula and the measured value are approximately the same.

- ★ The value of Common-Mode Rejection Ratio (CMRR) can be calculated using the formula:

$$CMRR = 20 \times \log \frac{A_d}{A_c}$$

$$CMRR = 20 \times \log(107.755/0.892) = \mathbf{41.624}.$$

EXPERIMENT 9

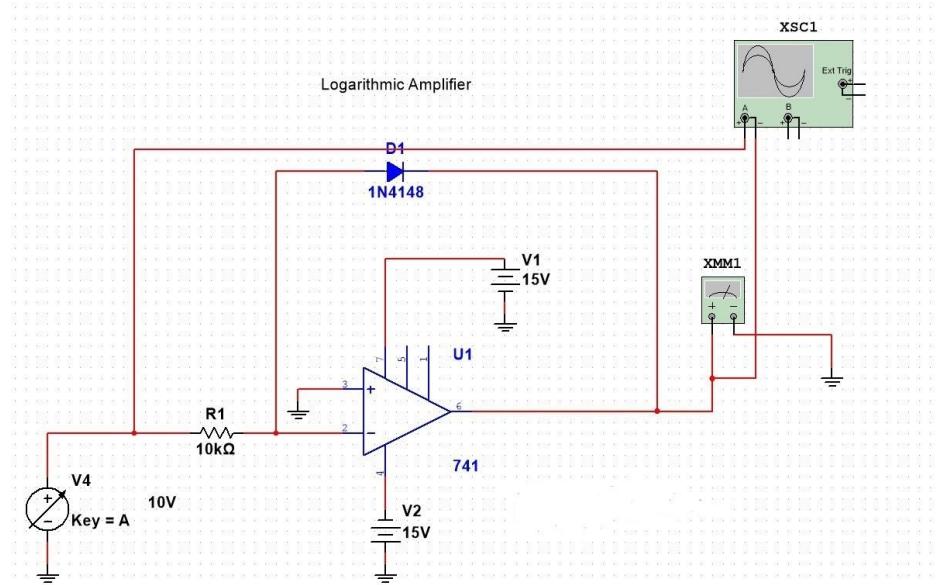
AIM: Design and determine the characteristics of logarithmic and anti-logarithmic amplifiers using OP-AMP and plot the outputs.

SOFTWARE USED : MULTISIM 14.1

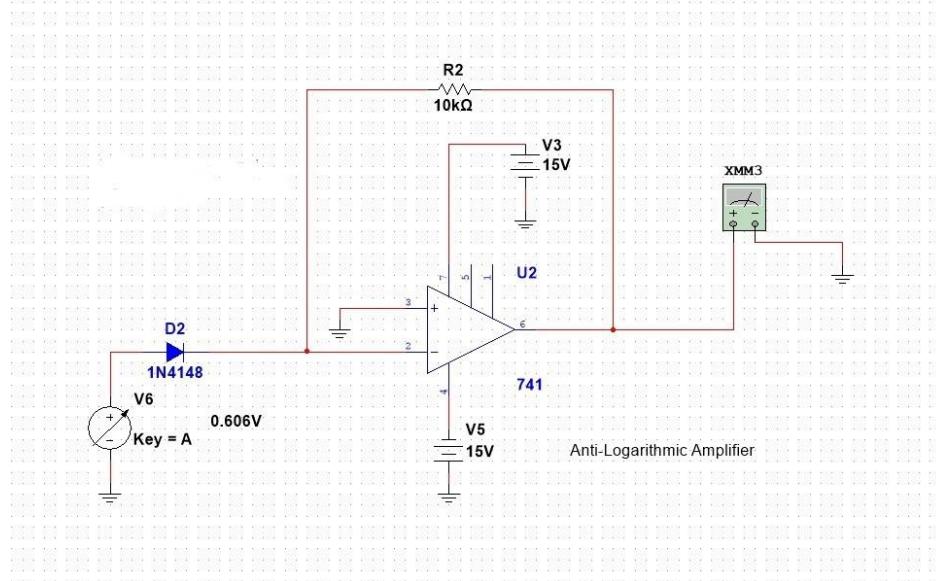
CIRCUIT DIAGRAM:

OBSERVATIONS:

- LOGARITHMIC AMPLIFIER:



- ANTI-LOGARITHMIC AMPLIFIER:



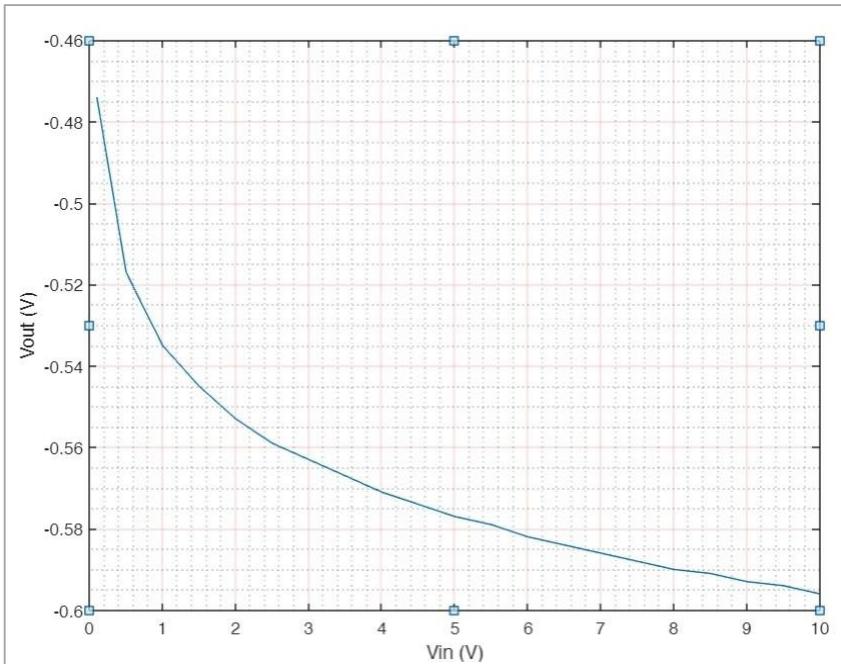
LOGARITHMIC AMPLIFIER:

V _{in} (V)	V _{out} (mV)
0.1	-474.97
0.5	-517.021
1.0	-535.073
1.5	-545.655
2.0	-555.183
2.5	-559.039
3.0	-563.838
3.5	-567.907
4.0	-571.422
4.5	-574.57
5.0	-577.376
5.5	-579.921
6.0	-582.253
6.5	-584.403
7.0	-586.401
7.5	-588.265
8.0	-590.015
8.5	-591.663
9.0	-593.222
9.5	-594.701
10.0	-596.107

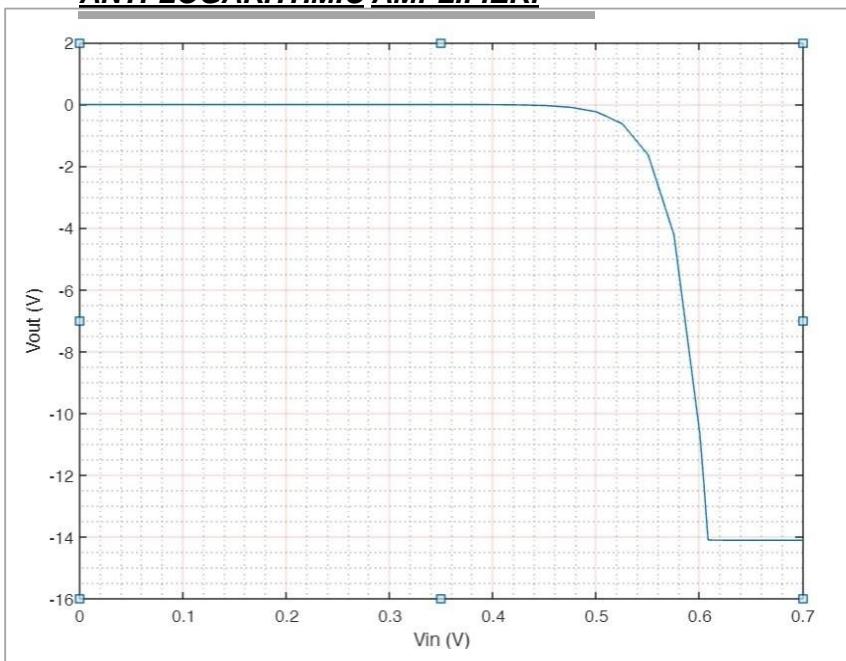
- **ANTI-LOGARITHMIC AMPLIFIER:**

V _{in} (V)	V _{out} (V)
0.0	0.0017
0.10	0.0017
0.20	0.0017
0.25	0.0017
0.30	0.0016
0.35	0.00009
0.375	-0.0002
0.40	-0.0032
0.425	-0.011
0.45	-0.032
0.475	-0.089
0.50	-0.236
0.525	-0.624
0.55	-1.633
0.575	-4.225
0.60	-10.66
0.606	-13.23
0.608	-14.11
0.625	-14.115
0.65	-14.116

- **LOGARITHMIC AMPLIFIER:**



ANTI-LOGARITHMIC AMPLIFIER:



RESULTS:

1. The output of the Logarithmic Amplifier is the $\log(V_{in})$ where V_{in} = Input voltage vs V_{out} (i.e Output voltage). This is verified by plotting the points obtained.
2. The output of the Anti-Logarithmic Amplifier is the $\text{antilog}(V_{in})$ where V_{in} = Input voltage vs V_{out} (i.e Output voltage). This is verified by plotting the points obtained.

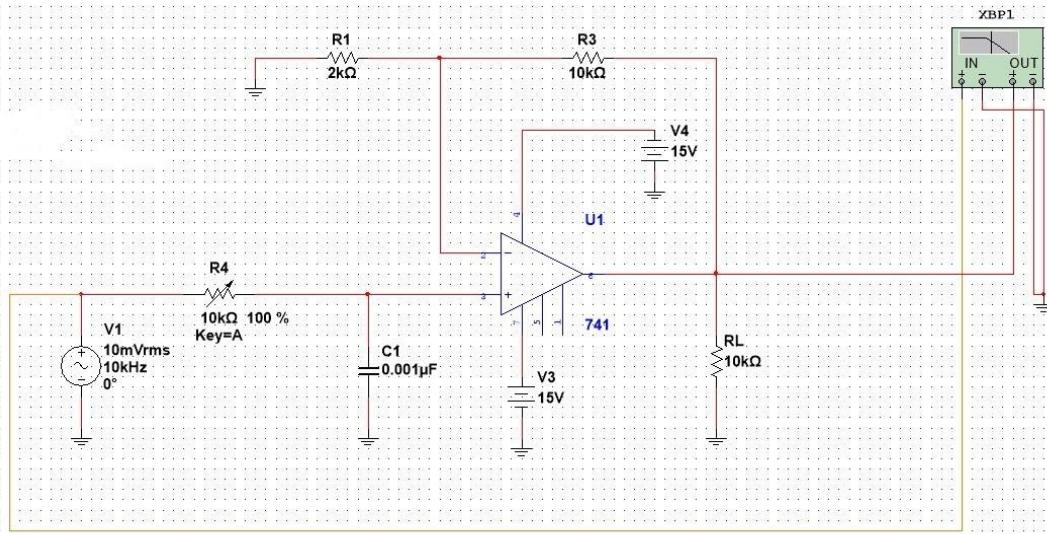
EXPERIMENT 10

AIM: Design a Low Pass filter, High Pass filter, Band Pass filter and Band Stop filter and find their frequency response.

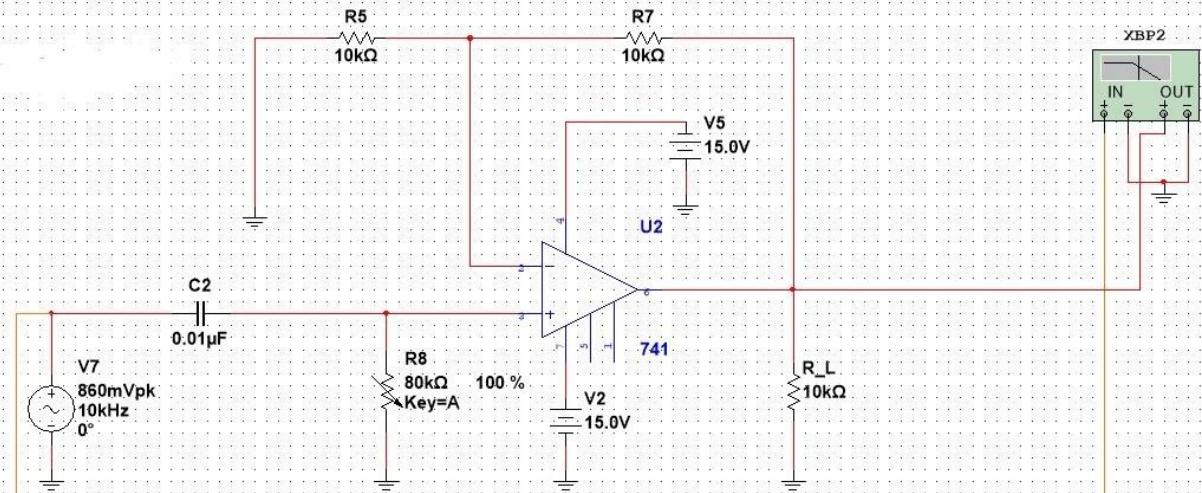
SOFTWARE USED: NI Multisim 14.1

CIRCUIT DIAGRAM:

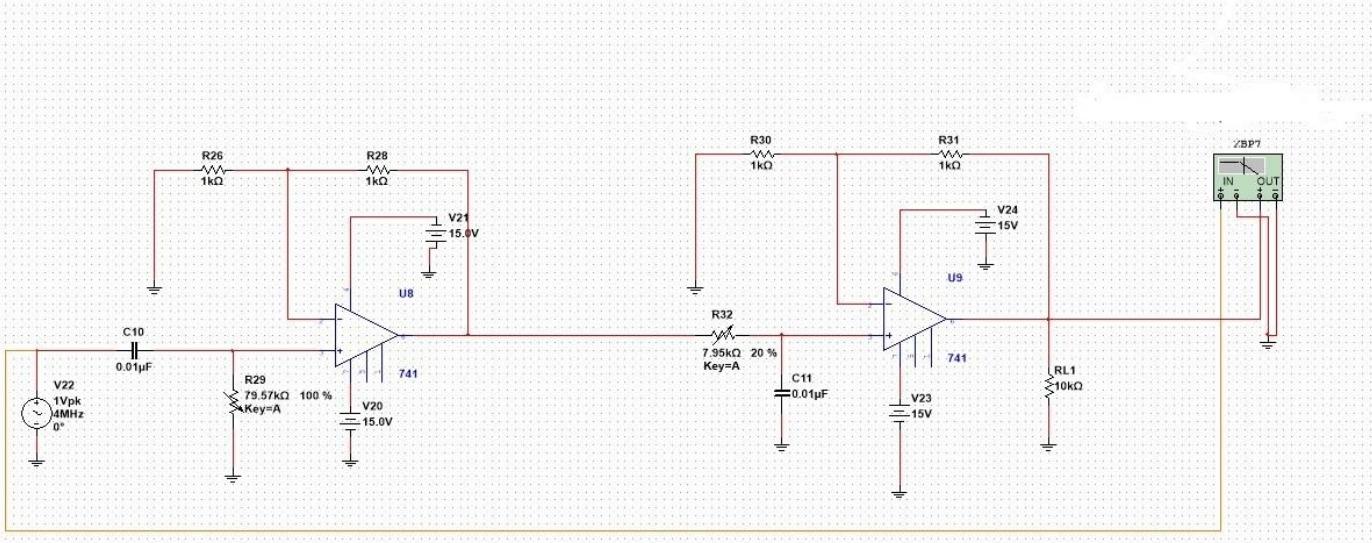
Low Pass:



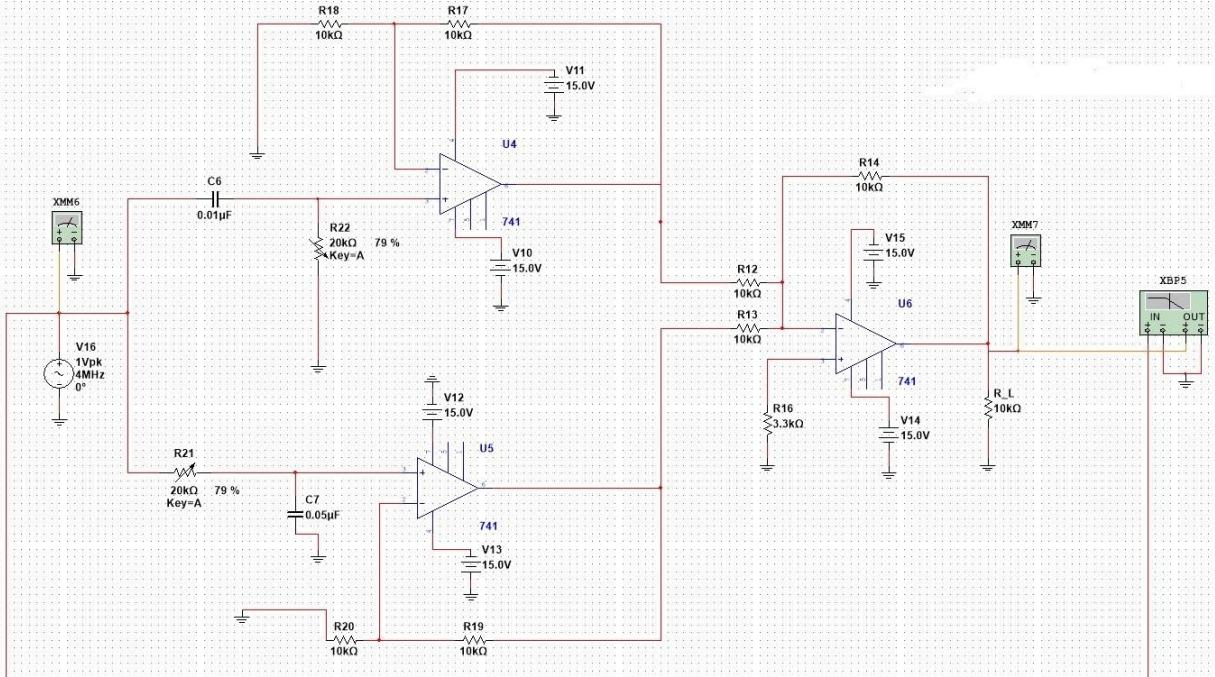
High Pass:



Band Pass: (Wide band)



Band Reject:(Wide Band):



OBSERVATIONS:

1. Low Pass Frequency Response :

Frequency (Hz)	Voltage Gain	dB Gain
1	5.92	15.53
100	5.92	15.53
500	5.93	15.56
1k	5.99	15.59

5k	5.81	15.22
10k	5.05	14.06
15.8k	4.23	12.53
50k	1.73	4.79
100k	0.80	-1.87
500k	0.05	-24.6
1M	0.01	-36.29
5M	0.0006	-64.30
10M	0.0001	-76.29
100M	0.000001	-118.0

2. High Pass Frequency Response :

Frequency (Hz)	Voltage Gain	dB Gain
1	0.0018	-54.8
50	0.49	-6.14
100	0.89	-0.92
198.7	1.41	3.01
500	1.85	5.38
1k	1.96	5.85
5k	1.99	6.01
10k	1.99	6.01
50k	1.99	6.01
100k	1.98	5.94
500k	1.77	4.99

3. Band Pass (Wide Band) Frequency Response:

Frequency (Hz)	Voltage Gain	dB Gain
1	0.02	-33.90
50	0.98	-0.13
100	1.79	5.07
193.3	2.77	8.87
500	3.71	11.38
1k	3.90	11.8
1.40k	3.92	11.86
5k	3.56	11.04
10k	2.79	8.99
10.43k	2.76	8.84
50k	0.76	-2.35
100k	0.37	-8.412
500k	0.03	-28.34

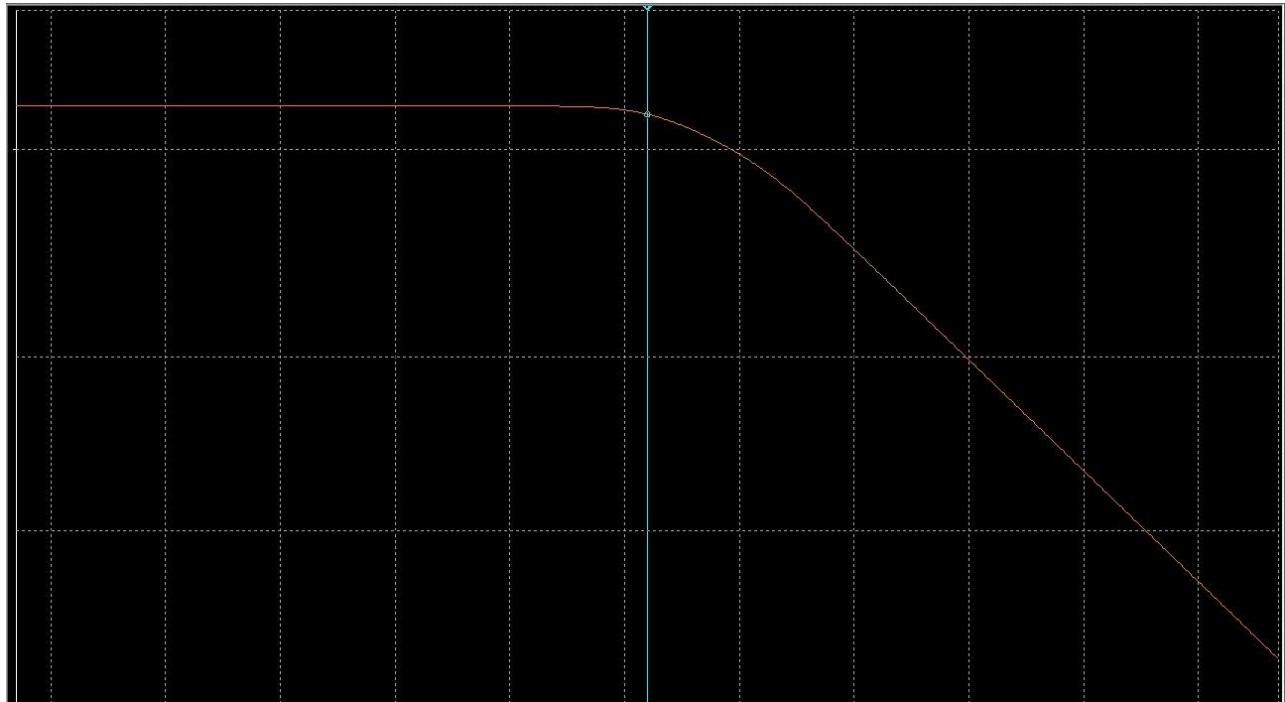
4. Band Reject (Wide Band) Frequency Response:

Frequency (Hz)	Voltage Gain	dB Gain
1	2.00	6.02
50	1.92	5.68
100	1.72	4.74
277.6	0.94	-0.52
449.3	0.66	-3.52
500	0.68	-3.31
732.4	0.94	-0.52
1k	1.24	1.88
5k	1.94	5.80
10k	1.98	5.95
50k	1.97	5.91

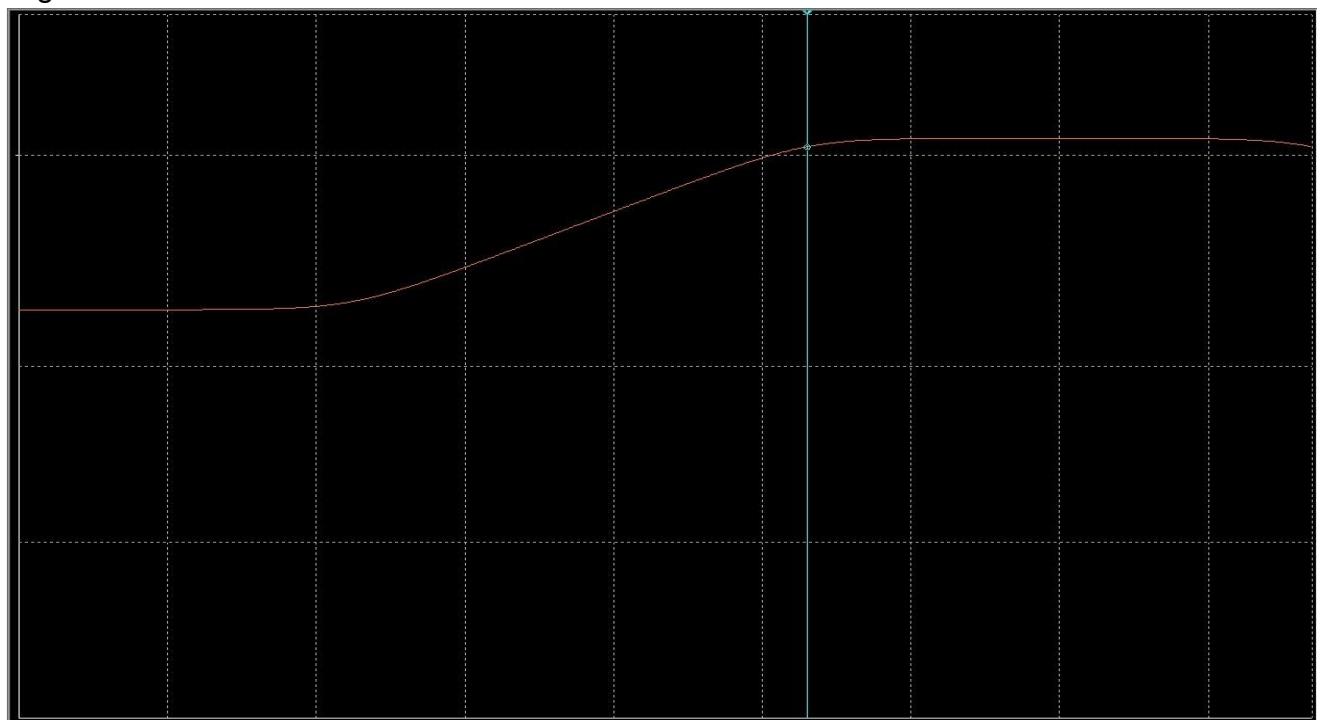
100k	1.96	5.85
500k	1.86	5.43

Bode Plotter:

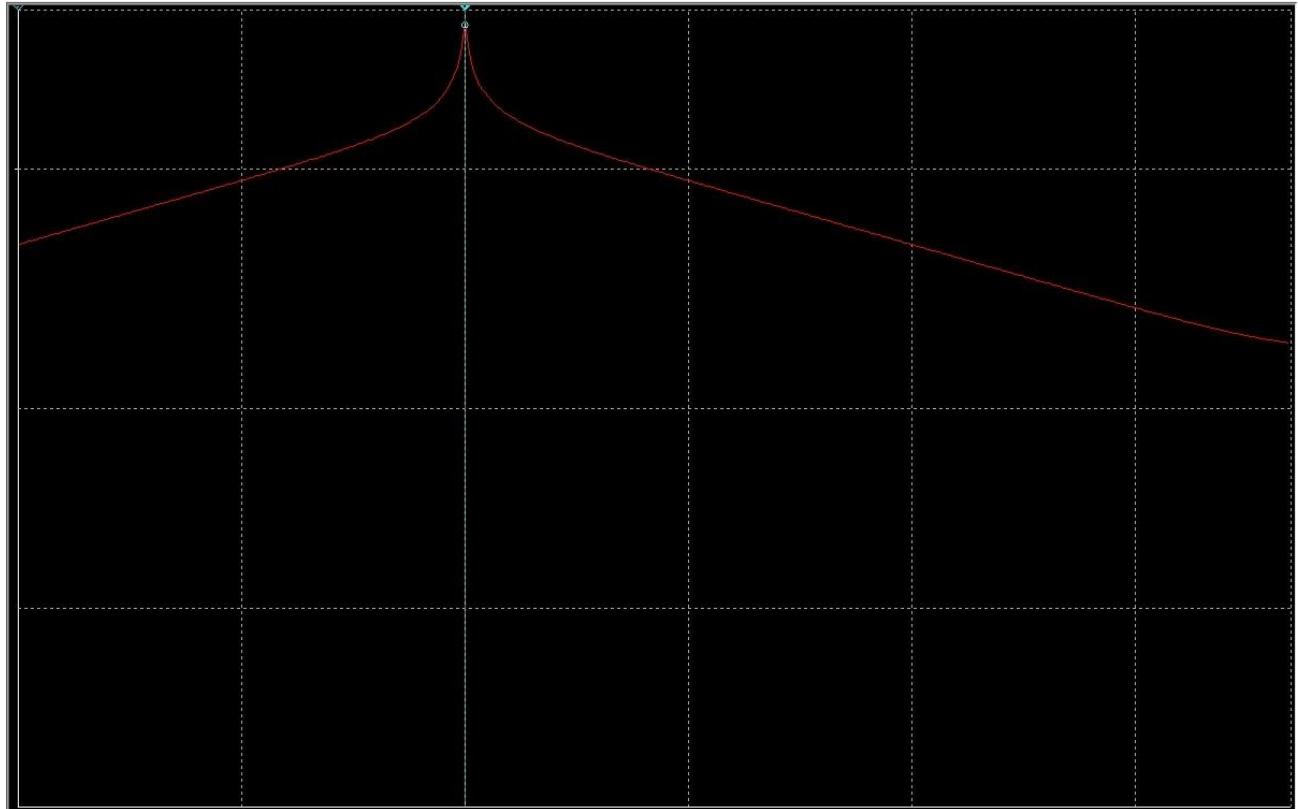
1. Low Pass Filter:



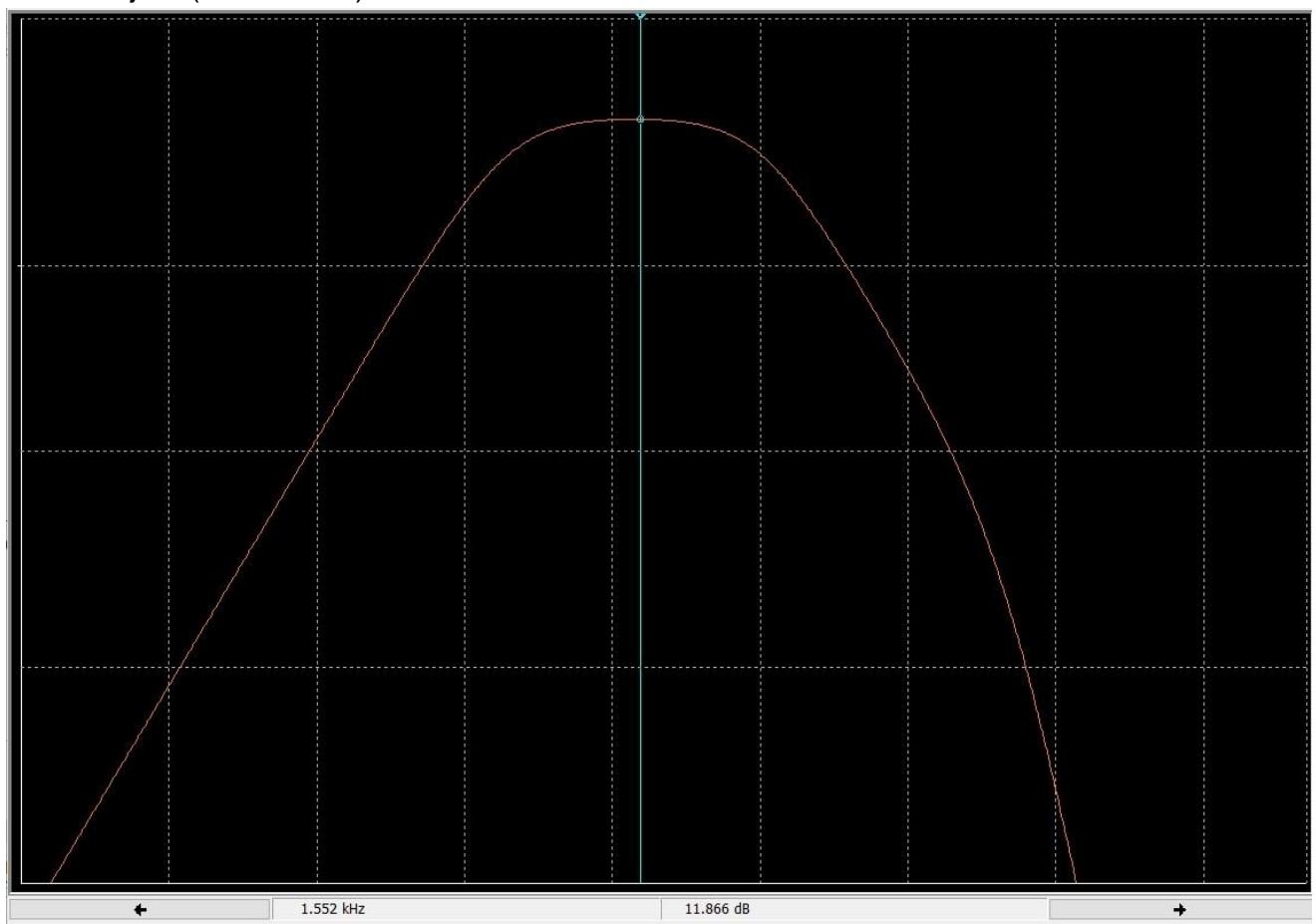
2. High Pass Filter:



3. Band Pass (Wide Band) Filter:



4. Band Reject (Wide Band) Filter:



Conclusion:

Performing the experiment, it can be concluded that :

1. For the First Order Low Pass Filter, the cut-off frequency (Fc) is Measured
Value : $F_c = 15.811 \text{ kHz}$ and it matches the theoretically calculated value.

2. For the First Order High Pass Filter, the cut-off frequency (Fc) is Measured
Value : $F_c = 198.783 \text{ Hz}$. and it matches the theoretically calculated value.

3. For the First Order Band Pass Filter (Wide Band), the Frequencies are :

Measured Value :

$F_n = 1.404 \text{ kHz}$.

$F_H = 10.43 \text{ kHz}$

$F_L = 193 \text{ Hz}$

and it matches the theoretically calculated value.

4. For the First Order Band Reject Filter (Wide Band), the Frequencies are
Measured Value :

$F_m = 449.372 \text{ Hz}$.

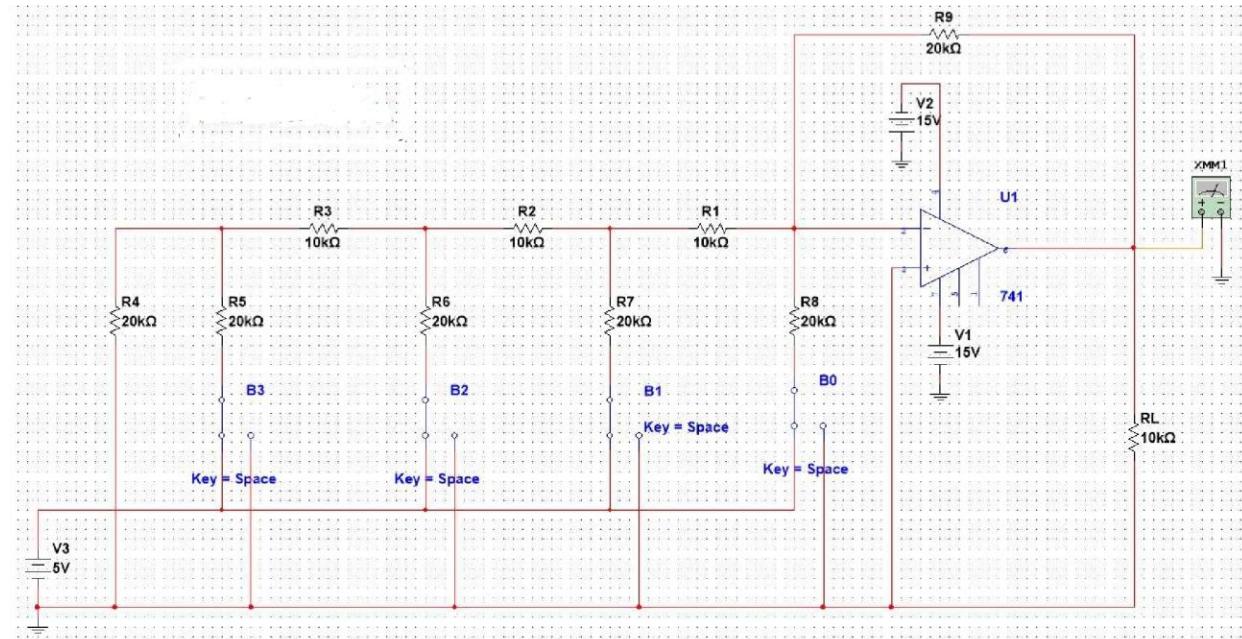
$F_H = 732 \text{ Hz}$

$F_L = 277 \text{ Hz}$. and it matches the theoretically
calculated value.

EXPERIMENT 11

AIM : Design a R-2R Ladder Digital to Analog Converter and find the resolution of the circuit.

CIRCUIT DIAGRAM :



OBSERVATIONS ($V_{ref} = 5 \text{ V}$) :

B3	B2	B1	B0	$V_{out} (\text{V})$
0	0	0	0	4.473m
0	0	0	1	-4.995
0	0	1	0	-2.495
0	0	1	1	-7.495
0	1	0	0	-1.246
0	1	0	1	-6.245
0	1	1	0	-3.745
0	1	1	1	-8.745

1	0	0	0	-620.518m
1	0	0	1	-5.62
1	0	1	0	-3.12
1	0	1	1	-8.12
1	1	0	0	-1.87
1	1	0	1	-6.87
1	1	1	0	-4.37
1	1	1	1	-9.37

RESULTS AND CONCLUSION:

Performing the experiment, it can be concluded that the R-2R Ladder Digital to Analog Converter han been designed successfully.

- The above configuration has $V_{ref} = 5V$; $R = RL = 10 k\Omega$ and $2R = R_f = 20 k\Omega$.

For Input bits = 1111 ;

Theoretical value of the Output Voltage is:

$$V_{out} = -\frac{R_f}{R} \times V_{ref} \times \left(\frac{B_0}{16} + \frac{B_1}{8} + \frac{B_2}{4} + \frac{B_3}{2} \right)$$

$$V_{out} = -\frac{20k\Omega}{10k\Omega} \times 5 \times \left(\frac{1}{16} + \frac{1}{8} + \frac{1}{4} + \frac{1}{2} \right) = -9.375V$$

Measured Value of the Output Voltage is:

$$V_{out} = -9.37V$$

Hence the calculated error percentage is **0.053%**.

- The resolution of above DAC is :

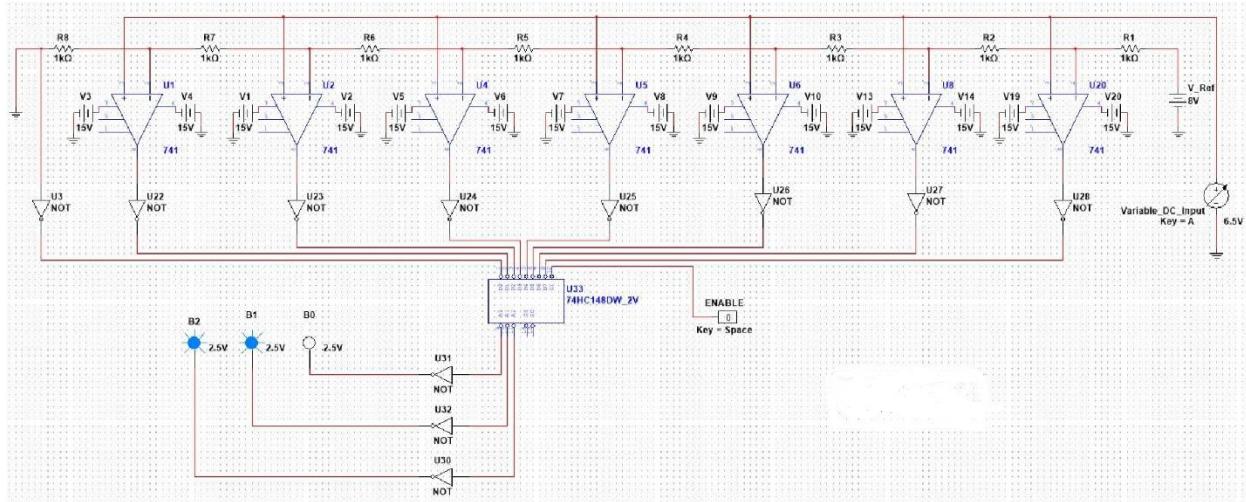
$$\text{Resolution} = \frac{V_{ref}}{2^n} \quad (\text{n is number of bits})$$

$$\text{Resolution} = \frac{5}{2^4} = 0.3125\%.$$

EXPERIMENT 12

AIM : Design a Flash Type Analog to Digital Converter using comparator and priority encoder.

CIRCUIT DIAGRAM :



OBSERVATIONS ($V_{ref} = 8V$ and Interactive DC Input as Analog Input) :

Analog Input Range (V)	DC Interactive Input (V)	B2	B1	B0
0 - 1	0.5	0	0	0
1 - 2	1.5	0	0	1
2 - 3	2.5	0	1	0
3 - 4	3.5	0	1	1
4 - 5	4.5	1	0	0
5 - 6	5.5	1	0	1
6 - 7	6.5	1	1	0

7 - 8	7.5	1	1	1
8 - 9	8.5	1	1	1

RESULTS AND CONCLUSION :

Performing the experiment it can concluded that, Flash Type Analog To Digital Converter has been designed successfully. In the experiment, an Interactive DC Voltage has been used to immitate Analog Input because Interactive DC Voltage can be controlled using knob and output can be observed easily while Analog Input has high frequency and the variations in the output are not visible to human eyes.

Using the comparator a 1-bit ADC has been made where the Analog Input (Interactive DC Voltage) is being compared with Vref divided at each comparator by voltage divider rule using same resistors. Priority Encoder has been used to encode 8 bit comparator output into 3 binary bit (B2, B1, B0) output.

For example, If Analog input is between 6-7 V, then output of the comparators i.e. D0-D6 is HIGH (1) and D7 is LOW (0) because Vref for comparator U8 is 6V (using Voltage divider rule) and all comparators till U8 gives output HIGH (1), hence, total 8-bit output is 11111110. This input to Priority encoder gives binary output 110.