VIVEKANAND EDUCATION SOCIETY'S INSTITUTE OF TECHNOLOGY

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B.E. PROJECT REPORT ON

DESIGNING & TESTING OF RECONFIGURABLE ADC USING RAMP GENERATION TECHNIQUE

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS OF THE DEGREE OF BACHELOR OF ENGINEERING ELECTRONICS

DEPT. OF ELECTRONICS ENGINEERING

UNIVERSITY OF MUMBAI

Academic Year: 2014-2015

Vivekanand Education Society's Institute of Technology

DEPARTMENT OF ELECTRONICS

CERTIFICATE

This is to certify that the project entitled "**Designing & Testing of Reconfigurable ADC using Ramp Generation Technique"** is a bonafide work of **Darshan Kulkarni (36), Nikhil Mattani (42), Shobhit Mittal (44), Priyal Nile (52)** submitted to the University of Mumbai in partial fulfillment of the requirements of the B.E. Degree in Electronics under the guidance of **Prof. Mrs. Jaymala Honmane** during the year 2014-15 as prescribed by Mumbai University.

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Project Report Approval for B. E.

This thesis / dissertation/project report entitled ***DESIGNING & TESTING OF RECONFIGURABLE ADC USING RAMP GENERATION TECHNIQUE*** by ***Darshan Kulkarni, Nikhil Mattani, Shobhit Mittal & Priyal Nile*** is approved for the degree of **Bachelor of Engineering.**

Examiners

1. ----------

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DECLARATION

We declare that this written submission represents our ideas in our own words and where others' ideas or words have been included, we have adequately cited and referenced the original sources. We also declare that we have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in our submission. We understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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(Name of student and Roll No.) (Signature)

Date:

ACKNOWLEDGEMENT

We express our sincere gratitude to **Prof. Jaymala Honmane**, our internal guide, for her valuable advice, support and guidance throughout this project work. We also thank her for her motivation and patience. We would also like to take this opportunity to thank **Prof. Abhijit Shete**, and our HOD, **Prof. Kavita Tewari**, for their encouragement and guidance.

We would also like to thank all the staff members who helped us in this project.

We are also grateful to our friends and families for their unconditional support and sincere feedback about the project, which has helped us to improve our work.

Our sincere thanks to the management of Vivekanand Education Society's Institute Of Technology for giving us required facilities to accomplish our project work.

ABSTRACT

Reconfigurable 12 bit integrating ADC (Analog to Digital Converter) will be designed using ramp generation technique. To achieve the reconfigurability in single slope ADC we need to change the slope of ramp. This change in slope changes the resolution & conversion Time. There are different ways to change the slope of ADC. If we change the capacitor value or current value, Reconfigurability with respect to resolution and conversion time can be achieved. But, as resolution increases conversion time also increases. So to reduce the conversion time and to achieve the better resolution we need to obtain multiple slopes of Ramp during the conversion only. Generation of ramp with multiple slopes can be achieved by changing the controlling bits.

DAC with integrator is used to generate the ramp. This ramp signal is added with the input singal then it is compared with LSB. As soon as the input goes below LSB, the comparator output sets the flip flop & change the current through DAC. As the current changes the slope of ramp also changes. The current is decreased so slope of ramp chnages slowly & it takes many clock cycles. So resolution increases.

So we can reconfigure single slope ADC by reconfiguring slope of ramp with maximum resolution & optimum conversion time.

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