

# **VIVEKANAND EDUCATION SOCIETY'S INSTITUTE OF TECHNOLOGY**

Collector's Colony, Chembur-400074



## **B.E. PROJECT REPORT ON DESIGNING & TESTING OF RECONFIGURABLE ADC USING RAMP GENERATION TECHNIQUE**

SUBMITTED BY:

**Darshan Kulkarni (36)**

**Nikhil Mattani (42)**

**Shobhit Mittal (44)**

**Priyal Nile (52)**

Under the Guidance of

**Prof. Jaymala Honmane**

**IN PARTIAL FULFILLMENT OF THE REQUIREMENTS OF THE DEGREE OF  
BACHELOR OF ENGINEERING ELECTRONICS**

**DEPT. OF ELECTRONICS ENGINEERING**

**UNIVERSITY OF MUMBAI**

Academic Year: 2014-2015



Vivekanand Education Society's Institute of Technology

DEPARTMENT OF ELECTRONICS

**CERTIFICATE**

This is to certify that the project entitled “**Designing & Testing of Reconfigurable ADC using Ramp Generation Technique**” is a bonafide work of **Darshan Kulkarni (36), Nikhil Mattani (42), Shobhit Mittal (44), Priyal Nile (52)** submitted to the University of Mumbai in partial fulfillment of the requirements of the B.E. Degree in Electronics under the guidance of **Prof. Mrs. Jaymala Honmane** during the year 2014-15 as prescribed by Mumbai University.

(Name and sign)  
Supervisor/Guide

(Name and sign)  
Co-Supervisor/Guide

(Name and sign)  
Head of Department

(Name and sign)  
Principal

## Project Report Approval for B. E.

This thesis / dissertation/project report entitled ***DESIGNING & TESTING OF RECONFIGURABLE ADC USING RAMP GENERATION TECHNIQUE*** by ***Darshan Kulkarni, Nikhil Mattani, Shobhit Mittal & Priyal Nile*** is approved for the degree of **Bachelor of Engineering**.

Examiners

1. -----

2. -----

Date:

Place:

# DECLARATION

We declare that this written submission represents our ideas in our own words and where others' ideas or words have been included, we have adequately cited and referenced the original sources. We also declare that we have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in our submission. We understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

-----  
(Name of student and Roll No.)

-----  
(Signature)

Date:

# ACKNOWLEDGEMENT

We express our sincere gratitude to **Prof. Jaymala Honmane**, our internal guide, for her valuable advice, support and guidance throughout this project work. We also thank her for her motivation and patience. We would also like to take this opportunity to thank **Prof. Abhijit Shete**, and our HOD, **Prof. Kavita Tewari**, for their encouragement and guidance.

We would also like to thank all the staff members who helped us in this project.

We are also grateful to our friends and families for their unconditional support and sincere feedback about the project, which has helped us to improve our work.

Our sincere thanks to the management of Vivekanand Education Society's Institute Of Technology for giving us required facilities to accomplish our project work.

# ABSTRACT

Reconfigurable 12 bit integrating ADC (Analog to Digital Converter) will be designed using ramp generation technique. To achieve the reconfigurability in single slope ADC we need to change the slope of ramp. This change in slope changes the resolution & conversion Time. There are different ways to change the slope of ADC. If we change the capacitor value or current value, Reconfigurability with respect to resolution and conversion time can be achieved. But, as resolution increases conversion time also increases. So to reduce the conversion time and to achieve the better resolution we need to obtain multiple slopes of Ramp during the conversion only. Generation of ramp with multiple slopes can be achieved by changing the controlling bits.

DAC with integrator is used to generate the ramp. This ramp signal is added with the input signal then it is compared with LSB. As soon as the input goes below LSB, the comparator output sets the flip flop & change the current through DAC. As the current changes the slope of ramp also changes. The current is decreased so slope of ramp changes slowly & it takes many clock cycles. So resolution increases.

So we can reconfigure single slope ADC by reconfiguring slope of ramp with maximum resolution & optimum conversion time.

# TABLE OF CONTENT

<b>CHAPTER 1: INTRODUCTION</b>	<b>01</b>
1.1 Application And Reconfigurability Of ADCs	04
1.2 Single Slope ADC	05
1.3 Dual Slope ADC	06
<b>CHAPTER 2: LITERATURE SURVEY</b>	<b>08</b>
2.1. Basic Building Block Of Reconfigurability	09
2.2. Comparison Of Conventional ADC With Reconfigurable ADC	10
<b>CHAPTER 3: PARAMETERS OF ADC</b>	<b>11</b>
3.1 Resolution	12
3.2 Quantisation Error	13
3.3 Dither	14
3.4 Accuracy	14
3.5 Non Linearity	14
3.6 Jitter	15
3.7 Sampling Rate	16
3.8 Aliasing	16
3.9 Oversampling	17
<b>CHAPTER 4: HARDWARE DESCRIPTION</b>	<b>18</b>
4.1 IC AD7541AKN	19
4.2 IC LF356	20
4.3 IC LM311P	20
4.4 IC ADG201HS	21
4.5 IC 7400	21
4.6 IC SN74LS157	22
<b>CHAPTER 5: PRINCIPLE</b>	<b>23</b>
5.1 Calculations	25

<b>CHAPTER 6: WORKING AND BLOCK DIAGRAMS</b>	<b>27</b>
6.1 Stage 1	28
6.2 Stage 2	29
6.3 Stage 3	30
6.4 Block Diagram Description	31
6.4.1 Ramp Generator	31
6.4.2 Adder	31
6.4.3 Comparator	32
6.4.4 Control Block	32
6.5 Illustration	33
 <b>CHAPTER 7: ANALYSIS, EXPERIMENTATION &amp; RESULT</b>	 <b>34</b>
7.1 PCB Fabrication	35
7.2 Designing Of Layout	35
7.3 Soldering	36
7.4 Troubleshooting	36
7.5 Schematic of PCB	37
7.6 PCB Layout	38
7.7 Negative of PCB	38
7.8 Readings	39
7.9 Waveform Obtained	41
 <b>CHAPTER 8: FUTURE SCOPE</b>	 <b>43</b>
 <b>CHAPTER 9: APPLICATIONS</b>	 <b>45</b>
9.1 Music Recording	46
9.2 Digital Signal Processing	46
9.3 Scientific Instruments	46
 <b>CHAPTER 10: CONCLUSION</b>	 <b>47</b>
 <b>CHAPTER 11: REFERENCES</b>	 <b>49</b>
 <b>CHAPTER 12: APPENDIX</b>	 <b>50</b>
 <b>CHAPTER 13: DATASHEETS</b>	 <b>51</b>



# LIST OF FIGURES

<b>Figure No.</b>	<b>Title</b>	<b>Page No.</b>
Figure 1	Comparison Between ADC Architecture	4
Figure 2	Integrating Single Slope ADC	5
Figure 3	Dual Slope Integrating ADC	6
Figure 4	Output Waveform Of Dual Slope ADC	7
Figure 5	Structure Of Basic Building Block	9
Figure 6	An 8-level ADC Coding Scheme	12
Figure 7a	R-2R Ladder	19
Figure 7b	Pinout of AD7541 DAC	19
Figure 8	Pinout of LF356	20
Figure 9	Pinout of LM311	20
Figure 10	Pinout of ADG201	21
Figure 11	Pinout of 7400 NAND Gate	21
Figure 12	Pinout of 74157 Quad SPST Switch	22
Figure 13	Comparison of ADC Based on No. of Bits Used	24
Figure 14	Resolution Vs Conversion Time	26
Figure 15	Stage 1	28
Figure 16	Stage 2	29
Figure 17	Stage 3	30
Figure 18	Ramp Generator	31

Figure 19	Adder	31
Figure 20	Comparator	32
Figure 21	Negative Slope	32
Figure 22	Schematic of PCB	37
Figure 23	PCB Layout	38
Figure 24	Negative of PCB	38
Figure 25	Phase 1 Output	41
Figure 26	Zoomed Output	42
Figure 27	The Reconfigurable Converter Prototype	44
Figure 28	Electrical Symbol OF ADC	48

## LIST OF TABLES

<b>Table No.</b>	<b>Title</b>	<b>Page No.</b>
1	Comparison of ADC Techniques	4
2	Signal Frequency	15
3	Comparator Output	32
4	Testing of DAC	39
5A	MSB at Logic High (1)	40
5B	LSB at Logic High (1)	40