CHAPTER 1
INTRODUCTION

An analog-to-digital converter (ADC, A/D, or A to D) is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

The conversion involves quantization of the input, so it necessarily introduces a small amount of error. Instead of doing a single conversion, an ADC often performs the conversions ("samples" the input) periodically. The result is a sequence of digital values that have been converted from a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal.

An ADC is defined by its bandwidth (the range of frequencies it can measure) and its signal to noise ratio (how accurately it can measure a signal relative to the noise it introduces). The actual bandwidth of an ADC is characterized primarily by its sampling rate, and to a lesser extent by how it handles errors such as aliasing. The dynamic range of an ADC is influenced by many factors, including the resolution (the number of output levels it can quantize a signal to), linearity and accuracy (how well the quantization levels match the true analog signal) and jitter (small timing errors that introduce additional noise). The dynamic range of an ADC is often summarized in terms of its effective number of bits (ENOB), the number of bits of each measure it returns that are on average not noise. An ideal ADC has an ENOB equal to its resolution. ADCs are chosen to match the bandwidth and required signal to noise ratio of the signal to be quantized. If an ADC operates at a sampling rate greater than twice the bandwidth of the signal, then perfect reconstruction is possible given an ideal ADC and neglecting quantization error. The presence of quantization error limits the dynamic range of even an ideal ADC, however, if the dynamic range of the ADC exceeds that of the input signal, its effects may be neglected resulting in an essentially perfect digital representation of the input signal.

An ADC may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current. However, some non-electronic or only partially electronic devices, such as rotary encoders, can also be considered ADCs. The digital output may use different coding schemes. Typically the digital output will be a two's complement binary number that is proportional to the input, but there are other possibilities. An encoder, for example, might output a Gray code.

The inverse operation is performed by a digital-to-analog converter (DAC).

Reconfigurable ADCs (analog to digital converter) are the ADCs which can be configured to obtain optimum performance with respect to important performance parameters such as resolution, conversion time and power dissipation etc. There is a requirement for development of such ADC in the field of multi-standard communication, wireless networking, software defined radio, sensors, etc.

If resolution of a conventional ADC is increased then there is an increase in its conversion time ultimately decreasing the speed.

But in Reconfigurable ADCs, we increase the resolution in such a way that the process gets completed in optimum conversion time.

However most of the ADCs utilized in field of electronics, communication and instrumentation are not presently reconfigurable. Because of fixed performance parameters, such ADC can't be used to the maximum capabilities for a given range of application.

There are several popular ADC architectures such as Flash, Successive Approximation, Sigma-Delta, cyclic and Pipeline etc. Each type of ADC is applicable for narrow of range of resolution, power dissipation as well as speed given by conversion time of ADC. Each ADC designed using a particular technique of Analog to Digital conversion gives fixed performance parameters like resolution and conversion time and can be used only for specific applications. These conventional ADCs with fixed method of conversion technique and parameters can't be efficiently employed for the task of digitizing signals over wide range of bandwidth at varying resolution with adaptive power consumption. An alternate approach is to employ an array of ADCs, each customized to work at narrow ranges of resolution and input bandwidth. Such a converter implementation would require a large number of ADCs to achieve optimal power consumption with a reasonably high resolution over input bandwidth.

The various A/D conversion techniques described here are useful for a given range of applications. However a single ADC with reconfigurable parameter and reconfigurable conversion technique would be able to achieve the goal for wider range of applications. Such ADCs will utilize the hardware which is reconfigurable leading to flexible resolution and can be optimized. Different methods will be researched and implemented to design adaptive and reconfigurable ADCs. These ADCs when developed will have much wide range of applications as compared to conventional ADCs. Efforts will be also made to design ADC for optimum power dissipation.

A comparison of application and reconfigurability of different A/D converters is given below.

1.1 Application and Reconfigurability of ADCs:

After the ADC concept was initially published in the middle 50's, different techniques have been developed. According to various parameters they have been classified as follows:-

Table 1.Comparison of ADC Techniques

Parameters	Flash	Pipeline	Cyclic	SA ADC	Σ Δ	Integration
Speed	Fastest	Fast	Medium	Medium	Low-medium	Low
Resolution	Lowest	Medium	Medium	Medium	High	Medium-high
Area	Largest	Medium	Smallest	Small	Medium	Medium
Power Efficiency	Lowest	Highest	Low	High	Medium	Medium
Reconfigurability	Low	High	Highest	Medium	High	Medium

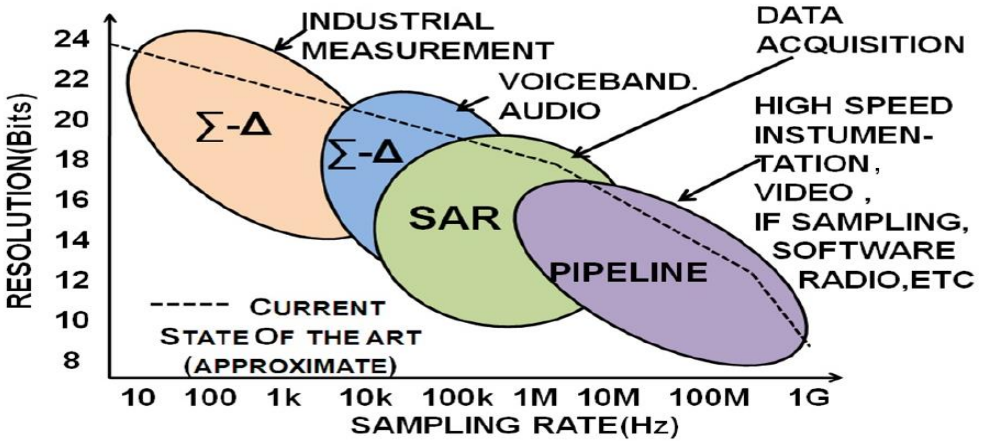


Figure 1.Comparison Between ADC Architecture

1.2 Single slope ADC

The simplest form of an integrating ADC uses a single-slope architecture [9] .It is Simplest form of ADC .The reference voltage is integrated and compared with the input . Time required for the reference signal to reach to input signal is counted by the stable oscillator and associated logic circuits.

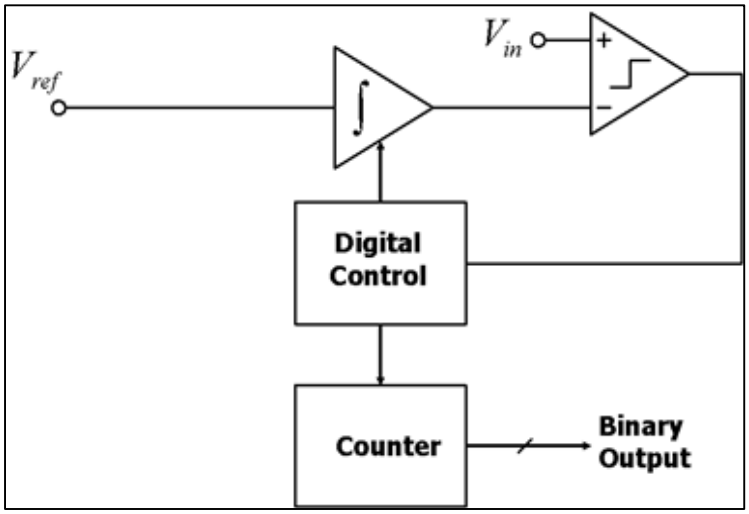


Figure 2. Integrating Single Slope ADC

Limitations:

- One drawback to this approach is that the accuracy is also dependent on the tolerances of the integrator's R and C values utilised to generate linear ramp. Thus in a production environment, slight differences in each component's value change the conversion result and make measurement repeatability quite difficult to attain.
- The analog signal is “noisy’ contains 50Hz noise.

  To overcome this sensitivity to the component values and noise, the dual-slope integrating architecture is used.

1.3 Dual Slope Integrating ADC

In the dual-slope A/D converter, an integrator circuit is driven positive and negative in alternating cycles to ramp down and then up, rather than being reset to 0 volts at the end of every cycle.

In one direction of ramping, the integrator is driven by the positive analog input signal for a fixed amount of time, as measured by a counter with a precision frequency clock. This fixed time is decided by power line frequency and is 20 milliseconds for supply frequency of 50 Hz.

Then, in the other direction, same integrator is driven with a fixed reference voltage with time measured by the same counter. The counter stops counting when the integrator's output reaches the same voltage as it was when it started the fixed-time portion of the cycle. The amount of time it takes for the integrator's capacitor to discharge back to its original output voltage, measured as number of clock pulses counted by the counter, becomes the digital output of the ADC circuit.

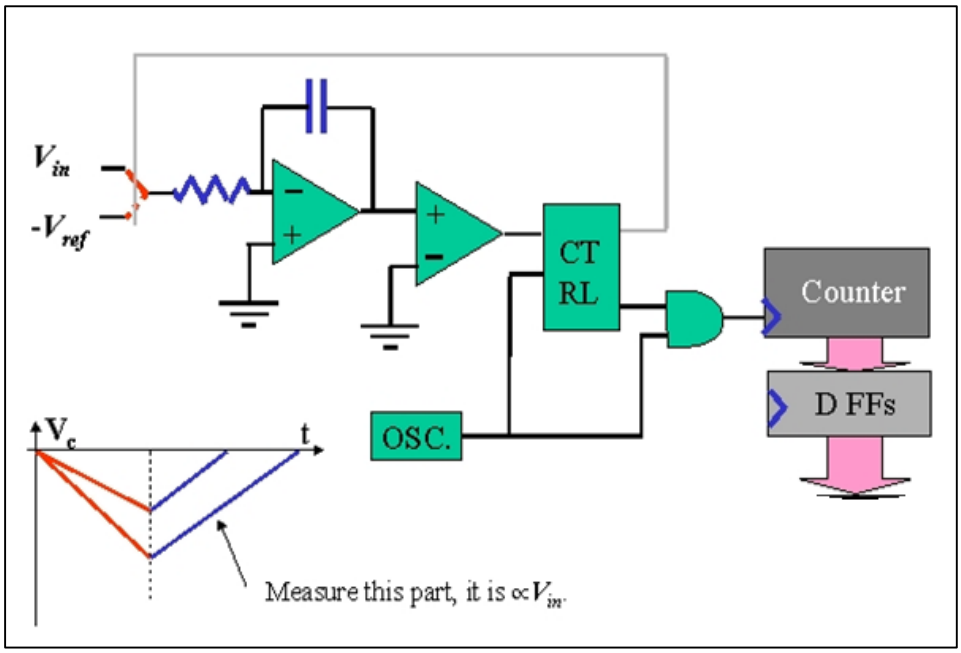


Figure 3.Dual Slope Integrating ADC

Dual Slope Operation

Phase I (autozero)	Phase II (signal integrate)	Phase III (reference integrate)

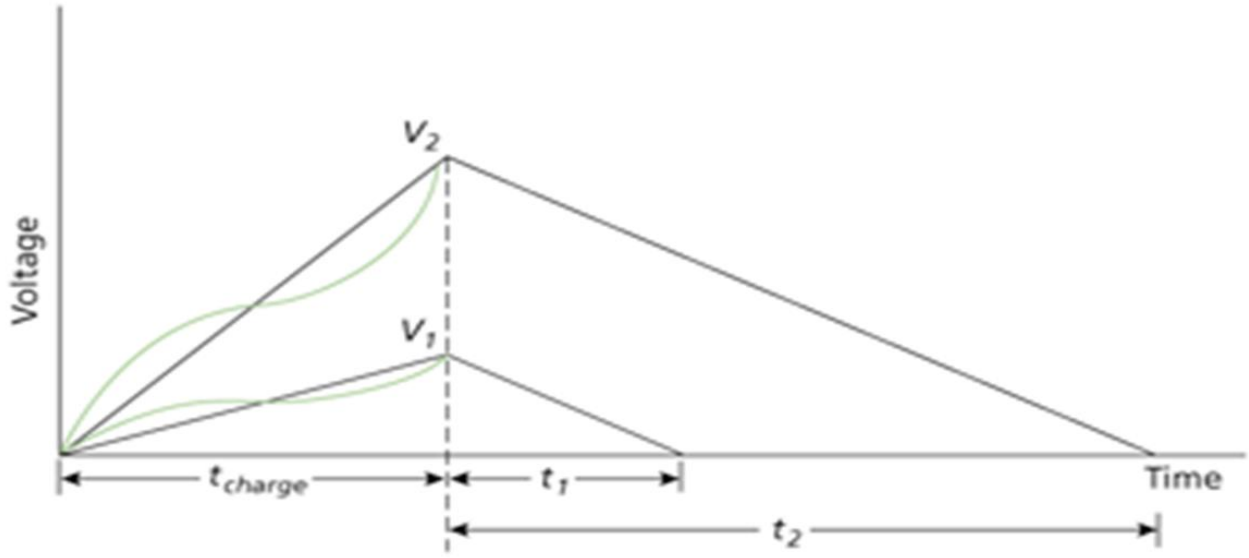


Figure 4. Output Waveform of Dual Slope ADC

Limitations:

- Slow, conversion time more than 20ms.
- High precision external components required to achieve accuracy.

CHAPTER 2

LITERATURE SURVEY

2.1 Basic Building Block of Reconfigurability

Recently studies are being done regarding the adaptivity and compatibility of the ADCs leading to adaptive and reconfigurable ADCs. However no systematic study has been done and reported in the literature regarding re-configurability of the ADCs. Hence all existing methods of ADC will be studied and analyzed from the point of view of concept of reconfigurability and adaptively. Currently Successive approximation register, Pipeline, Sigma-Delta and Flash ADCs have been implemented with variable resolution and bandwidth for low power dissipation purpose. Different methods have been used to implement these reconfigurable ADCs as reported in the literature described below.

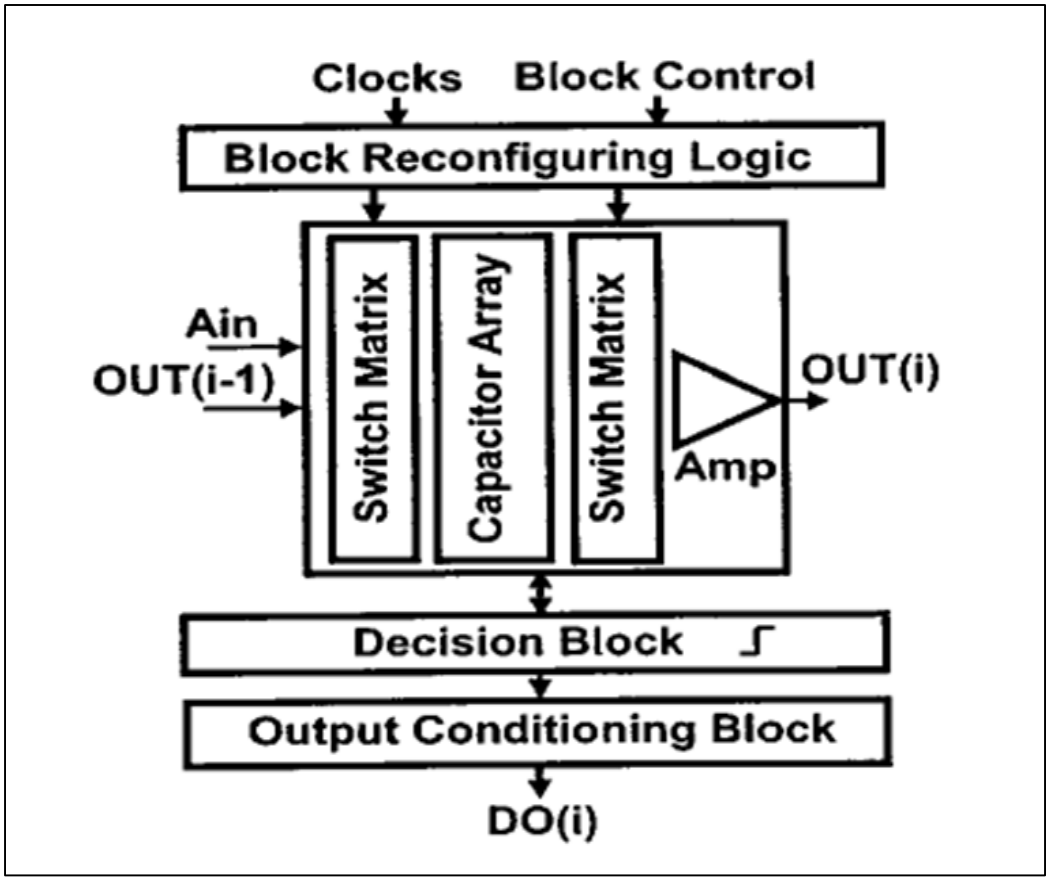


Figure 5. Structure of Basic Building Block

2.2 Comparison Of Conventional ADC With Reconfigurable ADC

Most of the ADCs utilized in field of electronics, communication and instrumentation are not presently reconfigurable. Because of fixed performance parameters, such ADC can't be used to the maximum capabilities for a given range of application.

There are several popular ADC architectures such as Flash, Successive Approximation, Sigma-Delta, cyclic and Pipeline etc. Each type of ADC is applicable for narrow of range of resolution, power dissipation as well as speed given by conversion time of ADC. Each ADC designed using a particular technique of Analog to Digital conversion gives fixed performance parameters like resolution and conversion time and can be used only for specific applications. These conventional ADCs with fixed method of conversion technique and parameters can't be efficiently employed for the task of digitizing signals over wide range of bandwidth at varying resolution with adaptive power consumption. An alternate approach is to employ an array of ADCs, each customized to work at narrow ranges of resolution and input bandwidth .Such a converter implementation would require a large number of ADCs to achieve optimal power consumption with a reasonably high resolution over input bandwidth.

A single ADC with reconfigurable parameter and recofigurable conversion technique would be able to solve all these problems and achieve the goal for wider range of applications. Such ADCs will utilize the hardware which is reconfigurable leading to flexible resolution and can be optimized. Different methods will be researched and implemented to design adaptive and reconfigurable ADCs.

CHAPTER 3

PARAMETERS OF ADC

3.1 Resolution

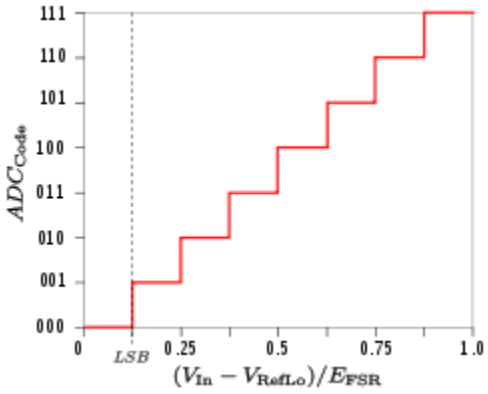


Figure 6. An 8-level ADC Coding Scheme.

The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The resolution determines the magnitude of the quantization error and therefore determines the maximum possible average signal to noise ratio for an ideal ADC without the use of oversampling. The values are usually stored electronically in binary form, so the resolution is usually expressed in bits. In consequence, the number of discrete values available, or "levels", is assumed to be a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$. The values can represent the ranges from 0 to 255 (i.e. unsigned integer) or from −128 to 127 (i.e. signed integer), depending on the application.

Resolution can also be defined electrically, and expressed in volts. The minimum change in voltage required to guarantee a change in the output code level is called the least significant bit (LSB) voltage. The resolution Q of the ADC is equal to the LSB voltage. The voltage resolution of an ADC is equal to its overall voltage measurement range divided by the number of discrete values:

$$Q = \frac{E_{\mathrm{FSR}}}{2^M},$$

where M is the ADC's resolution in bits and E_{FSR} is the full scale voltage range (also called 'span'). E_{FSR} is given by

$$E_{\mathrm{FSR}} = V_{\mathrm{RefHi}} - V_{\mathrm{RefLow}},$$

where V_{RefHi} and V_{RefLow} are the upper and lower extremes, respectively, of the voltages that can be coded.

Normally, the number of voltage intervals is given by

$$N = 2^M,$$

where M is the ADC's resolution in bits.[1]

That is, one voltage interval is assigned in between two consecutive code levels.

Example:

- Coding scheme as in figure 1 (assume input signal x(t) = Acos(t), A = 5V)
- Full scale measurement range = -5 to 5 volts
- ADC resolution is 8 bits: 2^8 = 256 quantization levels (codes)
- ADC voltage resolution, Q = (10 V − 0 V) / 256 = 10 V / 256 ≈ 0.039 V ≈ 39 mV.

In practice, the useful resolution of a converter is limited by the best signal-to-noise ratio (SNR) that can be achieved for a digitized signal. An ADC can resolve a signal to only a certain number of bits of resolution, called the effective number of bits (ENOB). One effective bit of resolution changes the signal-to-noise ratio of the digitized signal by 6 dB, if the resolution is limited by the ADC. If a preamplifierhas been used prior to A/D conversion, the noise introduced by the amplifier can be an important contributing factor towards the overall SNR.

3.2 Quantization error

Quantization error is the noise introduced by quantization in an ideal ADC. It is a rounding error between the analog input voltage to the ADC and the output digitized value. The noise is non-linear and signal-dependent.

In an ideal analog-to-digital converter, where the quantization error is uniformly distributed between −1/2 LSB and +1/2 LSB, and the signal has a uniform distribution covering all quantization levels, theSignal-to-quantization-noise ratio (SQNR) can be calculated from

$$\text{SQNR} = 20\log_{10}(2^Q) \approx 6.02 \cdot Q \text{ dB}$$

Where Q is the number of quantization bits. For example, a 16-bit ADC has a maximum signal-to-noise ratio of 6.02 × 16 = 96.3 dB, and therefore the quantization error is 96.3 dB below the maximum level. Quantization error is distributed from DC to the Nyquist frequency, consequently if part of the ADC's bandwidth is not used (as in oversampling), some of the quantization error will fall out of band, effectively improving the SQNR. In an oversampled system, noise shaping can be used to further increase SQNR by forcing more quantization error out of the band.

3.3 Dither

In ADCs, performance can usually be improved using dither. This is a very small amount of random noise (white noise), which is added to the input before conversion.

Its effect is to cause the state of the LSB to randomly oscillate between 0 and 1 in the presence of very low levels of input, rather than sticking at a fixed value. Rather than the signal simply getting cut off altogether at this low level (which is only being quantized to a resolution of 1 bit), it extends the effective range of signals that the ADC can convert, at the expense of a slight increase in noise – effectively the quantization error is diffused across a series of noise values which is far less objectionable than a hard cutoff. The result is an accurate representation of the signal over time. A suitable filter at the output of the system can thus recover this small signal variation.

3.4 Accuracy

An ADC has several sources of errors. Quantization error and (assuming the ADC is intended to be linear) non-linearity are intrinsic to any analog-to-digital conversion.

These errors are measured in a unit called the least significant bit (LSB). In the above example of an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%.

3.5 Non-linearity

All ADCs suffer from non-linearity errors caused by their physical imperfections, causing their output to deviate from a linear function (or some other function, in the case of a deliberately non-linear ADC) of their input. These errors can sometimes be mitigated by calibration, or prevented by testing.

Important parameters for linearity are integral non-linearity (INL) and differential non-linearity (DNL). These non-linearities reduce the dynamic range of the signals that can be digitized by the ADC, also reducing the effective resolution of the ADC.

3.6 Jitter

When digitizing a sine wave, the use of a non-ideal sampling clock will result in some uncertainty in when samples are recorded. Provided that the actual sampling time *uncertainty* due to the *clock jitter* is the error caused by this phenomenon can be estimated as. This will result in additional recorded noise that will reduce the effective number of bits (ENOB) below that predicted by quantization error alone.

The error is zero for DC, small at low frequencies, but significant when high frequencies have high amplitudes. This effect can be ignored if it is drowned out by the *quantizing error*. Jitter requirements can be calculated using the following formula:

$$\Delta t < \frac{1}{2^q \pi f_0},$$

Where, q is the number of ADC bits.

Table 2. Signal Frequency

Output size (bits)	Signal Frequency						
	1 Hz	1 kHz	10 kHz	1 MHz	10 MHz	100 MHz	1 GHz
8	1,243 µs	1.24 µs	124 ns	1.24 ns	124 ps	12.4 ps	1.24 ps
10	311 µs	311 ns	31.1 ns	311 ps	31.1 ps	3.11 ps	0.31 ps
12	77.7 µs	77.7 ns	7.77 ns	77.7 ps	7.77 ps	0.78 ps	0.08 ps
14	19.4 µs	19.4 ns	1.94 ns	19.4 ps	1.94 ps	0.19 ps	0.02 ps
16	4.86 µs	4.86 ns	486 ps	4.86 ps	0.49 ps	0.05 ps	–
18	1.21 µs	1.21 ns	121 ps	1.21 ps	0.12 ps	–	–
20	304 ns	304 ps	30.4 ps	0.30 ps	0.03 ps	–	–

Clock jitter is caused by phase noise. The resolution of ADCs with a digitization bandwidth between 1 MHz and 1 GHz is limited by jitter.

When sampling audio signals at 44.1 kHz, the anti-aliasing filter should have eliminated all frequencies above 22 kHz. The input frequency (in this case, < 22 kHz), not the ADC clock frequency, is the determining factor with respect to jitter performance.

3.7 Sampling Rate

The analog signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called the *sampling rate* or *sampling frequency* of the converter.

A continuously varying bandlimited signal can be sampled (that is, the signal values at intervals of time T, the sampling time, are measured and stored) and then the original signal can be *exactly* reproduced from the discrete-time values by an interpolation formula. The accuracy is limited by quantization error. However, this faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal. This is essentially what is embodied in the Shannon-Nyquist sampling theorem.

3.8 Aliasing

An ADC works by sampling the value of the input at discrete intervals in time. Provided that the input is sampled above the Nyquist rate, defined as twice the highest frequency of interest, then all frequencies in the signal can be reconstructed. If frequencies above half the Nyquist rate are sampled, they are incorrectly detected as lower frequencies, a process referred to as aliasing. Aliasing occurs because instantaneously sampling a function at two or fewer times per cycle results in missed cycles, and therefore the appearance of an incorrectly lower frequency. For example, a 2 kHz sine wave being sampled at 1.5 kHz would be reconstructed as a 500 Hz sine wave.

To avoid aliasing, the input to an ADC must be low-pass filtered to remove frequencies above half the sampling rate. This filter is called an *anti-aliasing filter*, and is essential for a practical ADC system that is applied to analog signals with higher frequency content. In applications where protection against aliasing is essential, oversampling may be used to greatly reduce or even eliminate it.

Although aliasing in most systems is unwanted, it should also be noted that it can be exploited to provide simultaneous down-mixing of a band-limited high frequency signal (see undersampling and frequency mixer). The alias is effectively the lower heterodyne of the signal frequency and sampling frequency.

3.9 Oversampling

Signals are often sampled at the minimum rate required, for economy, with the result that the quantization noise introduced is white noise spread over the whole pass band of the converter. If a signal is sampled at a rate much higher than the Nyquist rate and then digitally filtered to limit it to the signal bandwidth there are the following advantages:

- digital filters can have better properties (sharper roll-off, phase) than analogue filters, so a sharper anti-aliasing filter can be realised and then the signal can be downsampled giving a better result
- a 20-bit ADC can be made to act as a 24-bit ADC with 256× oversampling
- the signal-to-noise ratio due to quantization noise will be higher than if the whole available band had been used. With this technique, it is possible to obtain an effective resolution larger than that provided by the converter alone
- The improvement in SNR is 3 dB (equivalent to 0.5 bits) per octave of oversampling which is not sufficient for many applications. Therefore, oversampling is usually coupled with noise shaping (see sigma-delta modulators). With noise shaping, the improvement is 6L+3 dB per octave where L is the order of loop filter used for noise shaping. e.g. – a 2nd order loop filter will provide an improvement of 15 dB/octave.

Oversampling is typically used in audio frequency ADCs where the required sampling rate (typically 44.1 or 48 kHz) is very low compared to the clock speed of typical transistor circuits (>1 MHz). In this case, by using the extra bandwidth to distribute quantization error onto out of band frequencies, the accuracy of the ADC can be greatly increased at no cost. Furthermore, as any aliased signals are also typically out of band, aliasing can often be completely eliminated using very low cost filters.

The key parameters to test a SAR ADC are the following:

1. DC Offset Error
2. DC Gain Error
3. Signal to Noise Ratio (SNR)
4. Total Harmonic Distortion (THD)
5. Integral Non Linearity (INL)
6. Differential Non Linearity (DNL)
7. Spurious Free Dynamic Range
8. Power Dissipation

CHAPTER 4

HARDWARE DESCRIPTION

The components used are

1. **IC AD7541AKN -** 12 bit DAC
2. **IC LF 356 –** JFET opamp
3. **IC LM 311P -** Voltage Comparator
4. **IC ADG201HS –** High Speed Quad SPST Switch
5. **IC SN74LS00N –** NAND Gate
6. **IC SN74LS157N-** Quad 2 input Mux
7. Resistors and Capacitors

Specifications and Justifications:

4.1] IC AD7541AKN - 12 Bit DAC

- Low settling time and High resolution
- 12 Bit monolithic Multiplying DAC with 18 Lead DIP
- Vdd = +15V
- Reference Voltage = +10V

Pin Configurations:

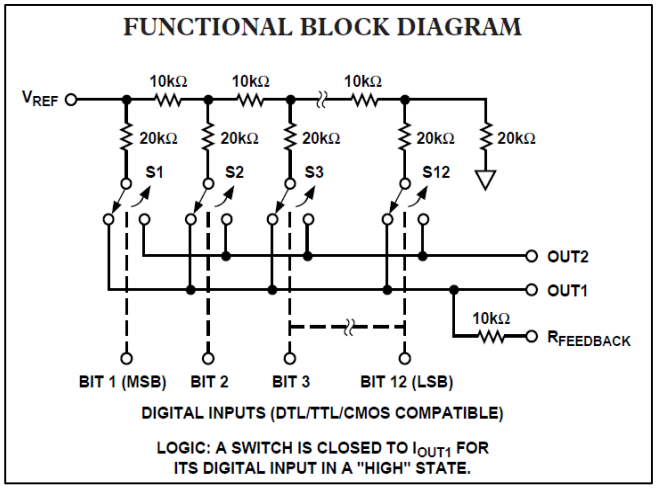


Figure 7a. R-2R Ladder

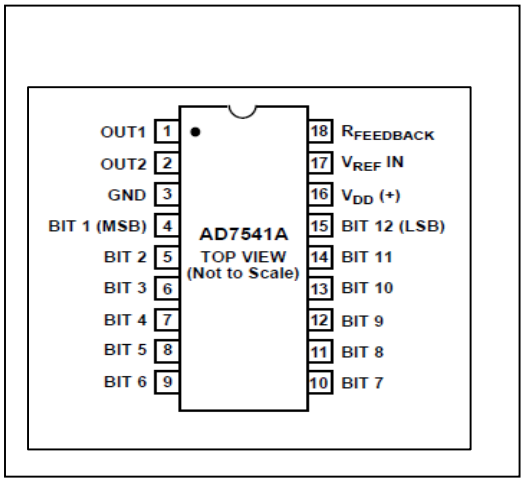


Figure 7b. Pinout of AD7541 DAC

4.2] IC LF356 – JFET OPAMP

- Low Bias Current, Moderate bandwith , Medium Slew Rate
- High input impedance JFET input stage
- High Speed J-FET OP-AMPs : up to 20MHz,50V/ms
- Offset Voltage Adjustment does not degrade drift or common mode rejection as in most of monolithic amplifiers
- Internal Compensation and large differential input voltage capability (upto Vcc+)

Pin Configurations:

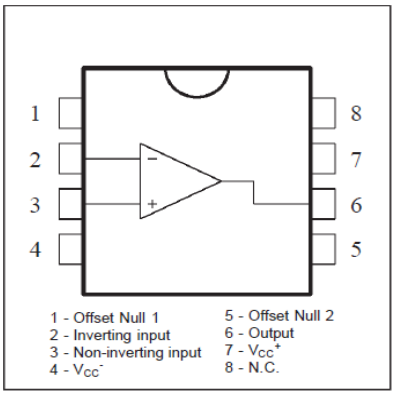


Figure 8. Pinout of LF356

4.3]IC LM 311P - Voltage Comparator

- Low input bias current : 250nA (Max)
- Low input offset current : 50nA (Max)
- Differential Input Voltage : ±30V
- Power supply voltage : single 5.0V supply to ±15V.
- Offset voltage null capability.
- Strobe capability.

Pin Configurations:

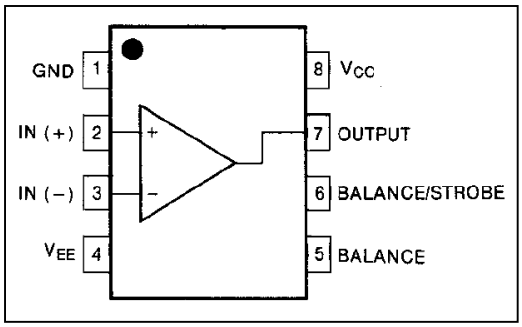


Figure 9. Pinout of LM311

4.4] **ADG201HS –** Analog Switch

- Monolithic CMOS Device
- 4 Independent SPST Switches
- Fast Switching Speed
- Low Ron.

Pin Configurations:

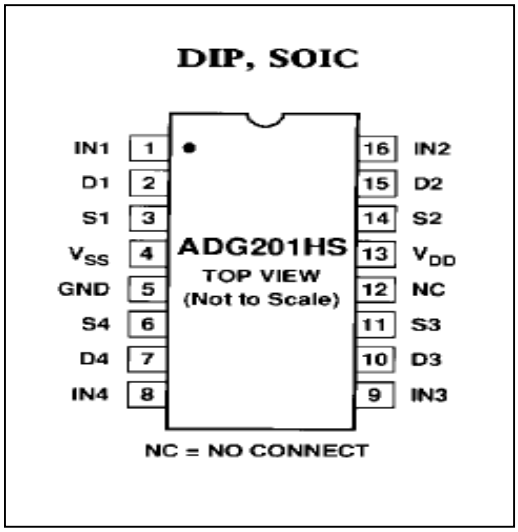


Figure 10. Pinout of ADG201

4.5] **IC 7400 -** NAND Gate

Pin Configurations:

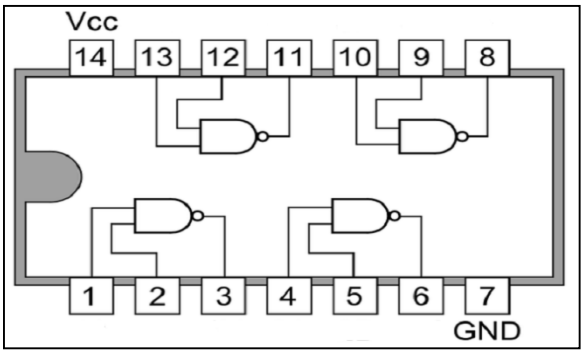


Figure 11. Pinout of 7400 NAND Gate

4.6] **SN74LS157**- High Speed Quad SPST Switch

The LSTTL/MSI SN54/74LS157 is a high speed Quad 2-Input Multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The LS157 can also be used to generate any four of the 16 different functions of two variables. The LS157 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Non-Inverting Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Special Circuitry Ensures Glitch Free Multiplexing
- ESD > 3500 Volts

Pin Configurations

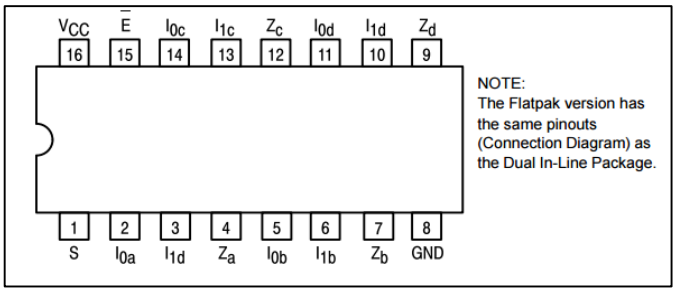
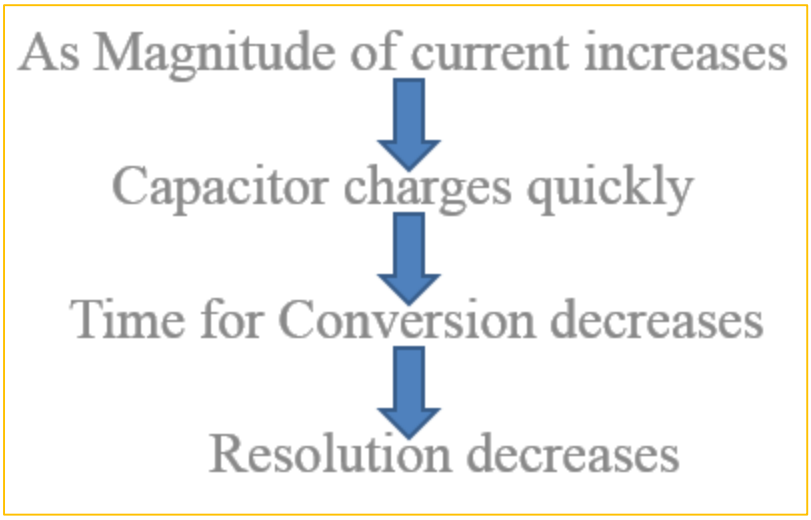


Figure 12. Pinout of 74157 Quad SPST Switch

CHAPTER 5

PRINCIPLE



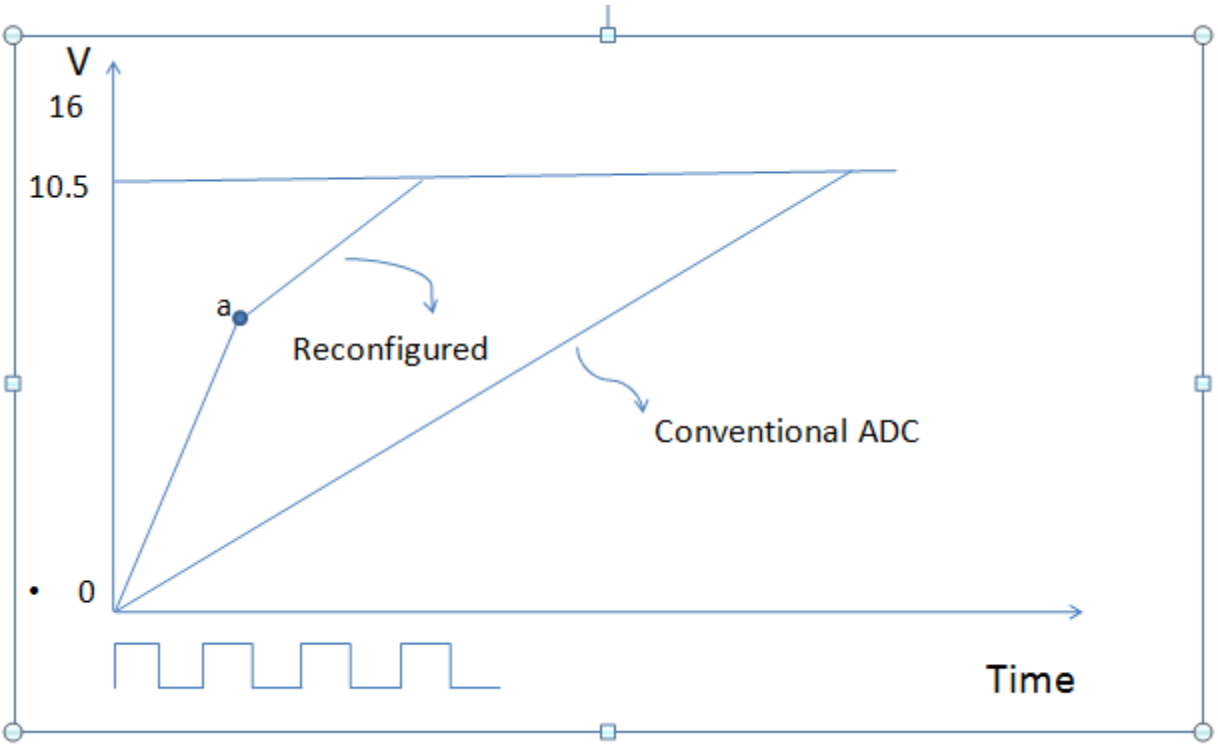


Figure 13. Comparison of ADC based on No. of Bits Used

CALCULATIONS :

- Consider 12 bit resolution,

$$LSB = \frac{\text{Full Range Voltage}}{2^{(n)}}$$

$$= \frac{16\ V}{4096} = 3.9\ mV$$

So, 1 LSB = 3.9 mV

1 clock ⟶ 3.9 mV

x clock cycles ⟶ 10.5 volts

So, x = 2692 clock cycles

- Consider 8 bit resolution,

$$LSB = \frac{\text{Full Range Voltage}}{2^{(n)}}$$

$$= \frac{16\ V}{256} = 62.5\ mV$$

So, 1 LSB = 62.5 mV

1 clock ⟶ 62.5 mV

x clock cycles ⟶ 10.5 volts

So, x = 168 clock cycles

So, Conversion Time = 168 µs

- Consider 4 bit resolution,

$$LSB = \frac{\text{Full Range Voltage}}{2^{(n)}}$$

$$= \frac{16\ V}{16} = 1\ V$$

So, 1 LSB = 1 V

1 clock ⟶ 1 V

So,10.5 (11) clock cycles will be reqd. for 10.5 V

So, Conversion Time = 11 µs.

RESOLUTION vs CONVERSION TIME

RESOLUTION	CONVERSION TIME
12 Bit	2692 µs
8 Bit	168 µs
4 Bit	11 µs

Figure 14. Resolution Vs Conversion Time

CHAPTER 6

WORKING & BLOCK DIAGRAMS

6.1 Stage 1:

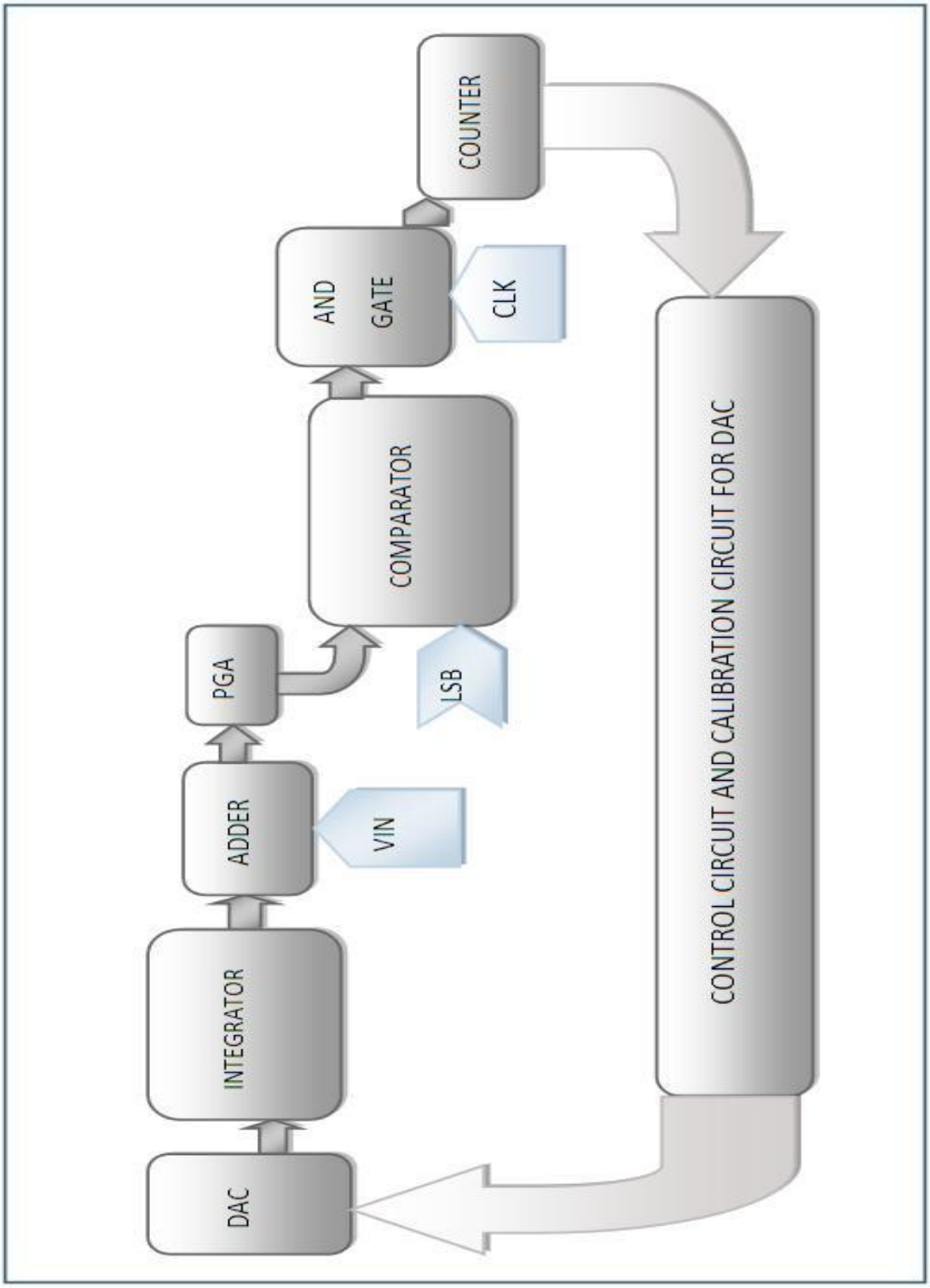


Figure 15. Stage 1

6.2 Stage 2:

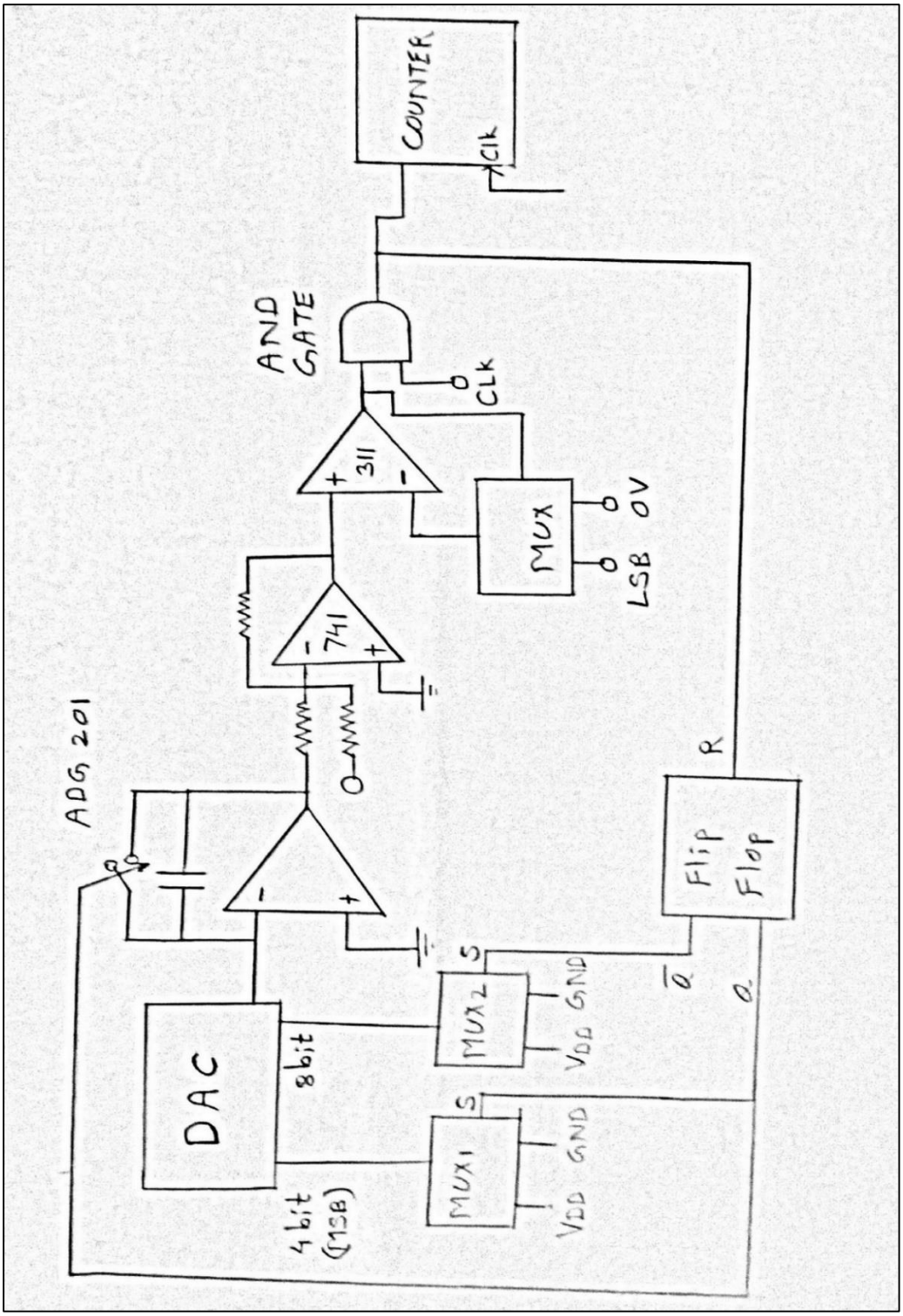


Figure 16. Stage 2

6.3 Stage 3:

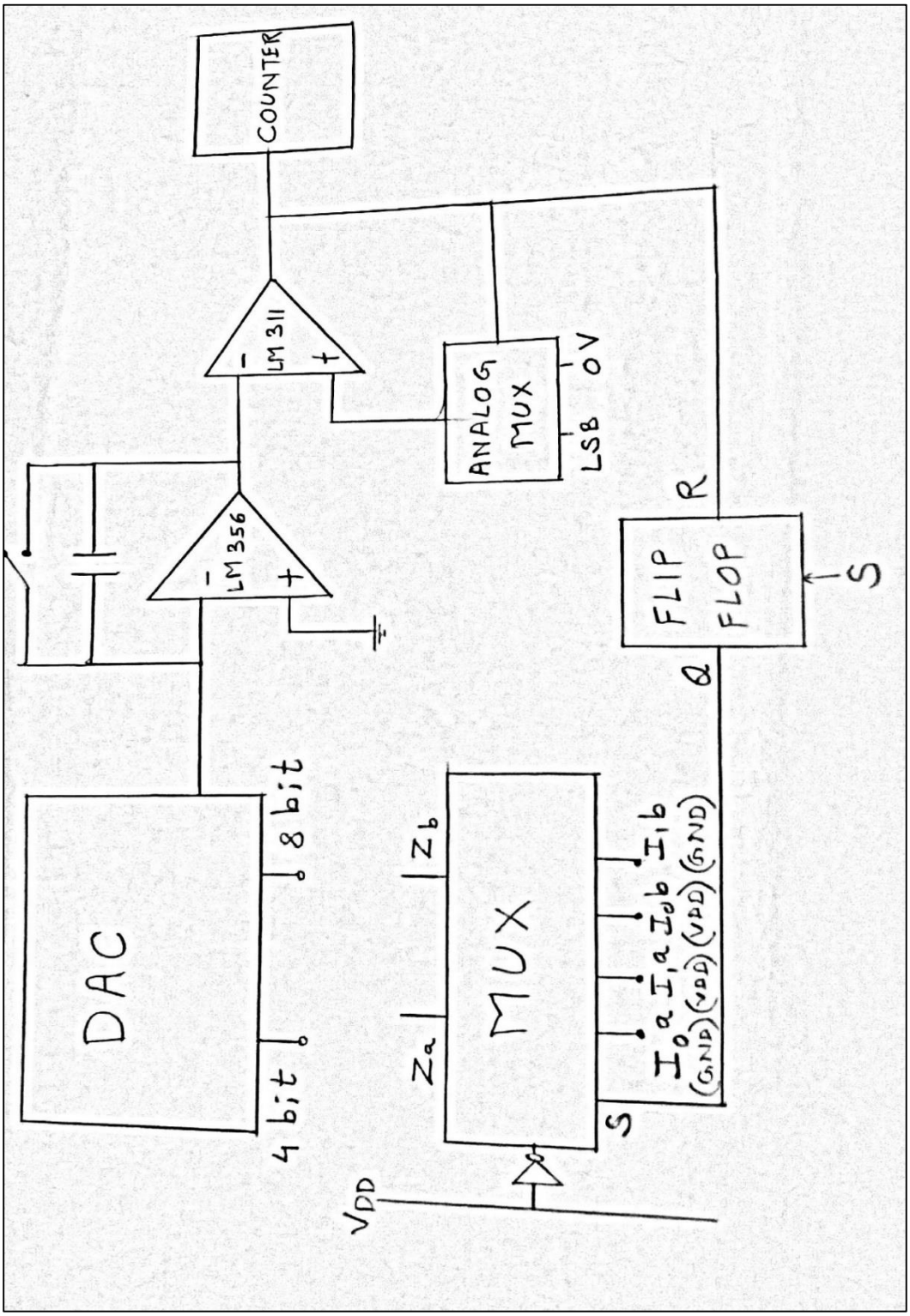


Figure 17. Stage 3

6.4 BLOCK DIAGRAM DESCRIPTION

RAMP GENERATOR BLOCK:

6.4.1 Ramp generator

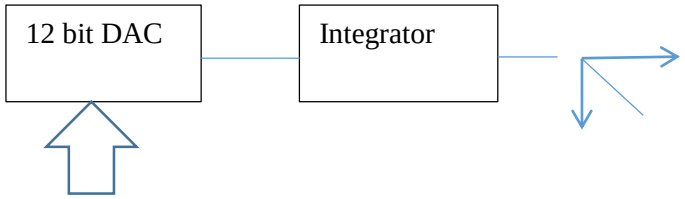


Figure 18. Ramp Generator

Ramp generator block consists 12-bit DAC and integrator as shown in figure 2. The 12-bit maximum resolution can be obtained depending upon the input to DAC. The input to DAC is decided by the control circuit which in turn decide the current output of DAC .This current value ,when it flows through capacitor of integrator decide the ramp voltage i.e. V_{ramp}. Mathematically,

$$V_{ramp} = -1/C \int i\, dt$$

The charging time taken by capacitor C to reach the voltage V_{ramp}depends upon current *i* which indirectly decide the resolution of proposed ADC.

Now, since an inverting Integrator is used, so the voltage we get is a negative going Ramp.

6.4.2 Adder:

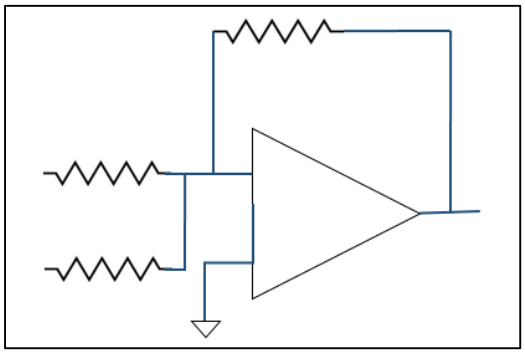


Figure 19. Adder

The output voltage from Integrator is added with a DC Input voltage as follows:

Vo = - V(ramp) + V(dc).

The adder has a unity Gain.

The output Voltage of adder is a positive going ramp starting at vtg -V(dc).

6.4.3 Comparator: (IC 8651)

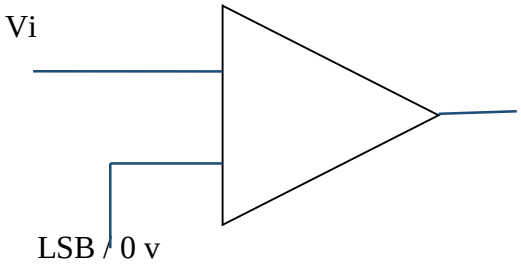


Figure 20. Comparator

Condition	Output of comparator
Vi < LSB	Logic 0
Vi > LSB	Logic 1

Table 3. Comparator Output

As the output voltage of the adder approaches 0 volts, it is compared with the LSB voltage by means of comparator IC .

As soon as the voltage reaches the level of LSB voltage, comparator output becomes high .

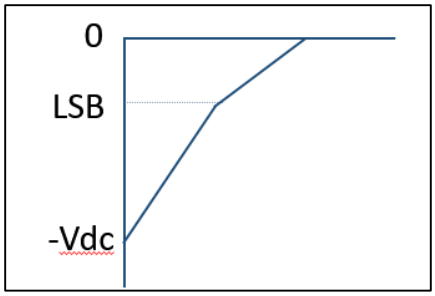


Figure 21. -ve slope

6.4.4 Control Block:

The Control Circuit is basically used to control the input given to the DAC and to the switch.

The circuitory basically consists of NAND gates which are used as FLIP FLOPs.

Depending upon the control block output, input bits applied to the DAC are varied thereby the output current from the DAC can be controlled.

6.5 ILLUSTRATION:

The entire project has been designed in several stages. The initial stages could not fulfill our design requirements.so, above circuit has been finalized till now which may need some further modifications.

As shown in above design,

1) IC 7541 is R-2R ladder DAC with ref. voltage +15V. It has 12 controlling bits (pin no. 4 to 15) with MSB at 4 and LSB at 15.
   Logic high => 5V
   Logic Low=> 0V

When a voltage Vref is applied at pin no. 17, we get the output current at pin no.1.The value of current depends on the input given to the controlling bits. When all the controlling bits are high, we will get the maximum output current. As the input at the controlling bits changes, correspondingly the output current (Pin no 1) will change. This change depends upon the value of LSB.

$$LSB = (Code * V_{ref})/2^n$$

The output current from DAC is given to inverting terminal (pin no 2) of JFET Opamp LF356.

2) LF356 is JFET op-amp with dual power supply of ±15V. It is used as integrator with capacitor(47pF) and analog switch ADG201. The output of the OPAMP is a negative ramp due to input at the inverting terminal. The output of this integrator (Pin no 6) is then given to the Voltage Comparator IC LM311 (pin no 3) through pull down resistor of 1KΩ each, in order to reduce the noise.
3) LM311 is a low input current/voltage comparator IC with a dual power supply of (±15V) which compares the input voltage (Pin no 3) with the reference voltage, LSB (Pin no 2). When the input voltage is less than the LSB, the output at pin no 7 is logic low (0V). As soon as the input voltage surpasses the reference voltage, the output voltage goes high. The output of 311 (pin no 7) is connected to the pull up resistor to get TTL Logic {i.e. we get the digital voltage either 0V or 5V}. This digital signal is given to the one terminal of AND Gate, having clock signal connected to another terminal. When both the terminal are at Logic High, the counter will start its operation of giving the exact count of number of clock pulses (time parameter).
4) When the input voltage of LM356 (pin no 6) is less than the reference voltage i.e. LSB, the output of comparator is low. This low signal is then fed back to analog Mux where it acts as a select line for mux. As soon as the input voltage is higher than the reference voltage, the output will be high. This high output will switch the reference voltage to 0. The speed of switching depends on the controlling bits of DAC.
5) ADG201 is an analog MUX which is connected across the capacitor for charging and discharging purpose. ADG201 has 4 independent switches. Each switch has 1 input pin (Pin no 3), 1 output pin (Pin no 2) and 1 control pin (Pin no 1).
6) The digital output of LM311 is given to the Reset (Pin no. 13) of Clocked SR Flip Flop, Whose output (Pin no. 6) given to the IC SN74LS157N- Quad 2 input Mux acts as a Select line for 2:1 Mux. Depending on the reset signal, pin no. 4 & pin no. 7 of a DAC will get connected either to GND or Vdd.

CHAPTER 7

ANALYSIS, EXPERIMENTATION AND RESULT

Hardware Implementation

7.1 P.C.B.Fabrication:

- P.C.B. is printed circuit board which is of insulating base with layer of thin copper-foil.
- The circuit diagram is then drawn on the P.C.B. with permanent marker and then it is dipped in the solution of ferric chloride so that unwanted copper is removed from the P.C.B. thus leaving components interconnection on the board.
- The specification of the base material is not important to know in most of the application, but it is important to know something about copper foil which is drawn through a thin slip.
- The resistance of the copper foil will have an effect on the circuit operation.
- Base material is made of lamination layer of suitable insulating material such as treated paper, fabric; or glass fibers and binding them with resin. Most commonly used base materials are formed paper bonded with epoxy resin.
- It is possible to obtain a range of thickness between 0.5mm to 3 mm.
- Thickness is the important factor in determining mechanical strength particularly when the commonly used base material is **"**Formea**"** from paper assembly.
- Physical property should be self supporting these are surface resistivity, heat dissipation, constant and dielectric strength.
- Another important factor is the ability to withstand high temperature.

7.2 Designing The Layout:

- While designing a layout, it must be noted that of the board should be as small as possible.
- Before starting, all components should be placed properly so that an accurate measurement of space can be made.
- The component should not be mounted very close to each other or so far away from away from one another and neither one should ignore the fact that some component reed ventilation, which consider the dimension of the relay and transformer in view of arrangement, the boiling arrangement is also considered.
- The layout is first drawn on paper then traced on copper plate which is finalized with the pen or permanent marker which is effecient and clean with etching.
- The resistivity also depends on the purity of copper, which is highest for low purity of copper. The high resistance paths are always undesired for soldered connections.
- The most difficult part of making an original printed circuit is the conversion from, theoretical circuit diagram into wiring layout, without introducing cross over and undesirable effect.
- Although it is difficult operation, it provides greatest amount of satisfaction because it is carried out with more care and skill.
- The board used for project has copper foil thickness in the range of 25 40 75 microns.
- The soldering quality requires 99.99% efficiency.

- It is necessary to design copper path extra-large. There are two reasons for this,
  i)The copper may be required to carry an extra-large current
  ii) It acts like a kind of screen or ground plane to minimize the effect of interaction.
- The first function is to connect the components together in their right sequence with minimum need for interlinking i.e. the jumpers with wire connections.
- It must be noted, that when layout is done, on the next day it should be dipped in the solution and board is move continuously right and left after etching perfectly the board is cleaned with water and is drilled.
- After that holes are drilled with 1 mm or 0.8mm drill. Now the marker on the P.C.B. is removed.
- The printed Circuit Board is now ready for mounting the components on it.

7.3 Soldering

- For soldering of any joints first the terminal to be soldered are cleaned to remove oxide film or dirt on it. If required flux is applied on the points to be soldered.
- Now the joint to be soldered is heated with the help of soldering iron. Heat applied should be such that when solder wire is touched to joint, it must melt quickly.
- The joint and the soldering iron is held such that molten solder should flow smoothly over the joint.
- When joint is completely covered with molten solder, the soldering iron is removed.
- The joint is allowed to cool, without any movement.
- The bright shining solder indicates good soldering.
- In case of dry solder joint, an air gap in between the solder material and the joint. It means that the soldering is improper. This is removed and again soldering is done.

7.4 Troubleshooting

- Checking for solder splashes.
- To check Power Supply Circuit in order to ensure a ripple free 5v supply is available at the Vcc of the IC AD7751.
- Checking for appropriate voltages across the components and rectify the errors caused by the solder splashes.

7.5 Schematic

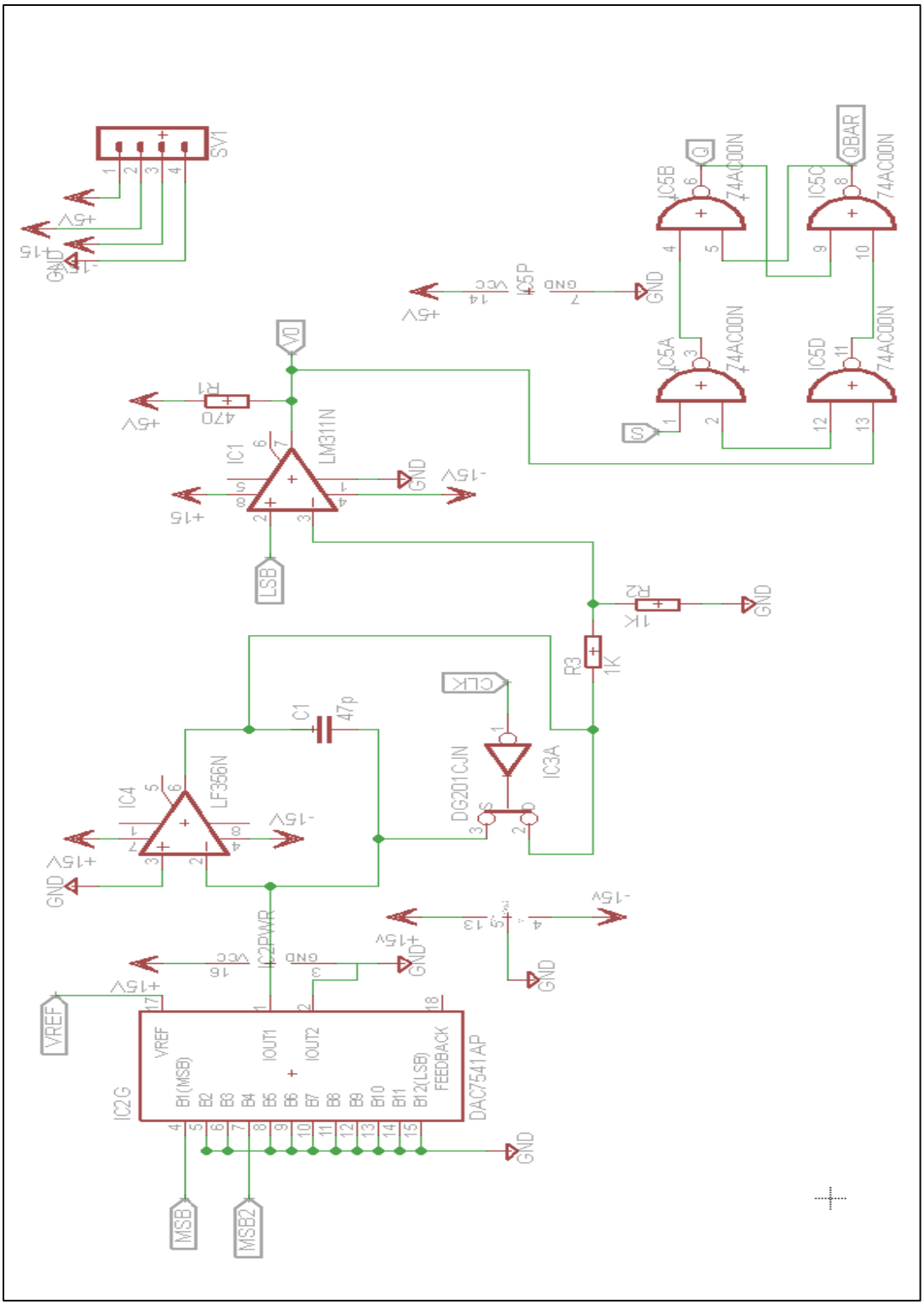


Figure 22. Schematic of PCB

7.6 PCB Layout

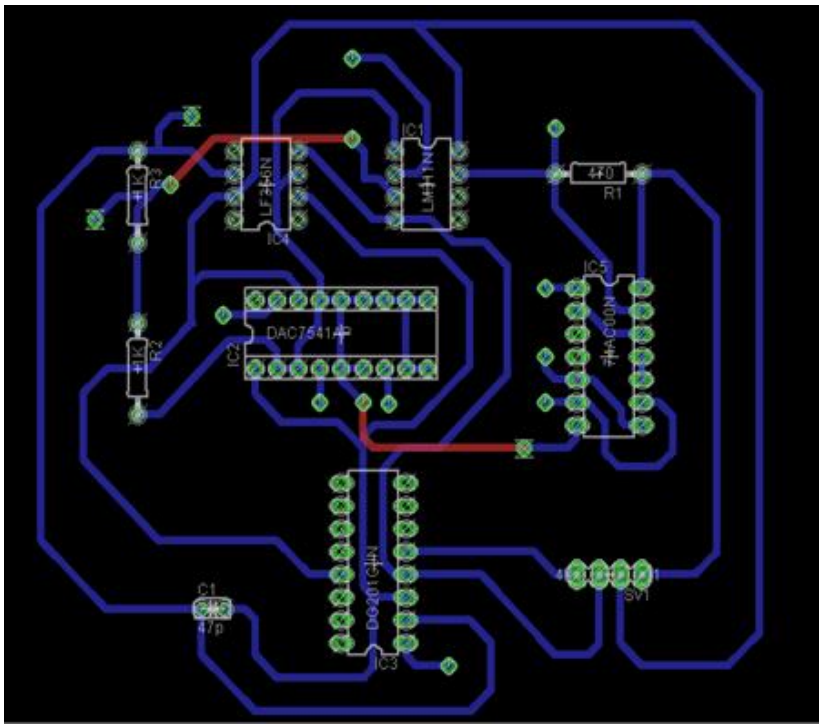


Figure 23. Layout of PCB

7.7 Negative

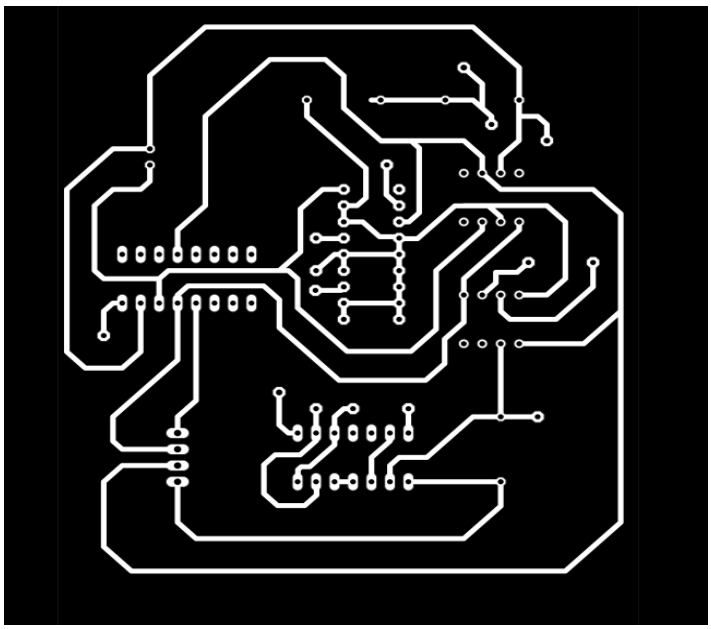


Figure 24. Negative of PCB

7.8 Readings

Table 4: Testing of DAC

Bit No	11	10	9	8	7	6	5	4	3	2	1	0	Theoretical Value	Practical Value
1.	1	1	1	1	1	1	1	1	1	1	1	1	10.26V	10.001V
2.	1	1	1	1	1	1	1	1	1	0	0	0	9.98V	9.976V
3.	1	1	1	1	1	1	1	1	1	0	0	1	9.983V	9.977V
4.	1	1	1	1	1	1	1	0	0	0	0	0	9.92V	9.907V
5.	1	1	1	1	0	0	0	0	0	0	0	0	9.375V	9.366V
6.	1	1	1	0	0	0	0	0	0	0	0	0	8.75V	8.749V
7.	1	1	0	0	0	0	0	0	0	0	0	0	7.5V	7.48V
8.	0	0	0	0	0	0	1	0	0	0	0	0	78.13mV	72.64mV
9.	0	0	0	0	0	0	0	0	0	0	1	0	5.01mV	9.10mV
10.	0	0	0	0	0	0	0	0	0	0	0	1	2.5mV	5.07mV
11.	0	0	0	0	0	0	0	0	0	0	0	0	0V	2.55mV
12.	1	0	0	0	0	0	0	0	0	0	0	0	5.0005V	4.984V
13.	1	0	0	0	0	0	0	0	0	0	0	1	5.002V	4.982V
14.	1	0	0	0	0	0	0	0	1	1	1	1	5.037V	5.033V

Output Voltage (Both Theoretical and Practical) has been tested for following bits as specified in the table.

Table 5.A MSB at Logic High (1)

Voltage Volt	Clock Cycles		Total Conversion Time (ns)	
	Theoretical	Practical	Theoretical	Practical
0.5		1.5		600
1		2		800
1.5		3		1000
2		4		1400
2.5		5		1800
3		6		2000
3.5		7		2400

Table 5.B LSB at Logic High (1)

Voltage Volt	Clock Cycles		Total Conversion Time (ns)	
	Theoretical	Practical (ms)	Theoretical	Practical
0.5		-		600
1		1.2		800
1.5		2		1000
2		4		1400
2.5		4		1800
3		5		2000
3.5		6		2400

7.9 Waveforms Obtained

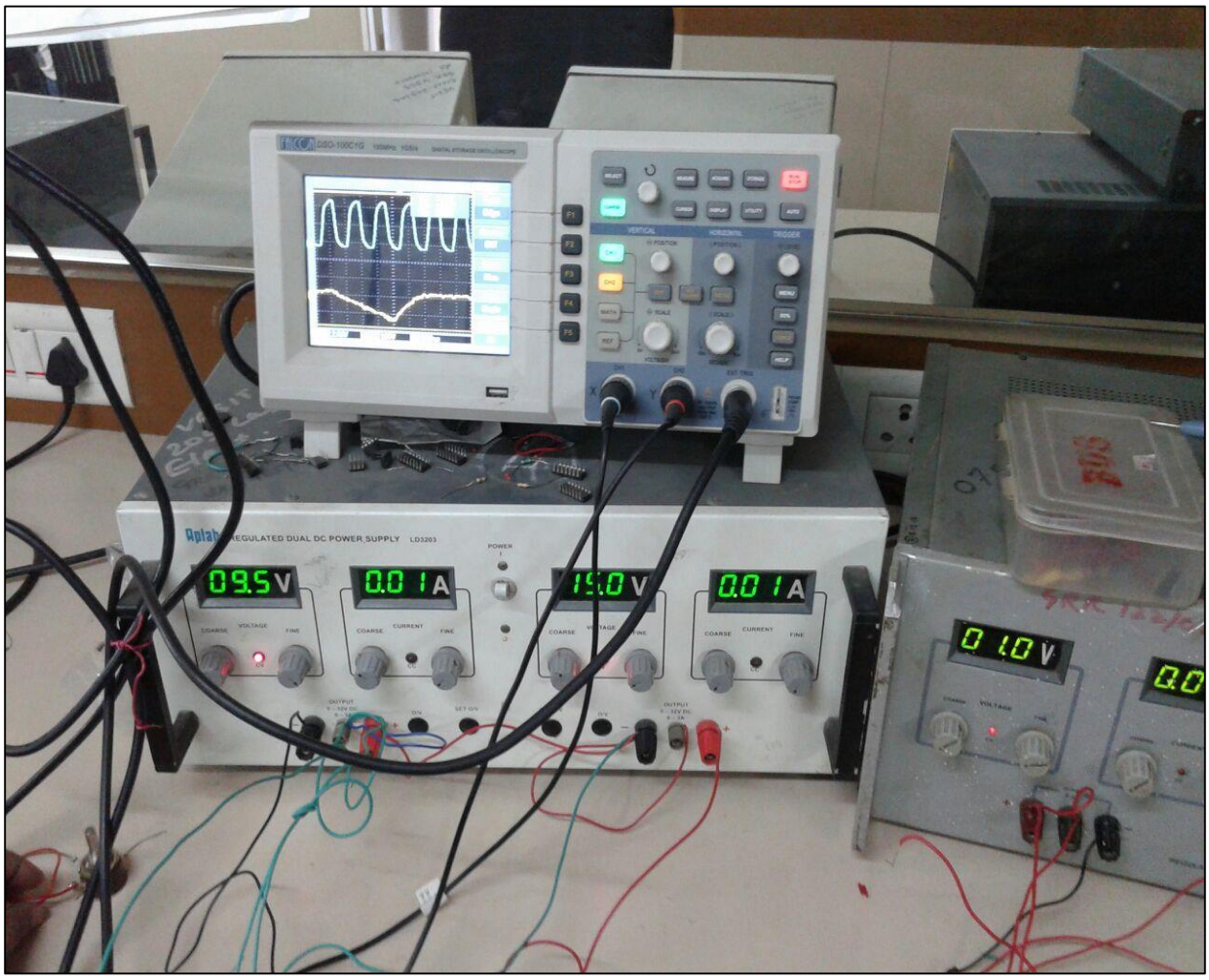


Figure 25. Phase 1 Output

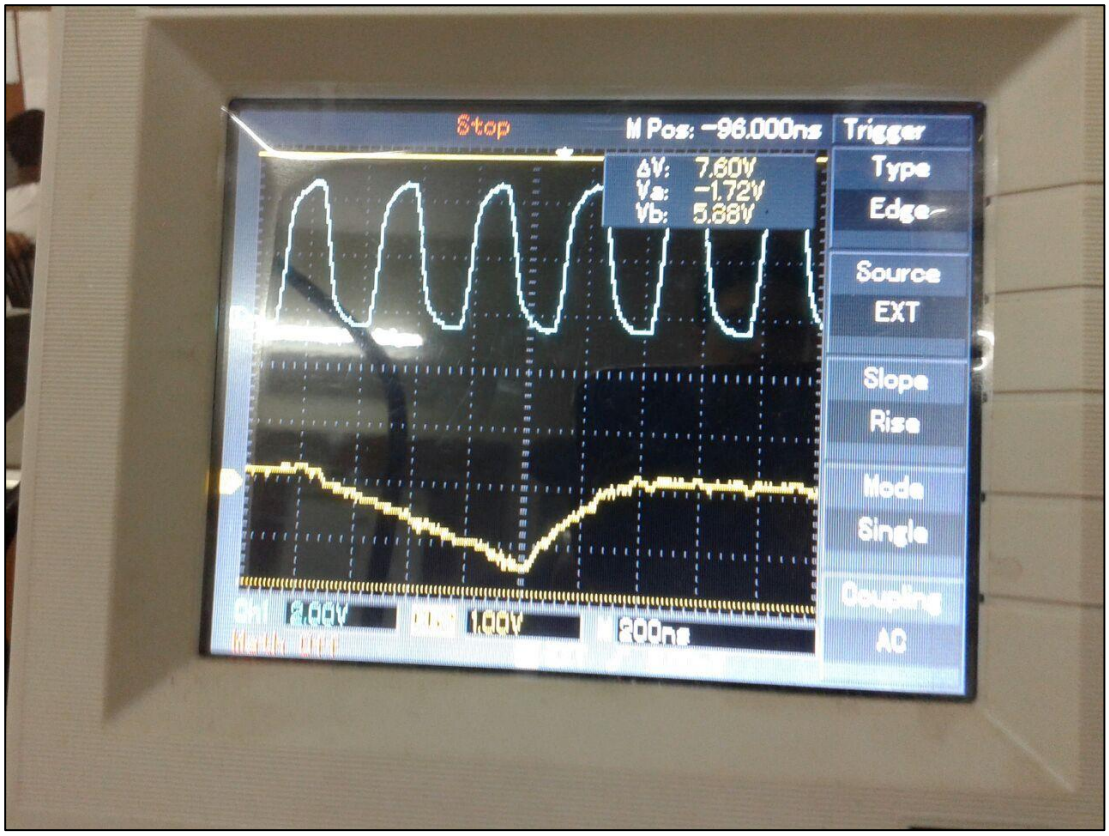


Figure 26. Zoomed Output

CHAPTER 8

FUTURE SCOPE

Low power reconfigurable ADC:

A reconfigurable ADC that can digitize signals over a bandwidth range of 0–10 MHz and a resolution range of 6–16 bits with adaptive power consumption has been proposed and described[20].It accomplishes its wide reconfiguration range through three levels of reconfiguration. The first level is architecture reconfiguration where the converter can be placed in either the delta–sigma or the pipeline modes. The second level is parameter reconfiguration, where a variety of variables such as capacitor values and converter length in the pipeline mode and oversampling ratio in the delta–sigma mode can be varied to tune the SNR. Finally, the bandwidth of the converter opamps can be tuned using a PLL scheme.

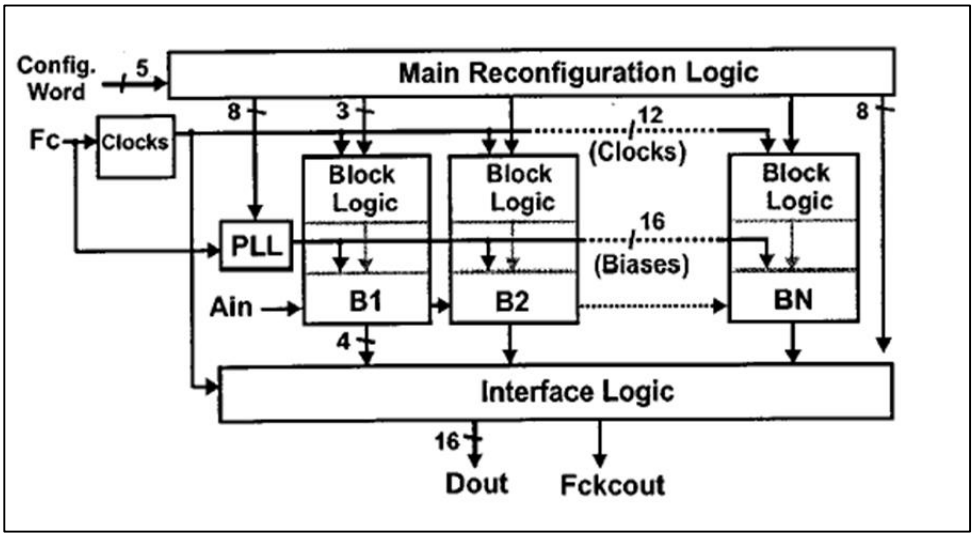


Figure 27. The Reconfigurable Converter Prototype

The reconfigurable converter prototype shown in Fig.20 contains a main reconfiguring logic that utilizes a user-defined configuration word to generate internal control bits to determine the global structure of the converter, the state of each of the basic building blocks B1–B8, and the other peripheral blocks of the converter as shown in the figure. The PLL uses the clock and determines the appropriate bias current of the converter based on the clock frequency and the resolution desired of the converter. The output interface consists of several registers for the task of temporal and spatial alignment of the output digital bits. The output interface then feeds the processed data to the output drivers that send the information out of the chip. The internal structure of each basic building block is shown in fig.21.

CHAPTER 9

APPLICATIONS

- Reconfigurability in terms of resolution and conversion time is possible using Reconfigurable DAC. Also Hybrid DACs can be made for better performance. A conventional ADC can't access all 3 types of wireless standards, but a Reconfigurable ADC can access it
- In the Medical Equipments where very high resolution is essential.
- Single slope adc can be used in Voltmeter and ammeter
- DSLR (Digital Cameras) in latest samsung smartphone
- Detection of internal Body signals (Biomedical Sensors)

9.1 Music recording

Analog-to-digital converters are integral to current music reproduction technology. People produce much music on computers using an analog recording and therefore need analog-to-digital converters to create the pulse-code modulation (PCM) data streams that go onto compact discs and digital music files.

The current crop of analog-to-digital converters utilized in music can sample at rates up to 192 kilohertz. Considerable literature exists on these matters, but commercial considerations often play a significant role. Most high-profile recording studios record in 24-bit/192-176.4 kHz pulse-code modulation (PCM) or in Direct Stream Digital (DSD) formats, and then downsample or decimate the signal for Red-Book CD production (44.1 kHz) or to 48 kHz for commonly used radio and television broadcast applications.

9.2 Digital signal processing

People must use ADCs to process, store, or transport virtually any analog signal in digital form. TV tuner cards, for example, use fast video analog-to-digital converters. Slow on-chip 8, 10, 12, or 16 bit analog-to-digital converters are common in microcontrollers. Digital storage oscilloscopes need very fast analog-to-digital converters, also crucial for software defined radio and their new applications.

9.3 Scientific instruments

Digital imaging systems commonly use analog-to-digital converters in digitizing pixels. Some radar systems commonly use analog-to-digital converters to convert signal strength to digital values for subsequent signal processing. Many other in situ and remote sensing systems commonly use analogous technology.

The number of binary bits in the resulting digitized numeric values reflects the resolution, the number of unique discrete levels of quantization (signal processing). The correspondence between the analog signal and the digital signal depends on the quantization error. The quantization process must occur at an adequate speed, a constraint that may limit the resolution of the digital signal.

CHAPTER : 10

CONCLUSIONS

The main aim of the project is designing & testing of a single slope reconfigurable ADC using ramp generation technique. We are designing this ADC so as to optimize the conversion time by maintaining the resolution. Such reconfigurable ADC can be used where we need the High Resolution & less conversion time.

Figure 28. Electrical Symbol OF ADC

CHAPTER 11

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CHAPTER 12

APPENDIX

Components	Cost per unit(Rs)	Quantity	Total cost (Rs.)
IC AD7541AKN	250	05	1250
IC LF356	40	10	400
IC LM311P	20	10	200
IC ADG201HS	90	06	540
1*1 Glass Epoxy board clad	183	01	183
16 pin base	02	05	10
14 Pin Base	01	05	05
8 pin base	01	07	07
Resistors & Capacitors	0.5	10	05
Total Cost(Rs.)	--	--	**2600**

CHAPTER 13

DATASHEETS