DIGITAL LOGIC AND MICROPROCESSOR

Registration Number:	**18BIT0272**
Name:	PRIYAL BHARDWAJ
Slot:	L7+L8
Experiment Name:	Verification of Characteristic Table of Flip-flops

Q.1 JK Flip-Flop

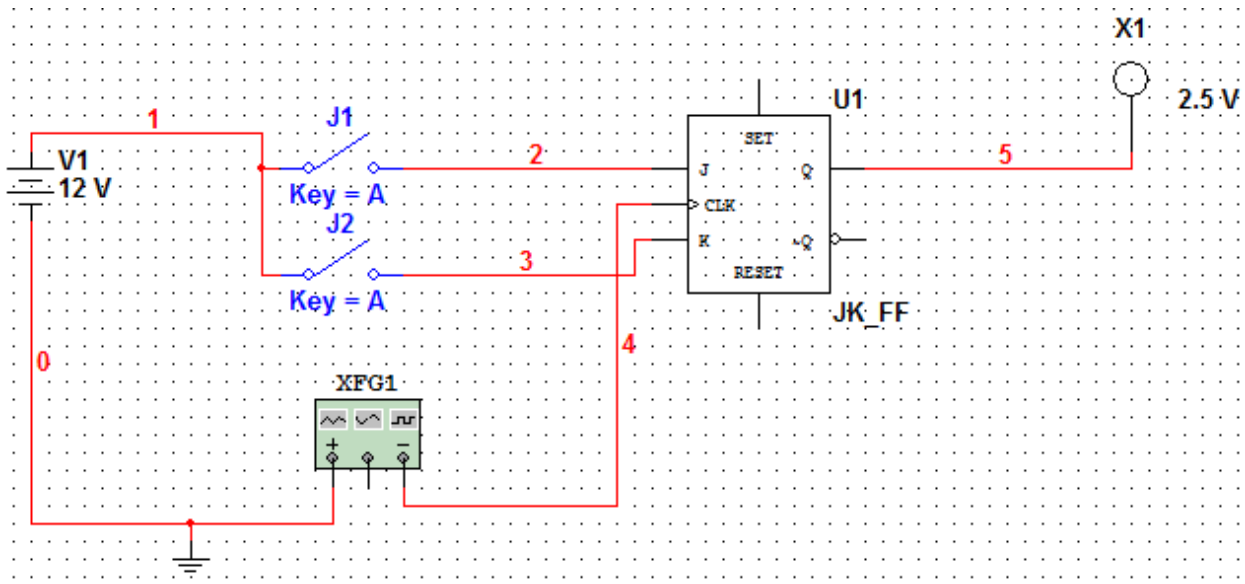
Characteristic Table:

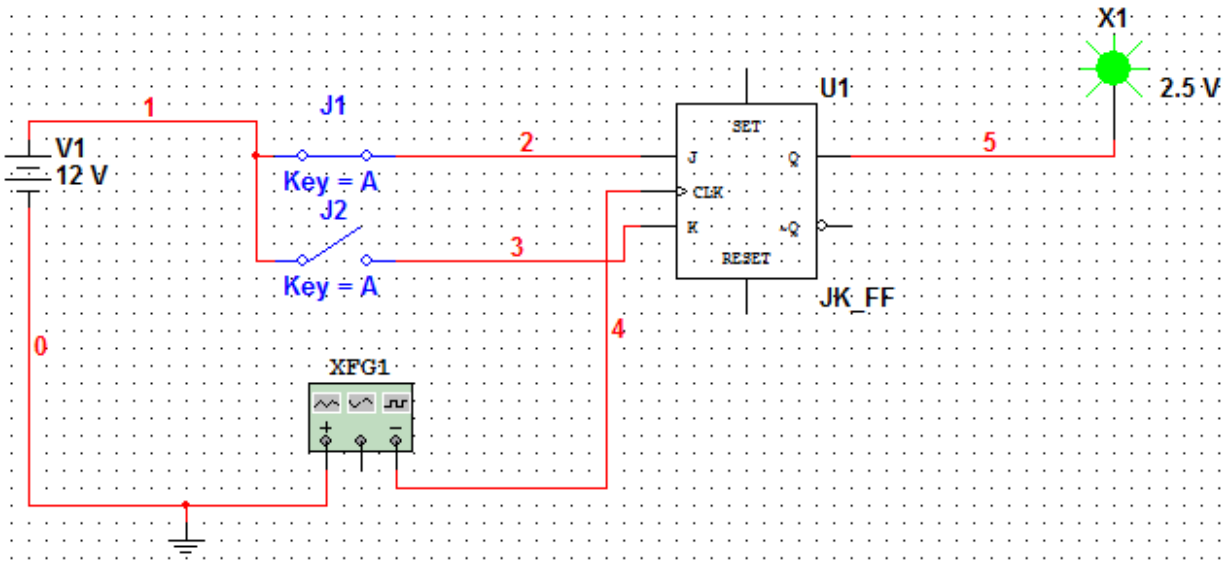
J	K	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Expression:

Qn+1 = JQn'+K'Qn

Multi Sim Circuit Diagram:





D Flip-Flop

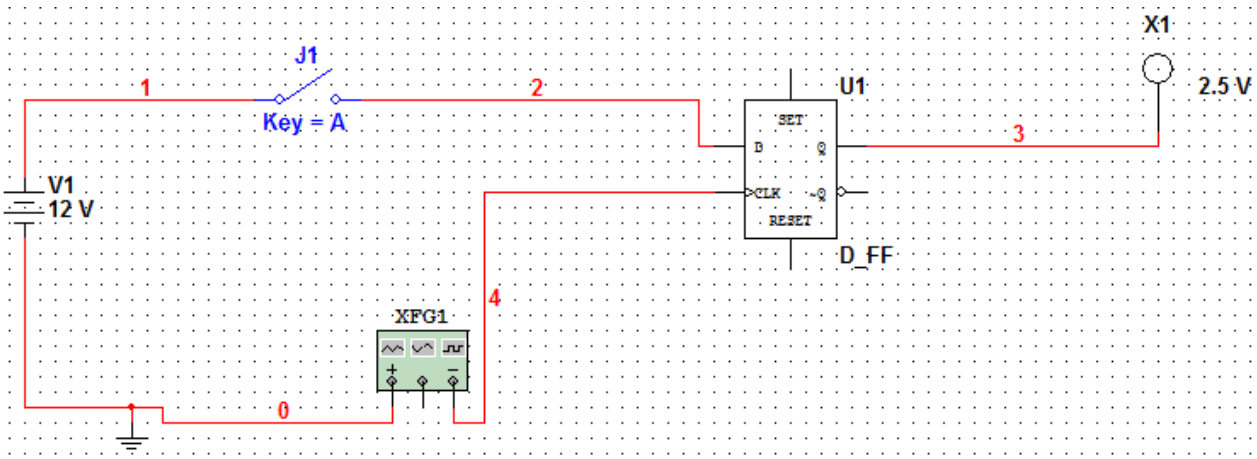
Characteristic Table:

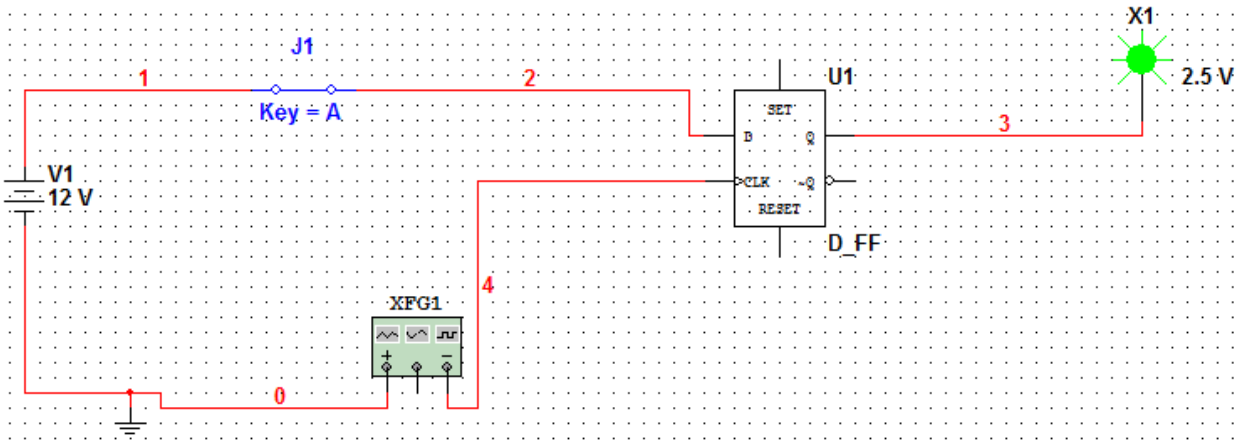
D	Qn	Qn+1
0	0	0
0	1	0
1	0	1
1	1	1

Expression:

Qn+1 = D

Multi Sim Circuit Diagram:





T Flip-Flop

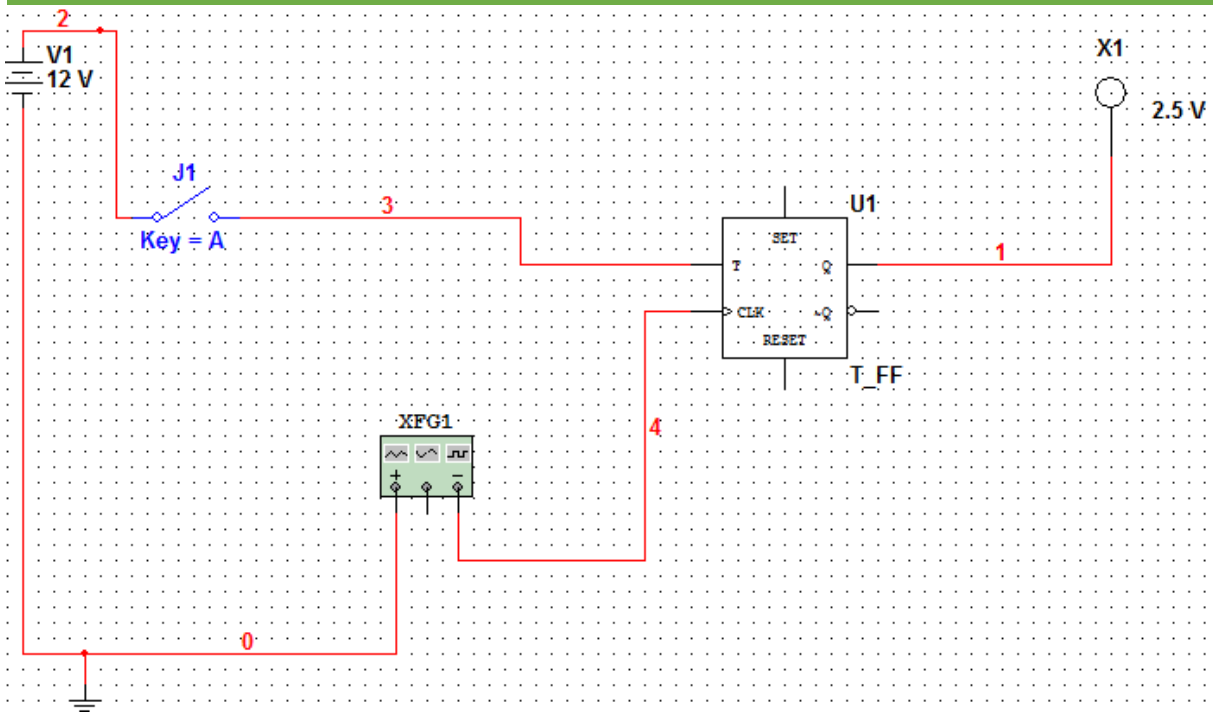
Characteristic Table:

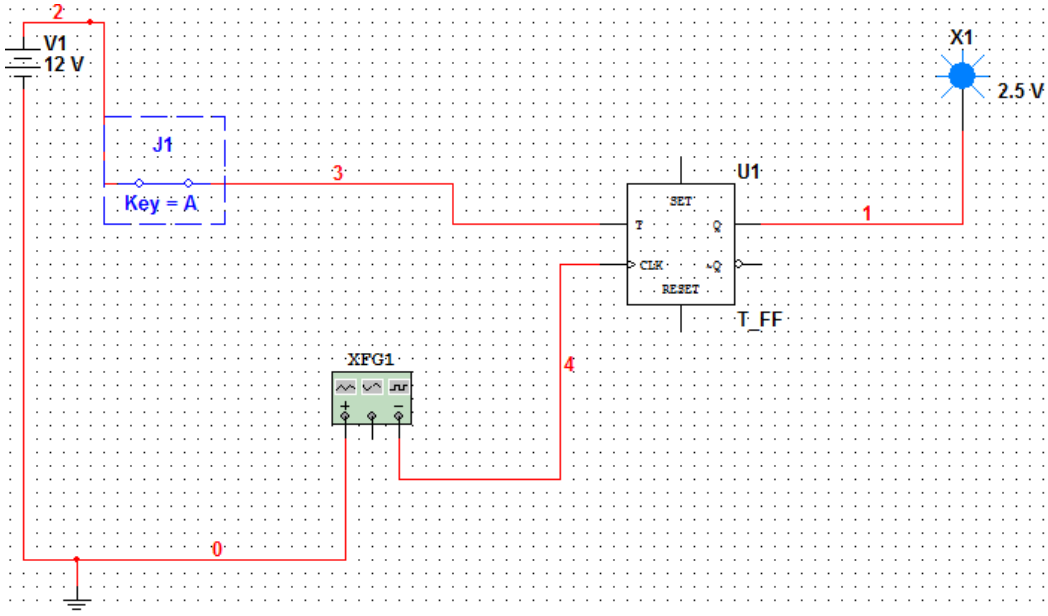
T	Qn	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

Expression:

Qn+1 = D

Multi Sim Circuit Diagram:





SR Flip-Flop

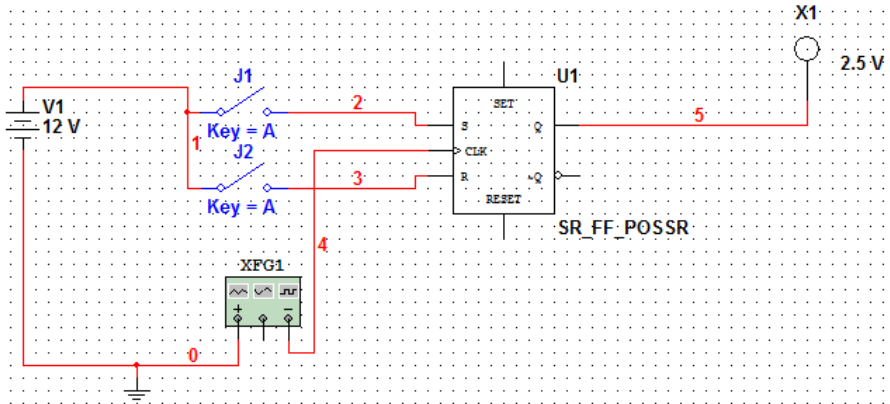
Characteristic Table:

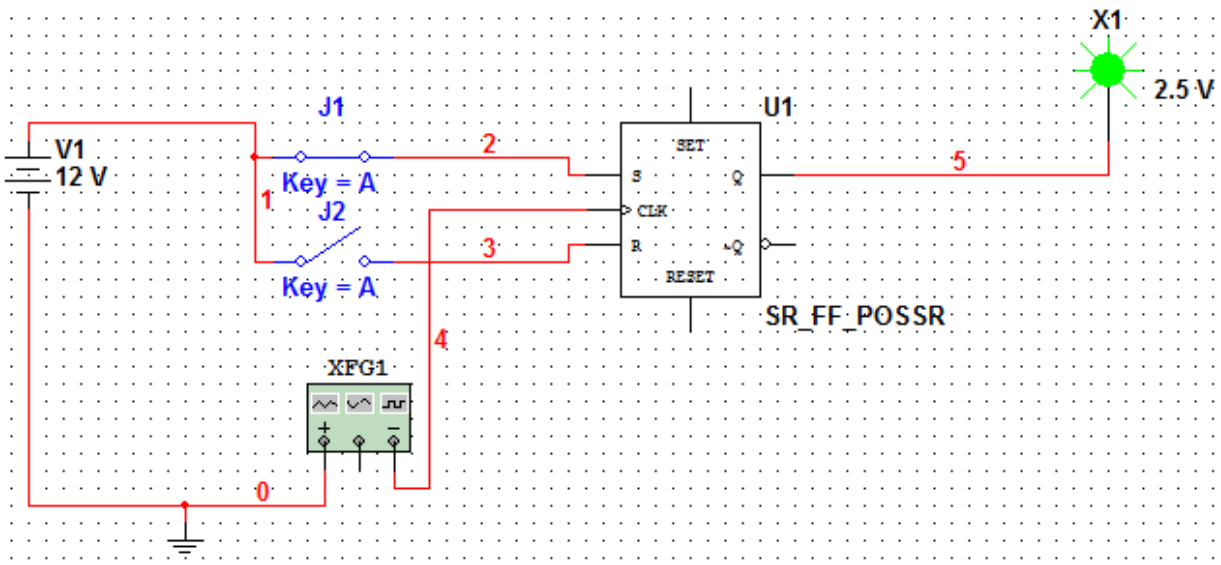
S	R	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Invalid
1	1	1	Invalid

Expression:

$Q_{n+1} = S + R'Q_n$

Multi Sim Circuit Diagram:





Q.2

Experiment Name: **Design a T flip flop using JK Flip flop**

Characteristic Table:

T	Qn	Qn+1	J	K
0	0	0	0	X
0	1	0	X	0
1	0	1	1	X
1	1	1	X	1

K-Map & Expression:

J:

	Q	Q'
T	0	X
T'	1	X

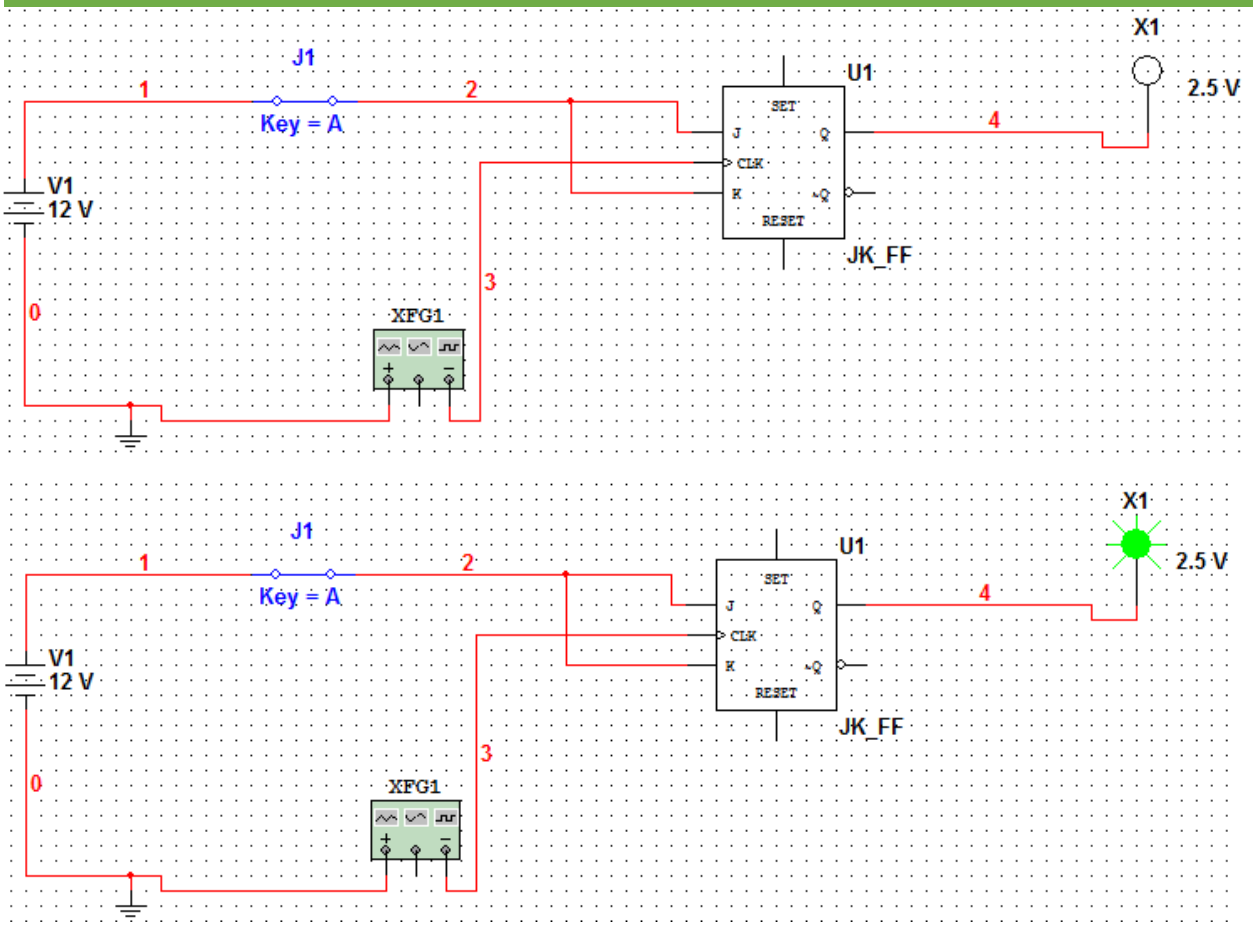
J = T

K:

	Q	Q'
T	X	0
T'	X	1

K = T

Multi Sim Circuit Diagram:



Q.3(a)

Experiment Name: **Design a sequential circuit using D Flip flop**

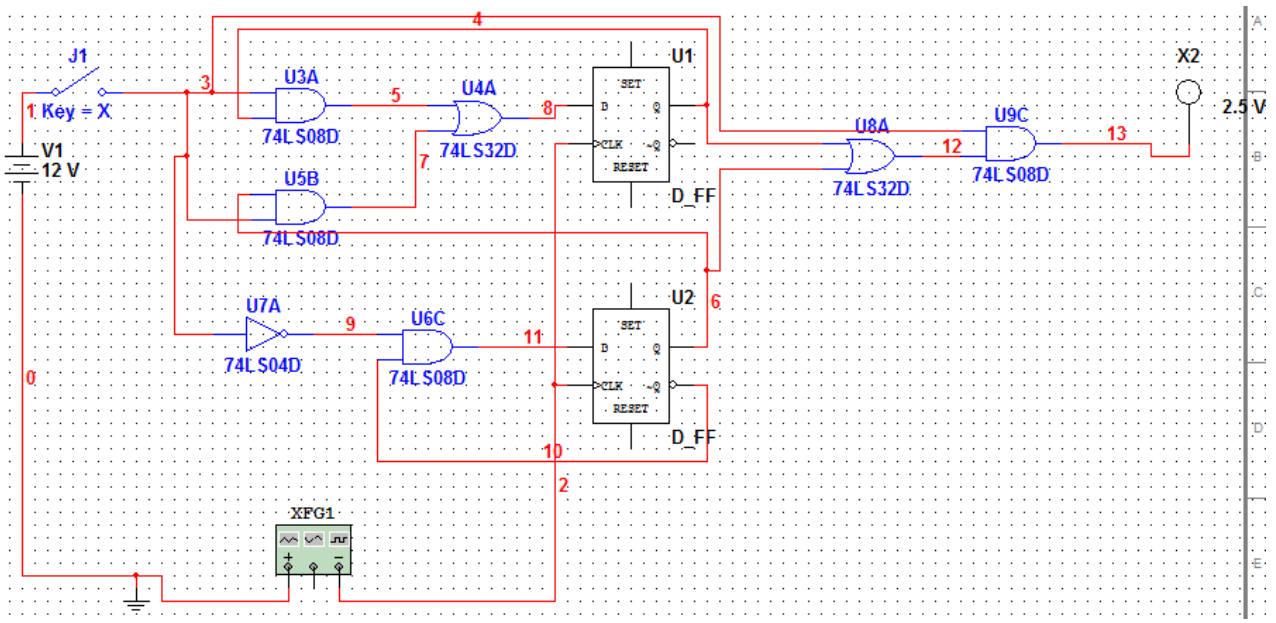
Expressions:

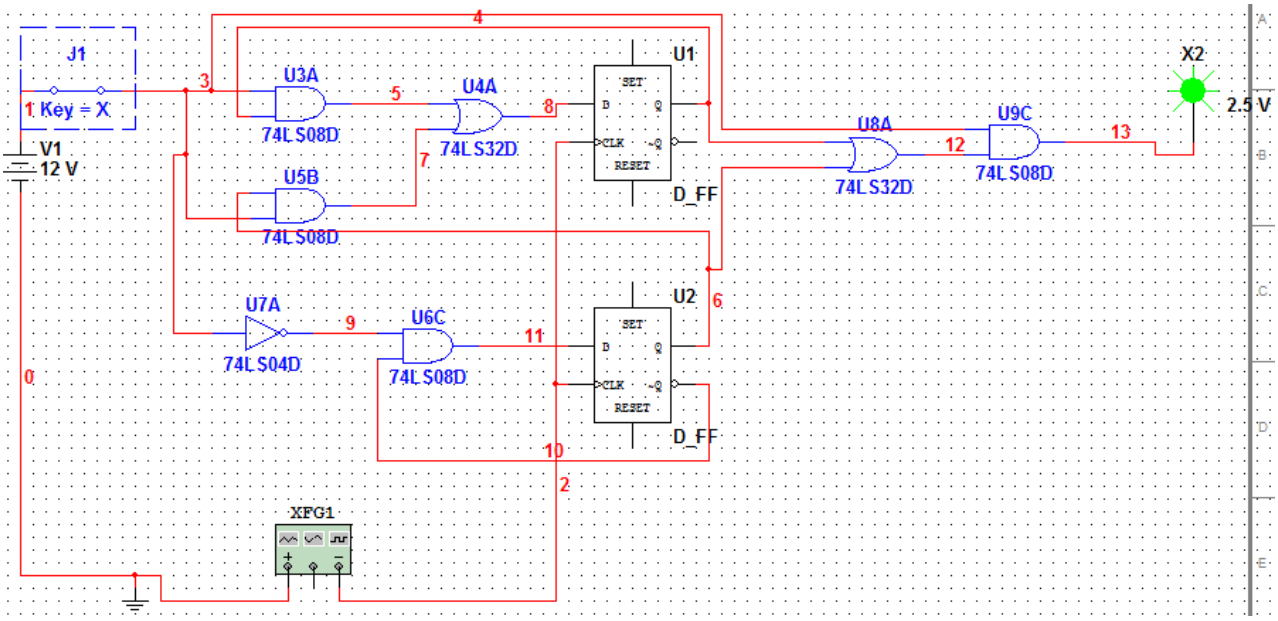
$$D_A = XA + XB$$
$$D_b = X'B'$$
$$Z = (A+B)\,X$$

Characteristic Table:

PRESENT STATE		INPUT	FLIP-FLOP INPUT		NEXT STATE		OUTPUT
A	B	X	Da	Db	An+1	Bn+1	Z
0	0	0	0	1	0	0	0
0	0	1	0	0	0	0	0
0	1	0	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	1	1	0	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	1	0
1	1	1	1	0	1	1	1

Multi Sim Circuit Diagram:





Q.3(b)

Experiment Name: **Design a sequential circuit using JK Flip flop**

Expressions:

$J_A = XY + A'B'$

$K_A = X'Y'$

$J_B = X+Y$

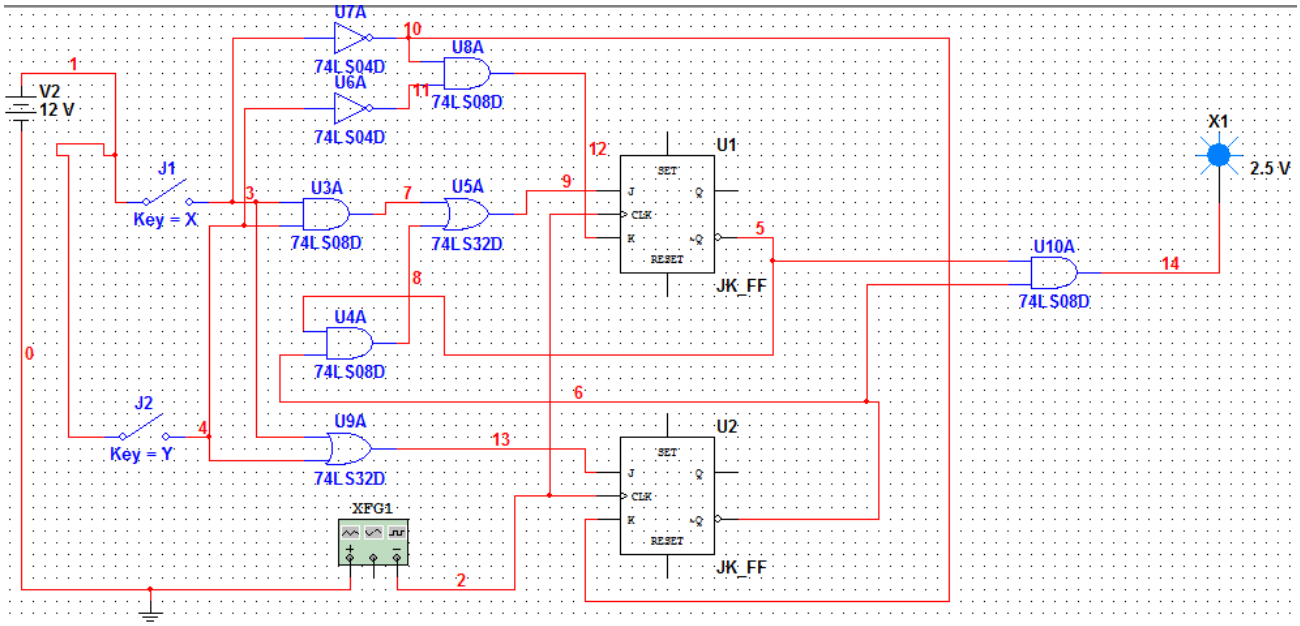
$K_B = X'$

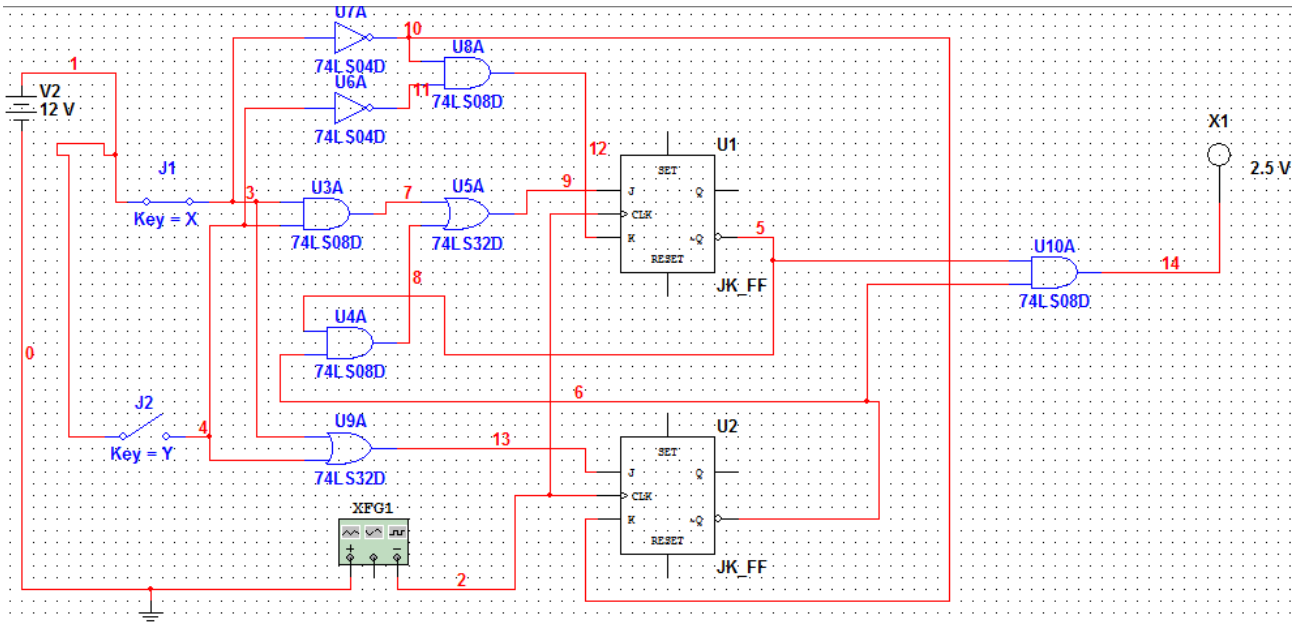
$Z = A'B'$

State Table:

PRESENT STATE		INPUT		FLIP-FLOP INPUT				NEXT STATE		OUTPUT
A	B	X	Y	Ja	Ka	Jb	Kb	An+1	Bn+1	Z
0	0	0	0	0	1	0	1	0	0	1
0	0	0	1	0	0	1	1	0	1	1
0	0	1	0	0	0	1	0	0	1	1
0	0	1	1	1	0	1	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0
0	1	0	1	0	0	1	1	0	0	0
0	1	1	0	0	0	1	0	0	1	0
0	1	1	1	1	0	1	0	1	1	0
1	0	0	0	0	1	0	1	0	0	0
1	0	0	1	0	0	1	1	1	1	0
1	0	1	0	0	0	1	0	1	1	0
1	0	1	1	1	0	1	0	1	1	0
1	1	0	0	1	1	0	1	0	0	0
1	1	0	1	1	0	1	1	1	0	0
1	1	1	0	1	0	1	0	1	1	0
1	1	1	1	1	0	1	0	1	1	0

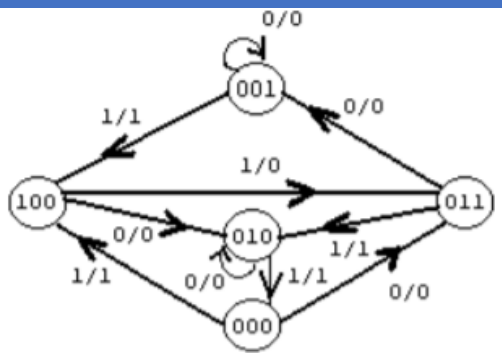
Multi Sim Circuit Diagram:





Q.4 [NOTE: *X* → Don't Care]

Experiment Name: **Design a sequential circuit for the following using T Flip flop.**



State Table:

PRESENT STATE			INPUT	FLIP-FLOP INPUT			NEXT STATE			OUTPUT
A	B	C	X	Ta	Tb	Tc	An+1	Bn+1	Cn+1	Z
0	0	0	0	0	1	1	0	1	1	0
0	0	0	1	1	0	0	1	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	1	1	1	0	1	1	0	0	1
0	1	0	0	0	0	0	0	1	0	0
0	1	0	1	0	1	0	0	0	0	1
0	1	1	0	0	1	0	0	0	1	0
0	1	1	1	0	0	1	0	1	0	1
1	0	0	0	1	1	0	0	1	0	0
1	0	0	1	1	1	1	0	1	1	0
1	0	1	0	*X*	*X*	*X*	*X*	*X*	*X*	*X*
1	0	1	1	*X*	*X*	*X*	*X*	*X*	*X*	*X*
1	1	0	0	*X*	*X*	*X*	*X*	*X*	*X*	*X*
1	1	0	1	*X*	*X*	*X*	*X*	*X*	*X*	*X*
1	1	1	0	*X*	*X*	*X*	*X*	*X*	*X*	*X*
1	1	1	1	*X*	*X*	*X*	*X*	*X*	*X*	*X*

K-Map & Expressions:

Ta:				
	C'X'	C'X	CX	CX'
A'B'	0	**1**	**1**	0
A'B	0	0	0	0
AB	***X***	***X***	***X***	***X***
AB'	**1**	**1**	***X***	***X***

Tb:				
	C'X'	C'X	CX	CX'
A'B'	**1**	0	0	0
A'B	0	**1**	0	**1**
AB	***X***	***X***	***X***	***X***
AB'	**1**	**1**	***X***	***X***

Ta = A+B'X

Tb = A+ B'C'X'+BC'X+BCX'

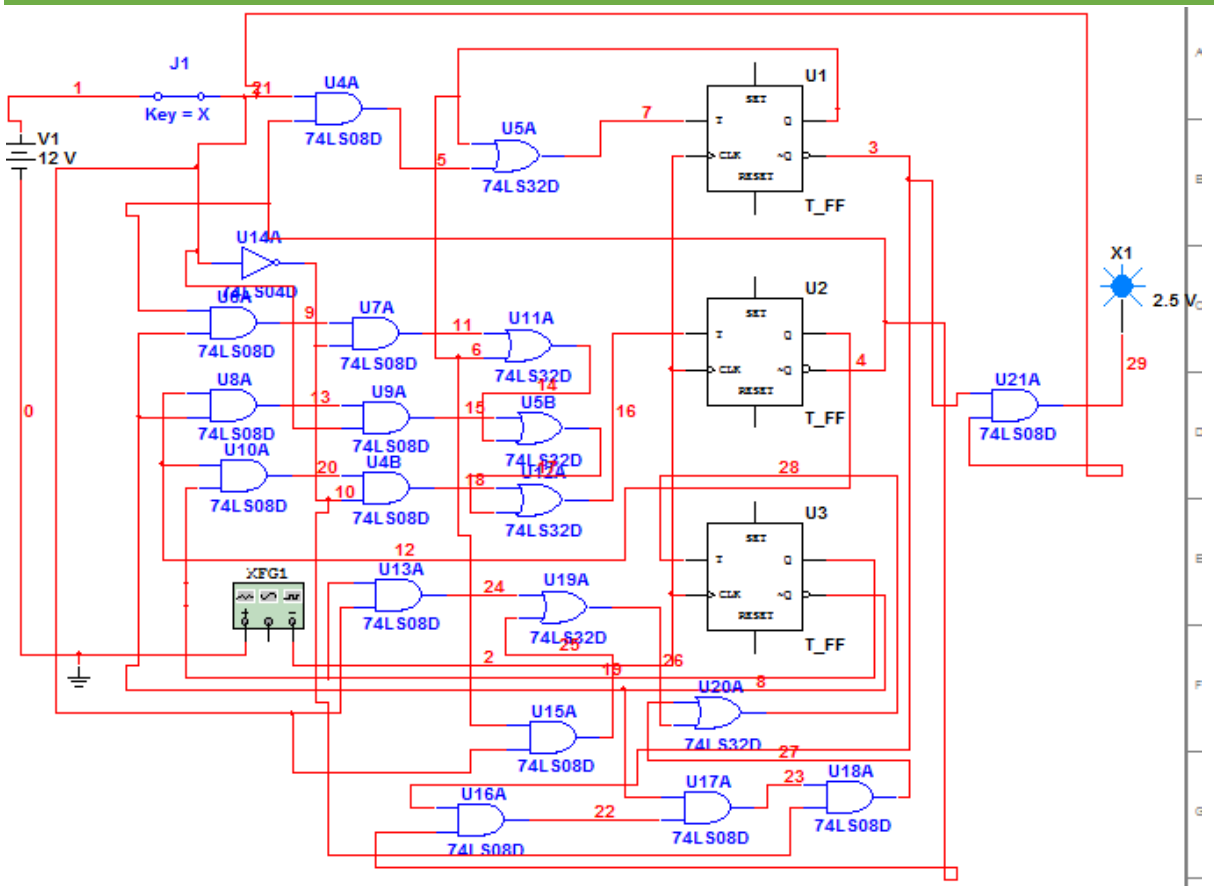
Tc:				
	C'X'	C'X	CX	CX'
A'B'	**1**	0	**1**	0
A'B	0	0	**1**	0
AB	***X***	***X***	***X***	***X***
AB'	0	**1**	***X***	***X***

Z:				
	C'X'	C'X	CX	CX'
A'B'	0	**1**	**1**	0
A'B	0	**1**	**1**	0
AB	***X***	***X***	***X***	***X***
AB'	0	0	***X***	***X***

Tc = AX+CX+A'B'C'X'

Z = A'X

Multi Sim Circuit Diagram:



Q.5

Experiment Name: **Design an Up-counter for counting the sequence 0,3,5,8,2,1,0,…**

State Table:

PRESENT STATE				NEXT STATE				FLIP-FLOP INPUTS							
A	B	C	D	An+1	Bn+1	Cn+1	Dn+1	Ja	Ka	Jb	Kb	Jc	Kc	Jd	Kd
0	0	0	0	0	0	1	1	0	X	0	X	1	X	1	X
0	0	0	1	0	0	0	0	0	X	0	X	0	X	X	1
0	0	1	0	0	0	0	1	0	X	0	X	X	1	1	X
0	0	1	1	0	1	0	1	0	X	1	X	X	1	X	0
0	1	0	0	0	0	0	0	0	X	X	1	0	X	0	X
0	1	0	1	1	0	0	0	1	X	X	1	0	X	X	1
0	1	1	0	0	0	0	0	0	X	X	1	X	1	0	X
0	1	1	1	0	0	0	0	0	X	X	1	X	1	X	1
1	0	0	0	0	0	1	0	X	1	0	X	1	X	0	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1
1	0	1	0	0	0	0	0	X	1	0	X	X	1	0	X
1	0	1	1	0	0	0	0	X	1	0	X	X	1	X	1
1	1	0	0	0	0	0	0	X	1	X	1	0	X	0	X
1	1	0	1	0	0	0	0	X	1	X	1	0	X	X	1
1	1	1	0	0	0	0	0	X	1	X	1	X	1	0	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

K-Map & Expressions:

Ja:				
	C'D'	C'D	CD	CD'
A'B'	0	0	0	0
A'B	0	**1**	0	0
AB	**X**	**X**	**X**	**X**
AB'	**X**	**X**	**X**	**X**

Ka:				
	C'D'	C'D	CD	CD'
A'B'	**X**	**X**	**X**	**X**
A'B	**X**	**X**	**X**	**X**
AB	**1**	**1**	**1**	**1**
AB'	**1**	**1**	**1**	**1**

Ja = BC'D

Ka = 1

Jb:				
	C'D'	C'D	CD	CD'
A'B'	0	0	**1**	0
A'B	**X**	**X**	**X**	**X**
AB	**X**	**X**	**X**	**X**
AB'	0	0	0	0

Kb:				
	C'D'	C'D	CD	CD'
A'B'	**X**	**X**	**X**	**X**
A'B	**1**	**1**	**1**	**1**
AB	**1**	**1**	**1**	**1**
AB'	**X**	**X**	**X**	**X**

Jb = A'CD

Kb = 1

Jc:				
	C'D'	C'D	CD	CD'
A'B'	1	0	X	X
A'B	0	0	X	X
AB	0	0	X	X
AB'	1	0	X	X

Kc:				
	C'D'	C'D	CD	CD'
A'B'	X	X	1	1
A'B	X	X	1	1
AB	X	X	1	1
AB'	X	X	1	1

Jc = B'D'

Kc = 1

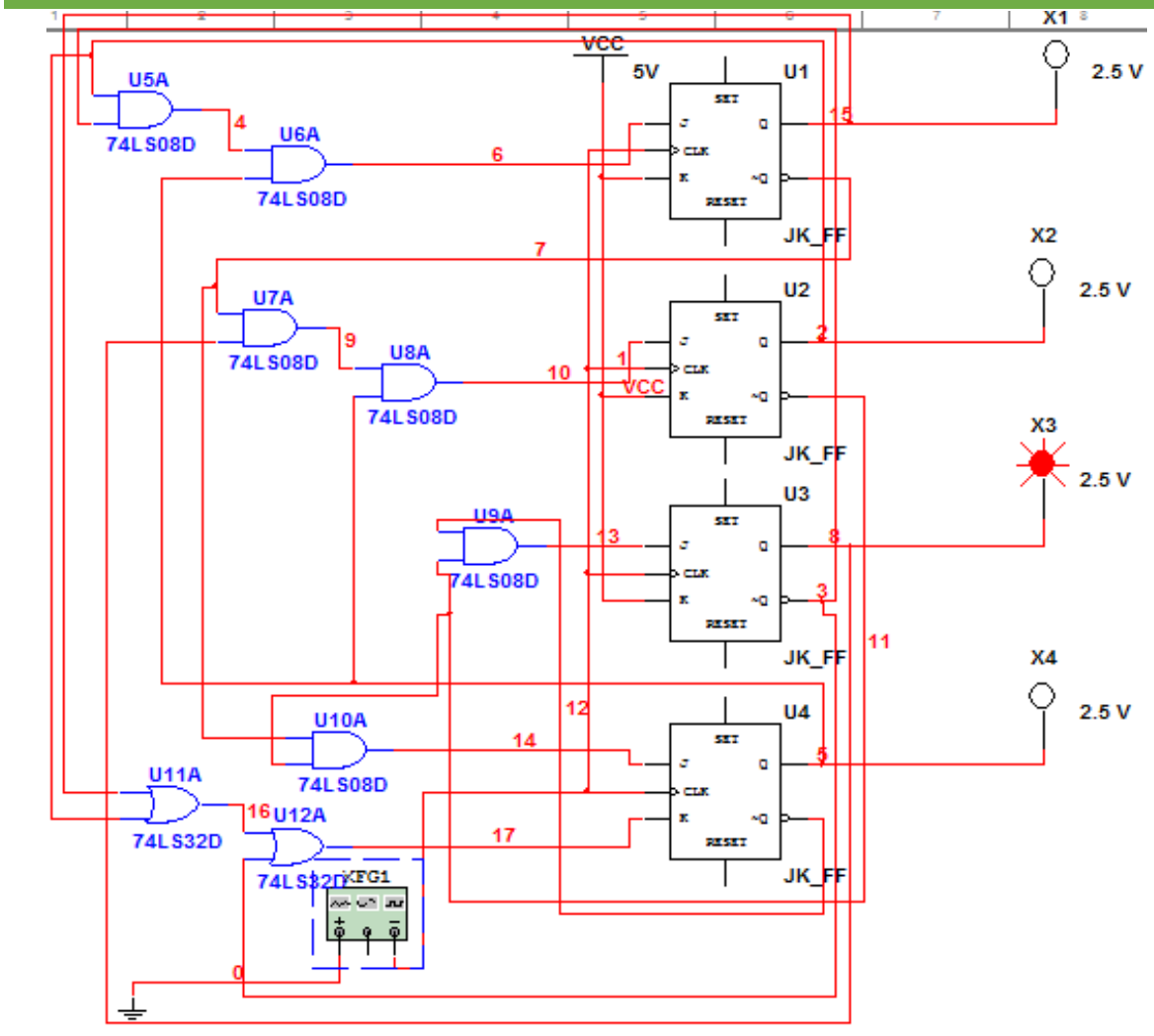
Jd:				
	C'D'	C'D	CD	CD'
A'B'	1	X	X	1
A'B	0	X	X	0
AB	0	X	X	0
AB'	0	X	X	0

Kd:				
	C'D'	C'D	CD	CD'
A'B'	X	1	0	X
A'B	X	1	1	X
AB	X	1	1	X
AB'	X	1	1	X

Jd = A'B'

Kd = A+B+C'

Multi Sim Circuit Diagram:



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J_A :

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	X	X	X	X
10	X	X	X	X

$J_A = B\bar{C}D$

K_A :-

AB \ CD	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	1	1	1
10	1	1	1	1

$K_A = 1$

J_B :

AB \ CD	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	0	0

$J_B = \bar{A}CD$

K_B :-

AB \ CD	00	01	11	10
00	X	X	X	X
01	1	1	1	1
11	1	1	1	1
10	X	X	X	X

$K_B = 1$

J_C :

AB \ CD	00	01	11	10
00	1	0	X	X
01	0	0	X	X
11	0	0	X	X
10	1	0	X	X

$J_C = \bar{B}\bar{D}$

K_C :-

AB \ CD	00	01	11	10
00	X	X	1	1
01	X	X	1	1
11	X	X	1	1
10	X	X	1	1

$K_C = 1$

J_D :

AB \ CD	00	01	11	10
00	1	X	X	1
01	0	X	X	0
11	0	X	X	0
10	0	X	X	0

$J_D = \bar{A}\bar{B}$

K_D :

AB \ CD	00	01	11	10
00	X	1	0	0
01	X	1	0	0
11	X	1	1	X
10	X	1	1	X

$K_D = A + B + \bar{C}$

Teacher's Signature : _____