

LAB ASSIGNMENT – 5

Course: Basic Electrical and Electronics Engineering

Course Code: EEE1001

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Slot: L-19+L-20

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Design of Half Adder and Full Adder circuits

Aim: Simulate and verify half-adder and full-adder logic circuits.

Apparatus/Tool required:

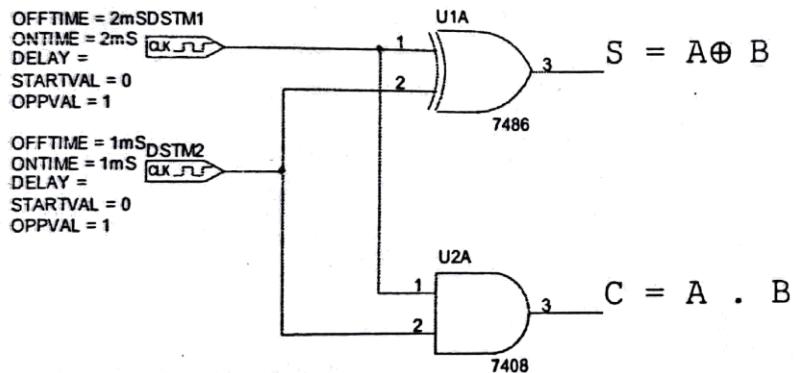
ORCAD / PSpice simulator -> 7400 Library – 7408, 7432 & 7486
Source Library - Digclock

Simulation Settings: Analysis Type - Time Domain

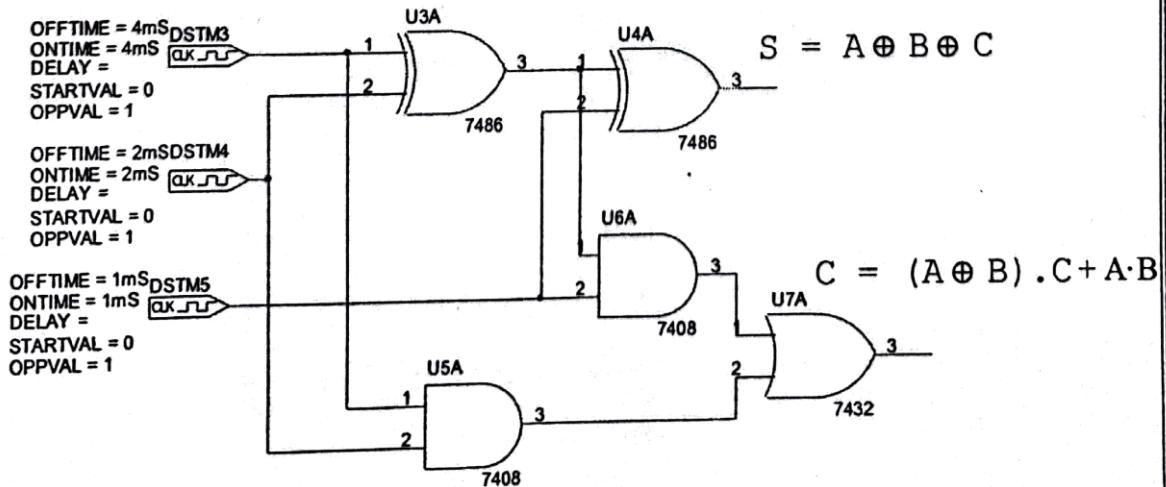
Run to time: 4ms (for Half Adder)
Run to time: 8ms (for Full Adder)

Circuit Diagram:

Half – Adder Circuit



Full – Adder Circuit



Theory:

Half Adder Circuit:

A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder.

Truth Table

A	B	$S = A \oplus B$	$C = A \cdot B$
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Addition will result in two output bits; one of which is the sum bit, S and the other is the carry bit, C. The boolean functions describing the half-adder are :-

$$S = A \oplus B C$$

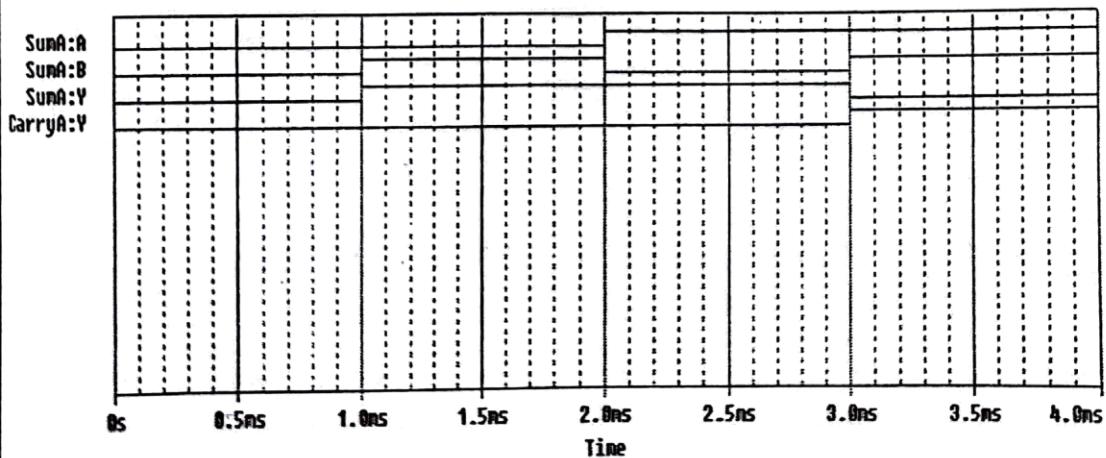
$$\text{Sum} = A \oplus B$$

$$C = AB$$

$$\text{Carry} = AB$$

Model Timing Diagram:

Half-Adder



Full Adder Circuit

Truth Table

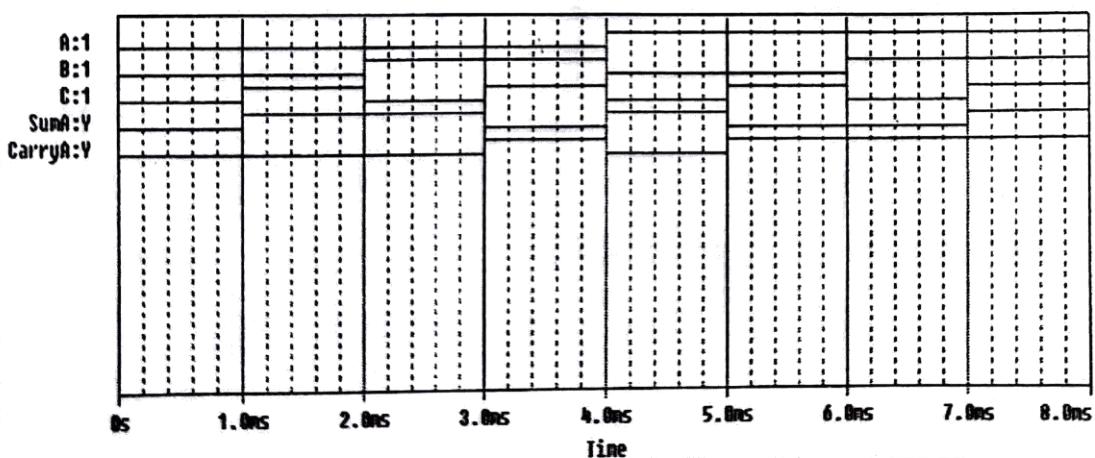
The half-adder does not take the carry bit from its previous stage into account.

This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds the two data bits, A and B, and a carry-in bit, is called a full adder. The Boolean functions describing the full-adder are:

$$\text{Sum} = X \oplus Y \oplus Z$$

$$\text{Carry} = Z(X \oplus Y) + XY$$

Full - Adder



Procedure:

- 1) Make connections as shown in the diagram
- 2) Construct the truth tables for both half-adder and full-adder.
- 3) For each input, record the sum and carry output of each half-adder and full-adder.
- 4) Verify the truth tables and observe the outputs.
- 5) Obtain the graph using PSpice.

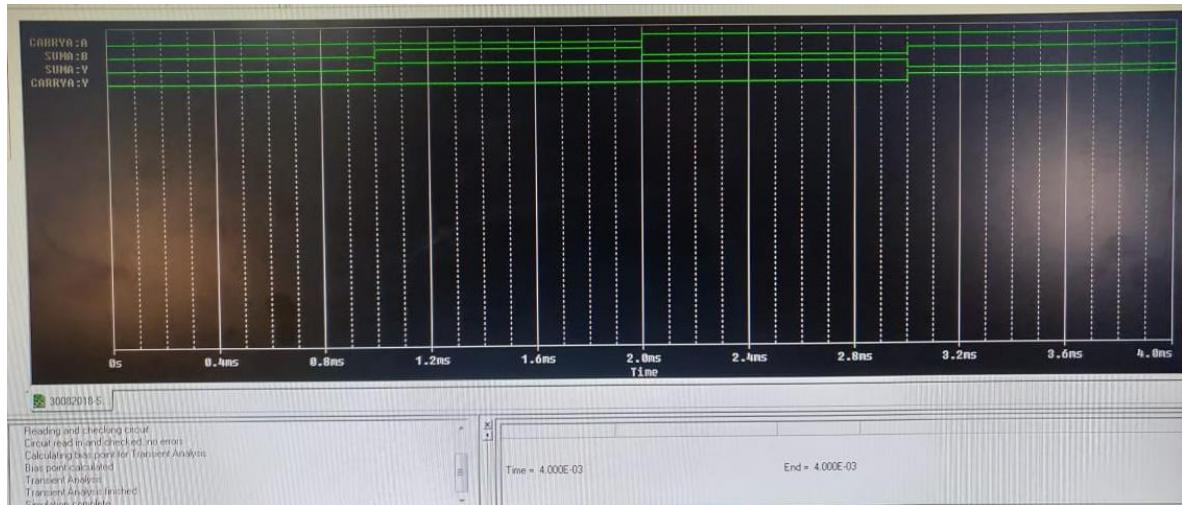
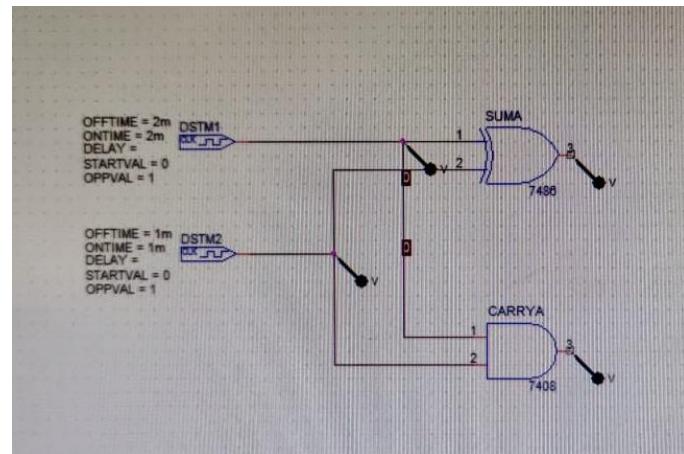
Result:

The model timing diagram is same as the simulated graph obtained.
Hence, the logic circuits are verified.

Inference:

- 1) The ALU (arithmetic logic circuitry) of a computer uses half-adder to compute the binary addition of two bits.
- 2) Full-adder reduces circuit complexity.

HALF-ADDER CIRCUIT & GRAPH:



FULL-ADDER CIRCUIT & GRAPH:

