DIGITAL LOGIC AND MICROPROCESSOR

Registration Number:	**18BIT0272**
Name:	PRIYAL BHARDWAJ
Slot:	L7+L8
Experiment Name:	Verification of GATES

OR GATE

Truth Table:

A	B	Output/C
0	0	0
0	1	1
1	0	1
1	1	1

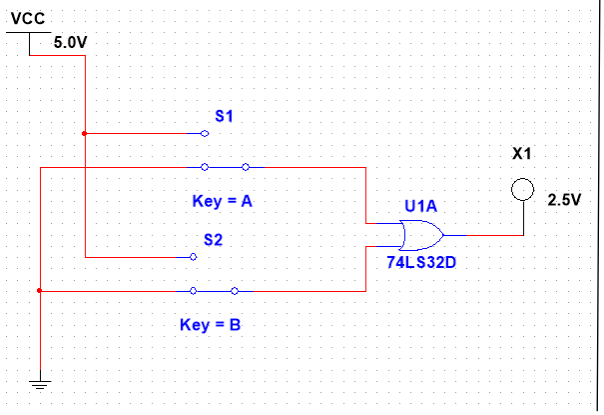
Expression:

A+B=C

Multi Sim Circuit Diagram:

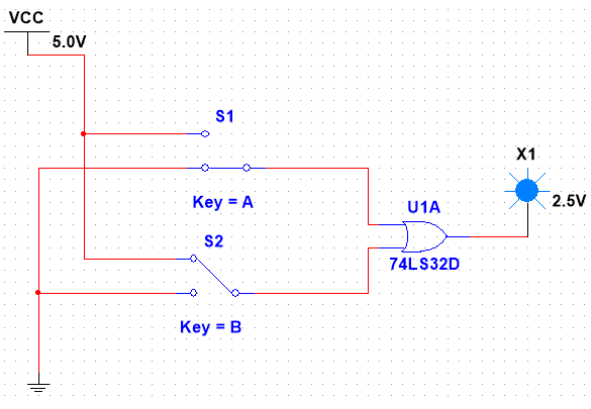
A B C

0 0 0



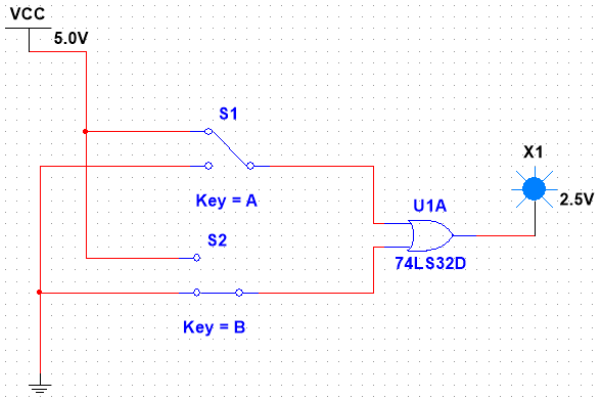
A B C

0 1 1



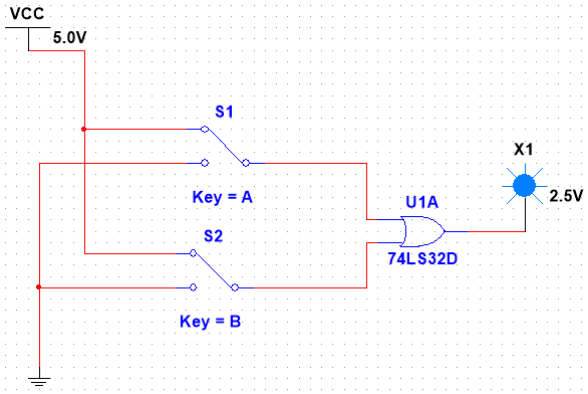
A B C

1 0 1



A B C

1 1 1



NOR GATE

Truth Table:

A	B	Output/C
0	0	1
0	1	0
1	0	0
1	1	0

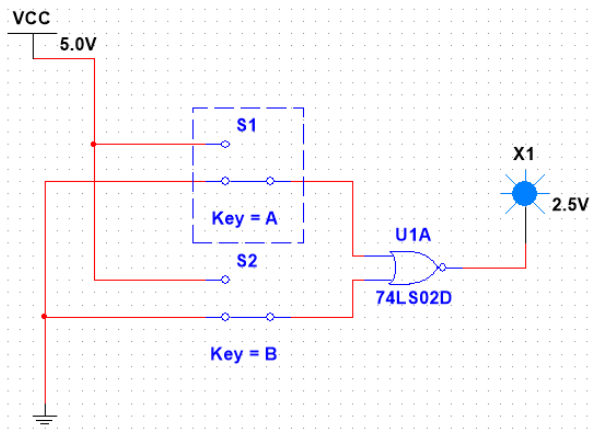
Expression:

$\overline{(A+B)}=C$

Multi Sim Circuit Diagram:

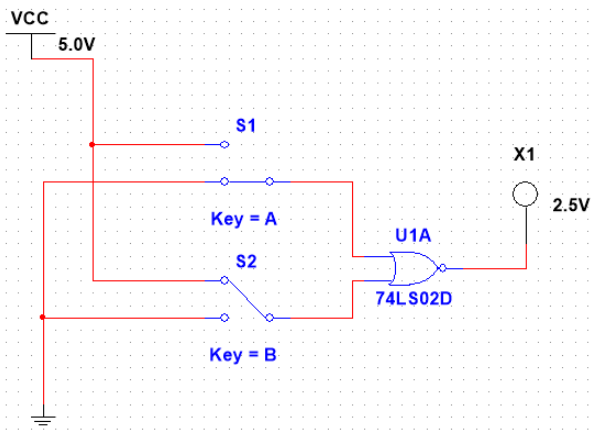
A B C

0 0 1



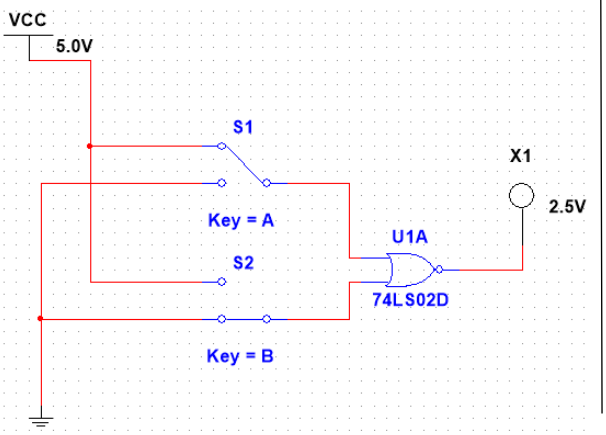
A B C

0 1 0



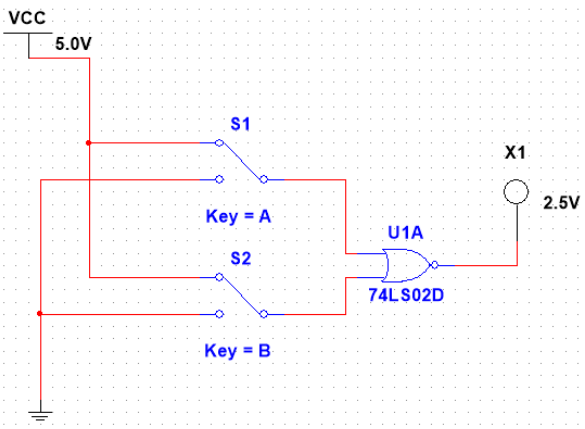
A B C

1 0 0



A B C

1 1 0



AND GATE

Truth Table:

A	B	Output/C
0	0	0
0	1	0
1	0	0
1	1	1

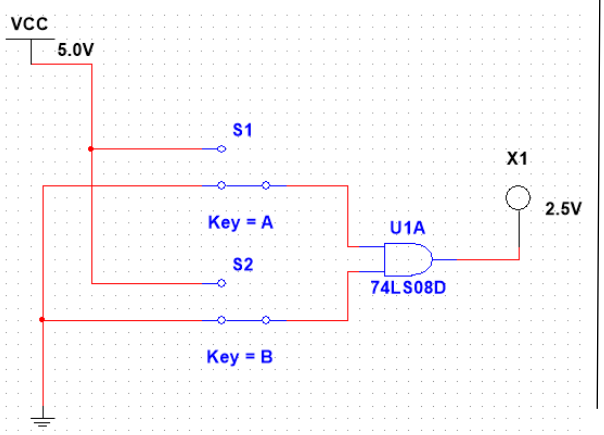
Expression:

AB=C

Multi Sim Circuit Diagram:

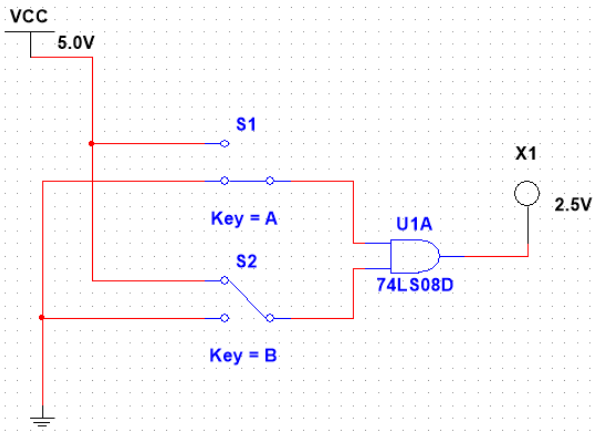
A B C

0 0 0

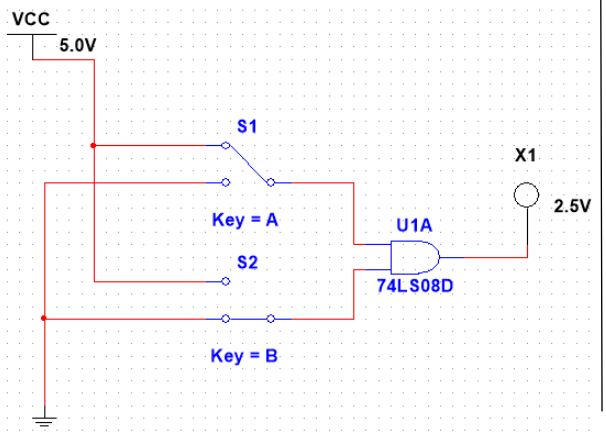


A B C

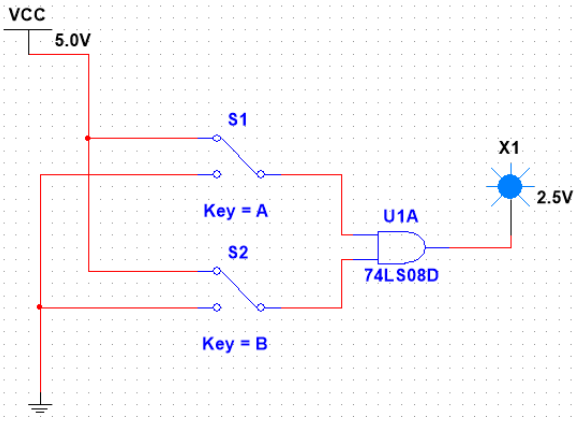
0 1 0



A	B	C
1	0	0



A	B	C
1	1	1



NAND GATE

Truth Table:

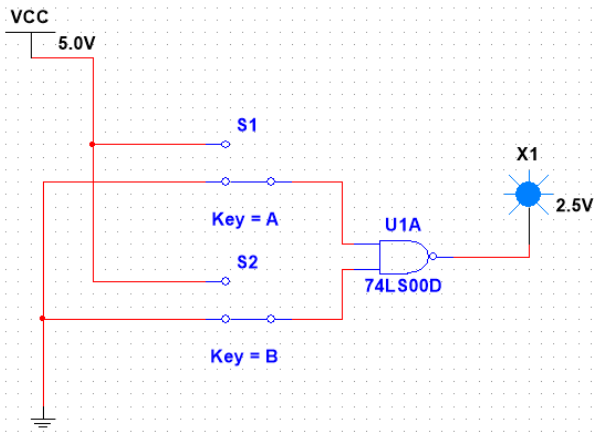
A	B	Output/C
0	0	1
0	1	1
1	0	1
1	1	0

Expression:

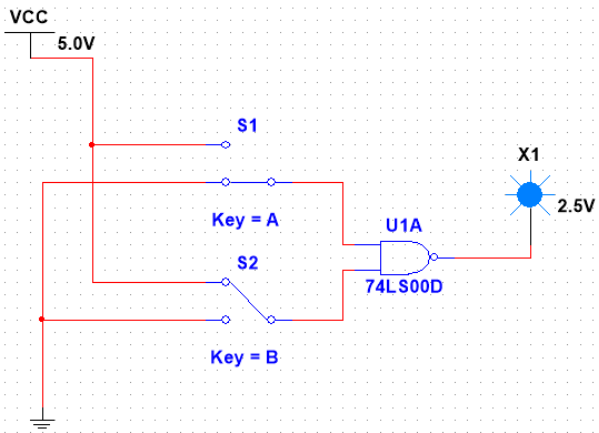
$\overline{A}\overline{B}=C$

Multi Sim Circuit Diagram:

A	B	C
0	0	1

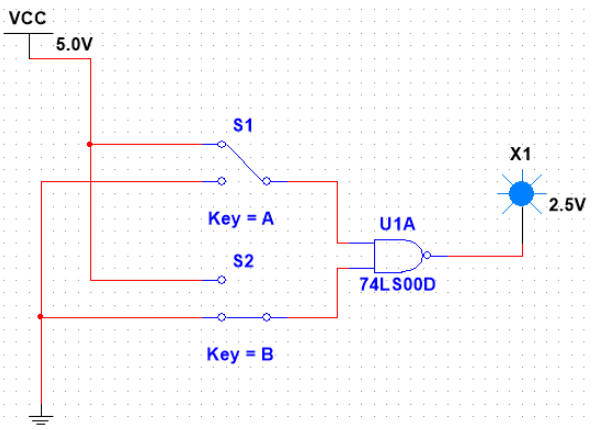


A	B	C
0	1	1



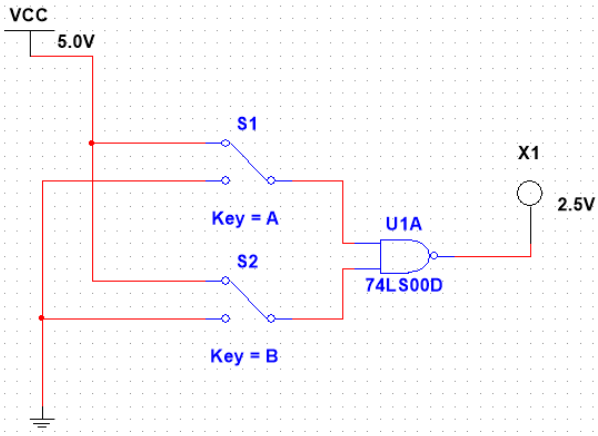
A B C

1 0 1



A B C

1 1 0



NOT GATE

Truth Table:

A	$\overline{A}$
0	1
1	0

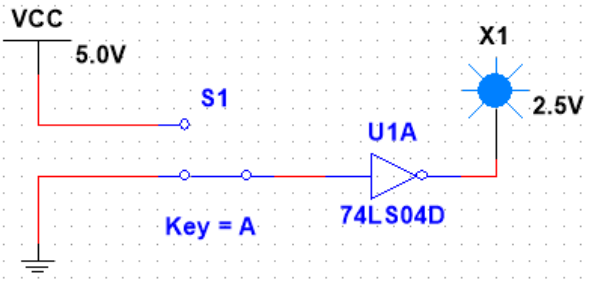
Expression:

$A=\overline{A}$

Multi Sim Circuit Diagram:

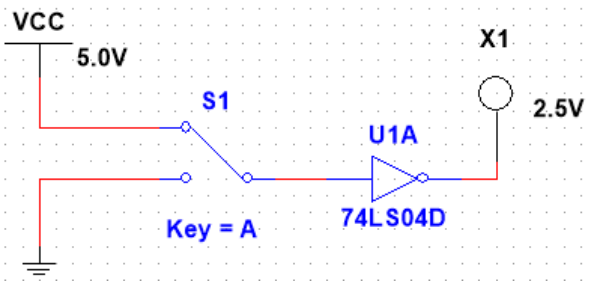
A $\overline{A}$

0 1



A $\overline{A}$

1 0



XOR GATE

Truth Table:

A	B	Output/C
0	0	0
0	1	1
1	0	1
1	1	0

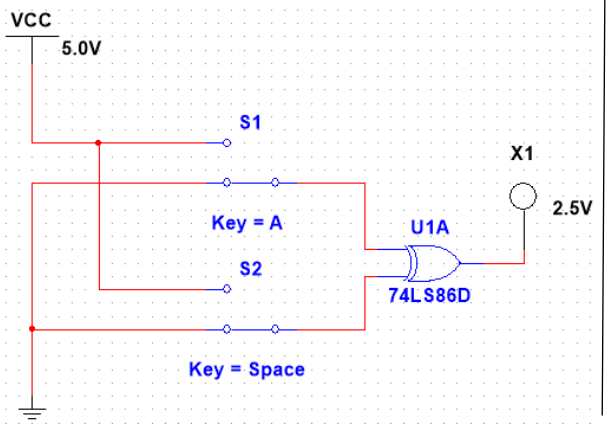
Expression:

$\overline{A}B+A\overline{B}=C$

Multi Sim Circuit Diagram:

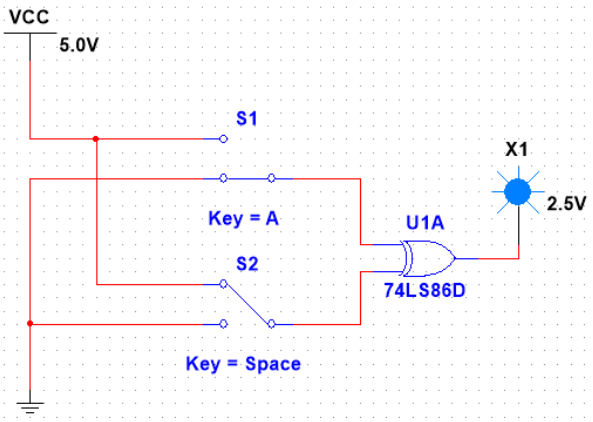
A B C

0 0 0



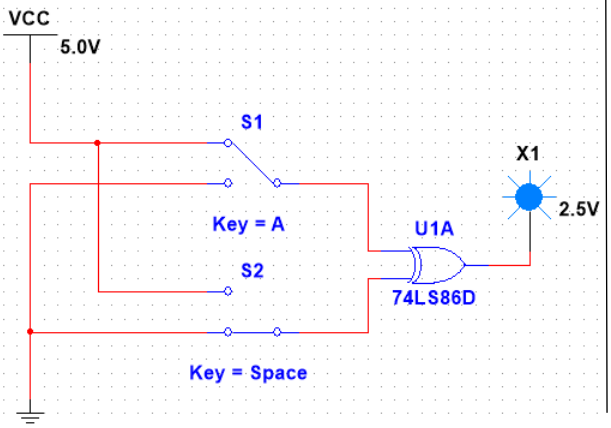
A B C

0 1 1



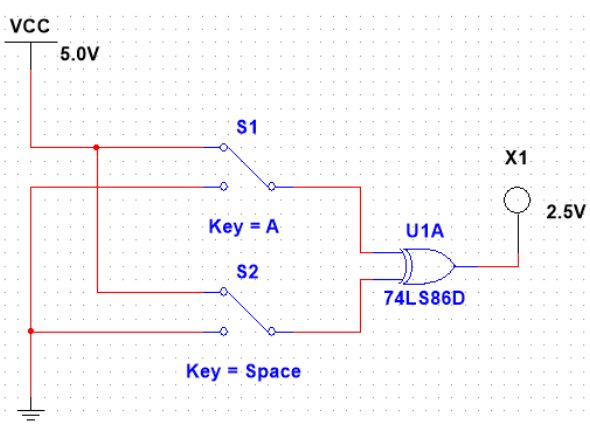
A B C

1 0 1



A B C

1 1 0



XNOR GATE

Truth Table:

A	B	Output/C
0	0	1
0	1	0
1	0	0
1	1	1

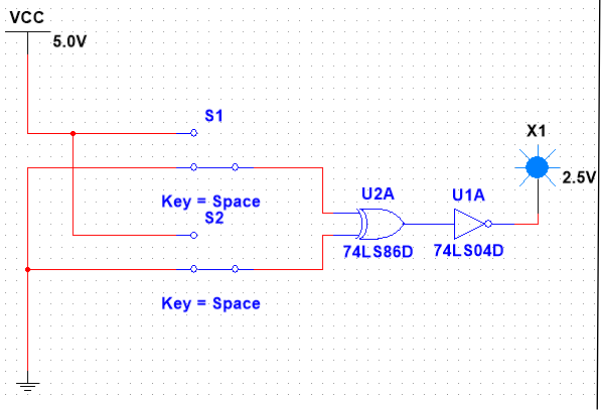
Expression:

$AB+\bar{A}\bar{B}=C$

Multi Sim Circuit Diagram:

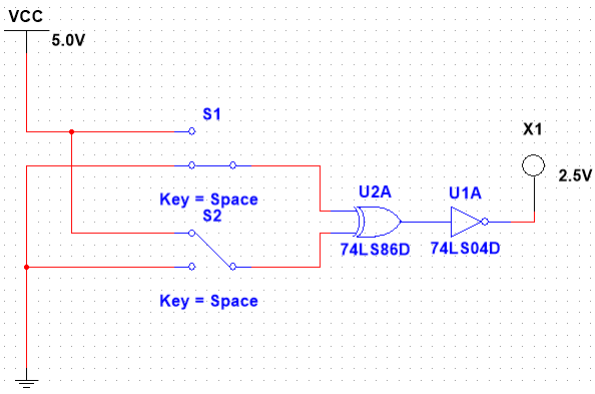
A B C

0 0 1



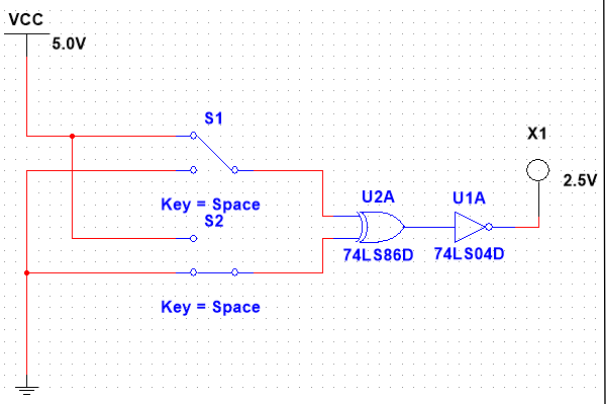
A B C

0 1 0



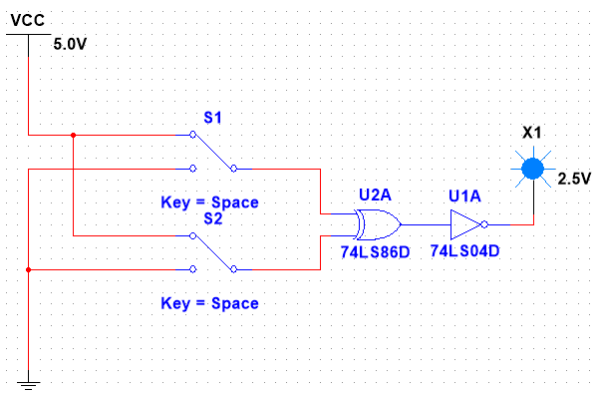
A B C

1 0 0



A B C

1 1 1



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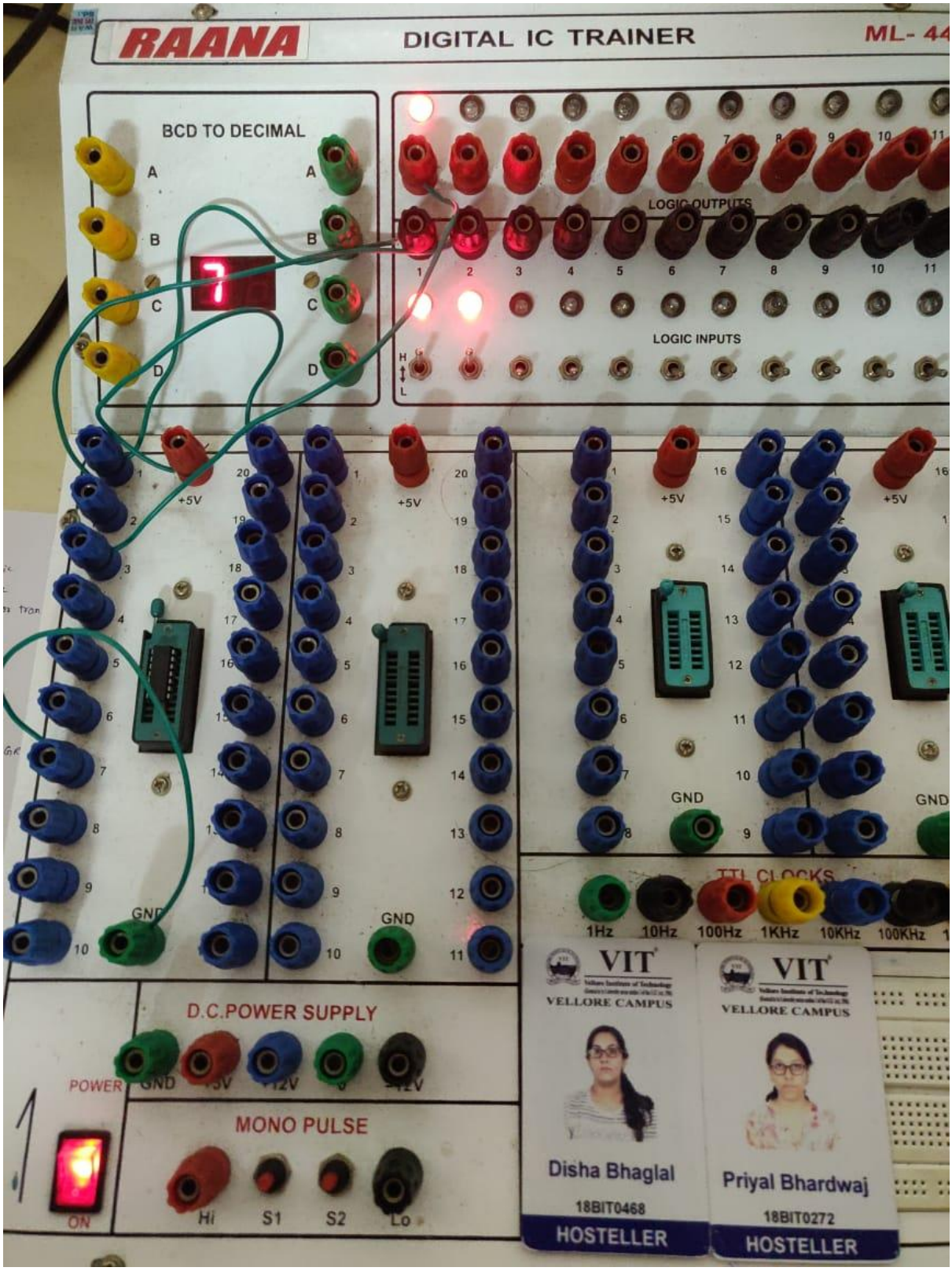
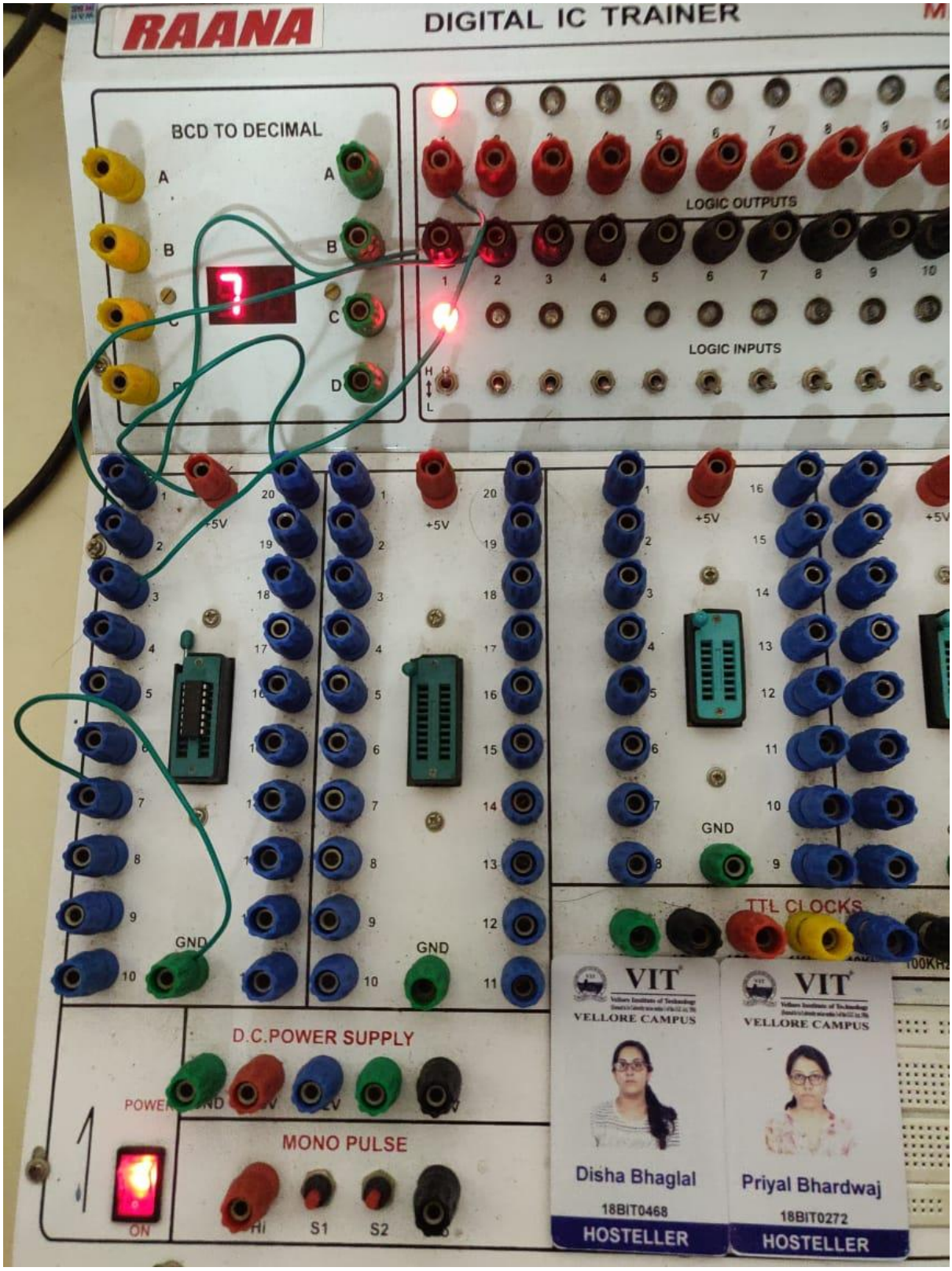
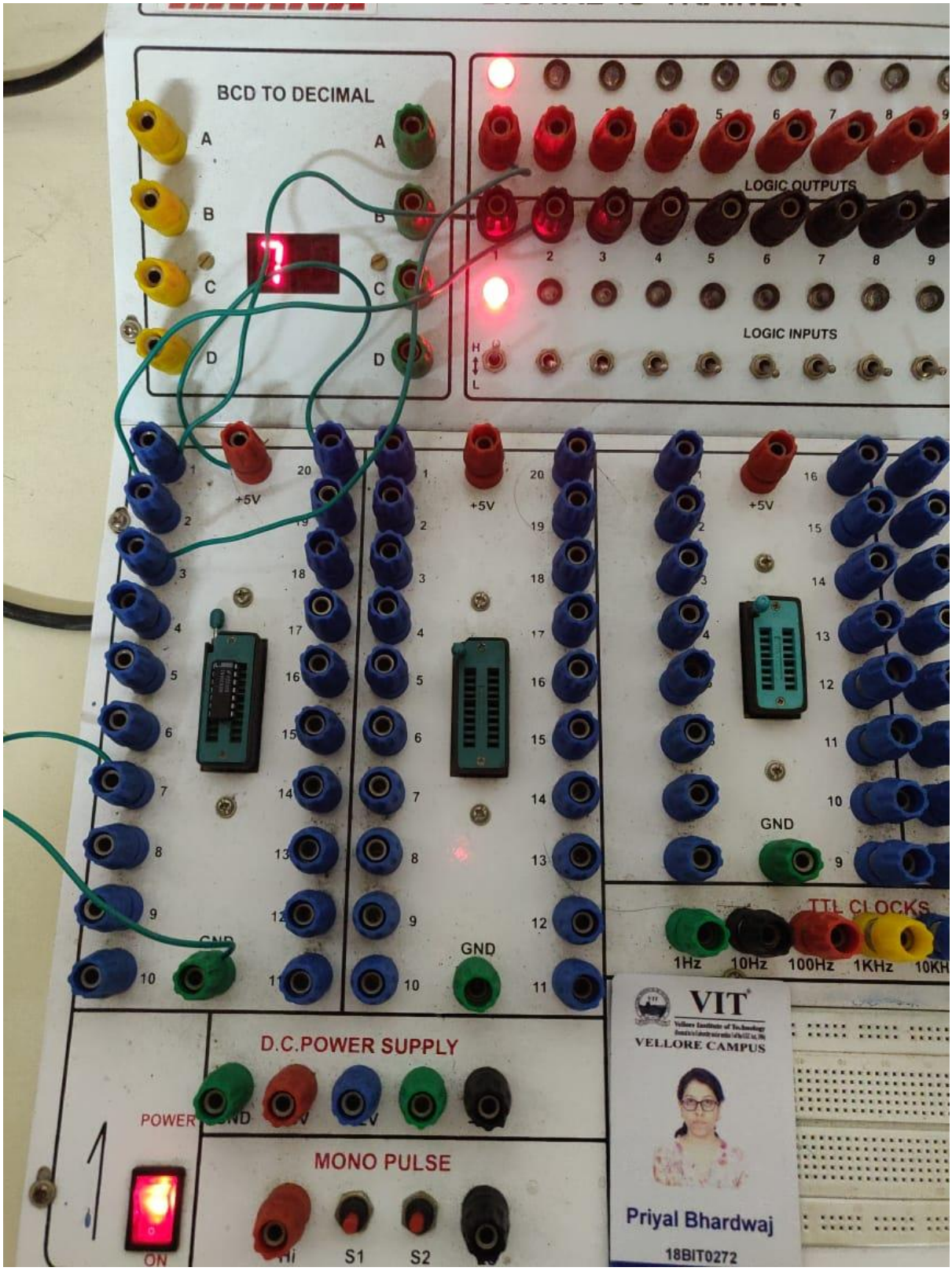
OR GATE:


RAANA
DIGITAL IC TRAINER
ML- 44
BCD TO DECIMAL
A
B
C
D
LOGIC OUTPUTS
LOGIC INPUTS
+5V
GND
TTL CLOCKS
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
D.C.POWER SUPPLY
POWER
ON
MONO PULSE
Hi
S1
S2
Lo
VIT
VELLORE CAMPUS
Disha Bhaglal
18BIT0468
HOSTELLER
VIT
VELLORE CAMPUS
Priyal Bhardwaj
18BIT0272
HOSTELLER

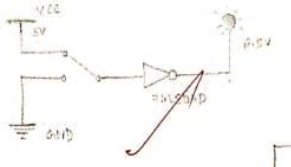
NAND GATE:


RAANA
DIGITAL IC TRAINER
BCD TO DECIMAL
A
B
C
D
LOGIC OUTPUTS
LOGIC INPUTS
+5V
GND
TTL CLOCKS
D.C.POWER SUPPLY
MONO PULSE
S1
S2
ON
VIT
VELLORE CAMPUS
Disha Bhaglal
18BIT0468
HOSTELLER
VIT
VELLORE CAMPUS
Priyal Bhardwaj
18BIT0272
HOSTELLER

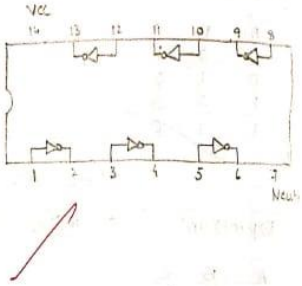
EX-OR GATE:


BCD TO DECIMAL
A
B
C
D
LOGIC OUTPUTS
LOGIC INPUTS
+5V
GND
TTL CLOCKS
1Hz
10Hz
100Hz
1KHz
D.C.POWER SUPPLY
POWER
ON
MONO PULSE
S1
S2
VIT
VELLORE CAMPUS
Priyal Bhardwaj
18BIT0272

Circuit



Pin diagram



Expt. No.....

Date.....

Page No. 3

Y. NOT GATE

Expression :- $B = \bar{A}$

A	B
0	1
1	0

H/W completed

Mr. Shubham

Teacher's Signature : _____

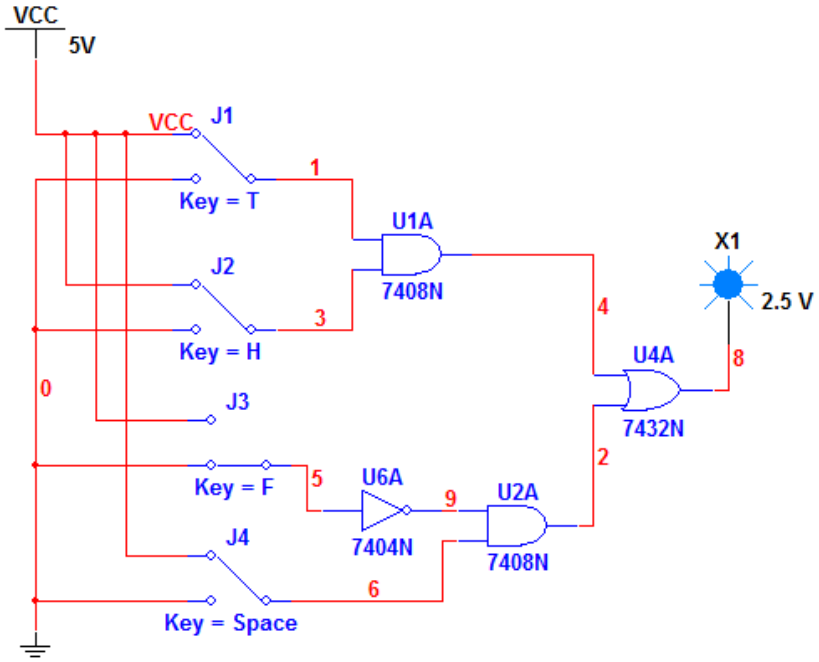
Experiment Name: **Implementation of Boolean Expressions**

1. Implement the following Boolean Expressions using Basic Logic Gates
   a. F = AB + C'D

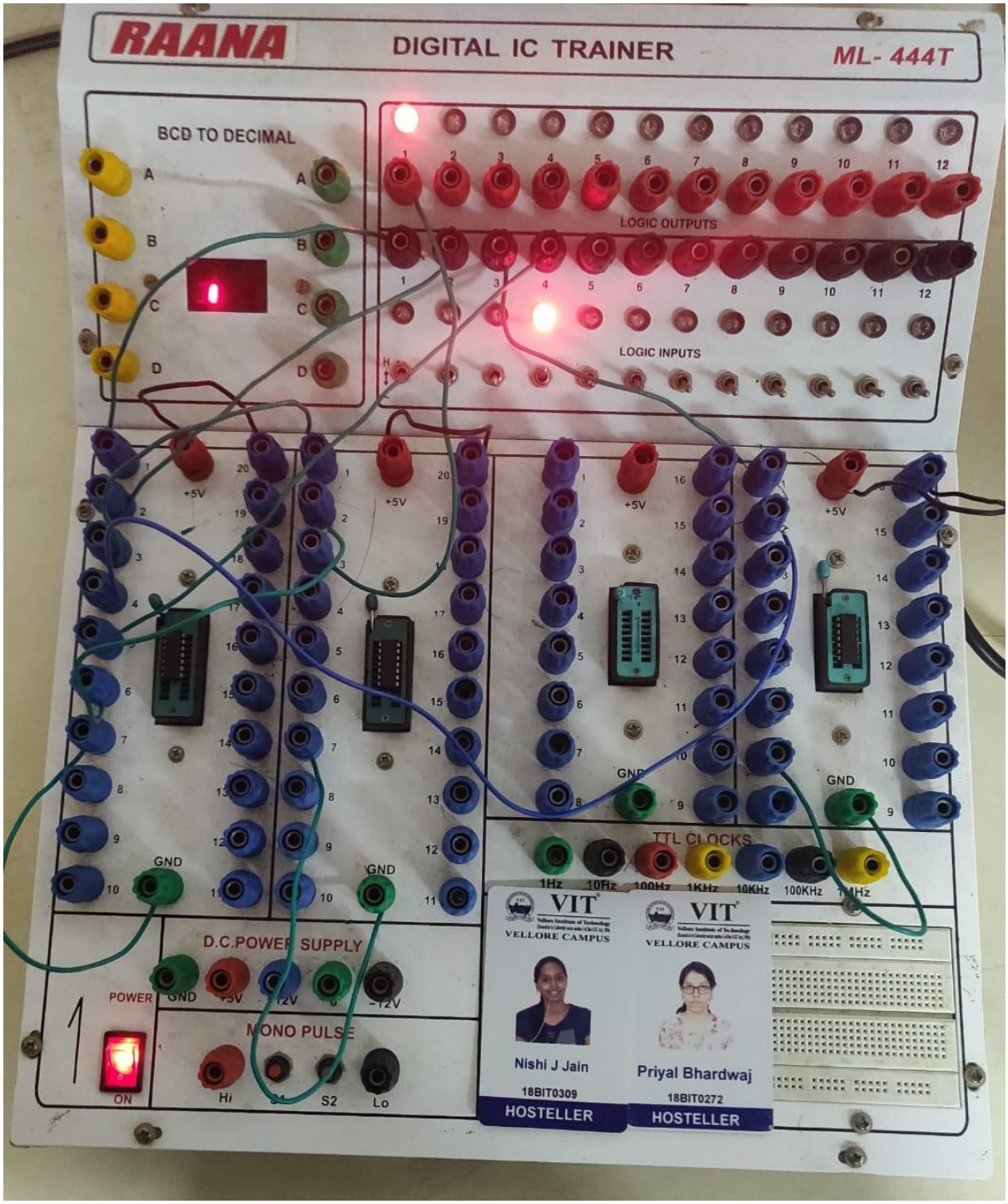
Truth Table:

A	B	C	D	C'	AB	C'D	F
0	0	0	0	1	0	0	0
0	0	0	1	1	0	1	1
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	1	0	0	0
0	1	0	1	1	0	1	1
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	1
1	1	1	0	0	1	0	1
1	1	1	1	0	1	0	1

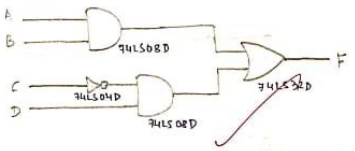
Multi Sim Circuit Diagram:



HARDWARE:


RAANA
DIGITAL IC TRAINER
ML- 444T
BCD TO DECIMAL
A
B
C
D
LOGIC OUTPUTS
LOGIC INPUTS
+5V
GND
TTL CLOCKS
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
D.C.POWER SUPPLY
POWER
ON
MONO PULSE
Hi
S2
Lo
VIT
VELLORE CAMPUS
Nishi J Jain
18BIT0309
HOSTELLER
Priyal Bhardwaj
18BIT0272
HOSTELLER

1(a)



H/W verified

Expt. No. 2 Date

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Implementation of Boolean expressions

(1) Implement the following boolean expressions using logic gates

(a) $F = AB + \bar{C}D$

A	B	C	D	$\bar{C}$	AB	$\bar{C}D$	F
0	0	0	0	1	0	0	0
0	0	0	1	1	0	1	1
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	1	0	0	0
0	1	0	1	1	0	1	1
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	1
1	1	1	0	0	1	0	1
1	1	1	1	0	1	0	1

Teacher's Signature :

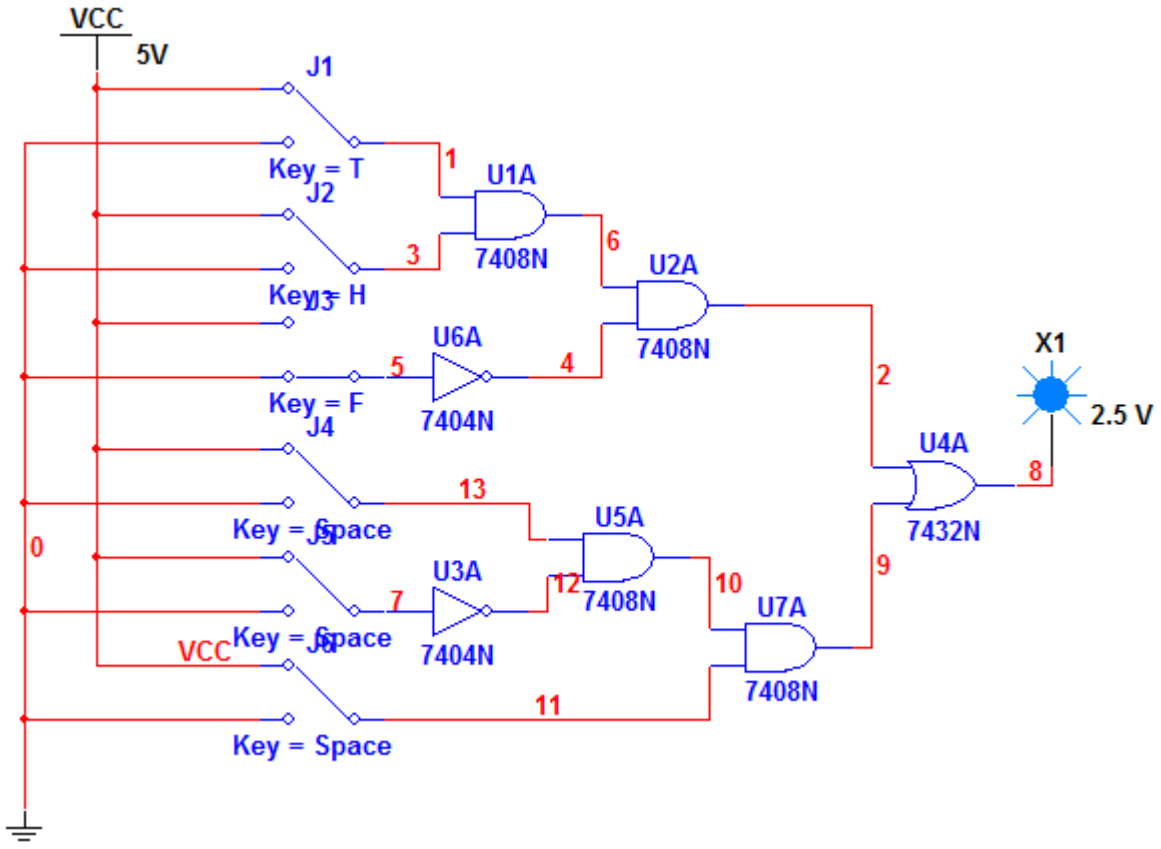
b. F = ABC’ + DE’F

Truth Table:

A	B	C	D	E	F	C’	E’	ABC’	DE’F	F
0	0	0	0	0	0	1	1	0	0	0
0	0	0	0	0	1	1	1	0	0	0
0	0	0	0	1	0	1	0	0	0	0
0	0	0	0	1	1	1	0	0	0	0
0	0	0	1	0	0	1	1	0	0	0
0	0	0	1	0	1	1	1	0	1	1
0	0	0	1	1	0	1	0	0	0	0
0	0	0	1	1	1	1	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0
0	0	1	0	0	1	0	1	0	0	1
0	0	1	0	1	0	0	0	0	0	0
0	0	1	0	1	1	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0
0	0	1	1	0	1	0	1	0	1	1
0	0	1	1	1	0	0	0	0	0	0
0	0	1	1	1	1	0	0	0	0	0
0	1	0	0	0	0	1	1	0	0	0
0	1	0	0	0	1	1	1	0	0	0
0	1	0	0	1	0	1	0	0	0	0
0	1	0	0	1	1	1	0	0	0	0
0	1	0	1	0	0	1	1	0	0	0
0	1	0	1	0	1	1	1	0	1	1
0	1	0	1	1	0	1	0	0	0	0
0	1	0	1	1	1	1	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0
0	1	1	0	0	1	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0	0
0	1	1	0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0
0	1	1	1	0	1	0	1	0	1	1
0	1	1	1	1	0	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0	0
1	0	0	0	0	0	1	1	0	0	0
1	0	0	0	0	1	1	1	0	0	0
1	0	0	0	1	0	1	0	0	0	0
1	0	0	0	1	1	1	0	0	0	0
1	0	0	1	0	0	1	1	0	0	0
1	0	0	1	0	1	1	1	0	1	1
1	0	0	1	1	0	1	0	0	0	0
1	0	0	1	1	1	1	0	0	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	1	0	0	0

1	0	1	0	1	0	0	0	0	0	0
1	0	1	0	1	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0
1	0	1	1	0	1	0	1	0	1	1
1	0	1	1	1	0	0	0	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	0	1	1	1	0	0
1	1	0	0	0	1	1	1	1	0	0
1	1	0	0	1	0	1	0	1	0	0
1	1	0	0	1	1	1	0	1	0	0
1	1	0	1	0	0	1	1	1	0	0
1	1	0	1	0	1	1	1	1	1	1
1	1	0	1	1	0	1	0	1	0	0
1	1	0	1	1	1	1	0	1	0	0
1	1	1	0	0	0	0	1	0	0	0
1	1	1	0	0	1	0	1	0	0	0
1	1	1	0	1	0	0	0	0	0	0
1	1	1	0	1	1	0	0	0	0	0
1	1	1	1	0	0	0	1	0	0	0
1	1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	0	0	0	0	0
1	1	1	1	1	1	0	0	0	0	0

Multi Sim Circuit Diagram:



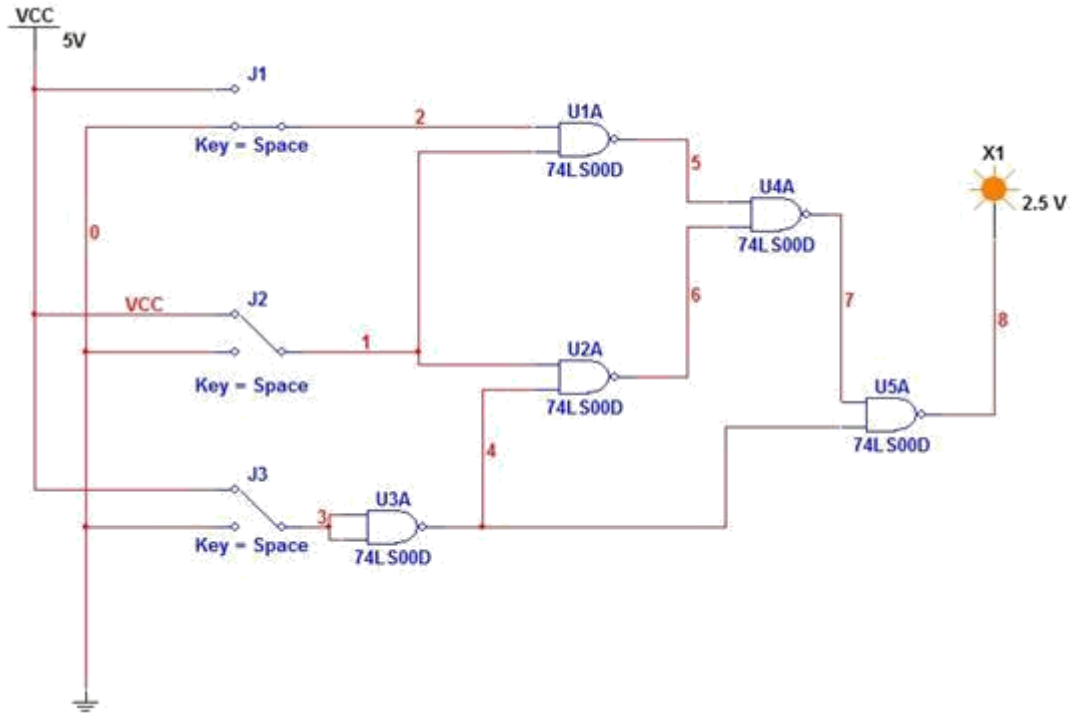
2. Implement the NAND Equivalent circuit for the Boolean Expression

   i. F = AB + BC' + C'

Truth Table:

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Multi Sim Circuit Diagram:

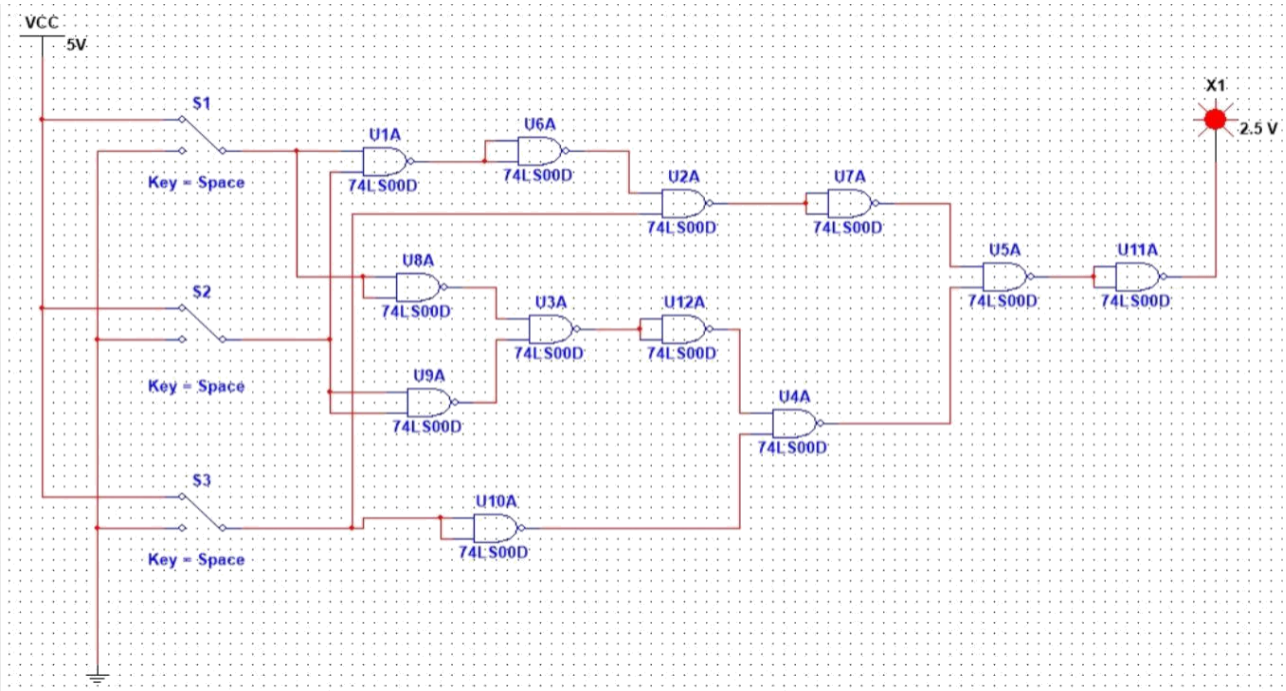


ii. F= (ABC)(A+B+C)

Truth Table:

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Multi Sim Circuit Diagram:

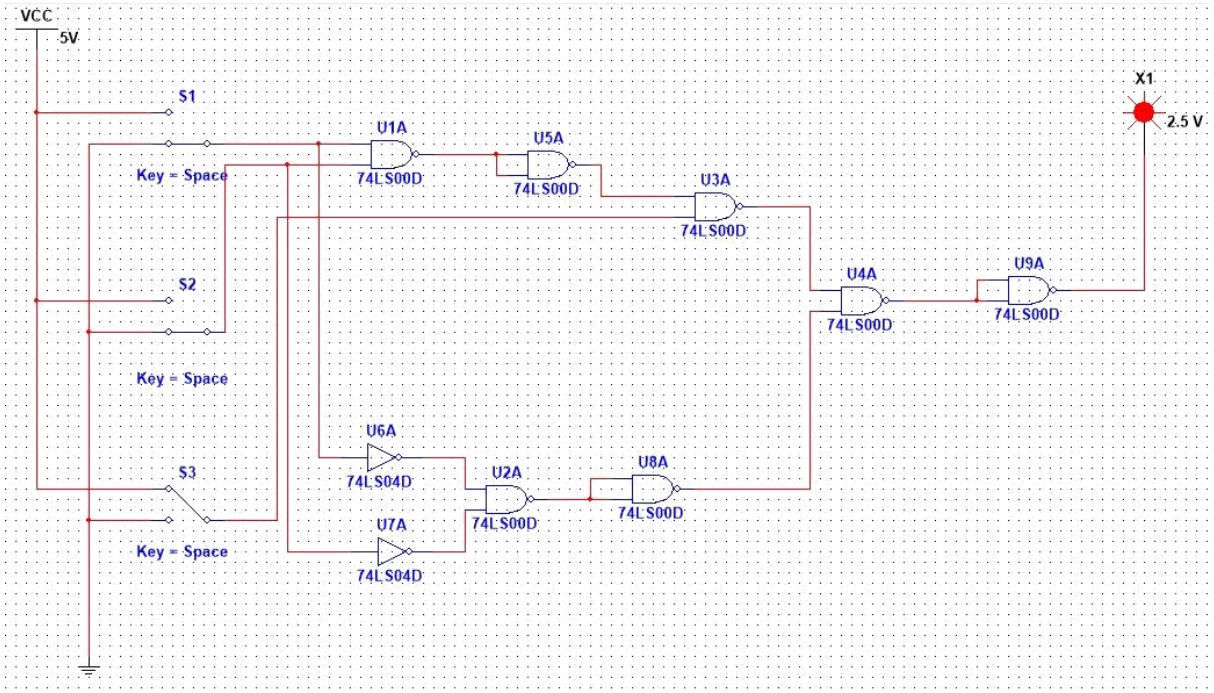


iii. F= (A'+B'+C')(A'B')

Truth Table:

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Multi Sim Circuit Diagram:



Experiment Name: **Design of Combinational Circuits**

1. A manufacturing plant needs to have a horn sound to signal quitting time. The horn should be activated when either of the following conditions is met:

a. It's after 5 o 'clock and all machines are shut down.

b. Its Friday, the production run for the day is complete, and all machines are shut down.

Design a logic circuit that will control the horn. (Hint: use four logic input variables to represent the various conditions, for example, input A will be High only when the time of day is 5 o'clock or later).

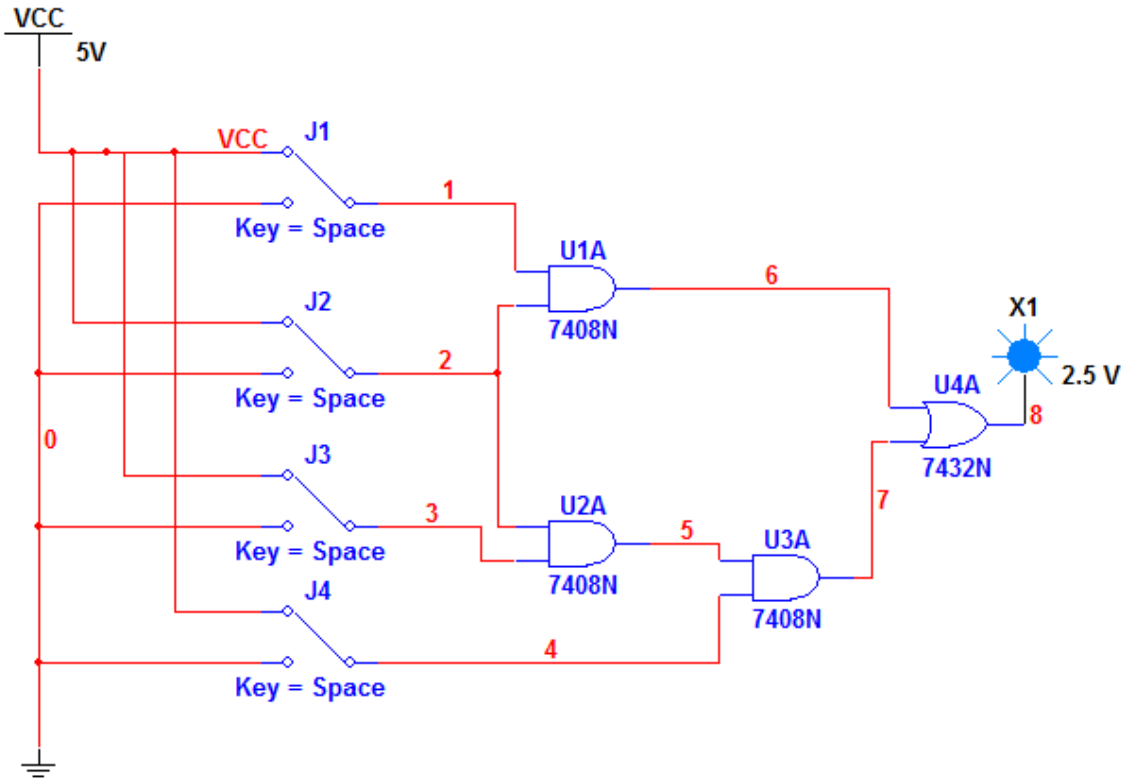
Truth Table:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Expression:

F(A,B,C,D)=m(7,12,13,14,15) **F=AB+BCD**

Multi Sim Circuit Diagram:



2. A bank vault has three locks with a different key for each lock. Each key is owned by a different person. In order to open the door, at least two people must insert their keys into the assigned locks. The signals A, B, and C are 1 if there is a key inserted into lock 1, 2, or 3, respectively. Write an equation for the variable Z, which is 1 if the door should open. Implement the same using basic gates.

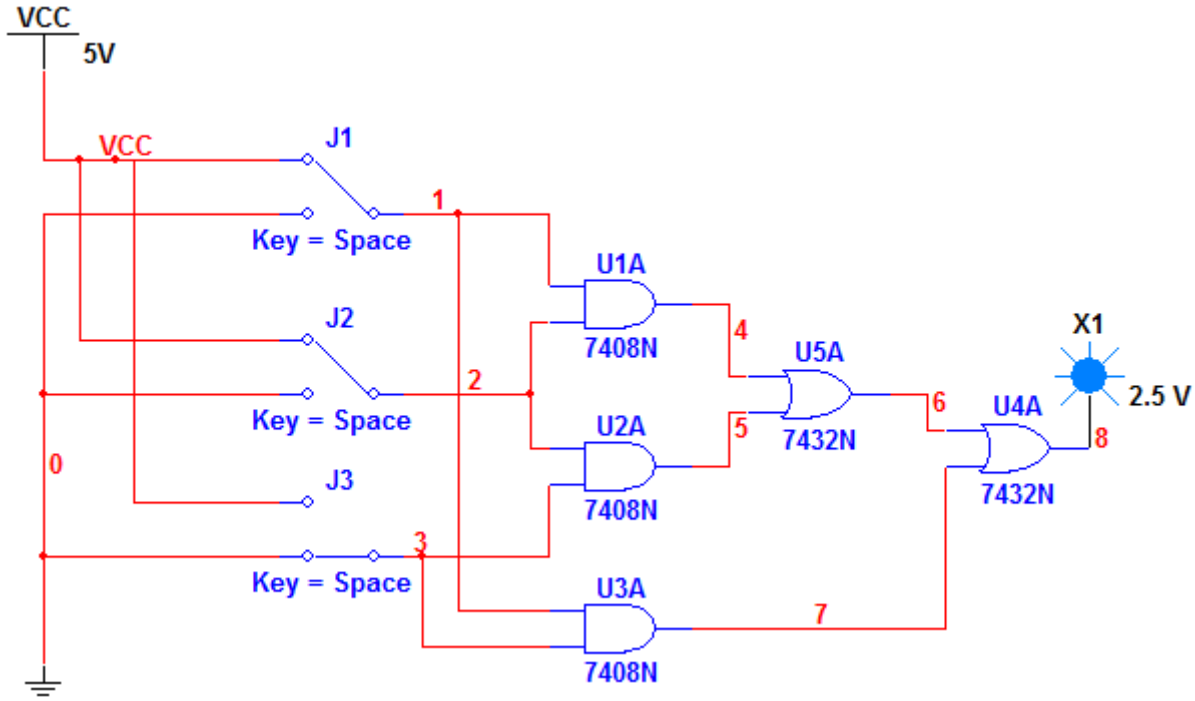
Truth Table:

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Expression:

Z(A,B,C)=m(3,5,6,7) **Z=AB+BC+AC**

Multi Sim Circuit Diagram:



3. Let variables T represent being tall, H being heavy and F being fast. Let's consider anyone who is not tall (T') as short, not heavy as light and not fast as slow. Write a Boolean equation to represent the following:

You may ride (represented by R) a particular amusement park ride only if you are either tall and light, or short and heavy and fast.

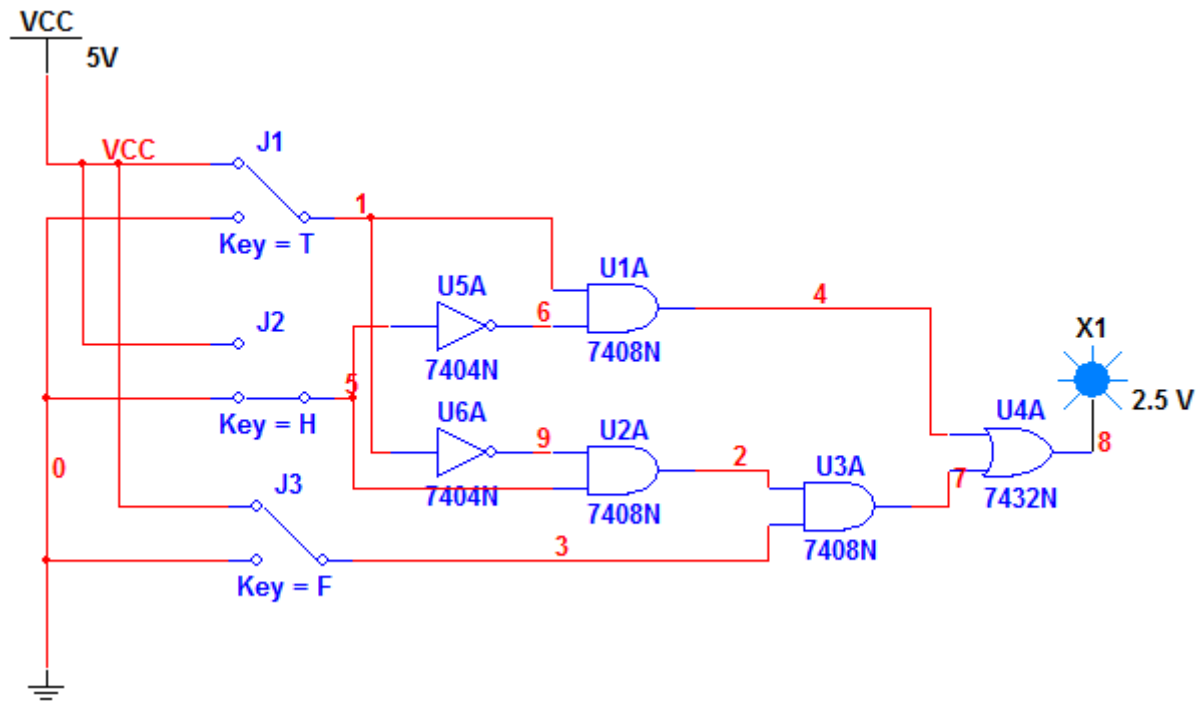
Truth Table:

T	H	F	R
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

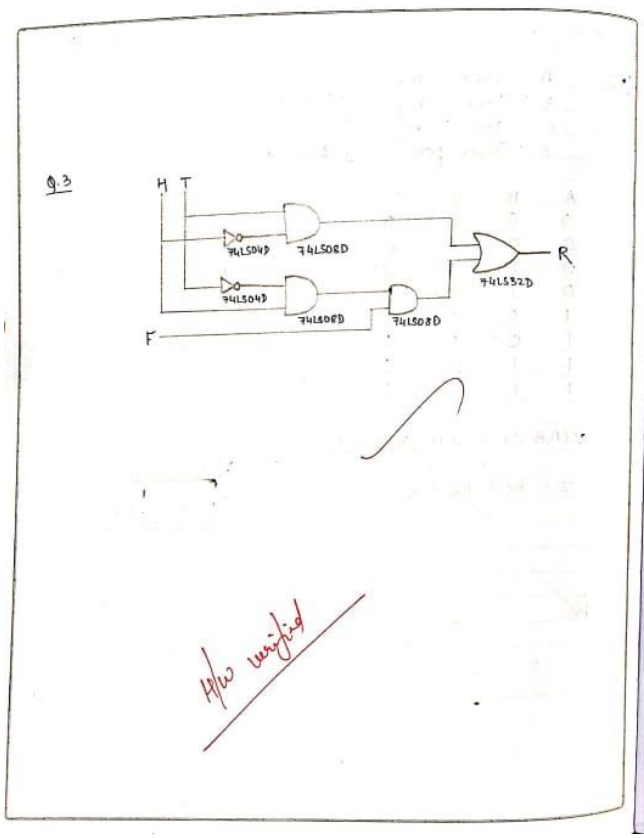
Expression:

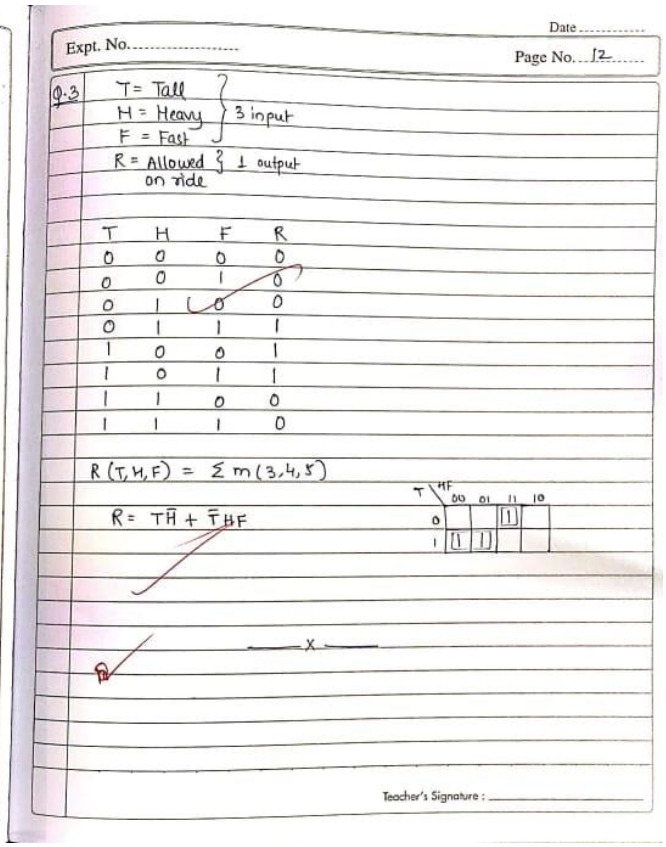
R(T,H,F)=m(3,4,5) **R=TH'+T'HF**

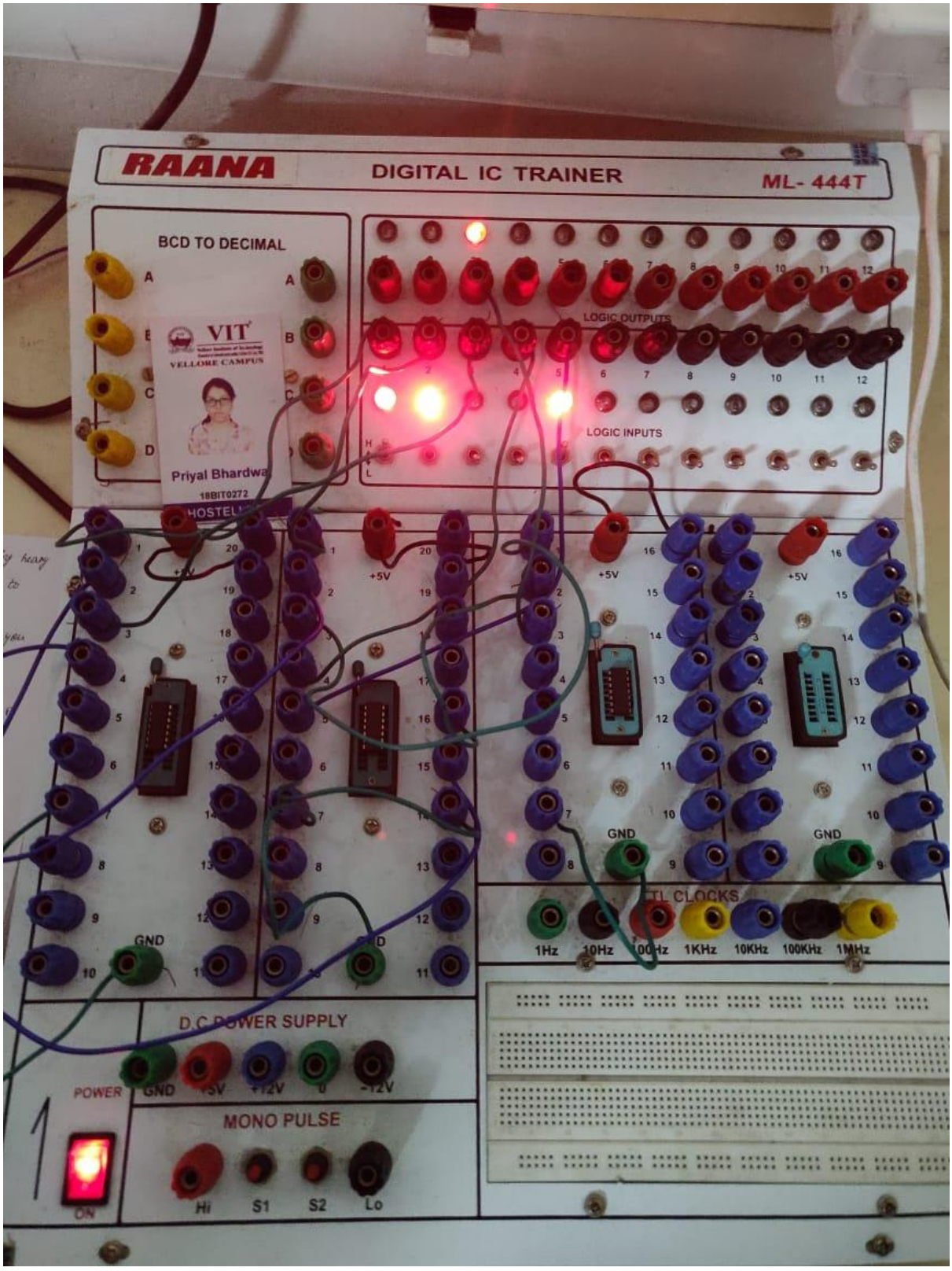
Multi Sim Circuit Diagram:



HARDWARE:






RAANA
DIGITAL IC TRAINER
ML- 444T
BCD TO DECIMAL
LOGIC OUTPUTS
LOGIC INPUTS
VIT
VELLORE CAMPUS
Priyal Bhardwa
18BIT0272
+5V
GND
TTL CLOCKS
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
D.C POWER SUPPLY
POWER
GND
+5V
+12V
0
-12V
MONO PULSE
Hi
S1
S2
Lo
ON

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