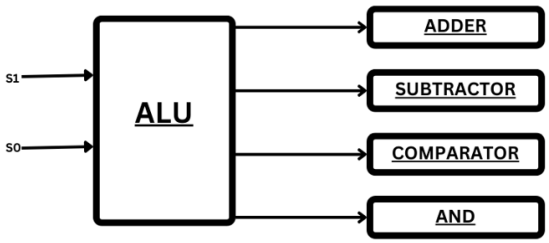
VLSI Project Monsoon 2023

Design an ALU that can perform a 4-Bit addition, subtraction, comparison, ANDing. Estimate the critical path, maximum delay possible in the circuit. Design the layout of your ALU, clearly indicate the location of each standard cell in the design. Compare your pre- and post-layout results. Also, Verify the functionality of your ALU using Verilog.

Tools that can be used:

- NG-SPICE for circuit design.
- Magic for Layout.
- Verilog.

Block Diagram:



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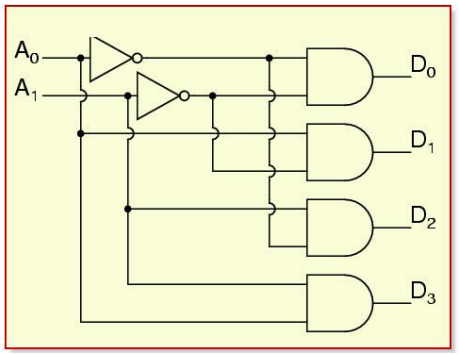
1)ALU-Block:

Here ALU block acts as router to out computational circuit. The operations that needed to be done by ALU is as follows

S1	S0	operation
0	0	Add
0	1	Subtract
1	0	Compare
1	1	And

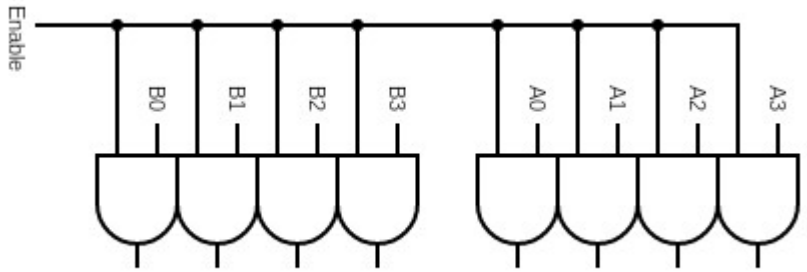
To establish this, we can use a 2-4 decoder.



The enables for the following circuits are as follows; D0 – Adder; D1 – Subtractor; D2 – Comparator; D3 – And

Enable Block:

This is made-up of 8 AND gates whose main purpose is send our values A3A2A1A1, B3B2B1B0 to their respective block if enable is 1 else 0.



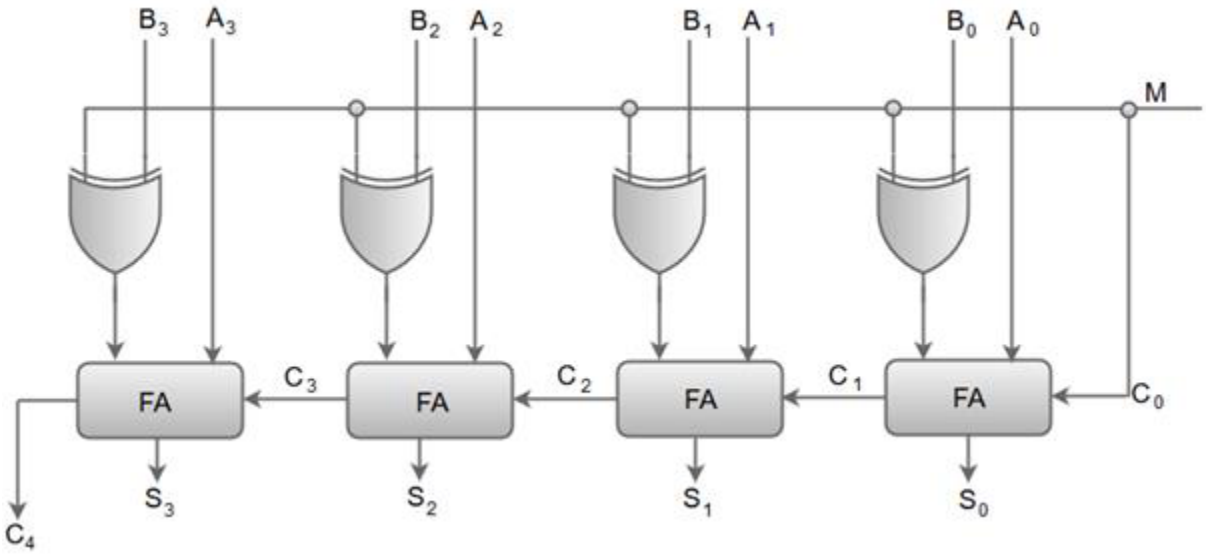
Adder/Subtractor:

Here instead of making a separate Adder and Subtractor we can use a single block which can both act as adder and subtractor. So here we can tie out C0/M wite to S0 directly which would give us an ADDER if input is 00 and a SUBTRACTOR if out input is 01.

Adder operation is A3A2A1A1+ B3B2B1B0

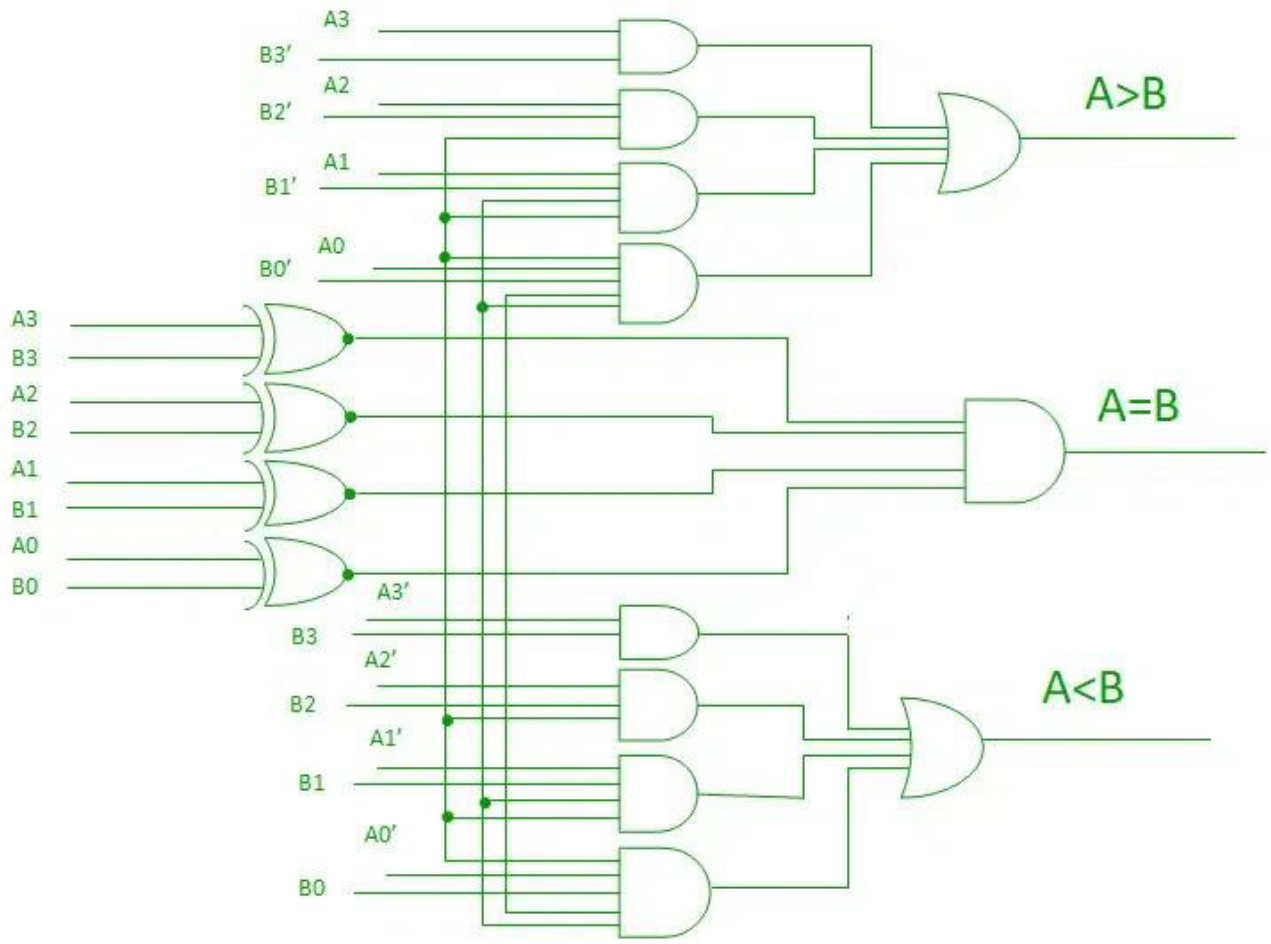
Subtractor operation is A3A2A1A1- B3B2B1B0

4 bit adder-subtractor:



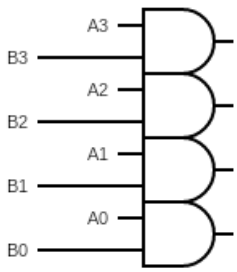
Comparator:

This block would compare our 4-Bit number and give result whether A3A2A1A1 is greater than or less than or equal to B3B2B1B0.



AND Block:

This block Performs AND operation on A3&B3; A0&B0; A1&B1; A0&B0.



Combining all these blocks would give us our ALU.

The final design included would be as follows;