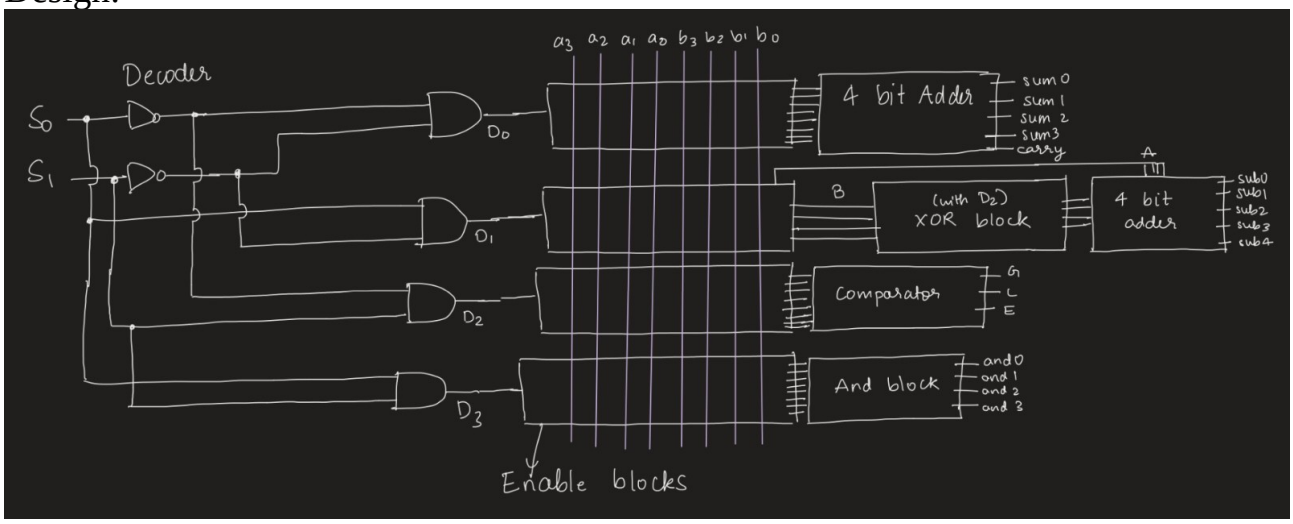
VLSI PROJECT- ALU

Goal : Design an ALU that can perform a 4-Bit addition, subtraction, comparison, ANDing.

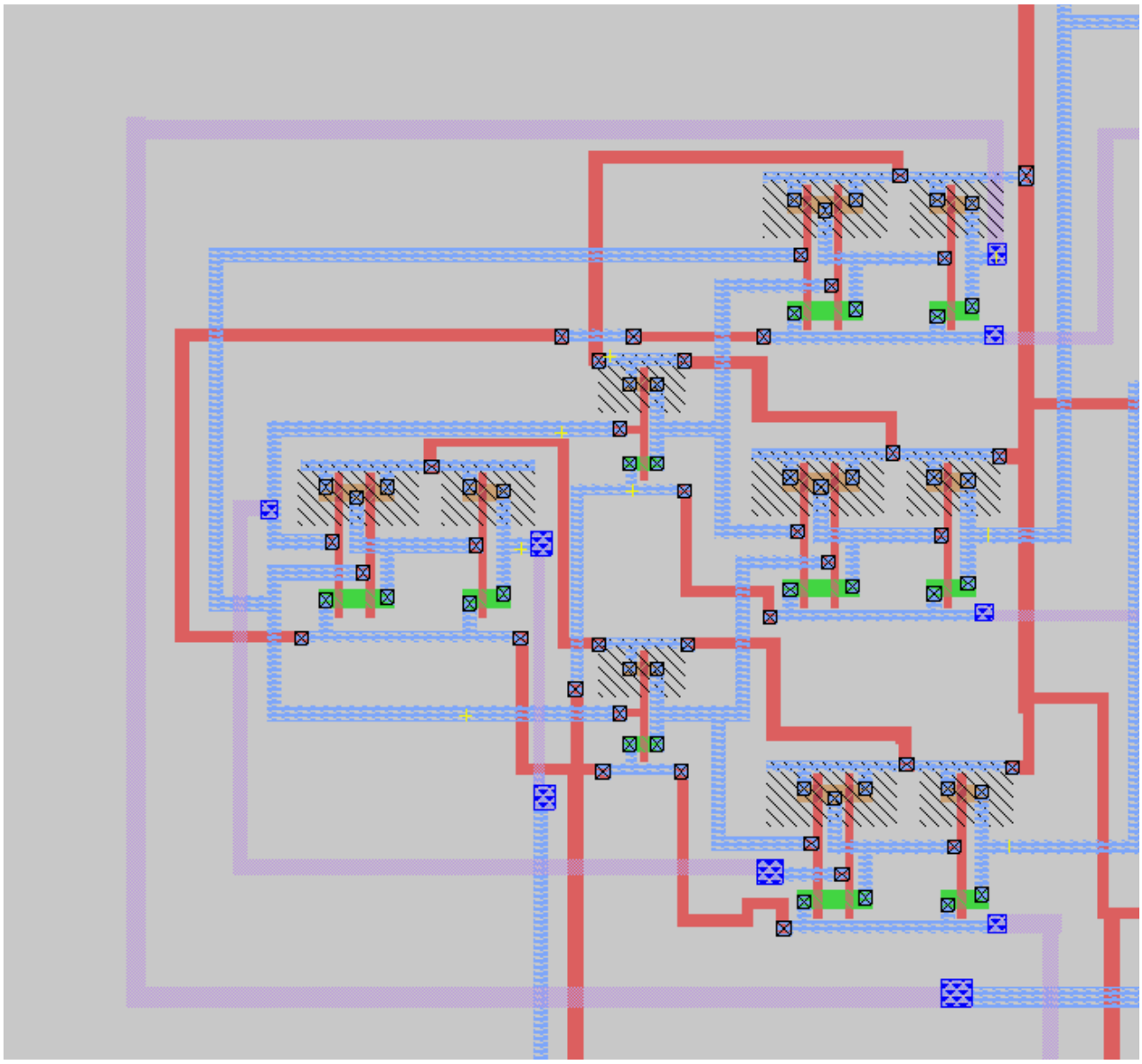
Design:



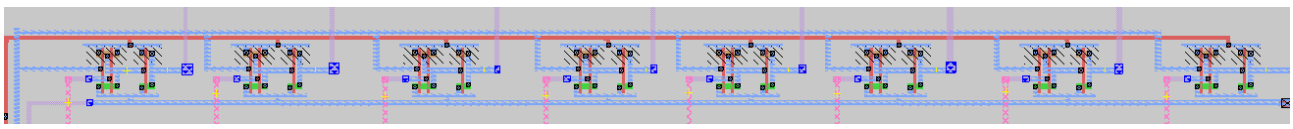
Decoder:

S1	S0	Operation
0	0	Add
0	1	Subtract
1	0	Comparator
1	1	And

Constructed using a 2:4 decoder: Two selection lines S0 and S1 given as input to decide the operation

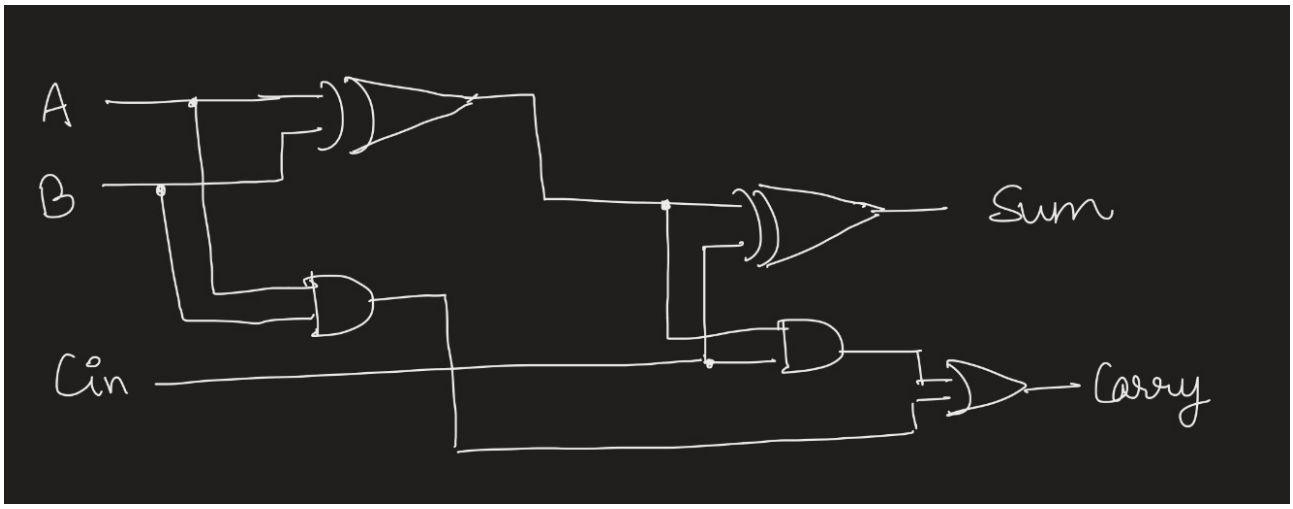


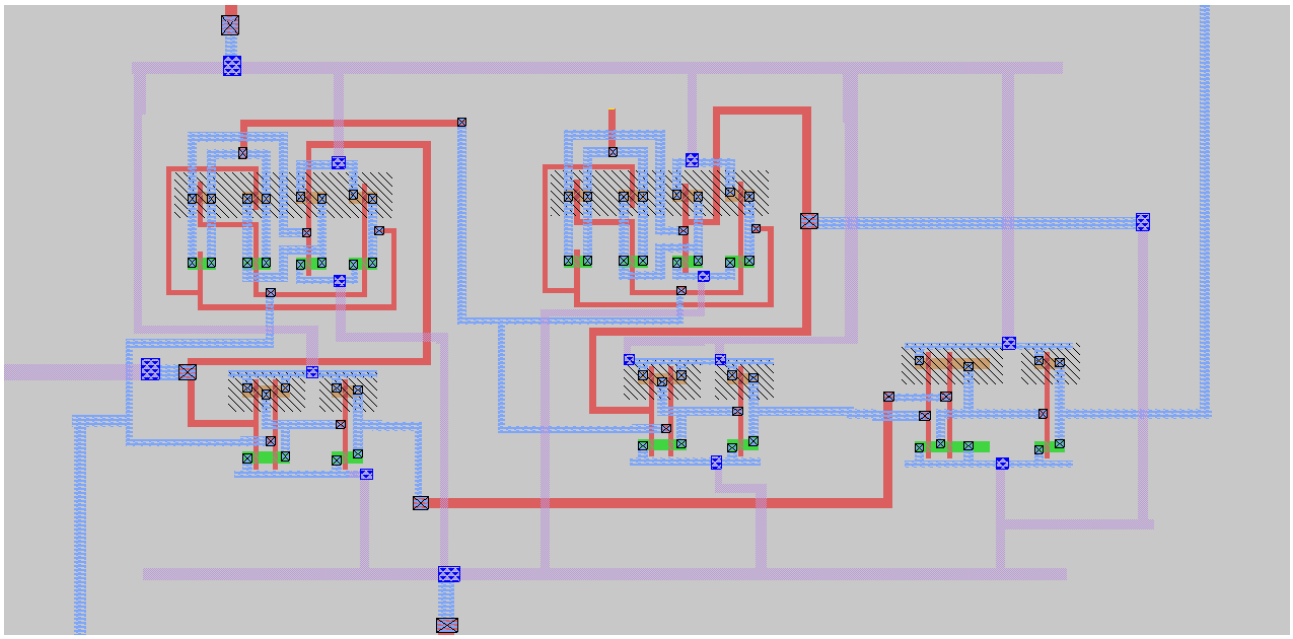
Enable blocks:
For every operation, the inputs A and B are sent to the enable block where they are individually ANDed with the their respective decoder output.

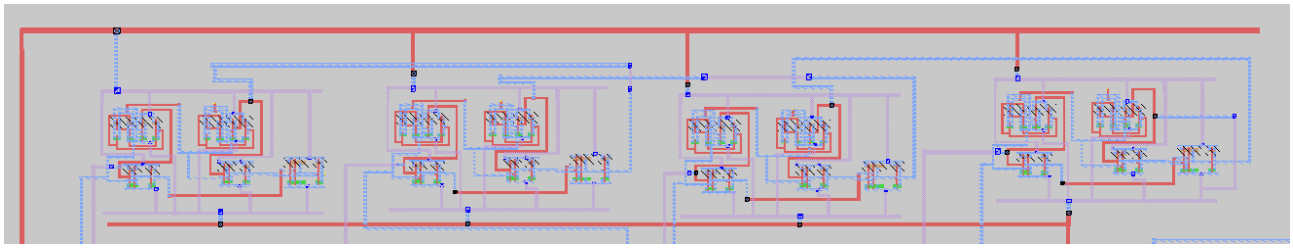


4 Bit Full Adder:

Made using four 1-bit full adders:





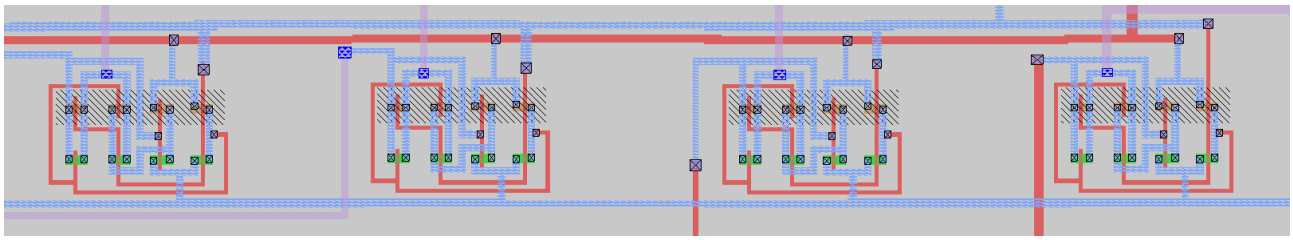


Output was 5 bit to take account of the final carry bit.

4 Bit Full subtractor

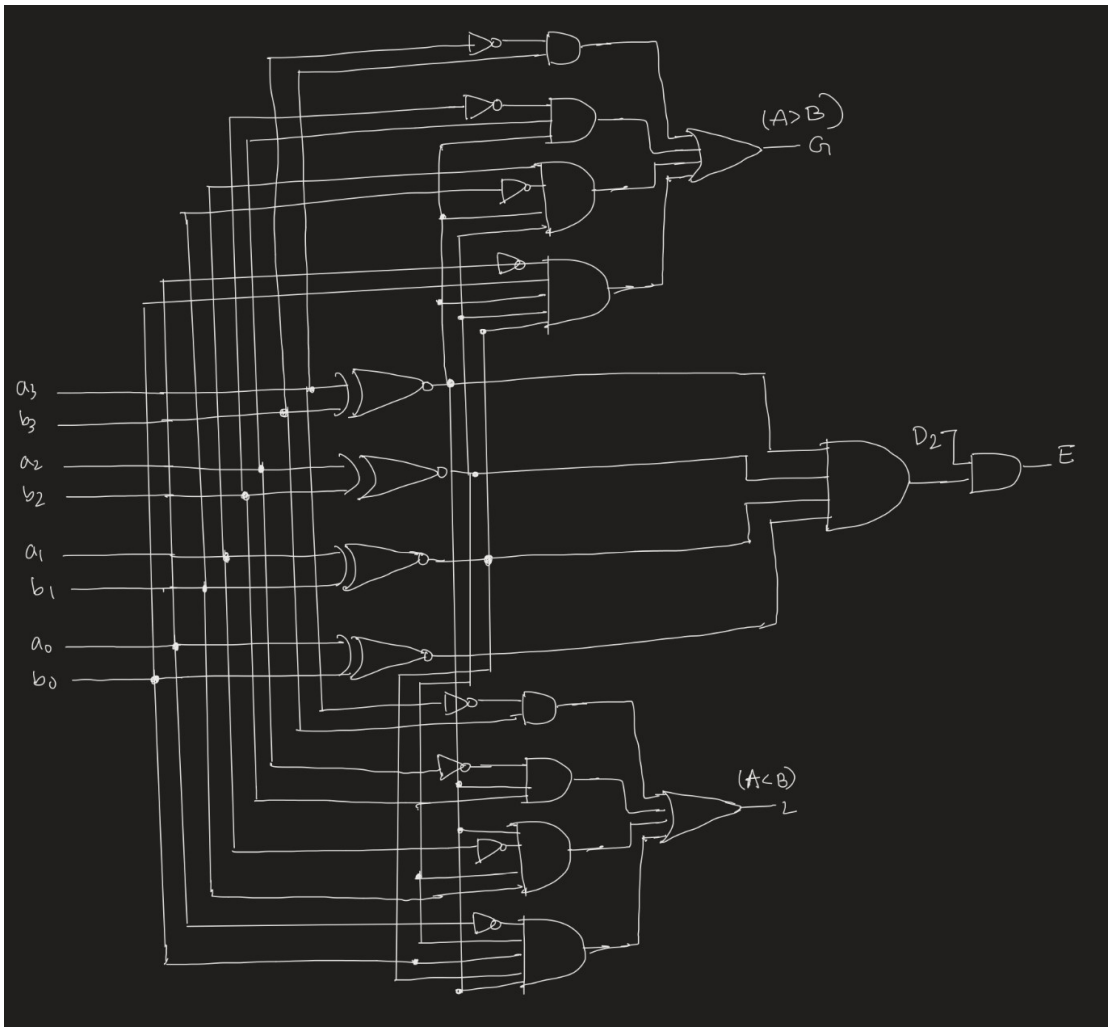
The Input B was first XORed with D1 and a carry of 1 was given to the first full adder to take two's complement and add it to input A.As a result the outputs are in 2's complement.

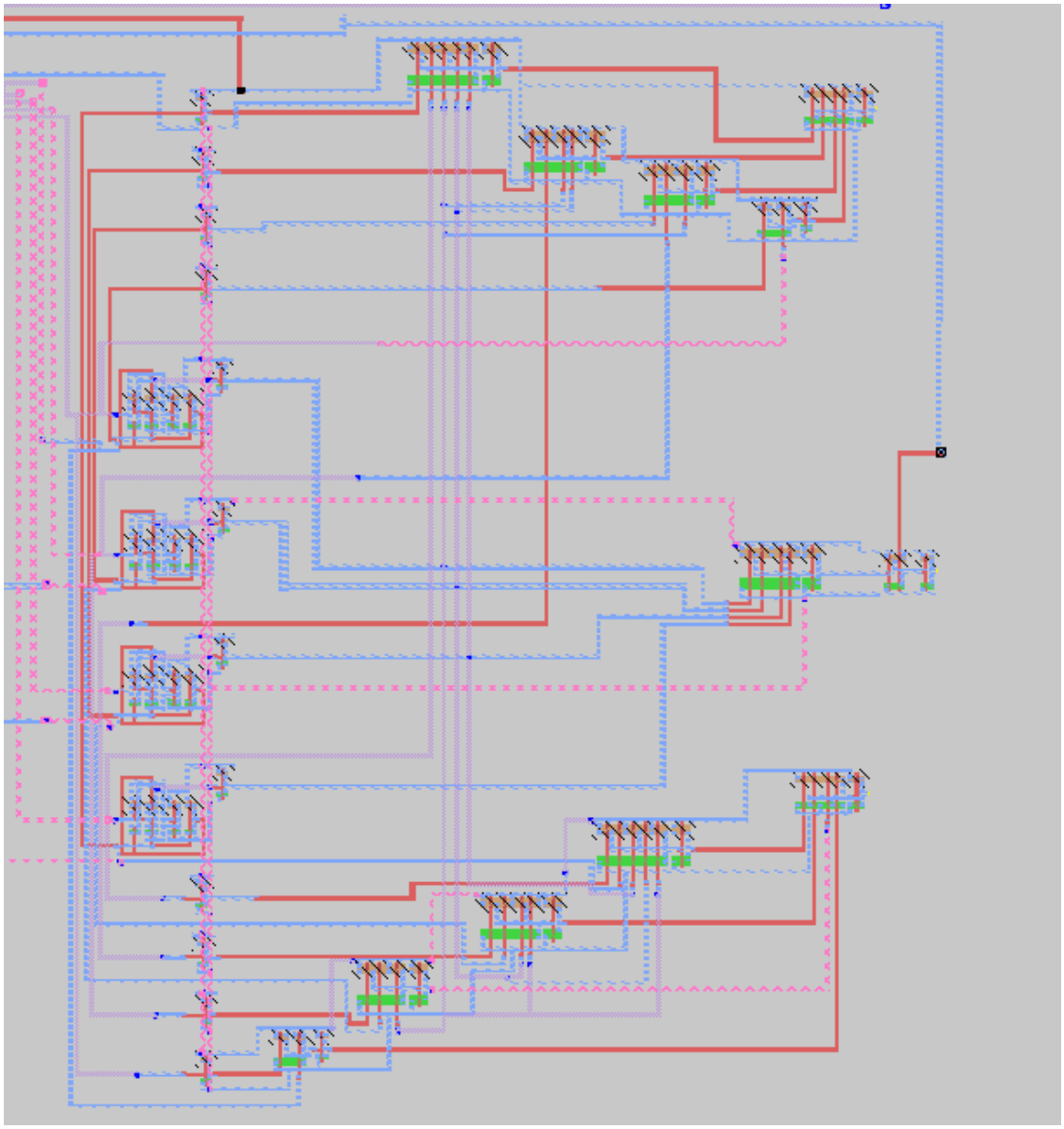
XOR block



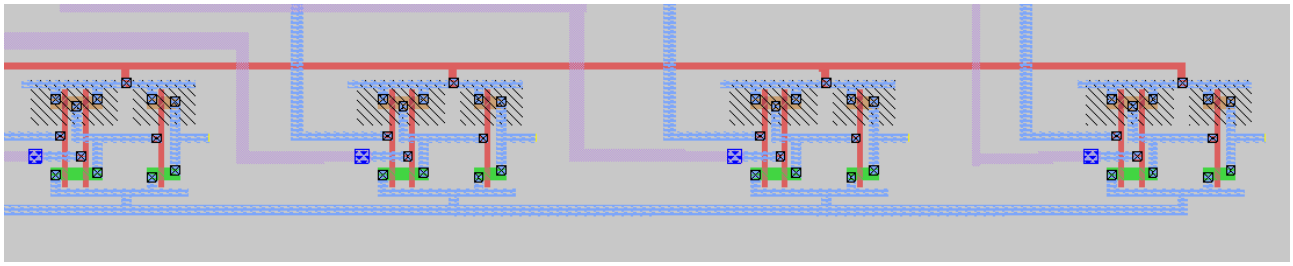
Comparator:

Logic used:

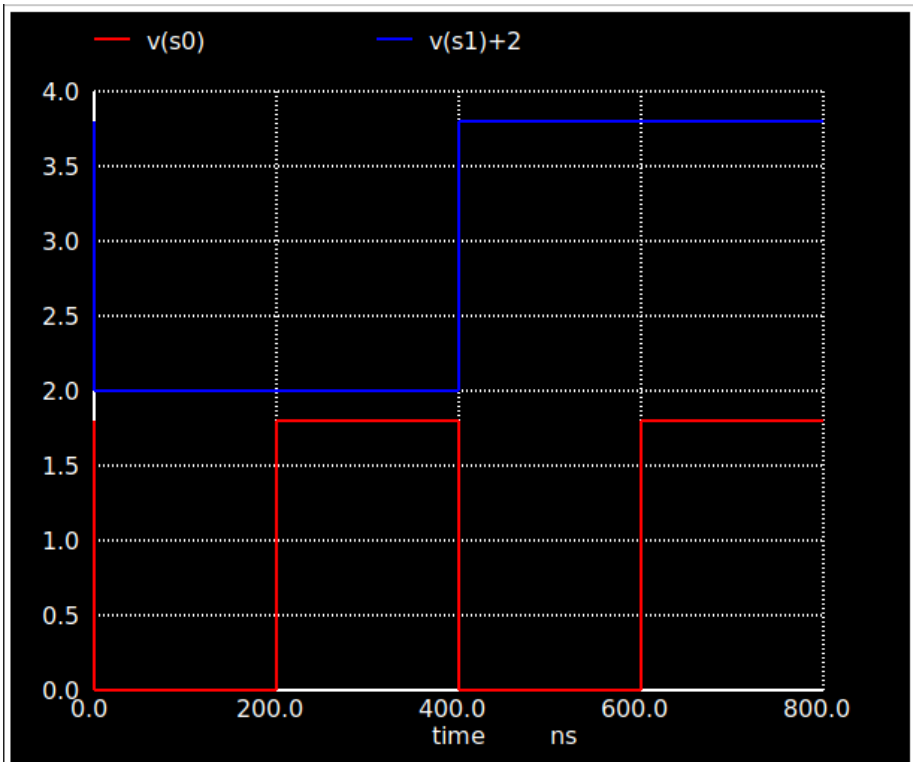




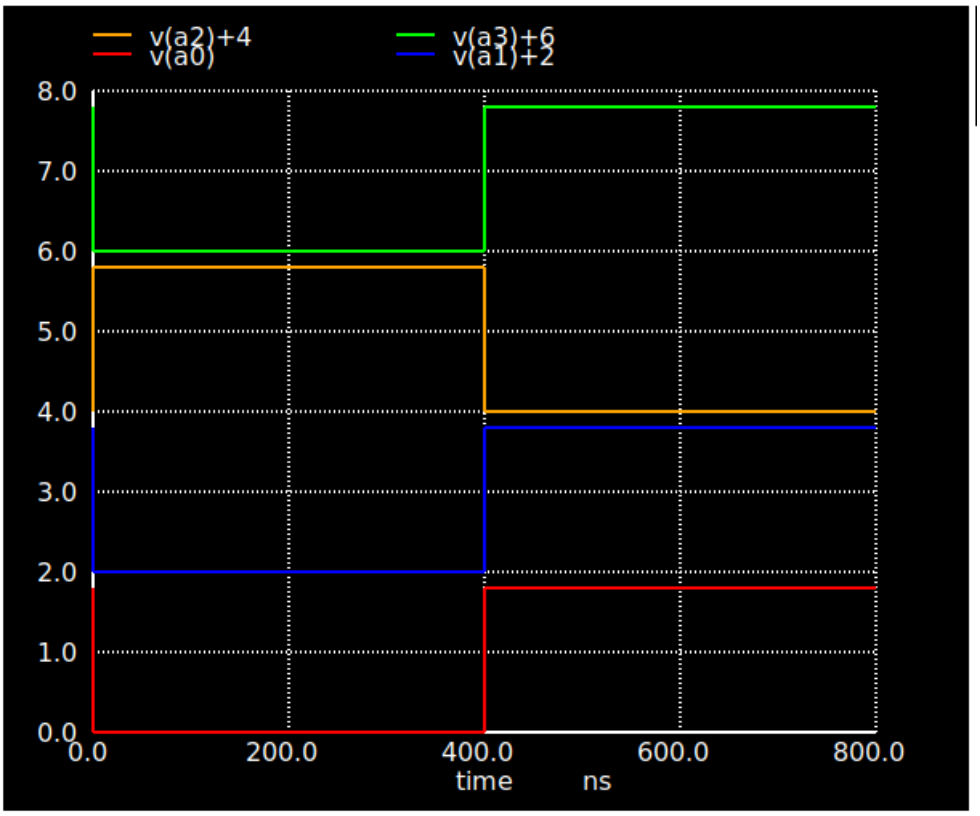
AND block:
Finally D3 ands the inputs A and B



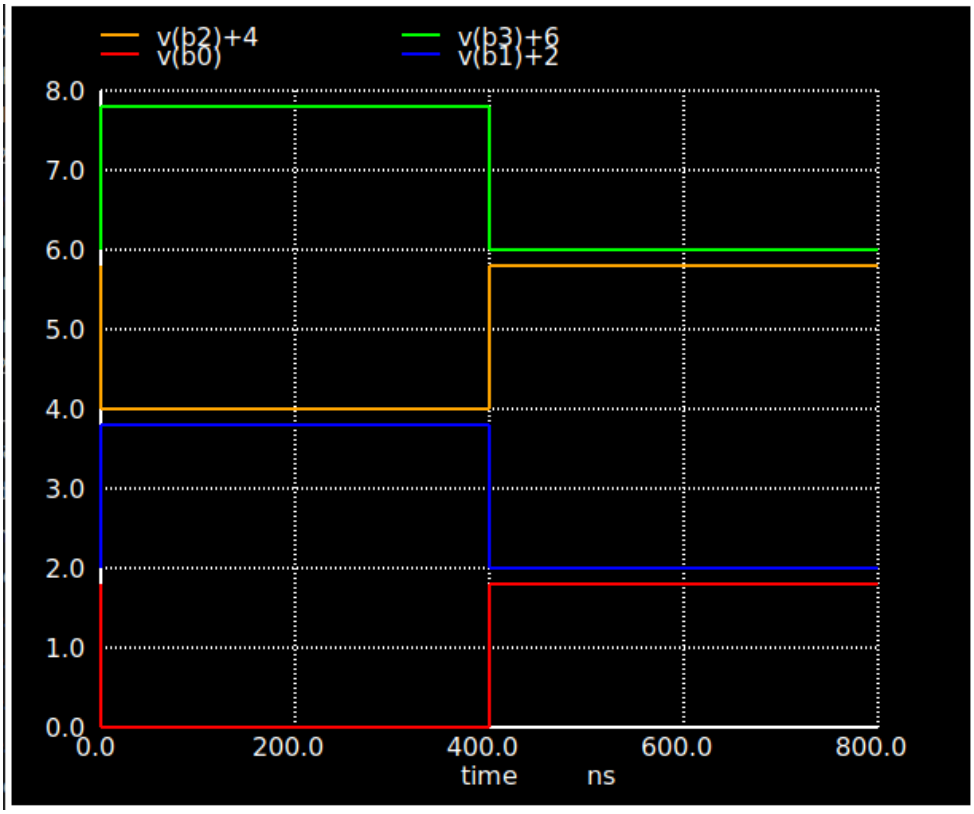
INPUTS:
Selection lines



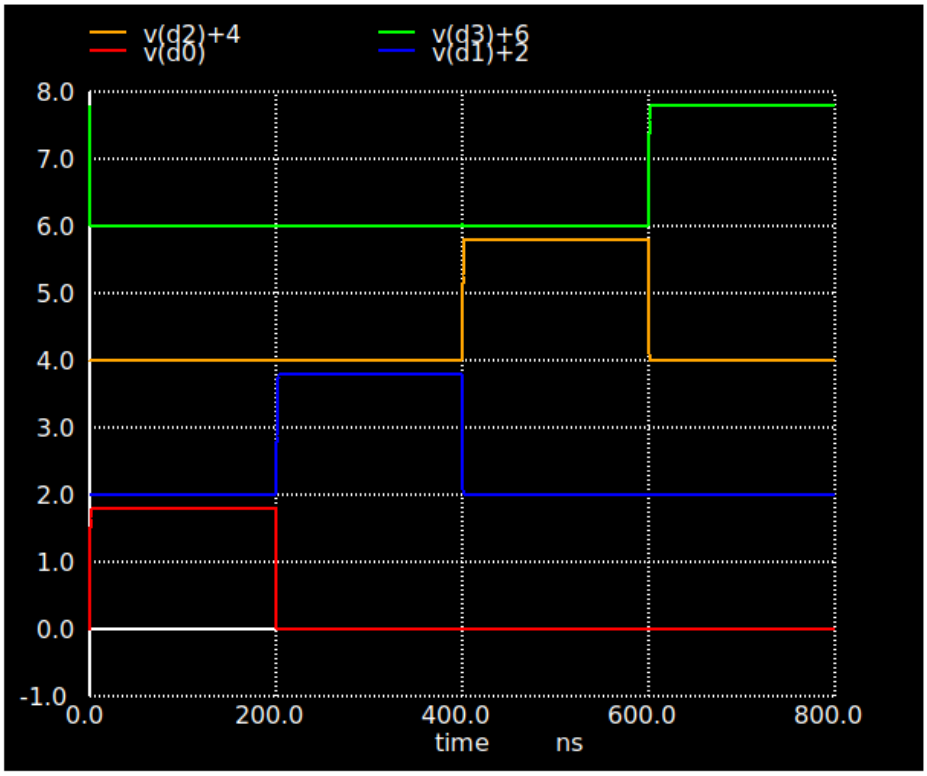
Input A



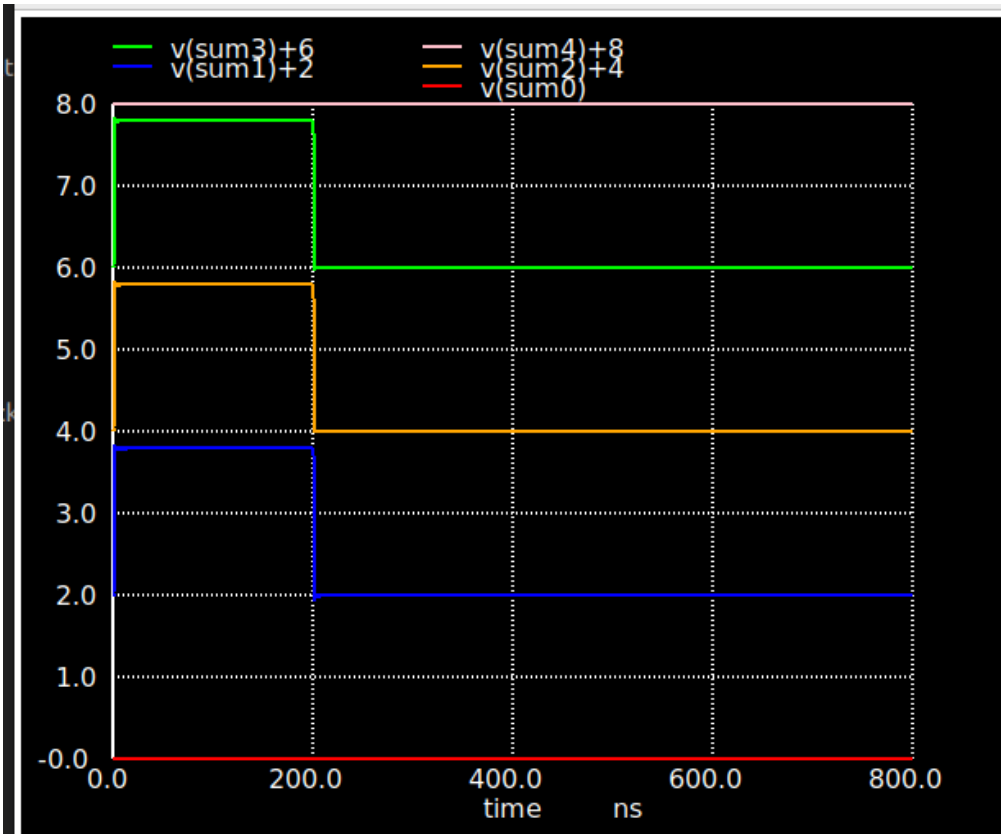
Input B


v(b2)+4
v(b0)
v(b3)+6
v(b1)+2
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
0.0
200.0
400.0
600.0
800.0
time
ns

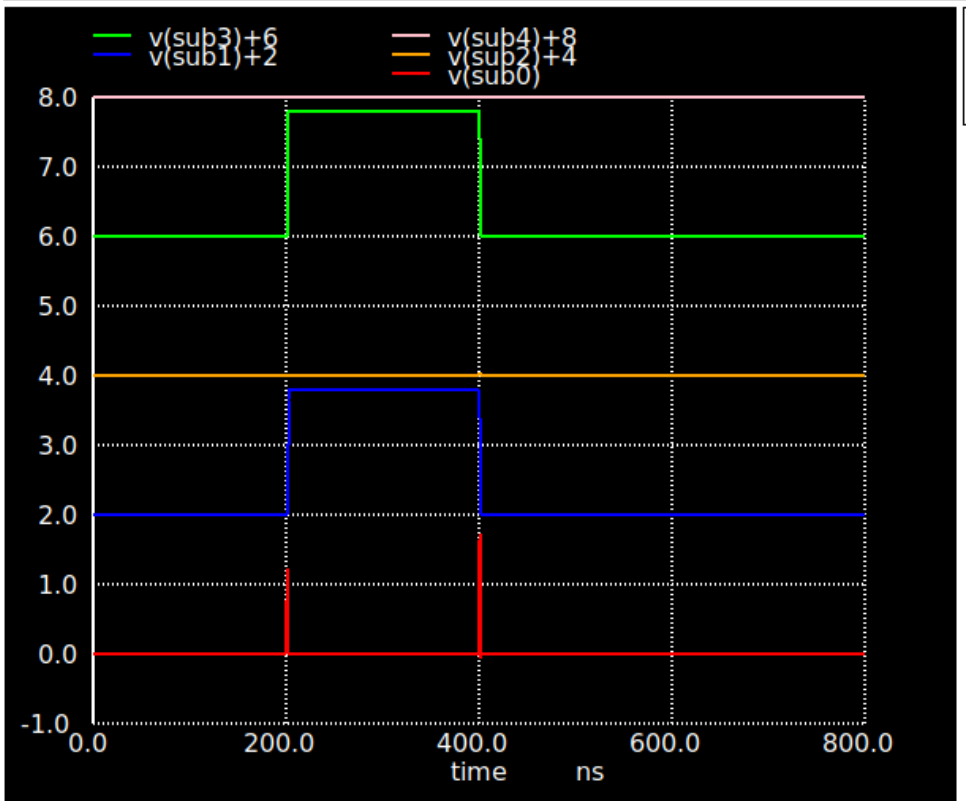
OUTPUTS:
Decoder



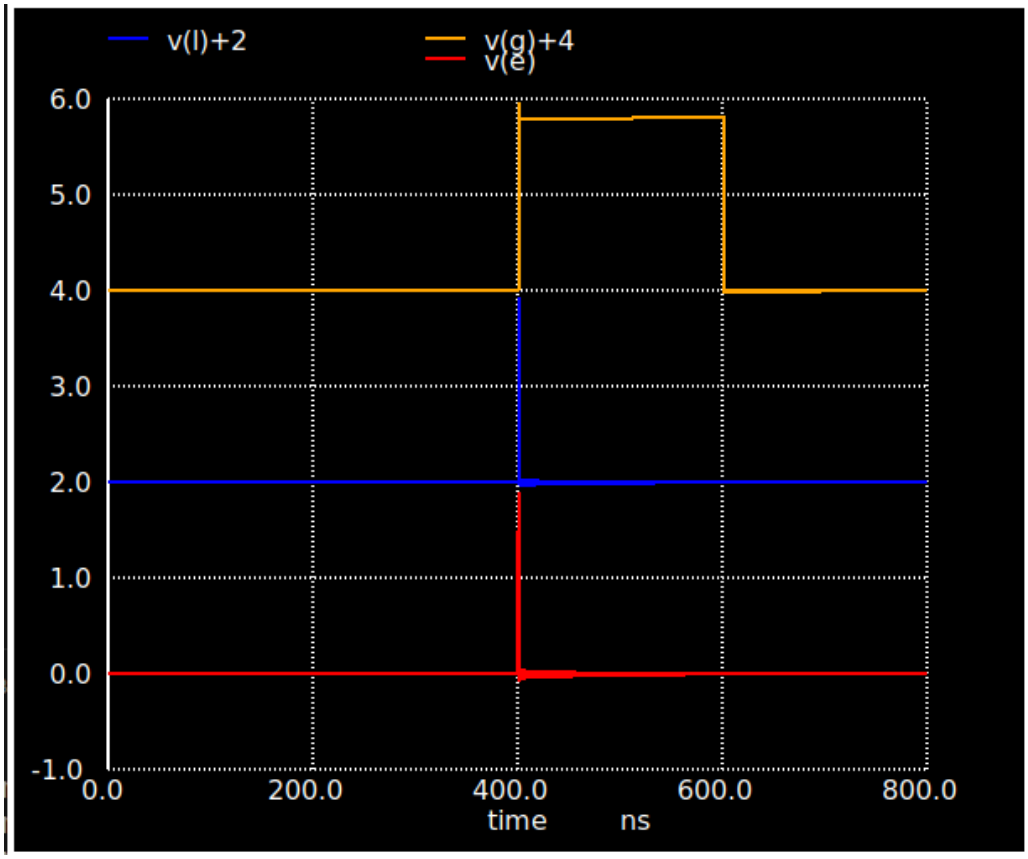
Full adder:



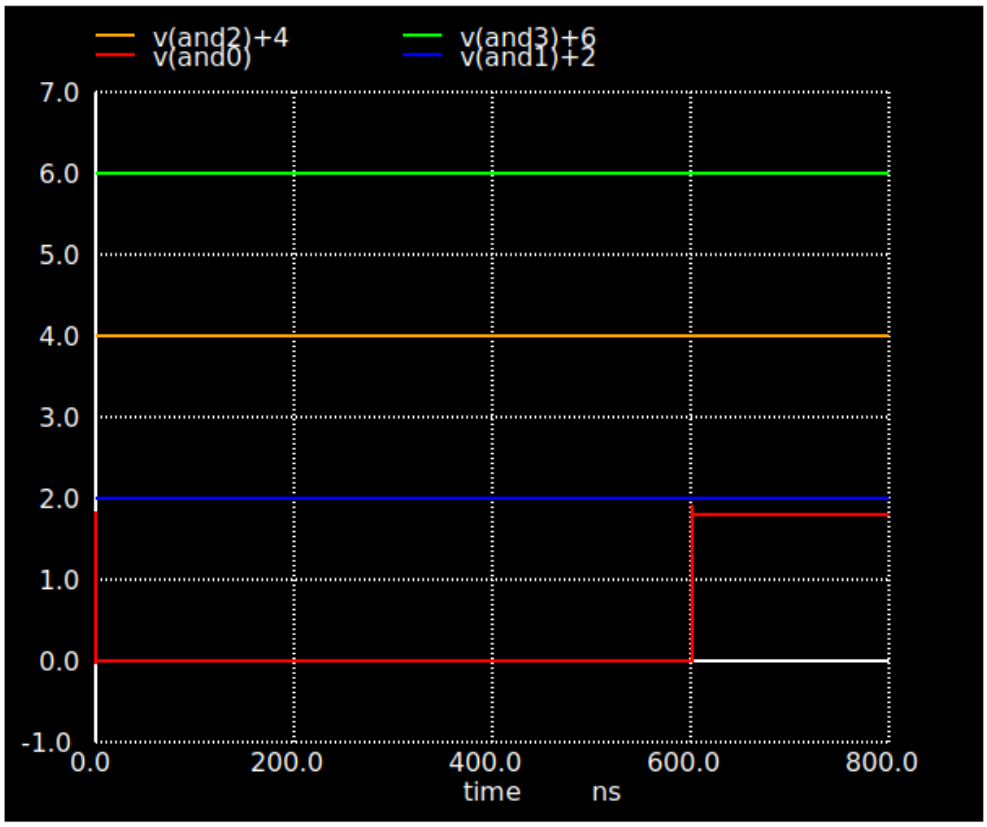
Full Subtractor:


v(sub3)+6
v(sub1)+2
v(sub4)+8
v(sub2)+4
v(sub0)
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
200.0
400.0
600.0
800.0
time
ns

Comparator:


v(l)+2
v(g)+4
v(e)
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
200.0
400.0
600.0
800.0
time
ns

And Block:


v(and2)+4
v(and0)
v(and3)+6
v(and1)+2
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
0.0
200.0
400.0
600.0
800.0
time
ns

DELAY ANALYSIS:
Critical path : Path with maximum delay
Adder

Delay_Analysis > output_add.txt

```
5.50721e-10 input = a0 output = sum0
5.14249e-10 input = a0 output = sum1
4.79123e-10 input = a0 output = sum2
5.32370e-10 input = a0 output = sum3
5.50721e-10 input = a1 output = sum0
5.14249e-10 input = a1 output = sum1
4.79123e-10 input = a1 output = sum2
5.32370e-10 input = a1 output = sum3
5.50721e-10 input = a2 output = sum0
5.14249e-10 input = a2 output = sum1
4.79123e-10 input = a2 output = sum2
5.32370e-10 input = a2 output = sum3
5.50721e-10 input = a3 output = sum0
5.14249e-10 input = a3 output = sum1
4.79123e-10 input = a3 output = sum2
5.32370e-10 input = a3 output = sum3
4.98113e-10 input = b0 output = sum0
4.99388e-10 input = b0 output = sum1
5.13420e-10 input = b0 output = sum2
4.99472e-10 input = b0 output = sum3
4.98113e-10 input = b1 output = sum0
4.99388e-10 input = b1 output = sum1
5.13420e-10 input = b1 output = sum2
4.99472e-10 input = b1 output = sum3
4.98113e-10 input = b2 output = sum0
4.99388e-10 input = b2 output = sum1
5.13420e-10 input = b2 output = sum2
4.99472e-10 input = b2 output = sum3
4.98113e-10 input = b3 output = sum0
4.99388e-10 input = b3 output = sum1
5.13420e-10 input = b3 output = sum2
4.99472e-10 input = b3 output = sum3
```

```
Critical Path:  input = a0 output = sum0
 Maximum Delay: 5.50721e-10
```

Subtracter:

output_sub.txt

```
7.04016e-10 input = a0 output = sub0
6.91497e-10 input = a0 output = sub1
6.65262e-10 input = a0 output = sub2
6.27227e-10 input = a0 output = sub3
7.04016e-10 input = a1 output = sub0
6.91497e-10 input = a1 output = sub1
6.65262e-10 input = a1 output = sub2
6.27227e-10 input = a1 output = sub3
7.04016e-10 input = a2 output = sub0
6.91497e-10 input = a2 output = sub1
6.65262e-10 input = a2 output = sub2
6.27227e-10 input = a2 output = sub3
7.04016e-10 input = a3 output = sub0
6.91497e-10 input = a3 output = sub1
6.65262e-10 input = a3 output = sub2
6.27227e-10 input = a3 output = sub3
9.91639e-10 input = b0 output = sub0
9.13094e-10 input = b0 output = sub1
9.26857e-10 input = b0 output = sub2
8.74684e-10 input = b0 output = sub3
9.91639e-10 input = b1 output = sub0
9.13094e-10 input = b1 output = sub1
9.26857e-10 input = b1 output = sub2
8.74684e-10 input = b1 output = sub3
9.91639e-10 input = b2 output = sub0
9.13094e-10 input = b2 output = sub1
9.26857e-10 input = b2 output = sub2
8.74684e-10 input = b2 output = sub3
9.91639e-10 input = b3 output = sub0
9.13094e-10 input = b3 output = sub1
9.26857e-10 input = b3 output = sub2
8.74684e-10 input = b3 output = sub3
```

```
Critical Path:  input = b0 output = su
Maximum Delay: 9.91639e-10
```

And Block:

Delay_Analysis > output_and.txt

```
6.47381e-10 input = a0 output = and0
6.48628e-10 input = a0 output = and1
6.45373e-10 input = a0 output = and2
6.41169e-10 input = a0 output = and3
6.47381e-10 input = a1 output = and0
6.48628e-10 input = a1 output = and1
6.45373e-10 input = a1 output = and2
6.41169e-10 input = a1 output = and3
6.47381e-10 input = a2 output = and0
6.48628e-10 input = a2 output = and1
6.45373e-10 input = a2 output = and2
6.41169e-10 input = a2 output = and3
6.47381e-10 input = a3 output = and0
6.48628e-10 input = a3 output = and1
6.45373e-10 input = a3 output = and2
6.41169e-10 input = a3 output = and3
2.25989e-10 input = b0 output = and0
2.41673e-10 input = b0 output = and1
2.42316e-10 input = b0 output = and2
2.42261e-10 input = b0 output = and3
2.25989e-10 input = b1 output = and0
2.41673e-10 input = b1 output = and1
2.42316e-10 input = b1 output = and2
2.42261e-10 input = b1 output = and3
2.25989e-10 input = b2 output = and0
2.41673e-10 input = b2 output = and1
2.42316e-10 input = b2 output = and2
2.42261e-10 input = b2 output = and3
2.25989e-10 input = b3 output = and0
2.41673e-10 input = b3 output = and1
2.42316e-10 input = b3 output = and2
2.42261e-10 input = b3 output = and3
```

```
Critical Path:  input = a0 output = and1
 Maximum Delay: 6.48628e-10
```

Comparator:
Less than:

```
tpd                    =  7.89336e-10 input = a0 output = l
tpd                    =  7.89336e-10 input = a1 output = l
tpd                    =  7.89336e-10 input = a2 output = l
tpd                    =  7.89336e-10 input = a3 output = l
tpd                    =  5.62867e-10 input = b0 output = l
tpd                    =  5.62867e-10 input = b1 output = l
tpd                    =  5.62867e-10 input = b2 output = l
tpd                    =  5.62867e-10 input = b3 output = l
```

```
Critical Path:  input = a0 output = l
Maximum Delay: 7.89336e-10
```

Equal to:

```
tpd                    =  3.03934e-09 input = a0 output = e
tpd                    =  3.03934e-09 input = a1 output = e
tpd                    =  3.03934e-09 input = a2 output = e
tpd                    =  3.03934e-09 input = a3 output = e
tpd                    =  9.05929e-10 input = b0 output = e
tpd                    =  9.05929e-10 input = b1 output = e
tpd                    =  9.05929e-10 input = b2 output = e
tpd                    =  9.05929e-10 input = b3 output = e
```

```
Critical Path:  input = a0 output = e
Maximum Delay: 3.03934e-09
```

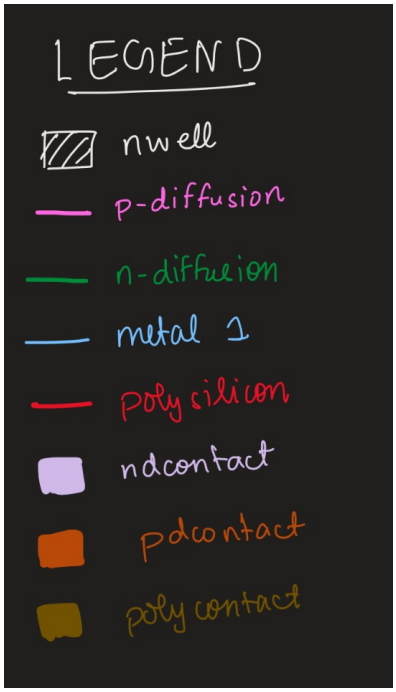
Greater than:

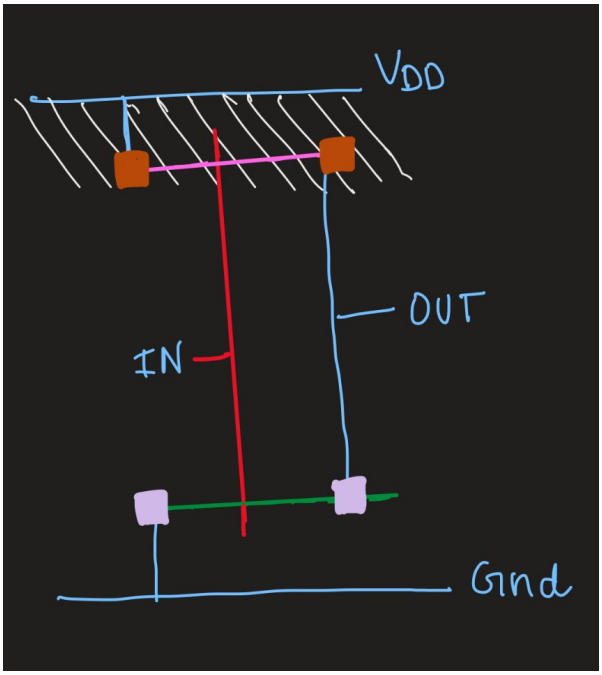
```
tpd                    =  6.63572e-10 input = a0 output = g
tpd                    =  6.63572e-10 input = a1 output = g
tpd                    =  6.63572e-10 input = a2 output = g
tpd                    =  6.63572e-10 input = a3 output = g
tpd                    =  6.84783e-10 input = b0 output = g
tpd                    =  6.84783e-10 input = b1 output = g
tpd                    =  6.84783e-10 input = b2 output = g
tpd                    =  6.84783e-10 input = b3 output = g
```

```
Critical Path:  input = b0 output = g
Maximum Delay: 6.84783e-10
```

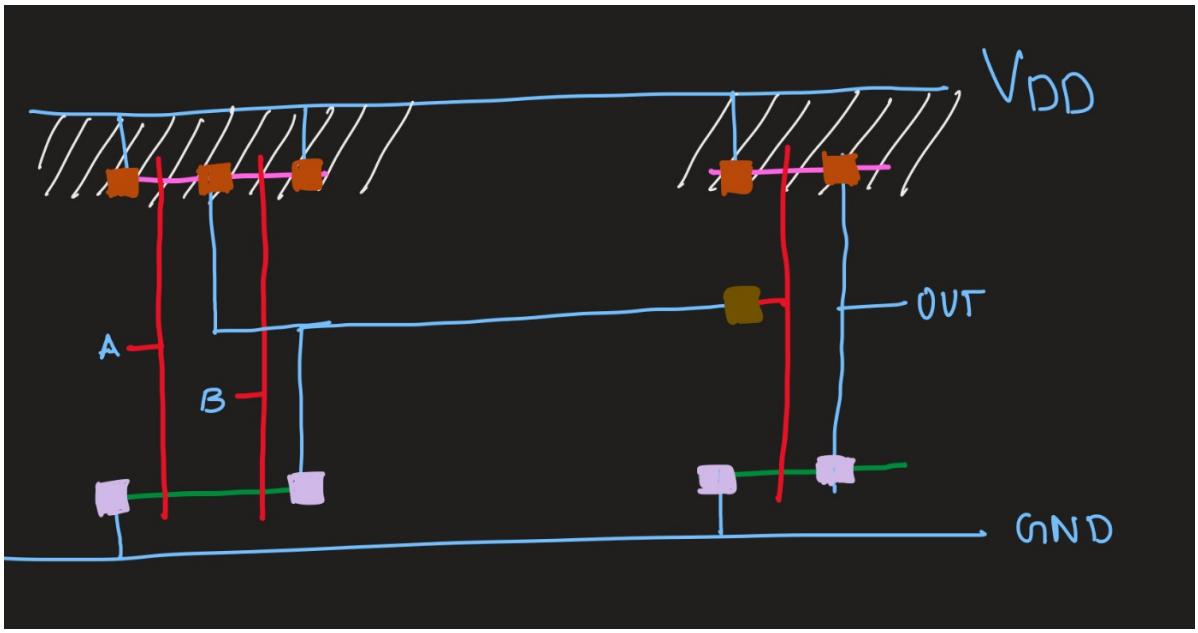
ADDITIONAL: Stick diagrams for NOT, 2 input AND, OR, XOR, XNOR for implementation in MAGIC. All the circuits were a combnation of these gates extrapolated to the required inputs

NOT

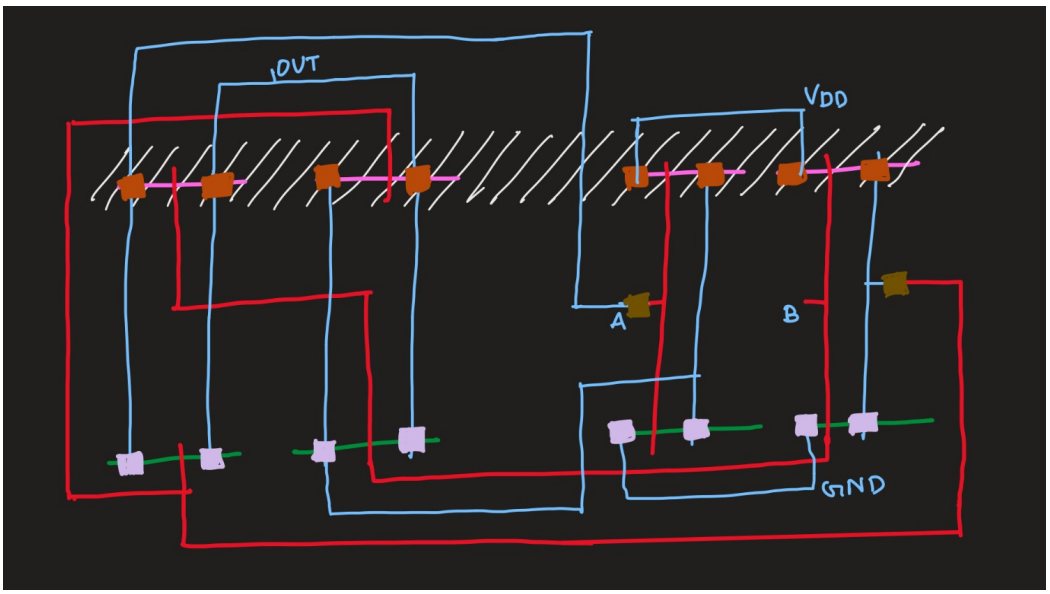




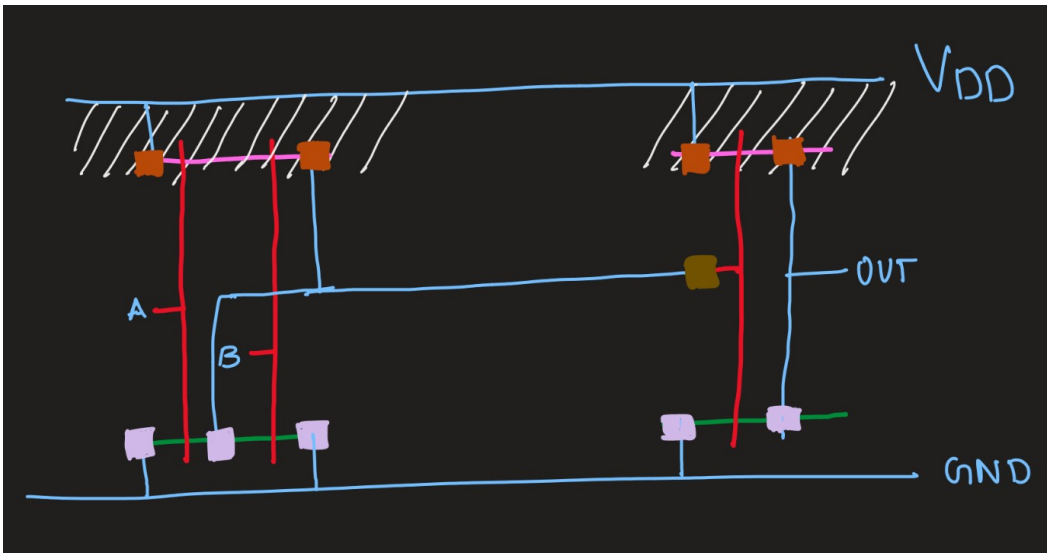
AND



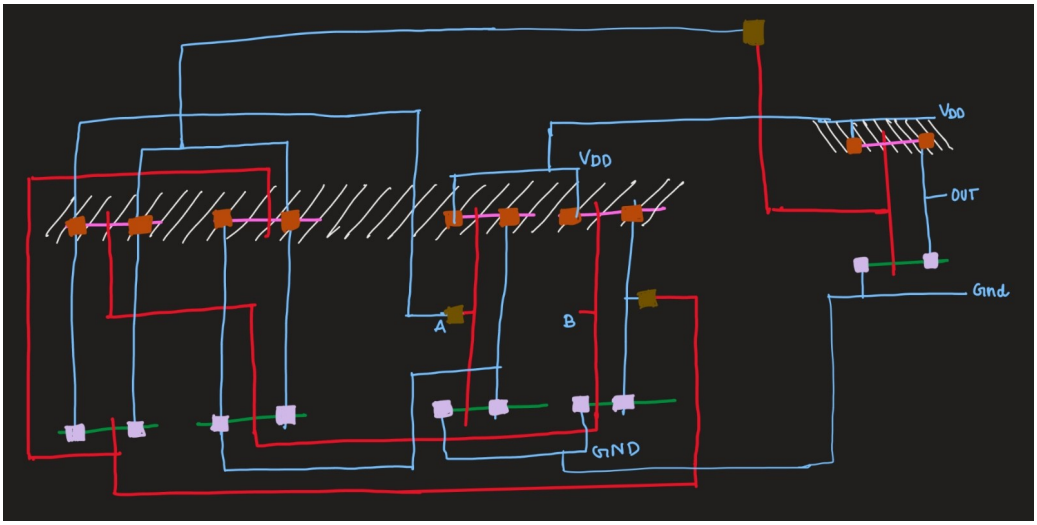
XOR



OR



XNOR



Further Optimization:

I could have combined the adder/subtractor blocks by taking the OR of D0 and D1 and sending that to asingular Enable block which would connect enabled B outputs to XOR with D1. The outputs of the latter and the enabled A outputs then can be sent to the 4 bit full adder. Also, for less than operation we need not remake the complex circuit and instead take XNOR of the greater than and equal to outputs. I could have also used a 3 input and gate for the AND block combining the enable and current and block.