BACHELOR OF COMP. SC. ENGG. EXAMINATION, 2010

(2nd Year, 1st Semester)

COMPUTER ORGANISATION

Time : Three hours Full Marks : 100

Answer any ***five*** questions.

Different parts of a question are to be answered together.

All Questions carry equal marks.

1. a) Design neatly the serial -parallel adder organisation to add 8-signed numbers of 5-bits each. Consider the delay with full adder be 100 n Sec and that for shift register be 70 n Sec. What will be the total time required to complete addition?

   b) How associative memory differs from conventional memory? Explain the organisation of associative memory with a neat diagram.

   Describe the match logic circuit used in associative memory. 10+10

2. a) Design an ALU with three control lines C_O, C_1 and C_2 and one carry input line and two 8-bit binary inputs A and B

to perform the following operations (show the first three stages only)

C_2	C_1	C_o	Operations
O	O	O	A AND B
O	O	1	A OR B
O	1	O	A XOR B
O	1	1	Complement A
1	O	O	A - 1
1	O	1	A + 1
1	1	O	A – B
1	1	1	A + B

b) Write program to evaluate the statement

$$A = \frac{(A + B) * A}{A - B}$$

using i) 3- address instruction

ii) 2-address instruction

iii) 1- address instruction

iv) 0-address instruction

3. a) Consider the following page reference sequence in a virtual memory system.

1, 2, 3, 4 ,1, 5 , 2, 3, 6, 5 ,4 ,1 6, 2, 5, 4

Find the optimal proposal from the followings :

i) Change from FIFO to LRU

ii) Increase the main memory capacity from 4 to 8

i) Calculate the no. of bits in each of the TAG, SET and WORD fields of the main memory address format.

ii) Assume that the cache is initially empty. Suppose that the CPU fetches 4352 words from locations 0,1,2,...4351 in order. It then repeats this fetch sequence nine more times.

If the cache is 10 times faster than the main memory, estimate the improvement factor resulting from the use of the cache (assume that LRU algorithm is used for block replacement).

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mantissa. The scale factor of the base is 4 and the exponents are represented in excess-64 format. Find the value of A + B where

A= 12.35 and B = $5\frac{1}{3}$

i) Represent A and B both in the above format and also the result A + B

ii) Find A - B also in the above format, normalise and rounded.

iii) What is the error introduced due to floating point representation.

b) Consider the following reservation table :

	1	2	3	4	5	6
S_1	*					*
S_2		*			*	
S_3			*			
S_4				*		
S_5		*			*	

i) Find the collision vector.

ii) Draw the state transition diagram.

iii) List all simple cycles and greedy cycles

iv) Determine the optimal constant latency cycle and the minimal average latency. 10+10

7. A computer has 1 Mbyte main memory and 4K bytes of cache organised in the block-set associative manner with 4 pages per set and 64 bytes per page.

iii) Both or any thing else.

b) Write short notes on (any two).

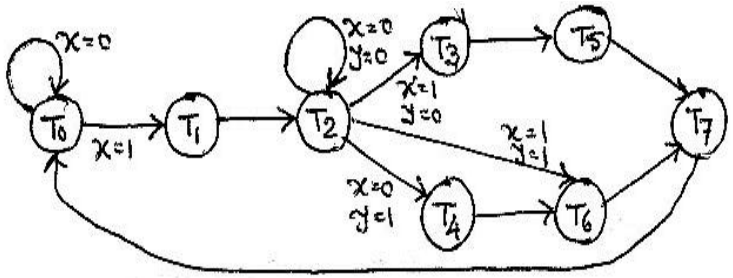
i) Virtual memory

ii) Carry Save addition

iii) Nano programming

iv) Rounding Techniques

4. A control unit has two inputs X, Y and eight states. The control state diagram is as follows.



a) Design the control using eight D flipflops

b) Design the address sequencing part of microprogram.

5. a) Draw the combinational circuit for paper pencil method of multiplication for two signed numbers -25 and + 18 Find also the total deley of multiplication.

b) Describe non-restoring type binary division algorithm and the corresponding sequential circuit for implementing it. Next verify step by step with the example of 19 divided by 5. 10+10

6. a) Consider a 20-bit floating point number in a format with 7-bit exponent and a 12-bit normalised fractional