Ref. No.: **Ex/CSE/T/115A/2018**

Bachelor of Computer Science and Engineering,
1st Year, 1st Semester Examination, 2017
Digital Logic

Full Marks: 100 Time : 3 Hr

Answer Five Questions : Q1 (Compulsory) and any four from the rest.
Write answers to the point and state used laws (wherever required).
Make assumptions wherever necessary.
ALL PARTS OF THE QUESTION SHOULD BE ANSWERED TOGETHER

Q 1) (a) What is the Gray equivalent of $(25)_{10}$. (2)

(b) Convert the decimal number 82.67 to its binary, hexadecimal and octal equivalents. $(3 \times 2 = 6)$

(c) Perform the following subtractions using 2's complement method and give the equivalent decimal value of the result $(3 + 3 = 6)$
(i) 01100 – 00011 (iii) 0011.1001 – 0001.1110

(d) Verify that the following operations are commutative but not associative (i) NAND (ii) NOR $(3 + 3 = 6)$

Q 2) (a) Minimize the following logic function using K-maps and realize using NAND and NOR gates. (10)

$$F(A, B, C, D) = \sum m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$$

(b) Design a 8 to 1 multiplexer by using the four variable function given by (10)

$$F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15)$$

Q 3) (a) How can a JK flip-flop be used as a 1-bit memory storage device? Use this configuration to build a 4-bit parallel data storage device. (5)

(b) Explain the operation of a left/right shift register. Use diagrams to explain the operation. (7)

(c) Design a synchronous circuit for the odd numbered Binary Coded Decimal in the Gray Code sequence (8)

Q 4) (a) For $F = ABC + BC\overline{D} + \overline{A}BC$, write the truth table. Simplify using Karnaugh map and realize the function using NAND gates only. (8)

(b) Design a circuit for adding 3 3-bit binary numbers, the inputs all given at the same time, e.g. addding $1101 + 1110 + 0111$ (12)

Q 5) (a) Prove the following equations using the Boolean algebraic theorems (5)

$$\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC = AB + BC + AC$$

(b) Describe the operation of a full-adder. How is a full adder constructed from two half-adders? In what situation would a half-adder not be sufficient, meaning that a full-adder would be required? $(3 + 3 + 2 = 8)$

(c) Develop and explain a base 7 asynchronous binary counter. (7)

Q 6) (a) Simplify the Boolean function F using the don't-care conditions d in (i) SOP and (ii) POS. Use Quine-McCluskey Algorithm to simplify the function (10)

$$F = A.C.E + \overline{A}.C.\overline{D}.\overline{E} + \overline{A}.\overline{C}.D.E$$

$$d = D.\overline{E} + \overline{A}.\overline{D}.E + A.\overline{D}.\overline{E}$$

(b) Design a 4×16 decoder using 2 3×8 decoders. Explain its functionality. (5)

(c) What is a Johnson Counter ? Explain with relevant diagrams (5)