VLSI
Assignment 5

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1 Describtion

- 2 bit comparator
  - Write a procedure for implementing 2-bit magnitude comparator.
  - Write a test bench for 2-bit magnitude comparator
- 4 bit comparator
  - Write a procedure for implementing 4-bit magnitude comparator using 2-bit magnitude comparator.
  - Write a test bench for 4-bit magnitude comparator
- 8 bit comparator
  - Write a procedure for implementing 8-bit magnitude comparator using 4-bit magnitude comparator.
  - Write a test bench for 8-bit magnitude comparator.
  - Write a procedure for implementing 8-bit magnitude comparator using 2-bit magnitude comparator.
  - Implement 8-bit magnitude comparator by structural modelling.

2 Block Diagram

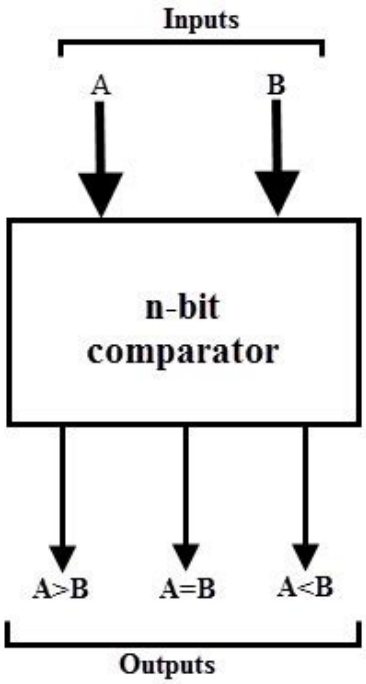


Figure 1: Decoder block diagram

3 Truth Table

A(1 - 0)	B(1 - 0)	C(2 - 0)
00	00	010
00	01	001
00	10	001
00	11	001
01	00	100
01	01	010
01	10	001
01	11	001
10	00	100
10	01	100
10	10	010
10	11	001
11	00	100
11	01	100
11	10	100
11	11	010

4 Circuit Diagram

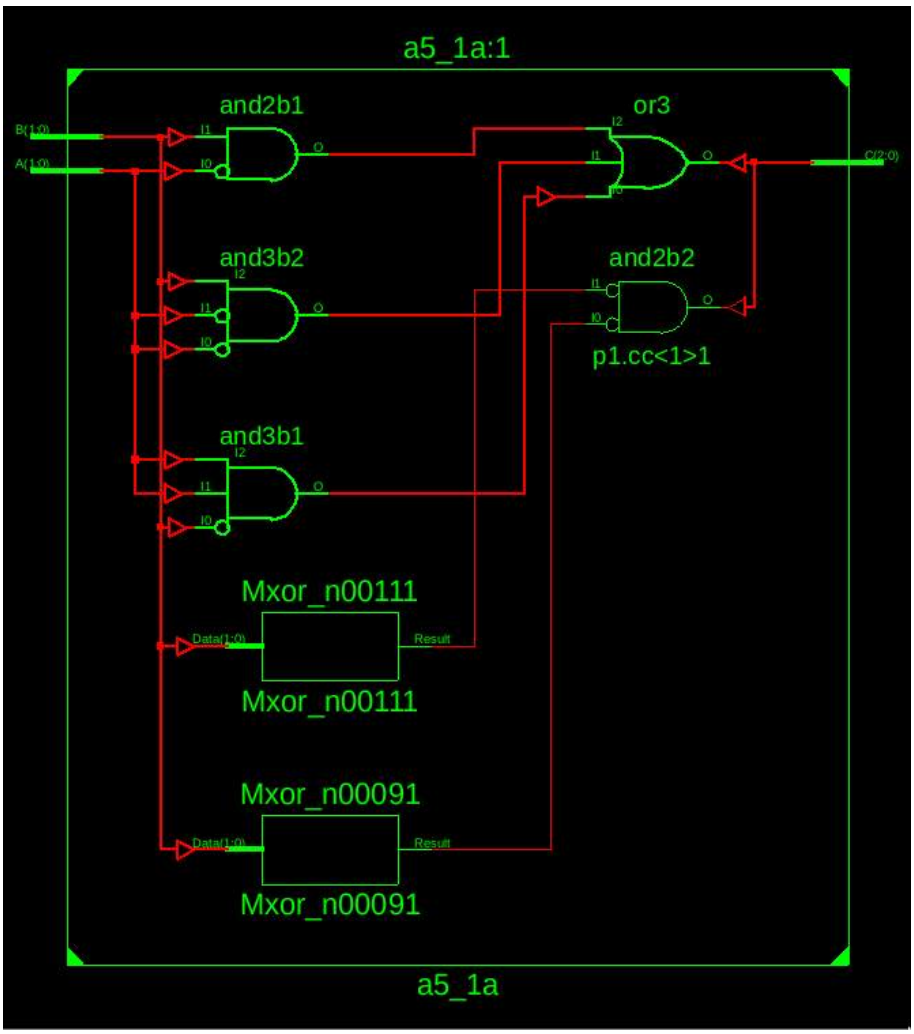


Figure 2: 2 bit comparator circuit diagram

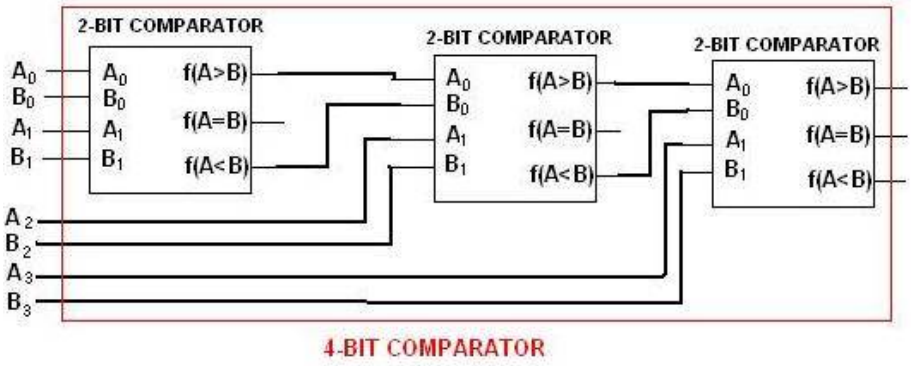


Figure 3: 4 bit comparator using 2 bit comparators

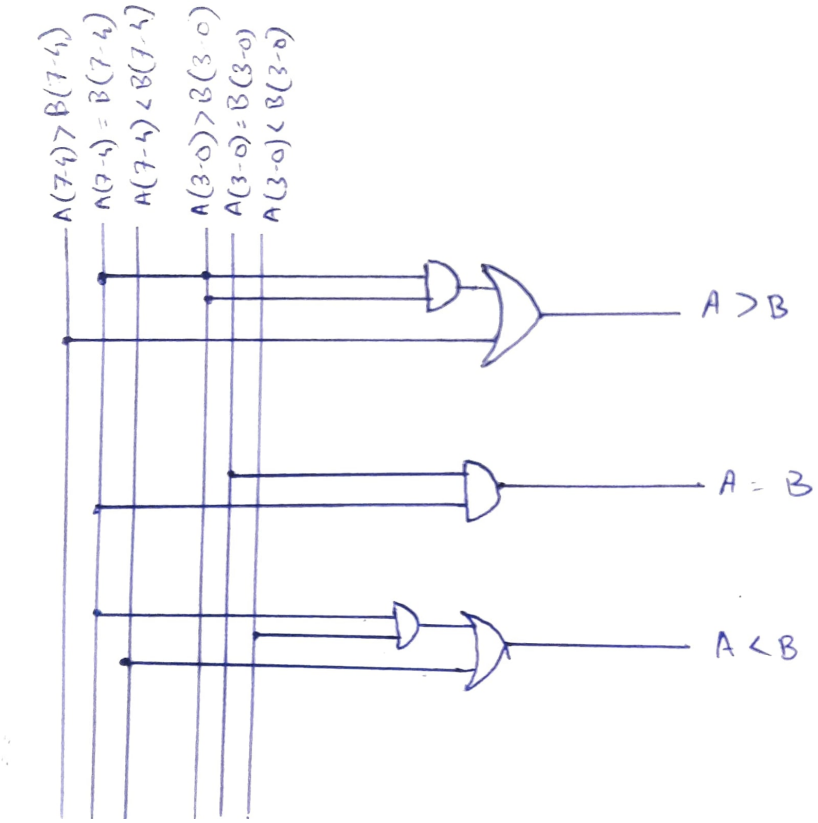


Figure 4: 8 bit comparator using 4 bit comparators

5 Code for package

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

package comparator_package is

        procedure comparator_2bit(
        A: in std_logic_vector(1 downto 0);
        B: in std_logic_vector(1 downto 0);
        C: out std_logic_vector(2 downto 0));
        procedure comparator_4bit(
        A: in std_logic_vector(3 downto 0);
        B: in std_logic_vector(3 downto 0);
        C: out std_logic_vector(2 downto 0));
```

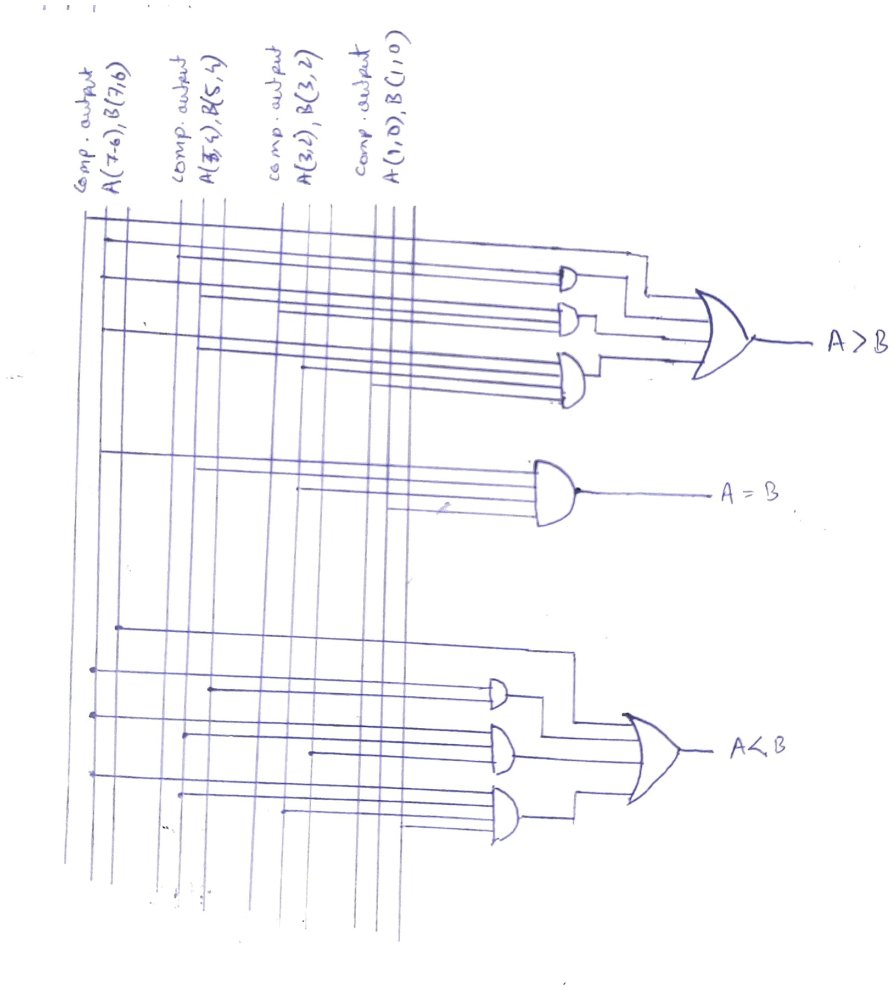


Figure 5: 8 bit comparator using 2 bit comparators

```
        procedure comparator_8bit(
        A: in std_logic_vector(7 downto 0);
        B: in std_logic_vector(7 downto 0);
        C: out std_logic_vector(2 downto 0));
        procedure comparator_8bit2(
        A: in std_logic_vector(7 downto 0);
        B: in std_logic_vector(7 downto 0);
        C: out std_logic_vector(2 downto 0));
        procedure dec_to_bin_proc(
        decimal: in integer;
        num_of_bits: in integer; binary:
        out std_logic_vector);

end comparator_package;

package body comparator_package is

        procedure dec_to_bin_proc(
        decimal: in integer;
        num_of_bits: in integer;
        binary: out std_logic_vector) is
   variable dec, bit_pos: integer;
   begin
                dec := decimal;
                bit_pos := 0;
```

```
            while(bit_pos < num_of_bits) loop
                    if (dec rem 2) = 0 then
                            binary(bit_pos) := '0';
                    else
                            binary(bit_pos) := '1';
                    end if;
                    dec := dec/2;
                    bit_pos := bit_pos + 1;
            end loop;
end procedure;

    procedure comparator_2bit(
    A: in std_logic_vector(1 downto 0);
    B: in std_logic_vector(1 downto 0);
    C: out std_logic_vector(2 downto 0)) is
    begin
            C(0) := (not A(1) and not A(0) and B(0))
            or (not A(1) and B(1))
            or (not A(0) and B(1) and B(0));
            C(1) := (A(1) xnor B(1)) and (A(0) xnor B(0));
            C(2) := (not B(1) and not B(0) and A(0))
            or (not B(1) and A(1))
            or (not B(0) and A(1) and A(0));
    end procedure;

    procedure comparator_4bit(
    A: in std_logic_vector(3 downto 0);
    B: in std_logic_vector(3 downto 0);
    C: out std_logic_vector(2 downto 0)) is
            variable cc2,cc1 : std_logic_vector(2 downto 0);
    begin
    comparator_2bit(A(3 downto 2),B(3 downto 2),cc2);
            comparator_2bit(cc2(2) & A(1),cc2(0) & B(1),cc1);
            comparator_2bit(cc1(2) & A(0), cc1(0) & B(0), C);
    end procedure;

    procedure comparator_8bit(
    A: in std_logic_vector(7 downto 0);
    B: in std_logic_vector(7 downto 0);
    C: out std_logic_vector(2 downto 0)) is
            variable cc2,cc1 : std_logic_vector(2 downto 0);
    begin
            comparator_4bit(A(7 downto 4),B(7 downto 4),cc2);
            comparator_4bit(A(3 downto 0),B(3 downto 0),cc1);

            if cc2 = "010" then
                    C := cc1;
            else
                    C := cc2;
            end if;
    end procedure;

    procedure comparator_8bit2(
    A: in std_logic_vector(7 downto 0);
    B: in std_logic_vector(7 downto 0);
    C: out std_logic_vector(2 downto 0)) is
            variable cc4,cc3,cc2,cc1 : std_logic_vector(2 downto 0);
    begin
            comparator_2bit(A(7 downto 6),B(7 downto 6),cc4);
            comparator_2bit(A(5 downto 4),B(5 downto 4),cc3);
```

```
                comparator_2bit(A(3 downto 2),B(3 downto 2),cc2);
                comparator_2bit(A(1 downto 0),B(1 downto 0),cc1);

                if cc4 /= "010" then
                        C := cc4;
                elsif cc3 /= "010" then
                        C := cc3;
                elsif cc2 /= "010" then
                        C := cc2;
                elsif cc1 /= "010" then
                        C := cc1;
                else
                        C := "010";
                end if;

        end procedure;

end comparator_package;
```

6 Code for 2 bit comparator

6.1 Module

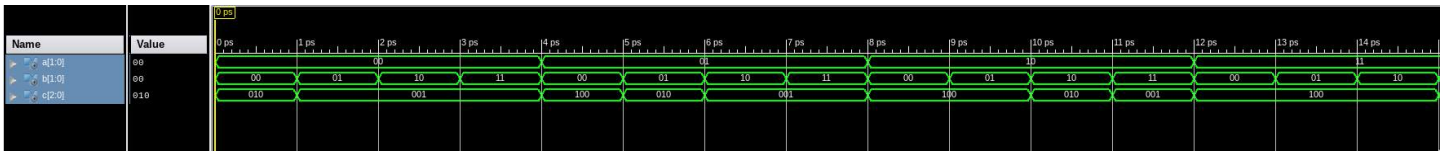
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use work.comparator_package.ALL;

entity a5_1a is
    Port ( A : in  STD_LOGIC_VECTOR (1 downto 0);
           B : in  STD_LOGIC_VECTOR (1 downto 0);
           C : out  STD_LOGIC_VECTOR (2 downto 0));
end a5_1a;

architecture Behavioral of a5_1a is

begin
        p1: process(A,B)
        variable cc : std_logic_vector(2 downto 0);
        begin
        comparator_2bit(A,B,cc);
        C <= cc;
        end process;

end Behavioral;
```

6.2 TestBench

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use work.comparator_package.ALL;

ENTITY tb_a5_1a IS
END tb_a5_1a;

ARCHITECTURE behavior OF tb_a5_1a IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT a5_1a
    PORT(
```

```
         A : IN  std_logic_vector(1 downto 0);
         B : IN  std_logic_vector(1 downto 0);
         C : OUT  std_logic_vector(2 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal A : std_logic_vector(1 downto 0) := (others => '0');
   signal B : std_logic_vector(1 downto 0) := (others => '0');

         --Outputs
   signal C : std_logic_vector(2 downto 0);
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name


BEGIN

         -- Instantiate the Unit Under Test (UUT)
   uut: a5_1a PORT MAP (
          A => A,
          B => B,
          C => C
        );


   -- Stimulus process
   stim_proc: process
        variable aa,bb : std_Logic_vector(1 downto 0);
   begin
                l1: for i in 0 to 3 loop
                        l2: for j in 0 to 3 loop
                                dec_to_bin_proc(i,2,aa);
                                A <= aa;
                                dec_to_bin_proc(j,2,bb);
                                B <= bb;
                                wait for 1 ps;
                        end loop;
                end loop;
   end process;

END;
```

6.3 Timing diagram



7 Code for 4 bit comparator using 2 bit comparator

7.1 Module

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use work.comparator_package.ALL;
```

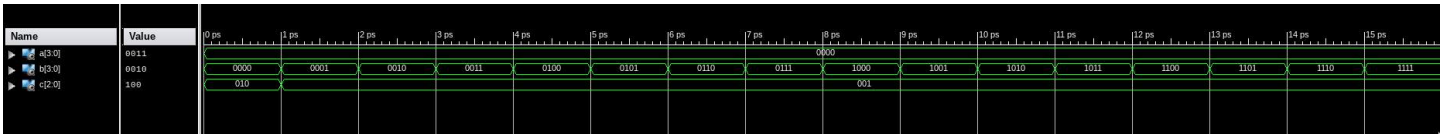
```
entity a5_1b is
    Port ( A : in  STD_LOGIC_VECTOR (3 downto 0);
           B : in  STD_LOGIC_VECTOR (3 downto 0);
           C : out  STD_LOGIC_VECTOR (2 downto 0));
end a5_1b;

architecture Behavioral of a5_1b is

begin
        p1: process(A,B)
        variable cc : std_logic_vector(2 downto 0);
        begin
        comparator_4bit(A,B,cc);
        C <= cc;
        end process;

end Behavioral;
```

7.2 TestBench

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use work.comparator_package.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY tb_a5_1b IS
END tb_a5_1b;

ARCHITECTURE behavior OF tb_a5_1b IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT a5_1b
    PORT(
         A : IN  std_logic_vector(3 downto 0);
         B : IN  std_logic_vector(3 downto 0);
         C : OUT  std_logic_vector(2 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal A : std_logic_vector(3 downto 0) := (others => '0');
   signal B : std_logic_vector(3 downto 0) := (others => '0');

         --Outputs
   signal C : std_logic_vector(2 downto 0);
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name


BEGIN

        -- Instantiate the Unit Under Test (UUT)
   uut: a5_1b PORT MAP (
          A => A,
          B => B,
```

```
          C => C
        );

   -- Stimulus process
   stim_proc: process
        variable aa,bb : std_Logic_vector(3 downto 0);
   begin
                l1: for i in 0 to 15 loop
                        l2: for j in 0 to 15 loop
                                dec_to_bin_proc(i,4,aa);
                                A <= aa;
                                dec_to_bin_proc(j,4,bb);
                                B <= bb;
                                wait for 1 ps;
                        end loop;
                end loop;
   end process;

END;
```

7.3 Timing diagram



8 Code for 8 bit comparator

8.1 Using 4 bit comparators

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use work.comparator_package.ALL;

entity a5_3 is
    Port ( A : in  STD_LOGIC_VECTOR (7 downto 0);
           B : in  STD_LOGIC_VECTOR (7 downto 0);
           C : out  STD_LOGIC_VECTOR (2 downto 0));
end a5_3;

architecture Behavioral of a5_3 is

begin

        p1: process(A,B)
        variable cc : std_logic_vector(2 downto 0);
        begin
        comparator_8bit(A,B,cc);
        C <= cc;
        end process;


end Behavioral;
```

8.2 TestBench for 8 bit using 4 bit comparators

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use work.comparator_package.ALL;
```

```
ENTITY tb_a5_3 IS
END tb_a5_3;

ARCHITECTURE behavior OF tb_a5_3 IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT a5_3
    PORT(
         A : IN  std_logic_vector(7 downto 0);
         B : IN  std_logic_vector(7 downto 0);
         C : OUT  std_logic_vector(2 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal A : std_logic_vector(7 downto 0) := (others => '0');
   signal B : std_logic_vector(7 downto 0) := (others => '0');

         --Outputs
   signal C : std_logic_vector(2 downto 0);
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name


BEGIN

        -- Instantiate the Unit Under Test (UUT)
   uut: a5_3 PORT MAP (
          A => A,
          B => B,
          C => C
        );


   -- Stimulus process
   stim_proc: process
        variable aa,bb: std_logic_vector(7 downto 0);
   begin
                l1: for i in 0 to 255 loop
                        l2: for j in 0 to 255 loop
                                dec_to_bin_proc(i,8,aa);
                                A <= aa;
                                dec_to_bin_proc(j,8,bb);
                                B <= bb;
                                wait for 1 ps;
                        end loop;
                end loop;
   end process;

END;
```

8.3 Using 2 bit comparators

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use work.comparator_package.ALL;
```

```
entity a4_4a is
    Port ( A : in  STD_LOGIC_VECTOR (7 downto 0);
           B : in  STD_LOGIC_VECTOR (7 downto 0);
           C : out  STD_LOGIC_VECTOR (2 downto 0));
end a4_4a;

architecture Behavioral of a4_4a is

begin

        p1: process(A,B)
        variable cc : std_logic_vector(2 downto 0);
        begin
        comparator_8bit2(A,B,cc);
        C <= cc;
        end process;


end Behavioral;
```

8.4 TestBench for 8 bit using 2 bit comparators

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use work.comparator_package.ALL;

ENTITY tb_a4_4a IS
END tb_a4_4a;

ARCHITECTURE behavior OF tb_a4_4a IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT a4_4a
    PORT(
         A : IN  std_logic_vector(7 downto 0);
         B : IN  std_logic_vector(7 downto 0);
         C : OUT  std_logic_vector(2 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal A : std_logic_vector(7 downto 0) := (others => '0');
   signal B : std_logic_vector(7 downto 0) := (others => '0');

         --Outputs
   signal C : std_logic_vector(2 downto 0);
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name


BEGIN

        -- Instantiate the Unit Under Test (UUT)
   uut: a4_4a PORT MAP (
          A => A,
          B => B,
          C => C
        );
```

```
   -- Stimulus process
   stim_proc: process
        variable aa,bb: std_logic_vector(7 downto 0);
   begin
                l1: for i in 0 to 255 loop
                        l2: for j in 0 to 255 loop
                                dec_to_bin_proc(i,8,aa);
                                A <= aa;
                                dec_to_bin_proc(j,8,bb);
                                B <= bb;
                                wait for 1 ps;
                        end loop;
                end loop;
   end process;

END;
```

8.5 Using Structural modelling

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity a5_4b is
    Port ( A : in  STD_LOGIC_VECTOR (7 downto 0);
           B : in  STD_LOGIC_VECTOR (7 downto 0);
           C : out  STD_LOGIC_VECTOR (2 downto 0));
end a5_4b;

architecture Behavioral of a5_4b is

component a5_1b is
    Port ( A : in  STD_LOGIC_VECTOR (3 downto 0);
           B : in  STD_LOGIC_VECTOR (3 downto 0);
           C : out  STD_LOGIC_VECTOR (2 downto 0));
end component;

signal c1,c2 : std_logic_vector(2 downto 0);

begin
        cp1: a5_1b port map(A(7 downto 4), B(7 downto 4), c2);
        cp2: a5_1b port map(A(3 downto 0), B(3 downto 0), c1);
        with c2 select C <= c1 when "010", c2 when others;

end Behavioral;
```

8.6 TestBench for 8 bit using structural modelling

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
use work.comparator_package.ALL;

ENTITY tb_a5_4b IS
END tb_a5_4b;

ARCHITECTURE behavior OF tb_a5_4b IS

    -- Component Declaration for the Unit Under Test (UUT)
```

```
    COMPONENT a5_4b
    PORT(
         A : IN  std_logic_vector(7 downto 0);
         B : IN  std_logic_vector(7 downto 0);
         C : OUT  std_logic_vector(2 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal A : std_logic_vector(7 downto 0) := (others => '0');
   signal B : std_logic_vector(7 downto 0) := (others => '0');

         --Outputs
   signal C : std_logic_vector(2 downto 0);
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name


BEGIN

         -- Instantiate the Unit Under Test (UUT)
   uut: a5_4b PORT MAP (
          A => A,
          B => B,
          C => C
        );


   -- Stimulus process
   stim_proc: process
        variable aa,bb: std_logic_vector(7 downto 0);
   begin
                l1: for i in 0 to 255 loop
                        l2: for j in 0 to 255 loop
                                dec_to_bin_proc(i,8,aa);
                                A <= aa;
                                dec_to_bin_proc(j,8,bb);
                                B <= bb;
                                wait for 1 ps;
                        end loop;
                end loop;
   end process;

END;
```

8.7 Timing diagram