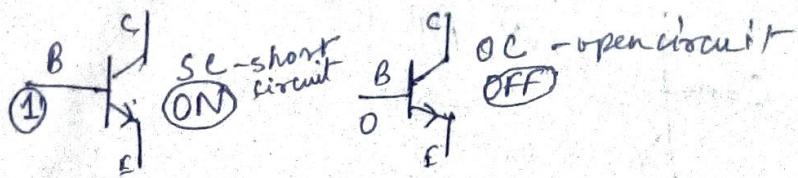


Digital Circuits.

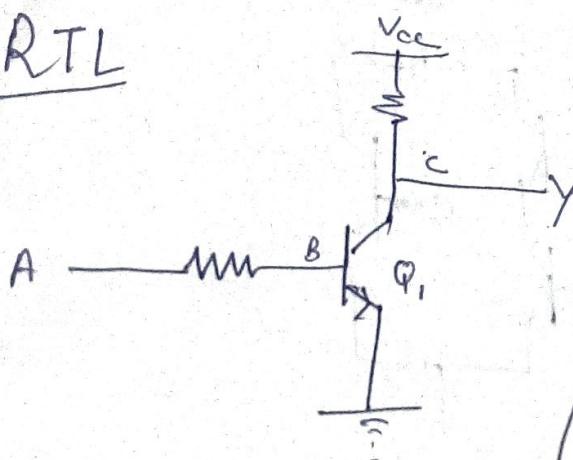
Anant Kumar
Digital Integrated Electronics
Siddhanta Jain & Sekhaling

For transistors:



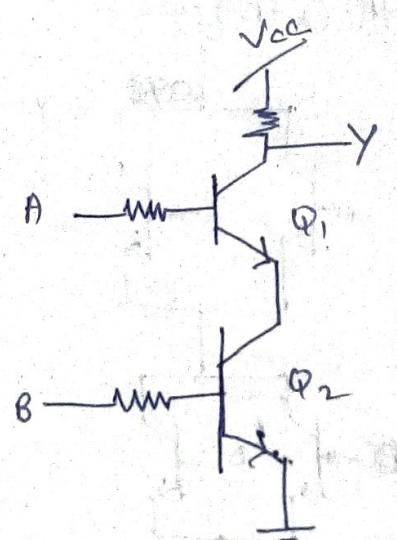
Logic families \rightarrow RTL,

RTL



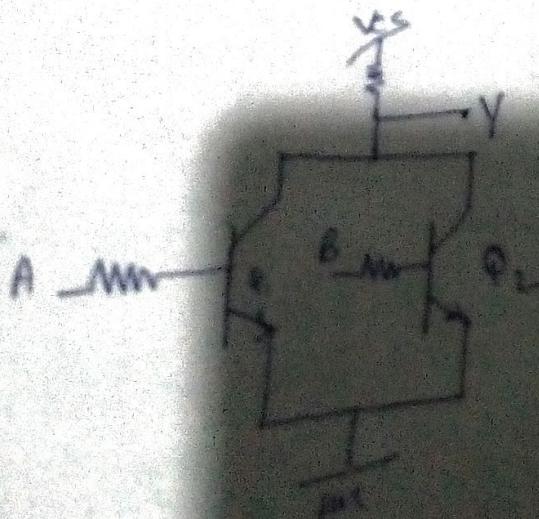
A	Q ₁	Y
0	OFF	1
1	ON	0

NOT GATE



A	B	Q ₁	Q ₂	Y
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

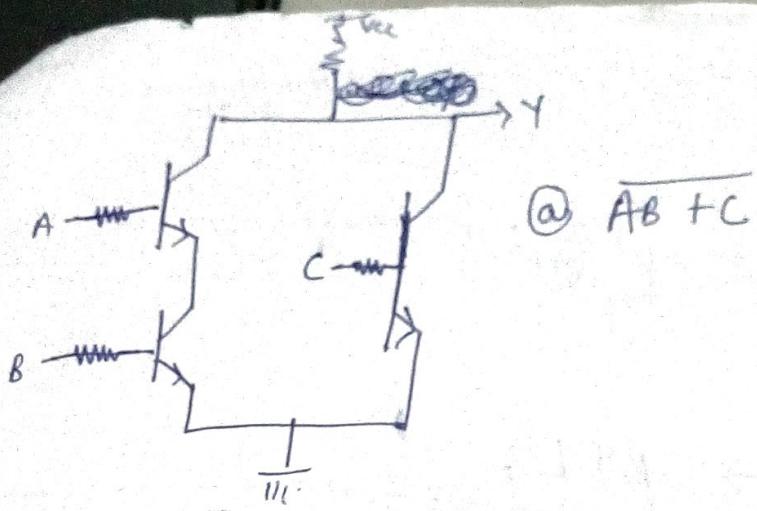
NAND GATE



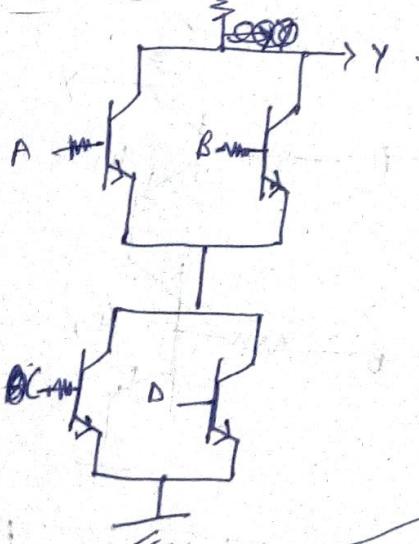
A	B	Q ₁	Q ₂	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

$$Y = \overline{AB}$$

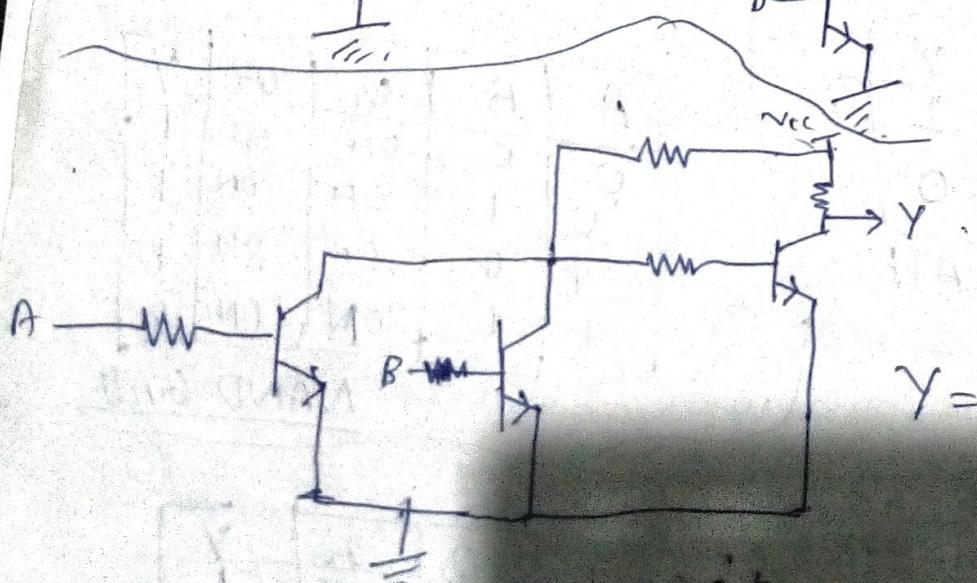
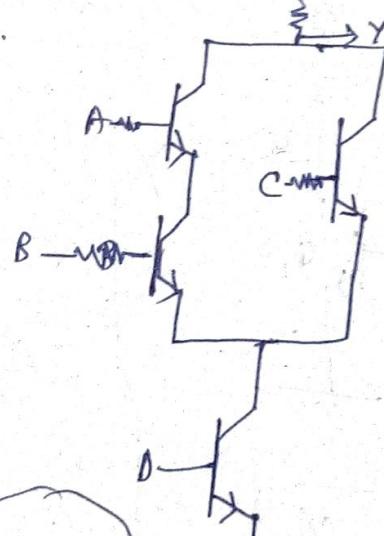
NOR
GATE



$$\textcircled{b} \quad Y = (\overline{A+B})(\overline{C+D}) \text{ vcc}$$



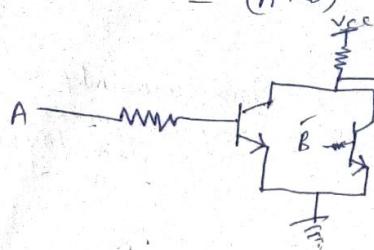
$$\textcircled{c} \quad Y = (\overline{AB} + \overline{CD}) \text{ vcc}$$



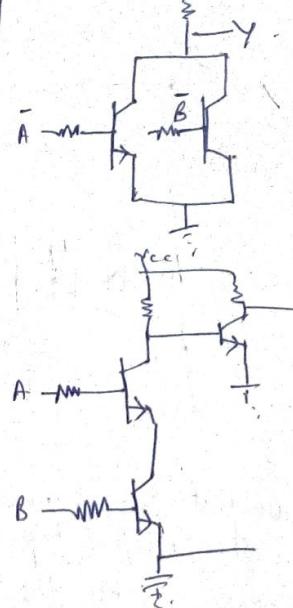
opt.
④ NAND

$$\overline{AB} + C$$

$$Y = \overline{A} \cdot B = (\overline{A} + \overline{B})$$



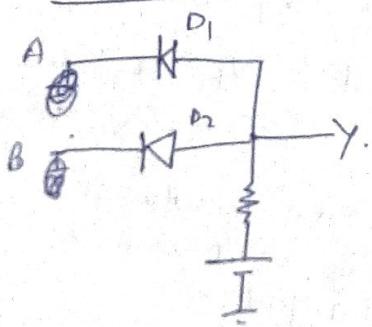
$$Y = A \cdot \overline{B} \cdot v_{cc}$$



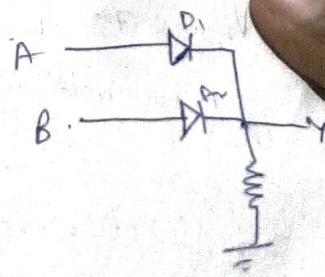
4 Transistor

3 Transistor

Diodes.



$$Y = OR.$$

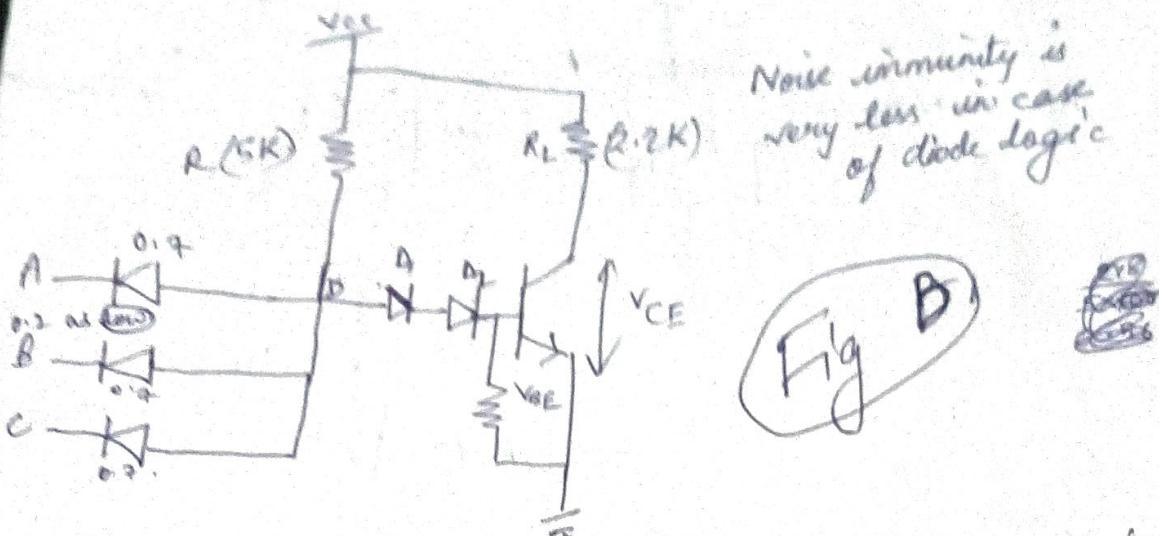


A	B	D ₁	D ₂	Y
0	0	ON	ON	0
0	1	ON	OFF	0
1	0	OFF	ON	0
1	1	OFF	OFF	1



Diode Transistor logic

DTL



The output signal may fluctuate due to the noise in the output input signal.

However when the output is fed through the transistor the final output is independent of the noise at the output.

$$V_{D_1} = 0.7 = V_{D_2} \quad V_{BE} = 0.8V \quad V_{CE} = 0.2V$$

$$\text{Hence minimum voltage at } D = V_{D_1} + V_{D_2} + V_{BE} \\ = 2.2V.$$

Two diodes are connected in series to obtain a sufficient noise immunity voltage at D so as to counteract the effect of noise at input.

If a single diode is connected, then min. voltage at D = $V_{D_2} + V_{BE} = 1.5V$

And, the difference in the voltage at D & at positive terminal of the diodes = $1.5 - 0.9$

$$= 0.6$$

which is bare minimum to counter the effect of noise.

\downarrow Fan-in & Fan-out

No. of similar gates which can be driven by a gate



Fan-in = 1



Fan-in = 2

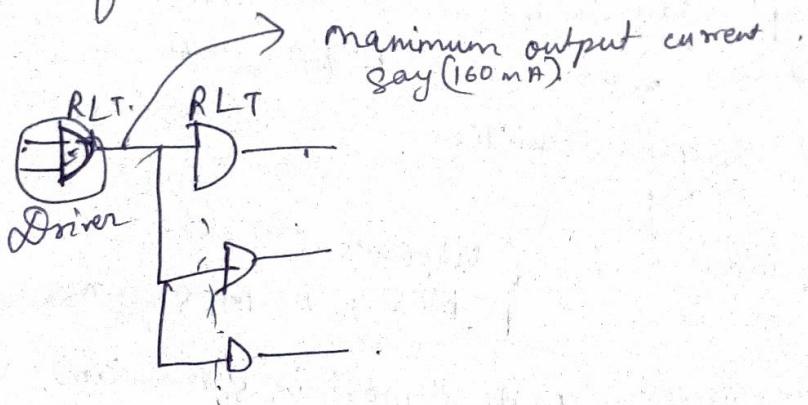


Fan-in = 4

\downarrow Fan-out.

No. of gates similar gates which

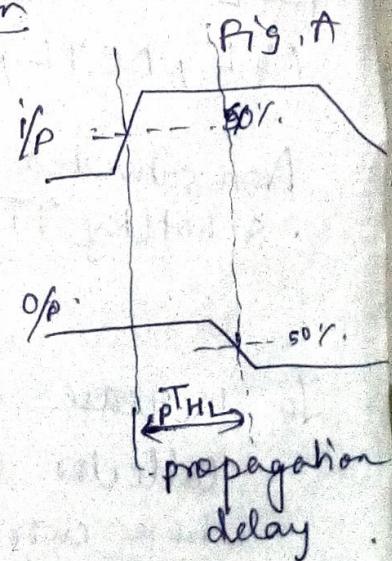
No. of leads connected to the output of a gate



Propagation delay / speed of operation

The speed of a digital circuit is specified in terms of propagation delay. The input & output waveform of logic gates are shown in Fig. A.

The delay times are measured between the fifty % voltage level of i/p off waveform



$$\text{average prop^n delay} = \frac{P_{THL}^T + P_{TOL}^T}{2}$$

$P_{THL}^T \rightarrow$ prop^n delay for high to low

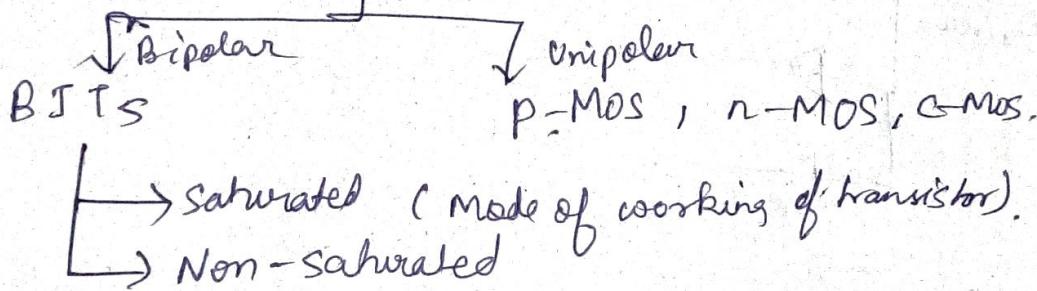
$P_{TOL}^T \rightarrow$ prop^n delay for low to high

~~The propⁿ~~ delay : This is
Power dissipation: The total power dissipated in an IC ~~is~~ is determined by the current I_{cc} that is drawn from the supply (V_{cc}).
Given By $P = V_{cc} \times I_{cc}$

Figure of merit: Propagation delay time \times power.

The unit of figure of merit = picosecond
if propⁿ delay is measured in nanosecond
• power diss. is in milli watt.

Digital logic families



~~RTL~~ The saturated bipolar logic families are RTL, DCTL, IIL, DTL, HTL, TTL.

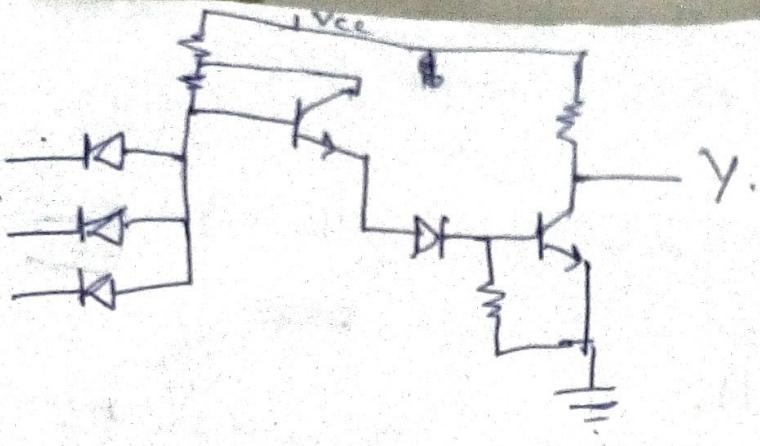
Non saturated bipolar logic families are ECL, Schottky TTL

Emitter coupled logic

To increase the fan-out, we need to increase the collector current. So we can increase the base current by replacing the diode D_1 with a 'transistor' (Ref Fig B).

The modified DTL circuit has a better fan-out

✓ TTL
Due
circ
envi
deg
do
H

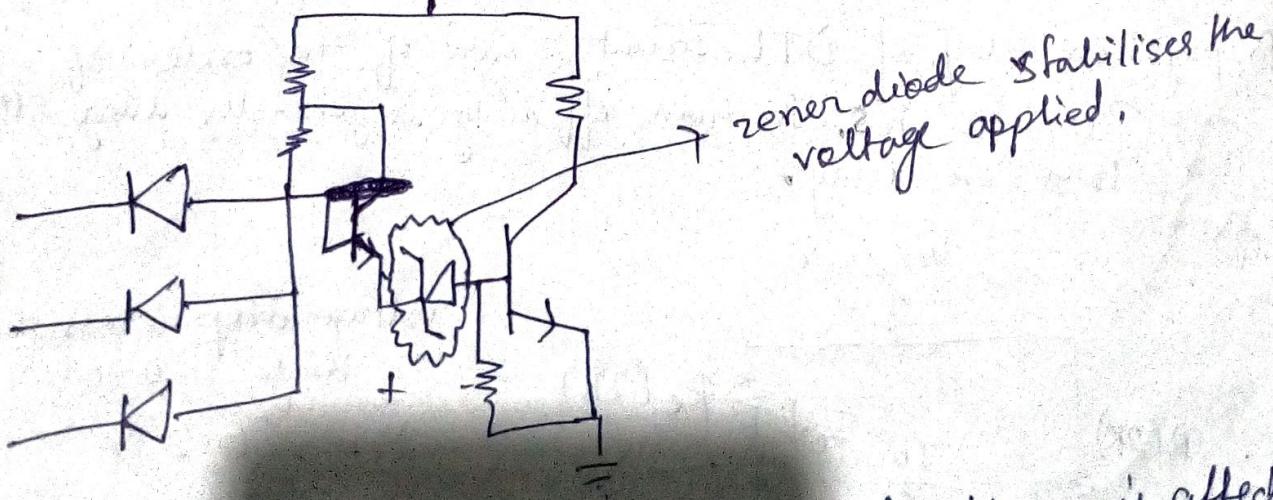


A circuit can behave as a current source / current sink.

HTL → High Threshold Logic.

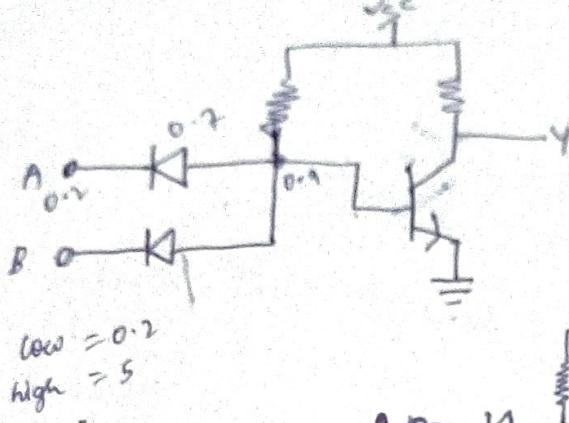
Due to presence of electric motors, on/off control circuits and high voltage switch in an industrial environment, the noise level is quite high and logic families like DTL, RTL and diode families ~~not~~ do not perform properly.

Hence zener diode is used.

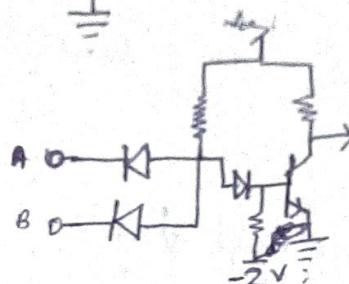


Disadvantage → propagation delay time is affected due to large resistance value.

Convert diode - AND to NAND



The output is always low



→ To correct the output, we connect a diode to the base terminal.

Negative potential decreases the switching speed.

However, dual power supply is reqd.

high resistance value is reqd.

potential drop will increase

power dissipation increases.

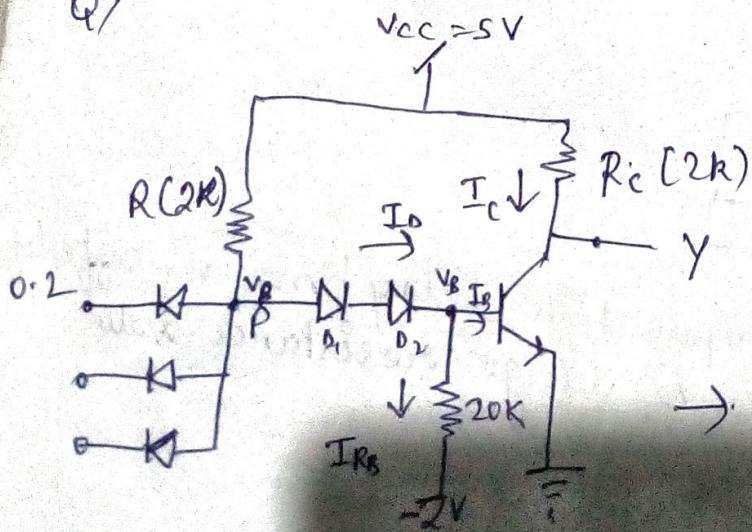
size of chip increases.

cost increases.

Propagation delay of DTL circuit are of the order of

30 - 80 μ s. The turn off delay is generally larger than turn-on delay.

9



Voltage drop across the diode = 0.65 V

$$V_{CE} = 0.2 \text{ V}$$

$$V_{BE} = 0.75 \text{ V}$$

$$V_A = V_{D_B} = 0.75V$$

s are low ($0.2V$)

$$V_P = 0.95 V$$

$$V_B = V_P - V_{A_1} - V_{B_2} = 0.95 - 1.30 = -0.35 \text{ V.}$$

If we neglect the base current

$$I_1 = \frac{-0.35 - (-2)}{0.000001}$$

$$\frac{1.65}{2} \times 10^4$$

output is always low

To rectify the output, we connect a diode to the base terminal.

Speed
reqd.
is reqd.
increase
increases.
 p increases

order of
ally larger than

across the
 $= 0.65 \text{ V}$

0.2 V

0.75 V

$= 0.75 \text{ V}$

(0.2 V)

V

$= -0.35 \text{ V}$

$\frac{1}{2} \text{ ms}$

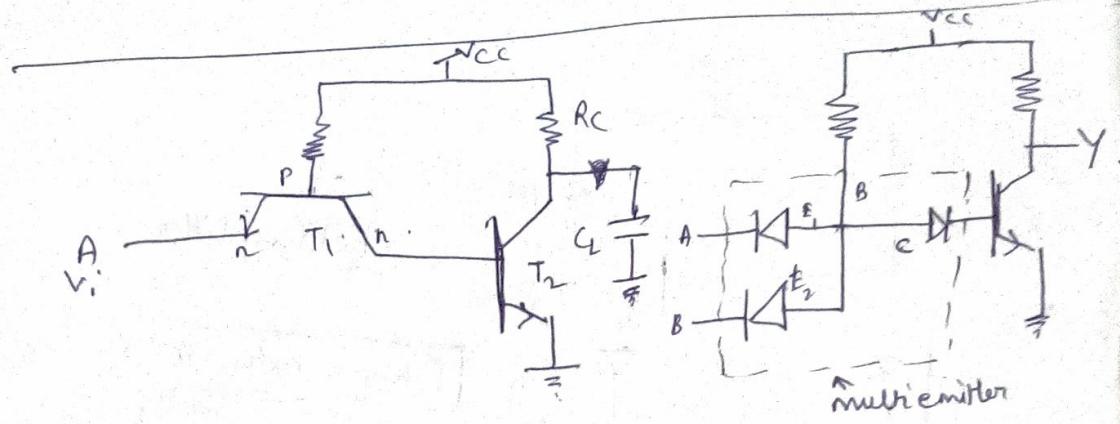
5 mA

When inputs are all high;
 $V_p = 5$, D_A, D_B, D_C are all off (open)

$$V_p = V_{D_1} + V_{D_2} + V_{BE} = 2.05 \text{ V}$$

$$I_D = \frac{V_{CC} - V_p}{2R} =$$

$$I_{RB} = \frac{2 + (0.75)}{20 \text{ k}}$$



When V_i at A = 5 V,
BE is reverse biased.

Hence it is reversely active transistor

$$T = R_C C_L$$

by decreasing the charging time of C_L
the switching time can be decreased

However C_L is constant

If R_C is decreased to a minimal amount, then a huge amount of current will flow through T_2 if transistor is on.

If an electrical component is connected to a power source (positive or negative) then it is a pull up.

If connected to ground it is connected to ground.

then it is a pull down.

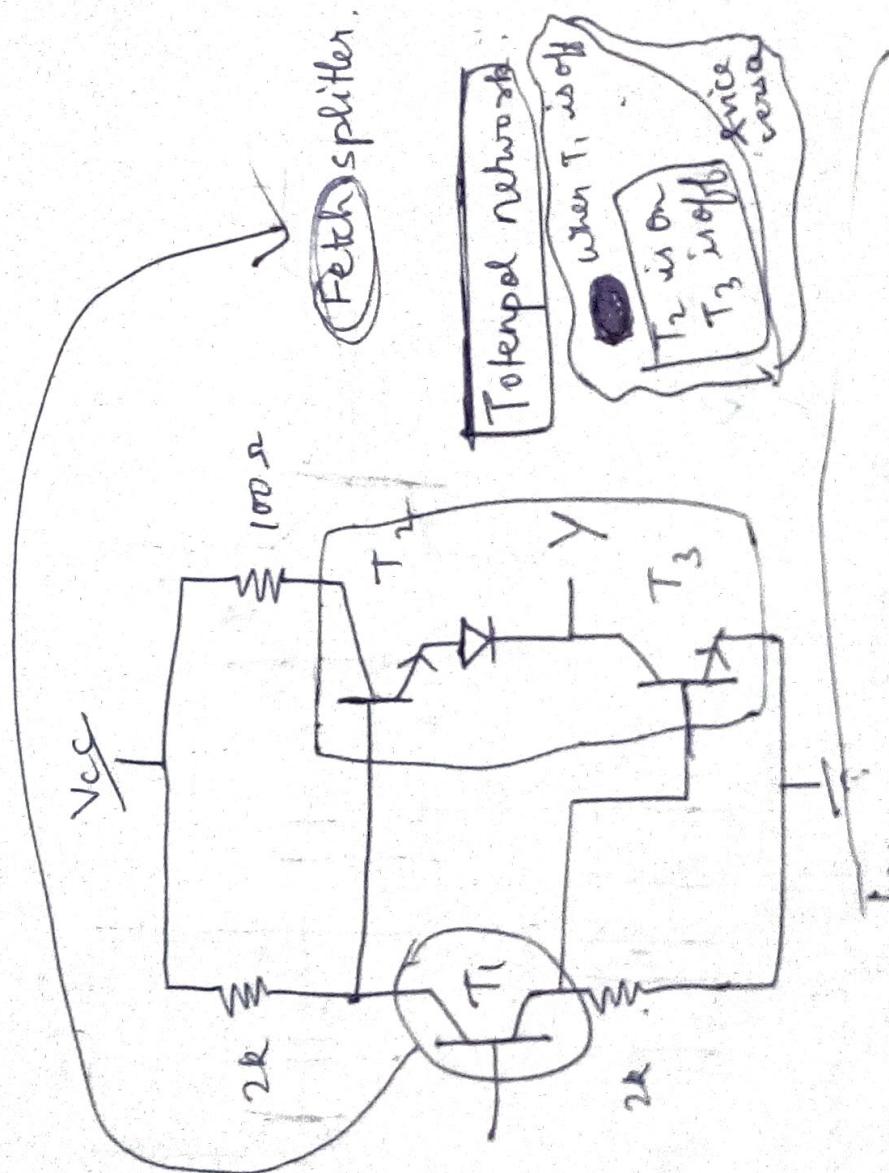
passive components cannot change their values during the working state.

active components can change their values during the execution, hence such components are used when dynamically resistances need to be changed.

Draw a RTL circuit.

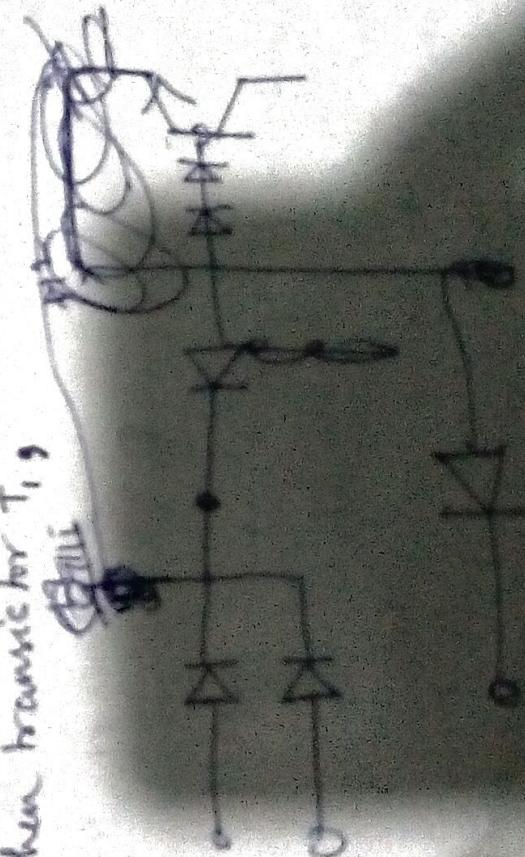
$$\psi_1 = \frac{(A+B)C}{(ABC+D)}$$

$$\psi_2 = \frac{ABC}{(ABC+D)}$$



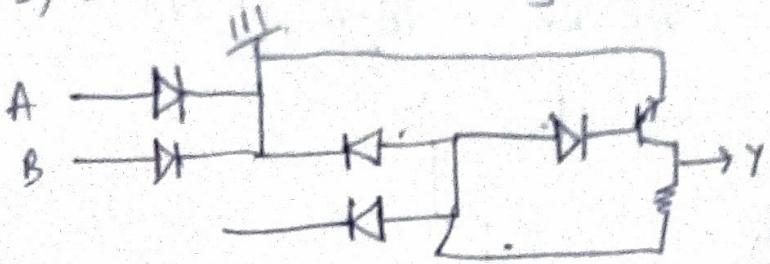
No need of -ve power supply.

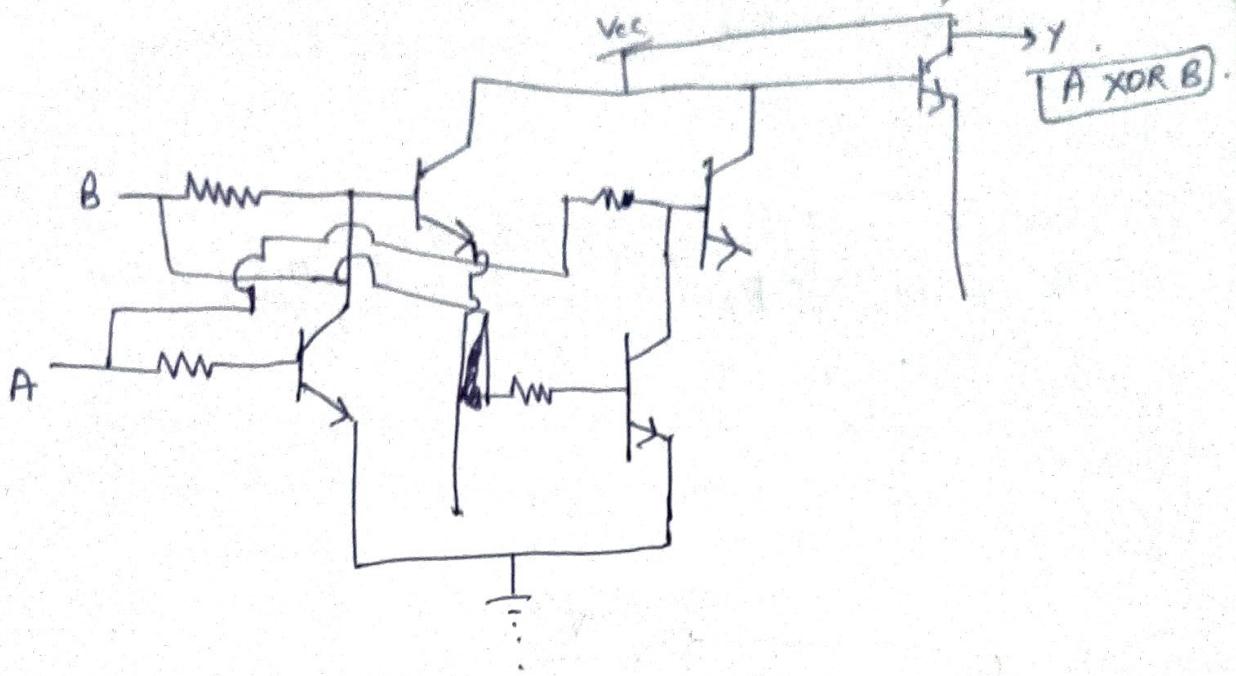
When transistors T_1 , T_2 & T_3



$\overline{(A+B)C}$

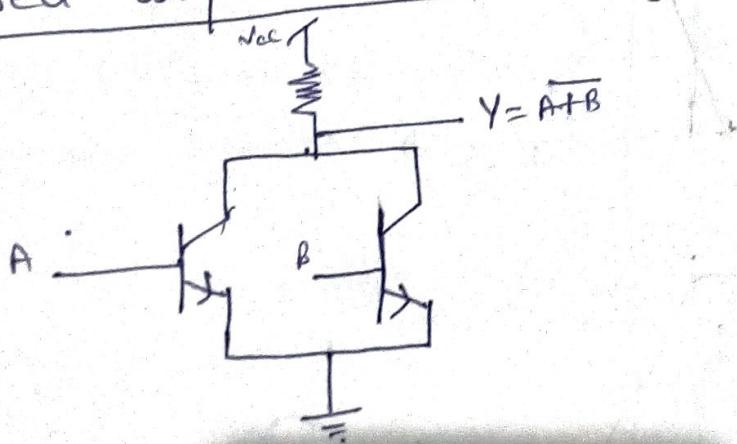
using DTL





Main disadvantage of RTL circuit:
Resistance increases the circuit area.

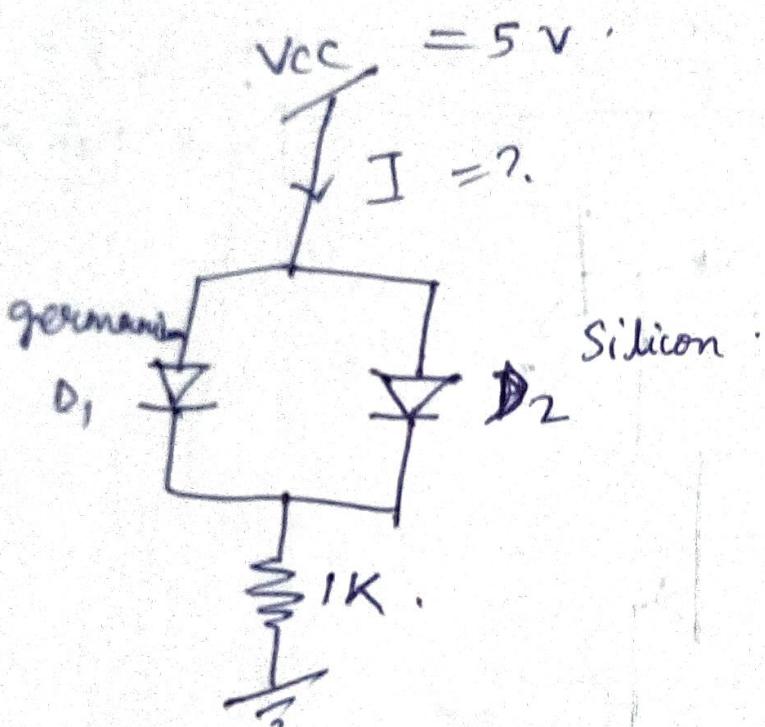
Direct coupled transistor logic (DCTL).



All the transistors used must be identical in all respects

Current hogging problem: (not properly distributed due to difference in inherent biasing.)

The transistors with lesser base emitter voltage draws more current.



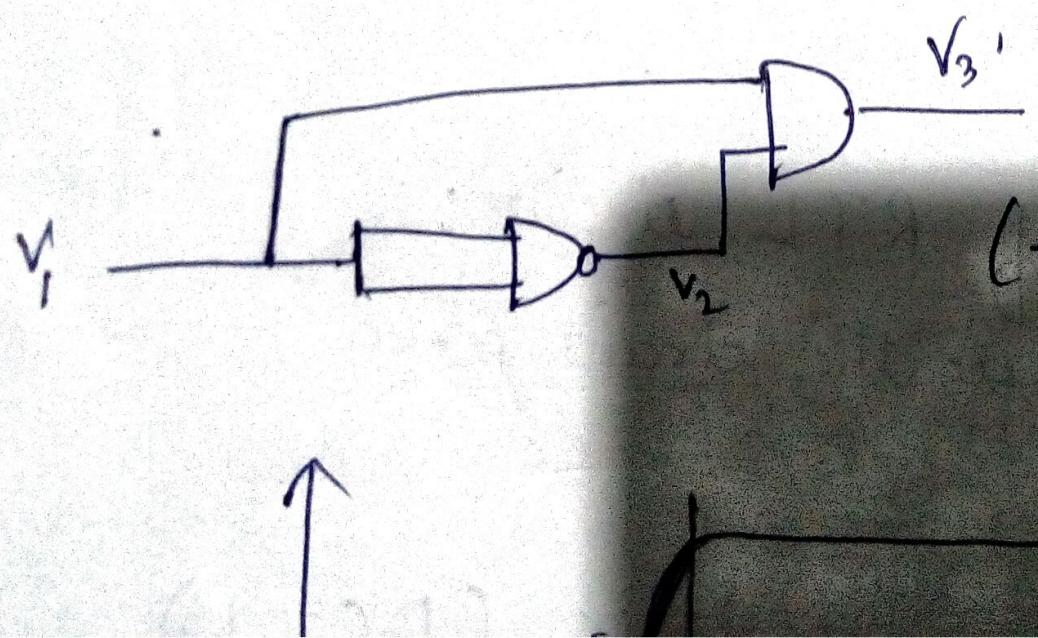
$$I = \frac{5 - 0.3}{1000} = 4.7 \text{ mA.}$$

Symmetric
reduci

N-MOS
of ele

Biasing

~~SCR~~



(If prop^n delay is
considered
then output fluctuates
between 0 & 1).

The m
in an
mobilit
in fast

Symmetrical structure of MOSFET helps in reducing the area, which is not possible in BJT.

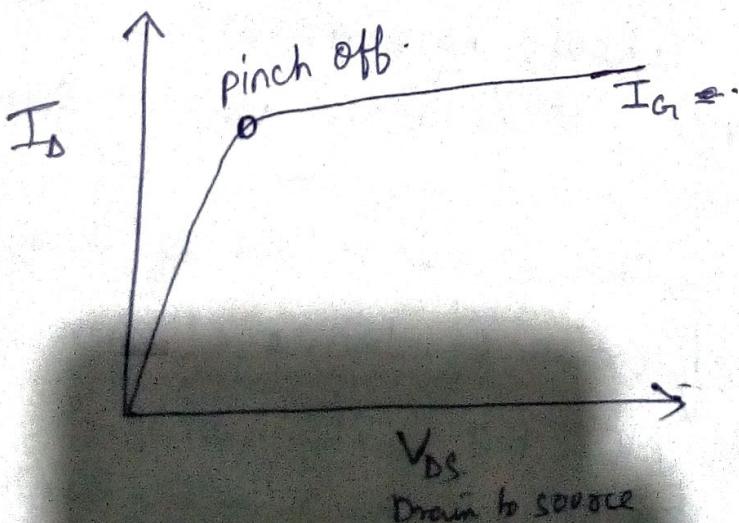
$$= 4.7 \text{ mA}$$

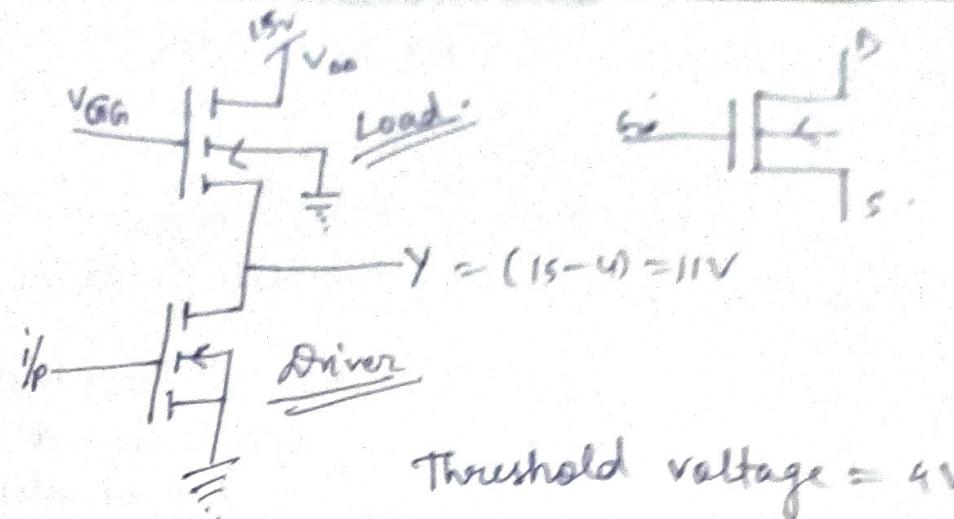
N-MOS is used instead of P-MOS because mobility of electron is much better than hole mobility.

Biasing resistance reqd. for MOS is very high.
~~SO~~ This is solved by using active elements/transistor to reduce the area & dynamically change its value of resistance.

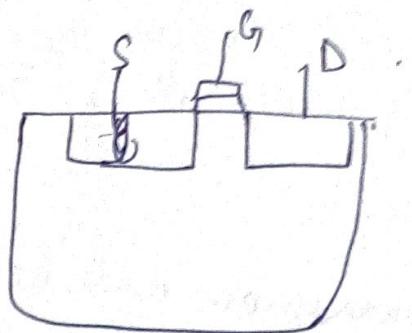
The mobility of electrons which are the carriers in an N-MOS is about 3 times greater than the mobility of hole carriers in P-MOS. Hence an N-MOS is faster a P-MOS.

In the digital circuitry, enhancement mode transistor is generally preferred, since it is a great convenience that the transistor be cut off at zero gate voltage.



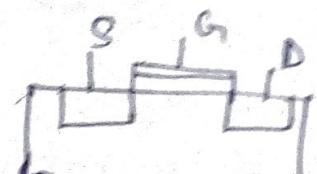


(Depletion)



Driver.

Area of cross section changes
length of channel changes



Load.

Driver transistor should have relatively high conductance, while load should have low conductance.

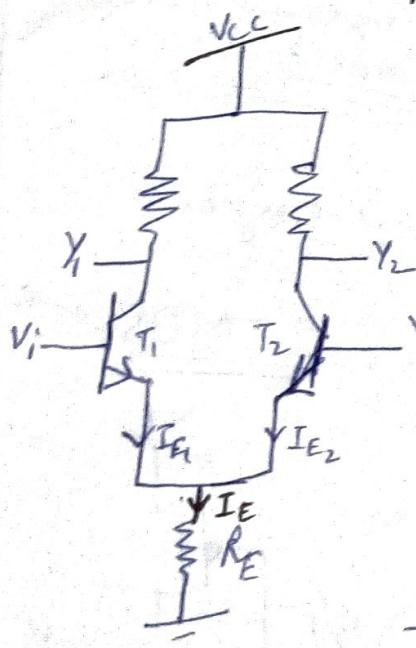
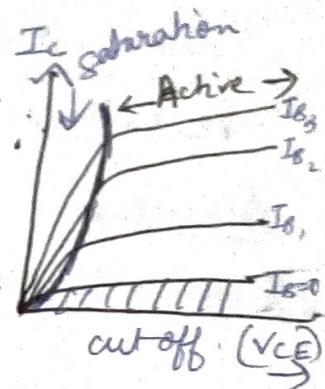
In the BJT switch circuit, use of load resistors of order of 1000s of ohm.

But for the MOSFET switch circuit - load resistance will be of many ~~to~~ 10 k of ohm. even upto over 100 k Ω .

ECI
 → Fast
 → I_{sat}
 → High
 → High
 speed

ECL (Emitter coupled logic)

- Fastest among other logics comparatively.
- Transistor moves from cut-off to active region.
Hence speed decreases.
- Higher resistance will dissipate less power and operate at lower speed. Lower resistance will dissipate more power but are faster



VR (Reference voltage fixed).

Biasing of T_1 from R_E

" " " " T_2 " " " " ; R_E

R_E = high, large
area
of
chip

$$I_E = I_{E1} + I_{E2}$$

If $V_i > VR$, $I_E \approx I_{E1}$,

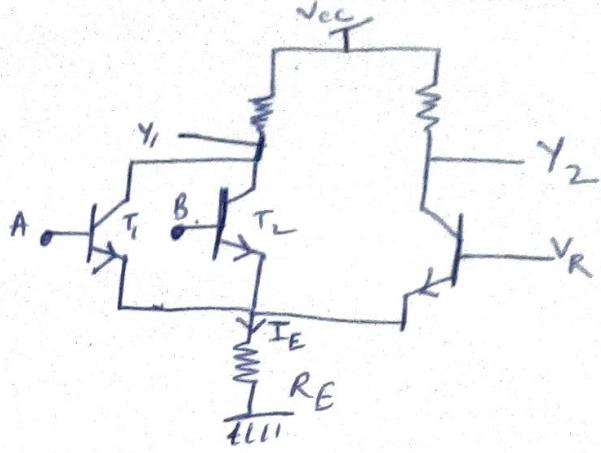
$V_i < VR$, $I_E \approx I_{E2}$

We obtain one output and other its complement from the same circuit (V_i is about VR)

(Contd.)

OR gate:

A	B	Y_1	Y_2
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1



In circuitry negative potential is used instead of ground and ground as V_{cc}

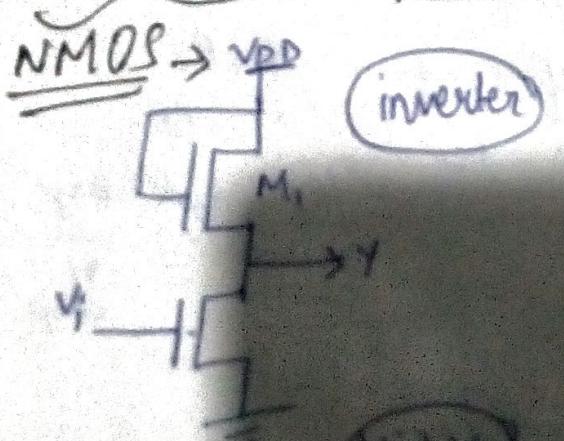
-Ve voltage favors noise margin.

Advantages:

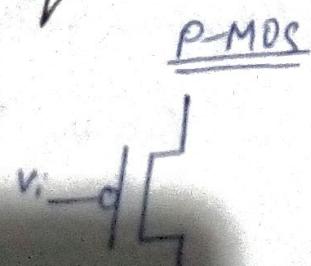
- ① Switching speed is fast → ECL generates complementary alongside output
- ② → Input impedance is very high and output impedance is very low (Differential Impedance)

Disadvantages

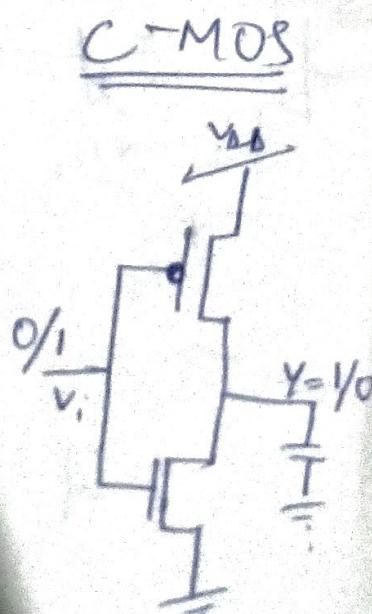
- R_E is high to keep transistors in active region.
∴ More space is reqd.



$V_i > V_T$
threshold
Remains on when $V_i = \text{high}$



Remains on when $V_i = \text{low}$



CML

i/p

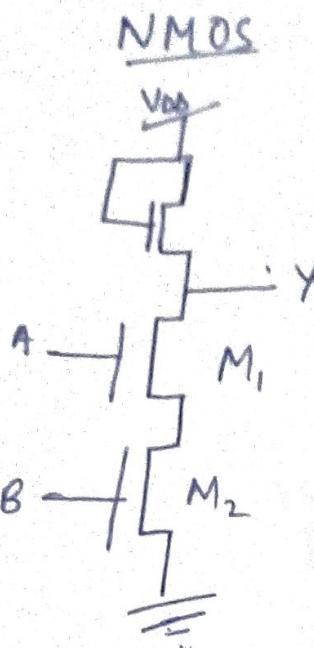
→

NMOS

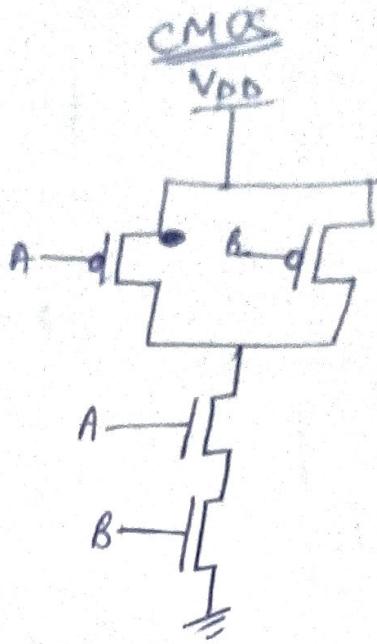
Q

(A)

NAND

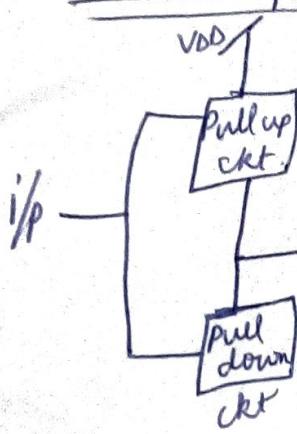


CMOS

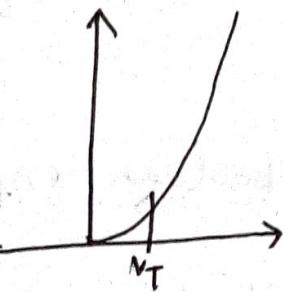


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

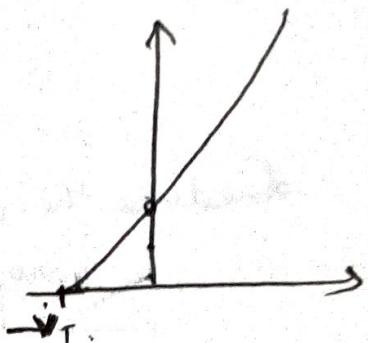
CMOS t_{on} t_{off}



E-MOS
O/p characteristics

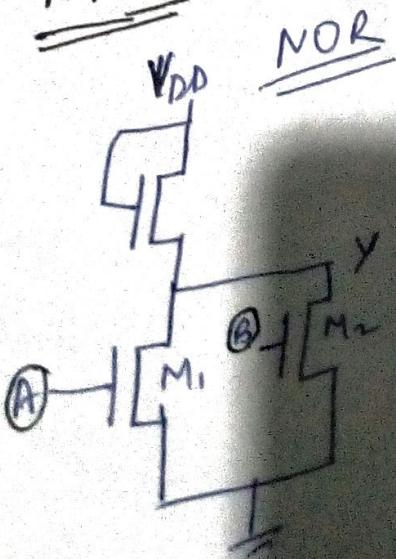


D-MOS
O/p charac.

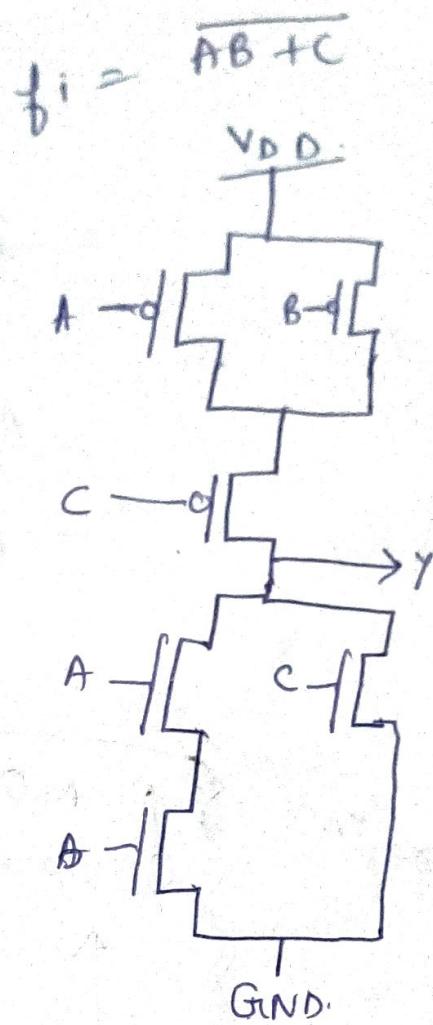
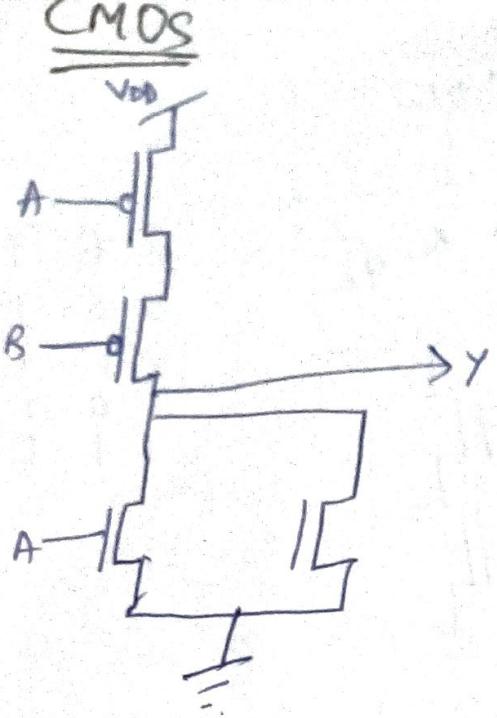


→ switching off time is high in DMOS
→ DMOS requires dual power supply

NMOS



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



Deduce the ~~logic~~ boolean expr.

