Ref. No.:EX/CSE/T/225A/82/2016

B.CSE 2nd YR 2nd SEM. Exam.-2016

COMPUTER ARCHITECTURE

Time: Three Hours **Full Marks:100**

Group-A

Match the correct pairs. 13×1=13

Set-I	Set-II
1.Any possible permutation of inputs and outputs without conflict	(i) 8
2. B-registers of Cray	(ii) 16-bits
3. Data-memory word-size on the Cray	(iii) 22-bits
4. Hazard detection unit	(iv) 24-bits
5.Multicomputers	(v) 64
6. Multiprocessors	(vi) 64-bits
7. Parcel	(vii) dynamic networks
8. Pipelining	(viii) false dependency
9. Register-renaming	(ix) inserting stalls
10. S-registers of Cray	(x) non-blocking network
11. T-registers of Cray	(xi) reservation stations
12. WAR	(xii) static network
13. Word addresses on the Cray	(xiii) successive subtasks

Group-B

Answer eighteen (18) questions 18×4=72

Choose the unique correct answer.

14. In the instruction sequence

```
add  $s0, $t0, $t1
sub  $t2, $s0, $t3
```

executed in a 5-stage pipeline (IF, ID, EX, MEM, WB),

(a) WAR hazard is involved
(b) pipelining is not possible and sequential execution must be used
(c) forwarding can resolve the hazard
(d) two parallel pipelines are essential

15. In the instruction sequence

```
lw   $s0, 20($t1)
sub  $t2, $s0, $t3
```

executed in a 5-stage pipeline (IF, ID, EX, MEM, WB),

(a) forwarding alone can resolve the data hazard
(b) both forwarding and stalling are required
(c) hazard resolution is impossible
(d) a Butterfly Network is essential

16. In the MIPS floating-point unit using dynamic scheduling, the component which holds an instruction that has been issued and is awaiting execution at a functional unit is called

(a) load buffer
(b) store buffer
(c) common data bus (CDB)
(d) reservation station

17. In the MIPS floating-point unit, the common data bus (CDB) is **NOT** connected to
(a) store buffers
(b) load buffers
(c) FP registers
(d) FP multipliers

For Q18-20

Consider the MIPS floating-point unit using dynamic scheduling.
In an arithmetic operation

```
op   a,b,c
```

Q_j and Q_k are the reservation stations that will produce b and c respectively. V_j and V_k are the values (can be a memory location or a register, whichever is referred earlier in the program) of the source operands b and c respectively.
Now consider the following instruction sequence:

1. L.D	F6, 34(R2)
2. L.D	F2, 45(R3)
3. MUL.D	F0, F2, F4
4. SUB.D	F8, F2, F6
5. DIV.D	F10, F0, F6
6. ADD.D	F6, F8, F2

Consider the point of time when instruction-1 has completed execution and the result is available on the CDB while the remaining instructions 2-6 have only been issued (but not completed).

18. For instruction-6, Q_j is
(a) instruction-1
(b) instruction-2
(c) instruction-3
(d) instruction-4

19. For instruction-5, V_k is
(a) Mem[34 + Regs[R2]]
(b) Mem[45 + Regs[R3]]
(c) Regs[F10]
(d) Regs[F0]

20. For instruction-3, V_k is
(a) Mem[45 + Regs[R3]]
(b) Regs[F0]
(c) Regs[F4]
(d) Regs[F2]

21.For issuing a one-parcel instruction in the Cray X-MP, it is first fetched into the
(a) CIP
(b) NIP
(c) LIP
(d) A-registers

22. For issuing a two-parcel instruction in the Cray X-MP, the second parcel is fetched into the
(a) LIP
(b) NIP
(c) CIP
(d) T-registers

23. During a vector operation on the Cray X-MP,
(a) source vector registers are reserved
(b) destination vector register is reserved
(c) functional unit is reserved
(d) all of the above

24. Massively parallel computers can be built with
(a) shared-memory systems
(b) distributed-memory systems
(c) single-bus multiprocessors
(d) vector processors

25. A distributed shared memory architecture
(a) is less scalable than a shared-memory system
(b) is more scalable than a shared-memory system
(c) has separate address spaces for the local memories
(d) is only a theoretical concept that cannot be implemented.

26. A multiple-bus interconnection network is a
(a) switching network
(b) multistage network
(c) shared-path network
(d) crossbar network

27. In centralized bus arbitration, if the bus-busy line is active, the arbiter
(a) allocates the bus to the highest priority requesting master
(b) deactivates the currently active grant line
(c) accepts only requests having higher priority than the current master
(d) does not accept any bus request

28. In a decentralized rotating arbiter,
(a) arbiter-i activates its local grant G-i if priority (i-1) is active
(b) there is no fairness
(c) a master must use the bus when its turn comes
(d) there are no request lines from masters

29. In a (3,3,4) symmetric Clos network, each middle-stage switch has
(a) 1 output
(b) 3 outputs
(c) 4 outputs
(d) 2 outputs

30. The number of crossbar switches in each stage of a k-ary n-fly Butterfly network is
(a) k^{n-1}
(b) k^n
(c) k^{n+1}
(d) n^k

31. The factor which determines how a network's resources such as channel bandwidth, buffer capacity, and control state are allocated to packets traversing an interconnection network is
(a) routing
(b) flow control
(c) topology
(d) none of the above

32. The basic unit of routing and sequencing is a
(a) flit
(b) message
(c) phit
(d) packet

33. The basic unit of bandwidth and storage allocation is a
(a) flit
(b) message
(c) phit
(d) packet

34. In buffered flow control, if the desired output channel at a node is busy, an arriving packet
(a) can wait until the output channel is free
(b) must be dropped or misrouted
(c) must be retransmitted
(d) causes a deadlock

35. In store-and-forward flow control, an incoming packet at a node
(a) flows to the output channel immediately
(b) is transmitted to the output two flits at a time
(c) must be completely received before it can be forwarded
(d) is appended to the preceding packet in the buffer

36. In wormhole flow control, buffers are allocated to
(a) phits
(b) flits
(c) packets
(d) bytes

Group-C

37. A processor has a five-stage pipeline: IF (fetch), ID (decode), RR (read registers), EX (execute), WB (write results back into registers). An instruction is said to have issued when it passes from the RR stage to the EX stage. The latency between an instruction I_1 and an instruction I_2 dependent on I_1 is the time-delay (cycles) between their issue cycles. If I_1 is an arithmetic operation, the latency is three(3) cycles because the RR stage of I_2 follows the WB stage of I_1. If I_1 is a branch instruction, the latency is four(4) cycles because the IF stage of I_2 follows the EX stage of I_1.

Now consider the following instruction sequence :

```
ADD     r1, r4, r7      ; r1 := r4 + r7
BEQ     r2, #0, r1      ;jump to address in r2 if (r1) = 0
SUB     r8, r10, r11
MUL     r12, r13, r14
```

What is the execution time (in cycles) ?

15

— END —