EX/CSE/T/215A/2017

BCSE 2nd Year 1st Semester EXAMINATION 2017

Computer Organization

Time : Three Hours Full Marks : 100

Answer any *five* questions

All parts of a question are to be answered together

1a) The value of a *float* type variable is represented using the single-precision 32-bit floating point format of IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A *float* type variable X is assigned the decimal value of −14.25. The representation of X in hexadecimal notation is

b) Consider a 16-bit floating number with 6-bit exponent (excess 31 format) 9-bit normalized mantissa. The base is of scale factor 2. Find A+B , A-B and represent the results in the above format, use truncation method of rounding.A = 0 100001 111101111 B = 0 011111 011011011
(Consider an implicit 1 to the left of normalized mantissa as in IEEE format.) (10 + 10)

2a) Instruction execution in a processor is divided into 5 stages, ***Instruction Fetch*** (IF), ***Instruction Decode*** (ID), ***Operand Fetch*** (OF), ***Execution*** (EX) and ***Write Back*** (WB). These five stages take 5, 4, 20, 10 and 3 nanoseconds respectively.The pipeline implementation of the processor requires buffering between the stages with a delay of 2 nanoseconds. Two pipeline implementations are contemplated:

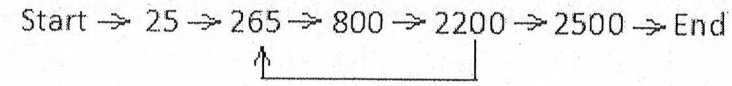
(i) A naïve pipeline implementation (NP) with 5stages

(ii) An efficient pipeline (EP) with 6 stages where the stage OF is divided into two stages OF1 and OF2 with execution times 12 and 8 nanoseconds respectively.

Find the speedup achieved by EP over NP in executing 20 independent instructions with no hazards.

b) Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 6 ns, 7 ns, 10 ns, 8 ns and 8 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 2ns. A program consisting of 14 instructions I1, I2, I3, ..., I14 is executed in this pipelined processor. Instruction I6 is the only branch instruction and its branch target is I12. If the branch is taken during the execution of this program, find the time (in ns) needed to complete the program. (10 + 10)

3. A typical computer system has 32K main memory and 2K fully associative cache memory. The cache block size is 128 bytes. (i) How many bits are there in the TAG field ? (ii) Find the successful hit ratio for the following program structure where LRU replacement policy is used. The program starts from address 25 and continues to address 2500 with a loop between 265 to 2200, which loops 10 times. (20)

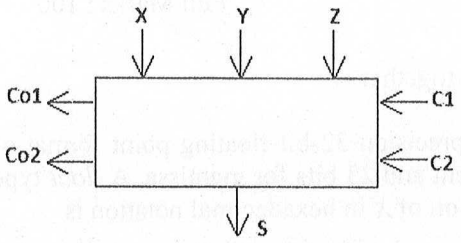


4a) Describe Booth's modified algorithm and show that just N/2 partial products are required to multiply two N bit binary numbers. Illustrate the algorithm with the example of multiplication of +29 and -31.

b) How associative memory differs from conventional memory ? Explain with neat diagram the organization of associative memory. Describe the operation of match logic used in associative memory. (10+ 10)

5a) Suggest a situation where it would be advantageous to define a virtual memory that may be smaller than available physical memory. Similarly suggest a situation where use of cache memory will be found detrimental.

b) Design a device capable of adding three binary bits simultaneously. The device has five inputs as shown below.



X, Y and Z are three arguments, C1 is the carry-in from the preceding stage, C2 is the carry-in from prior to preceding stage. The output S designates the sum, C01 is the carry-out for the succeeding stage and C02 is the carry-out for the next-to-the succeeding stage, Drive the minimal Boolean functions for each of the three outputs S, C01 and C02. Also calculate the delay involved in your design. (5 + 15)

6a) Draw the CSA organization to add 9 signed nos. of 6 bit each having CLA at last stage. Count the minimum no. of full adders, basic adders and CLCs required for your design. Also calculate the gate delay in your addition process.

b) The memory unit of a computer has 256K words of 32 bit each. The computer has an instruction format with four fields : an opcode field, a mode field to specify one of seven addressing modes, a register address field to specify one of 25 processor registers and memory address. Specify the instruction format and the no. of bits in each field, if each instruction is one memory word long. Also find the total no. of operations that can be performed by the ALU. (10+10)

7a) In a certain computer system with cache memory 550 micro sec. is the access time for cache miss and 50 micro sec. is the access time for cache hit. Find the percentage decrease in the effective access time if the hit ratio is increased from 75% to 95%.

b) Consider a 2-way set associative cache with 256 blocks and uses LRU replacement. Initially the cache is empty. Conflict misses are those which occur due the contention of multiple blocks for the same cache set. Compulsory misses occur due to first time access to the block. The following sequence of memory access is repeated 10 times. { 0,128,256,128,0,128,256,128,1,129,257,129,1,129,257,129 }
Find the number of conflict misses as well as compulsory misses. (10+10)

8. Write short notes on :

i) Belady's Anomally ii) Virtual memory

iii) Carry Look Ahead adder iv) Series parallel adder (4x5 = 20)