B.CSE 3rd YR 1st SEM. Exam.-2016

# COMPUTER ARCHITECTURE

**Time: Three Hours** **Full Marks:100**

## Group-A

Answer twenty questions. $20 \times 4 = 80$

Choose the unique correct answer

1. Consider the instruction sequence

```
lw  $s0, 20($t1)
sub $t2, $s0, $t3
```

The instruction pipeline has 5 stages.
To resolve the data hazard with forwarding, we would have to stall
(a) one stage
(b) two stages
(c) three stages
(d) none of the above

2. In Tomasulo's algorithm, register renaming is provided by the
(a) common data bus (CDB)
(b) operation bus
(c) load buffers
(d) reservation stations

3. The instruction sequence

```
mul r1, r2, r3
add r2, r4, r5
```

exhibits
(a) RAW dependency
(b) WAR dependency
(c) WAW dependency
(d) none of the above

4. Pipeline scheduling involves
(a) bypassing
(b) instruction reordering
(c) stalling
(d) register renaming

5. The vector POP/PARITY unit of the CRAY X-MP has
(a) 4 stages
(b) 5 stages
(c) 6 stages
(d) 7 stages

6. A word address on the CRAY X-MP is specified by
(a) 32 bits
(b) 64 bits
(c) 128 bits
(d) none of the above

7. A one-parcel instruction of the CRAY X-MP is decoded in the
(a) LIP
(b) NIP
(c) CIP
(d) any of the above, depending on the op-code

8.The instruction

SAR reg/mem, 1

of the Pentium can be paired if it is loaded in the
(a) U pipeline
(b) V pipeline
(c) U or V pipeline
(d) none of the above

9.The branch prediction logic of the Pentium allows it to avoid
(a) pipeline stalls
(b) buffer overwriting
(c) floating point errors
(d) interrupts

10. When the history bits of the Pentium are in the weakly taken state and branch is not taken, the next state becomes
(a) strongly taken
(b) weakly taken
(c) weakly not taken
(d) strongly not taken

11. Local memories are components of a global address space in a
(a) distributed shared memory system
(b) multicomputer
(c) multiprocessor
(d) SIMD architecture

12. The main disadvantage of shared memory systems is
(a) lack of message passing paradigm
(b) lack of scalability
(c) complicated synchronization
(d) memory failures

13. In order to achieve high performance in multicomputers, special attention should be paid to
(a) load balancing
(b) cache coherence
(c) network topology
(d) programming paradigm

14. The architecture of the Stanford Dash multiprocessor is
(a) UMA
(b) NUMA
(c) COMA
(d) CC-NUMA

15. In centralized arbitration, the bus busy line
(a) is activated by the bus arbiter
(b) is not used
(c) is activated by a requesting master
(d) is activated by a requesting master upon obtaining bus grant

16. In a daisy-chained bus grant scheme for arbitration, a master can access the shared bus if
(a) bus busy line is active and input grant line is passive
(b) both bus busy line and input grant line are active
(c) both bus busy line and input grant line are passive
(d) bus busy line is passive and input grant line is active

17. Dropping flow control is associated with
(a) buffered flow control
(b) bufferless flow control
(c) cut-through
(d) store-and-forward

18. Wormhole flow control is a method for
(a) bufferless flow control
(b) cache coherence
(c) flit-buffer flow control
(d) packet buffer flow control

19. A k-ary n-fly contains
(a) k stages
(b) n stages
(c) $k^n$ stages
(d) none of the above

20. A flit carries
(a) routing information
(b) sequencing information
(c)VCID
(d) all of the above

21. An x×y crossbar switch may be implemented with
(a) x y:1 multiplexers
(b) y x:1 multiplexers
(c) one x:y multiplexer
(d) all of the above

22. In credit-based flow control, each time the upstream router forwards a flit, thus consuming a downstream buffer, it
(a) resets the appropriate count
(b) increments the appropriate count
(c) decrements the appropriate count
(d) none of the above

23. In the MESI protocol, if the cache is in the exclusive(E) state and there is a PrWr event, the state becomes
(a) E
(b) I
(c) M
(d) S

24. In the MSI protocol, if a cache has a block in the modified state and observes a BusRd transaction on the bus,
(a) the cache flushes the data onto the bus
(b) the cache changes the state of the block to 'invalid'
(c) the cache remains passive and takes no action
(d) the system enters an illegal state

25. In the MSI protocol, if the present state of a cache is shared (S) and there is a PrWr event, the cache state changes to
(a) M
(b) S
(c) I
(d) none of the above

26. In a directory based cache coherence scheme, the node in whose main memory a block is allocated is called
(a) dirty node
(b) exclusive node
(c) home node
(d) owner mode

27. If the dirty bit for a block in a cache directory is ON,
(a) no node is caching the block
(b) exactly one node is caching the block
(c) exactly two nodes are caching the block
(d) all nodes are caching the block

## Group-B

28. A superscalar processor has four (4) execution units. Load operations have a 2-cycle latency, i.e. an instruction dependent on the load can be issued 2 cycles after the issue of the load. All other operations have a 1-cycle latency. Instructions may be issued out-of-order. If more than four (4) instructions can be issued in a cycle, the processor issues the instructions that occur earliest in the program. Assume that the processor examines the entire program to select the instructions to issue in each cycle. Now consider the following code sequence:

```
ADD     r1,r2,r3        ; r1 := r2 + r3
SUB     r5,r4,r5
LD      r4,(r7)         ; r4 := (r7)
MUL     r4,r4,r4
ST      (r7),r4         ; (r7) := r4
LD      r9,(r10)
LD      r11,(r12)
ADD     r11,r11,r12
MUL     r11,r11,r11
ST      (r12),r11
```

How long will the above code take to issue ? 20