EX/CSE/T/215A/2016

B.CSE 2nd YEAR 1st Semester EXAMINATION 2016

Computer Organization

Time : Three Hours | Full Marks : 100

Answer any ***five*** questions

All parts of a question are to be strictly answered together

1a) What are the advantages of using normalized mantissa and biased exponents in floating point representation of binary numbers? What are the IEEE standards for representing floating point numbers ? Represent +13.0165 in both single precision and double precision IEEE formats.

b) Consider a 16-bit floating number with 6-bit exponent (excess 31 format) 9-bit normalized mantissa. The base is of scale factor 2. Find A+B , A-B and represent the results in the above format, use truncation method of rounding.A = 0 100001 111101111 B = 0 011111 011011011
(Consider an implicit 1 to the left of normalized mantissa as in IEEE format.) (10 + 10)

2 a) A non pipelined processor X has clock rate of 250 MHz and CPI (Cycles per instruction) of 4. Another processor Y , the successor of X is designed with 4 stage linear instruction pipeline. It is found that a program containing 10000 instructions took same time for both the processors to execute. What is the clock rate for processor Y ?

b) A virtual memory system has block size 4K bytes. There are 8 secondary blocks and 4 primary blocks. The associative memory page table contains the following entries :

Secondary Block	Primary Block
2	3
5	2
0	0
4	1

Make list of virtual address spaces (in decimal) that cause page fault if addressed by CPU. (10 + 10)

3. A typical computer system has 32K main memory and 2K fully associative cache memory. The cache block size is 128 bytes. (i) How many bits are there in the TAG field ? (ii) Find the successful hit ratio for the following program structure where FIFO replacement policy is used. The program starts from address 25 and continues to address 2500 with a nested loop between addresses 265 and 2200.

Start → 25 → 265 → 800 → 2200 → 2500 → End (20)

4a) Suggest a situation where it would be advantageous to define a virtual memory that may be smaller than available physical memory. Similarly suggest a situation where use of cache memory will be found detrimental.

b) Design a minimal combinational circuit for multiplying two 4-bit signed binary numbers. Also calculate the gate delay for your circuit. (5+15)

5a) Describe Booth's modified algorithm and show that just N/2 partial products are required to multiply two N bit binary numbers. Illustrate the algorithm with the example of multiplication of +29 and -31.

b) Describe restoring binary division algorithm and the corresponding sequential circuit for implementing it. Next verify your circuit with the example of 18 divided by 5. (10+10)

6a) Draw the CSA organization to add 10 signed nos. of 8-bit each having CLA at last stage. Count the minimum no of full adders, basic adders and CLCs (4 function CLC) required for your design. Also calculate the gate delay in your addition process.

b) Design a combinational circuit for BCD subtraction. Indicate properly the borrow-in and borrow-out terminals for cascading. (10+10)

7. Study the microprogram given below. Draw the hardware configuration for implementing the microprogram. Next design the corresponding control unit using D-flip flops as well as Control Memory. What will be the size of the required Control Rom ?

Rom address			Control Signals					Mode bits		Next Address		
A2	A1	A0	C4	C3	C2	C1	C0	M1	M0	A2	A1	A0
0	0	0	1	0	0	0	0	1	1	x	x	x
0	0	1	0	1	0	0	1	0	0	x	x	x
0	1	0	0	0	1	1	0	0	1	1	0	0
0	1	1	0	1	0	0	0	1	1	0	0	0
1	0	0	0	0	0	1	1	1	0	1	1	0
1	0	1	0	0	0	0	1	1	1	0	0	0
1	1	0	0	0	1	0	0	0	0	x	x	x
1	1	1	0	1	0	1	0	1	1	0	0	0

M1	M0	
0	0	Increment
0	1	Load if S0 = 1
1	0	Load if S1 = 1
1	1	Load

(20)

8a) The conventional 4 block micro programmed control system has following propagation delay times. 40ns to generate the next address, 10ns to transfer the microinstruction into the control data register and 40ns to perform the required micro operations specified by the control word. What is the fastest clock frequency that the control can use ? What would the clock frequency be if the control data register is not used ?

b) A program takes 500ns for execution on a non-pipelined processor. Suppose we need to run 100 programs of same type on a five stage pipelined processor with a clock period of 20ns. What is the speed-up ratio of the pipeline ? What is the maximum achievable speed-up? (10 + 10)