Hybrid RRAM-NEM Relay Design for Programmable Logic Devices

White paper

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February 15, 2019

1 Motivation

Field-programmable gate arrays (FPGAs) are programmable logic devices (PLDs) that enable rapid prototyping of digital circuits and provide an alternative to the expensive application-specific integrated circuit (ASIC) design process today. However, when compared with ASICs performing the same function, SRAM-based FPGAs typically have 10-40 times lower logic density, 3-4 times higher delay, and 5-12 times higher dynamic power dissipation [1], [2], [3]. This is because reconfigurable components incur large overhead—instead of being packed tightly, configurable logic blocks (CLBs) in FPGAs are laid out relatively far apart to make space for routing components, resulting in greater interconnect delay, power dissipation, and chip area. The disparity in the performance of FPGAs and ASICs provides motivation to find ways to reduce reconfigurability overhead, so that ultimately PLDs can become competitive with ASICs at manufacturing scale. Possible solutions lie with PLD designs that trade off fine-grained CLBs with more specialized blocks e.g. coarse-grained reconfigurable arrays (CGRAs) [4], or with emerging nanotechnologies that enable novel design strategies in the space of reconfigurable semiconductor devices (to be discussed later).

Another topic of interest in semiconductor design today is "normally off, instantly on" device operation, which is critical for devices with weak, unreliable, or intermittent power sources. Energy-harvesting devices, wearables, and low-power nodes in the Internet of Things (IoT) will need to be able to operate in this mode to prevent unnecessary power dissipation between periods of action. Today, FPGAs need to load their configuration from off-chip memory into SRAM on startup. This has motivated the development of integrated non-volatile memory (NVM) that can replace (or work well in conjunction with) on-chip SRAMs to enable intermittent computing.

Here, we propose the use of two emerging nanotechnologies in PLD design for bridging the gap between PLDs and ASICs: resistive random access memory (RRAM) and nanoelectromechanical (NEM) relays. We describe a hybrid RRAM-NEM-based design for implementing PLDs with both "normally off, instantly on" device operation and low-overhead reconfigurable routing components. We exploit the properties of RRAM and NEM relays in a synergistic fashion to develop a novel NV-SRAM-based router that has all of its read circuitry implemented in back-end-of-line (BEOL), with RRAM cells directly controlling gate voltage of hysteretic NEM relays that behave as routers. We compare the design of a CGRA developed using the techniques described here versus designs that use (1) NEM relays only, (2) RRAM only, and (3) standard CMOS technologies (baseline).

2 Emerging nanotechnologies for PLDs

2.1 NEM relays

With technology scaling, it is becoming increasingly difficult to design FPGAs using NMOS pass transistors for programmable routing. An NMOS pass transistor introduces a threshold (V_t) drop when passing high voltage level, after which the voltage level must be restored. Unfortunately, pass transistor threshold voltage (V_t) cannot be further reduced due to leakage power constraints.

NEM relays are switches that are actuated electrostatically at the nanoscale. Their properties have been studied in depth, and they have gained interest for their potential as pass transistor replacements in FPGAs [5] [6]. NEM relays have extremely low static power dissipation and low ON-state resistance—however, they switch much slower than transistors (on the order of nanoseconds) and typically operate at higher voltages. NEM relays have a sharp I_{DS}-V_G curve (often referred to in literature as an infinite subthreshold slope) and also exhibit hysteresis in switching state based on applied gate voltage (V_G). This has led to NEM relay-based SRAM designs utilizing this property.

There are two kinds of NEM relays we will focus on: 3-terminal (3T) and 4-terminal (4T) devices (see Figure 3). 3T devices have a source, drain, and gate, and the voltage that controls the beam is the voltage between the gate

Table 1: NEMS devices reported in literature. Adapted from [8].

Research Group	Type	Area	c-gap	V_{pi}	R_c	Cycles	Material	Circuit
First CNT [10] [11]	3T	-	30 nm	4.5V	1 MΩ	>1	CNT	No
First Top-Down (KAIST) [12]	3T	-	40 nm	4V	-	> 10	TiN	No
Out-of-Plane (UC Berkeley) [7] [13] [14]	4T	-	80 nm	<1V	1kΩ	$>10^8$	W	Yes
	6T	-	80 nm	<1V	1kΩ	$>10^8$	Ru	Yes
	6T	-	250 nm	10V	-	1	TiO2	Yes
In-Plane (Stanford University) [15] [16] [17]	5T	-	-	7.9 V	3 kΩ	10^8	Pt	Yes
Curved (NEMIAC) [18] [19]	3T 4T	15 μm^2	50 nm	0.5 V	5 kΩ	$>10^8$	a-C	Yes
SiC Relays (CWR University) [20] [21]	3T	1 μm^2	100 nm	15 V	10 MΩ	>14,000	SiC	Yes
Sandia National Lab [22]	3T	(10 μm^2)	30 nm	>4 V	-	$2 \cdot 10^6$	Ru	No
Cornell University [23]	3T	(3 μm^2)	200 nm	10 V	10 MΩ	-	-	No
Piezoelectric (CM University) [24]	4T	58 μm^2	-	10 mV	16 kΩ	-	Pt	No

and source. This means that the source voltage affects the beam state, which is undesirable for a device that needs to behave as a pass transistor. The 4T device mitigates this problem by having the beam electrically isolated from the "bridge" that connects the source and drain [7]. Table 2.1 (adapted from [8]) describes characteristics of NEM relays found in literature. NEM relays can be fabricated at low-temperatures (< 400°C) making them compatible with CMOS back-end-of-line (BEOL), and they make use of materials already available in foundries. Simple lateral designs require 4-7 masks at the top layer of the device [9]. Research into scaling these devices to smaller sizes and integrating them in 3-dimensions is an ongoing effort.

Several studies have examined the performance implications of using NEM relays in PLDs. Architectural analysis with CMOS-NEM routing and logic lookup tables was performed in [26]. Using a 3D place-and-route scheme with NEM-based routers, a maximum of 41.9% performance gain was achieved over the baseline. However, this study assumed that multiple NEM devices could be viably stacked in 3-D, which has yet to be experimentally demonstrated. Another study claimed a 10-fold reduction in leakage power, 2-fold reduction in dynamic power, and 2-fold reduction in area [5]. A half-select programming scheme was used for the NEM relays which was verified experimentally (see Figure 2), but the use of a 3T device and a small hysteresis window would probably prevent these devices from functioning properly as pass transistor replacements—when a high voltage level is being passed, V_{gs} would fall below V_{po} causing the NEM relay to switch to the off-state unintentionally. The study also used optimistic device parameters/dimensions that have yet to be physically realized.

2.2 RRAM

RRAM is typically based on a metal oxide (such as HfO_2, Al_2O_3, Ta_2O_5) that is already used in CMOS fabrication processes e.g. for gate oxides. Usually, the device programming works via a filamentary process involving soft electric breakdown of the metal oxide to create conductive filaments that can be broken or reformed in subsequent programming (see Figure 1) [27]. RRAM can store multiple bits/cell, however in binary operation, it has a high-resistance state (HRS) which usually corresponds to a '0', and a low-resistance state (LRS) which usually corresponds to a '1'. RRAM has high-speed operation, low operating power, good switch endurance ($> 10^6$ cycles), geometric scalability down to 10 nm x 10 nm, and a relatively simple fabrication process. Many materials have been reported to have resistive hysteresis, and many architectures have been proposed for decoding/sensing the resistance state.

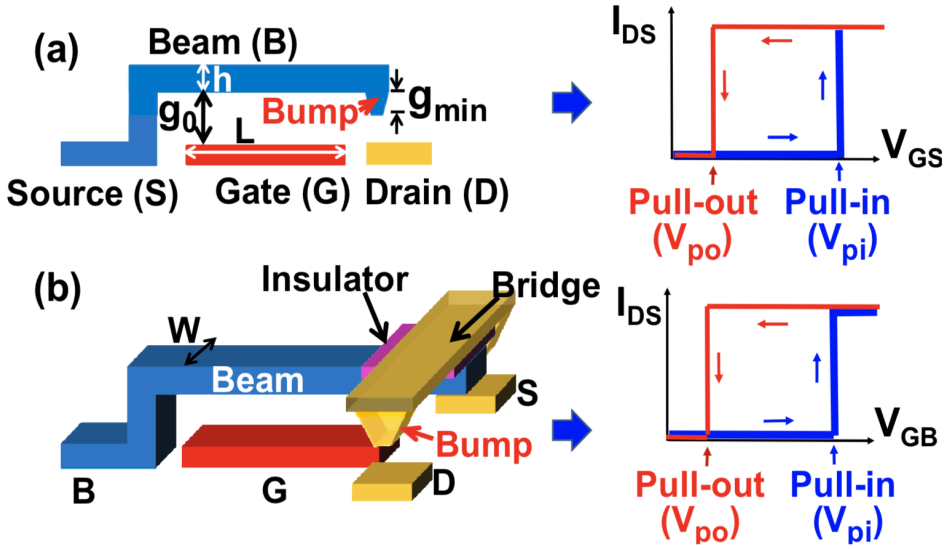


Figure 1: Figure adapted from [6]. (a) A 3T NEM relay and its I_{DS}-V_{GS} characteristics; (b) A 4T NEM relay and its I_{DS}-V_{GB} characteristics. The beam is insulated from the bridge for S/D contacts [25].

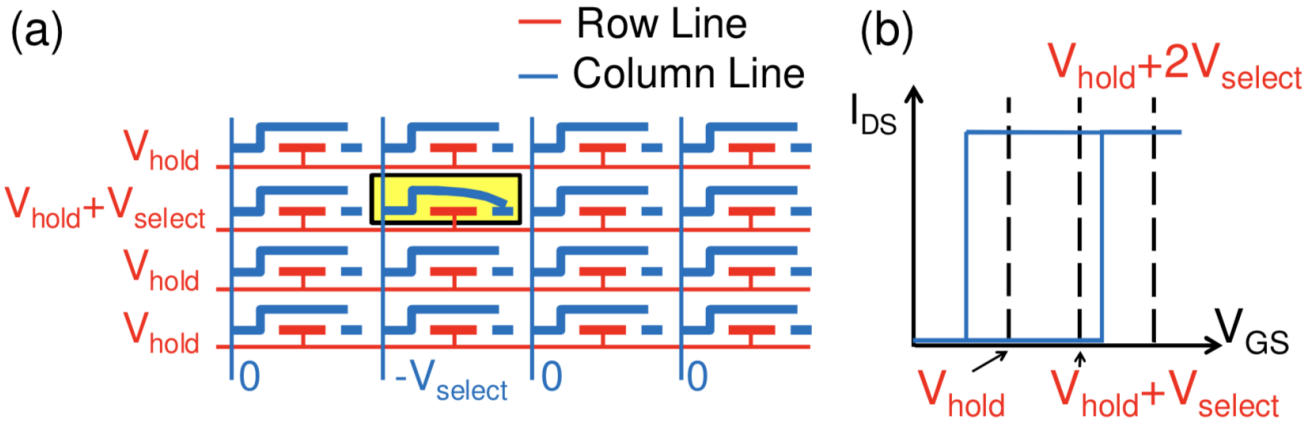


Figure 2: NEM relay half-select programming (adapted from [5]). (a) Array of relays. (b) NEM relay I-V curve with half-select programming voltages.

Table 2: Table of some RRAM device properties reported in literature. Adapted from [28].

Publication & Year	VLSI 2014	VLSI 2014	IEDM 2014	IEDM 2014	VLSI 2015	VLSI 2015
2D/3D Geometry	2D Planar	3D Vertical	2D Planar	3D Vertical	2D Planar	2D Planar
Switch Type	Bi	Bi	Bi	Bi	N/A	Bi
Structure	1T-1R	1R	1T-1R	1R	1T-1R	1R
Top Electrode	Al	TiN	TiN/Ti	Pt	Ir	TiN/TiO2
Material	AlOx/WOx	HfOx	HfO2	HfOx	Ta2O5/TaOx	TiO2/a-Si
Bottom Electrode	W	TiN	TiN	TiN	TaN	TiN
Cell Area (um^2)	0.0324 (.18um)	0.000003	0.01 (100nm)	1 (15nm)	0.0016(40nm)	0.0013
Speed [ns]	~1000	50	40	20	N/A	10
DC Peak Voltage [V]	N/A	<3	<3	<2.5	N/A	6.5
DC Peak Current [uA]	N/A	~500	~60	~100	N/A	5
HRS/LRS Ratio	>180	>10	10	100	10	10
R high [Ω]	$3 \cdot 10^7$	10^6	$2 \cdot 10^5$	$3 \cdot 10^7$	$5 \cdot 10^4$	10^8
R low [Ω]	$3 \cdot 10^4$	10^4	$2 \cdot 10^4$	$3 \cdot 10^4$	$4 \cdot 10^3$	10^7
Endurance	10^9	10^4	10^3	10^8	$> 10^5$	10^6
Retention	10y	20000h	10y	10y	10y	3y
Retention Temp.	85°C	250°C	70°C	RT	85°C	55°C

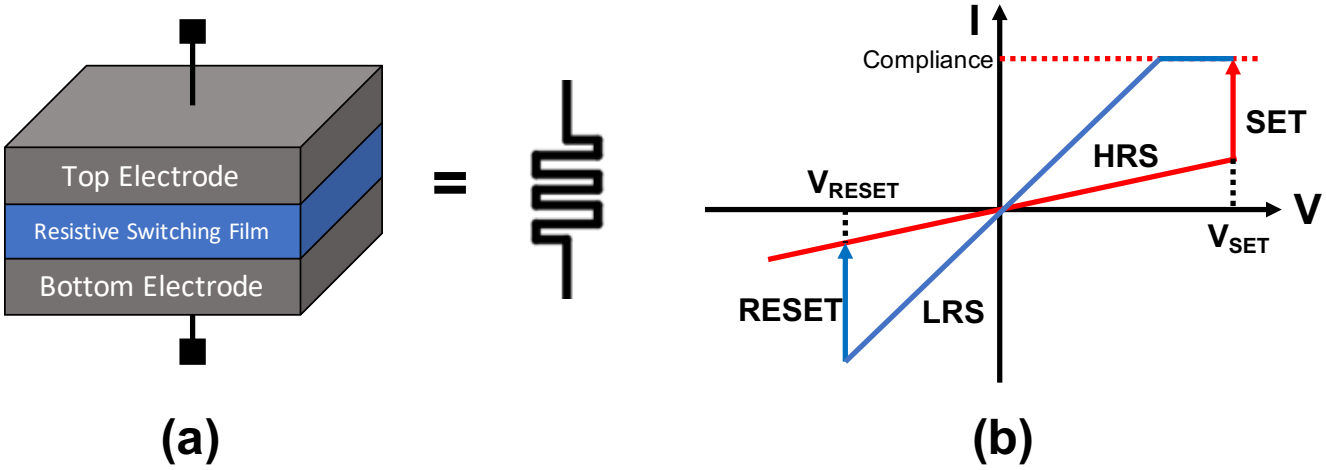


Figure 3: An RRAM device and its physical/electrical characteristics when operating in bipolar mode. (a) Device layers and electrical symbol. (b) I-V characteristic with indications of operating modes (HRS/LRS and SET/RESET).

Some examples which reported high endurance are given in Table 2.

RRAM has been studied for use in FPGAs as an SRAM replacement. An FPGA was fabricated using a 1T2R configuration with two RRAM cells having opposite resistance states to implement a voltage divider controlling a pass transistor (see Figure 4 for device operation) [29]. The device experimentally achieved a 57% smaller die area and a 28% lower energy-delay-product (EDP) than its SRAM-based counterpart. Additionally, the device had non-volatile configuration memory which enabled quick wake-up.

2.3 Integrated Thin Film Resistor (TFR)

Thin films can be deposited in the back-end-of-line to provide monolithic resistors. TFRs are commonly used in radio-frequency (RF) circuits, for which they need to have a low temperature coefficient of resistance (TCR), a measure of the rate at which resistance varies with temperature. TCR is defined as:

$$\text{TCR} = \frac{R_2 - R_1}{R_1(T_2 - T_1)} \cdot 10^{-6}$$

Above, R_1 is resistance at room temperature (Ω), R_2 is resistance at operating temperature (Ω), T_1 is room temperature, and T_2 is operating temperature.

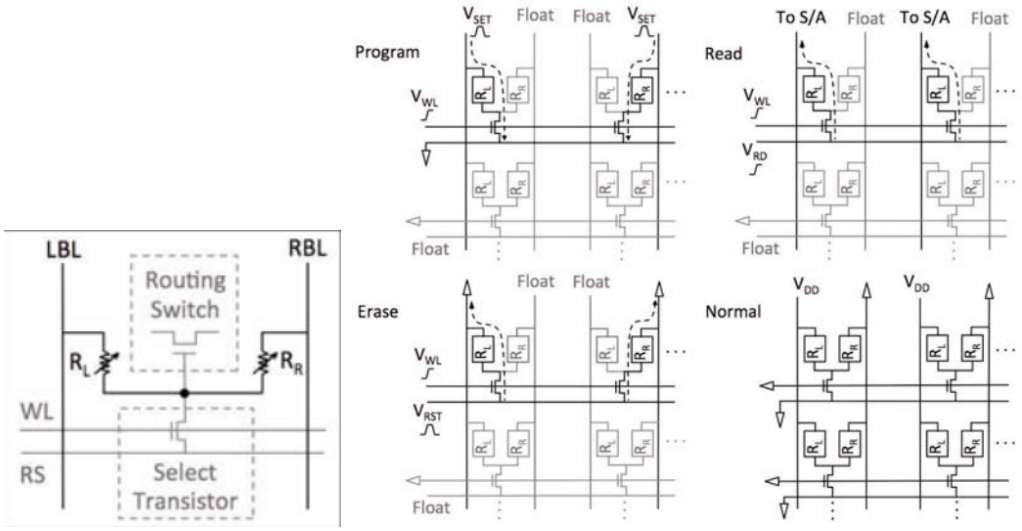


Figure 4: Adapted from [29]. (a) RRAM-based voltage divider cell design. Gray portions refer to circuit elements in the CMOS layer. (b) Schematic of four operation modes of the configuration memory.

Common options for integrated TFRs include [30]:

- **Nichrome (NiCr):** the most popular of films has the best electrical specifications in terms of absolute TCR. Common sheet resistivities are 50, 100, and 200 ohms per square.
- **Tantalum nitride (TaN_2):** when deposited and processed correctly produces an alloy which is impervious to moisture. Electrical performance not as good as nichrome. Used in applications where the resistors experience low power ($< 20\%$), no self-heating and high relative humidity (80%).
- **Silicon chrome (SiCr):** this material has a very high sheet resistivity (2000-3000 ohms per square) and is used to produce high resistances in a small area [31].

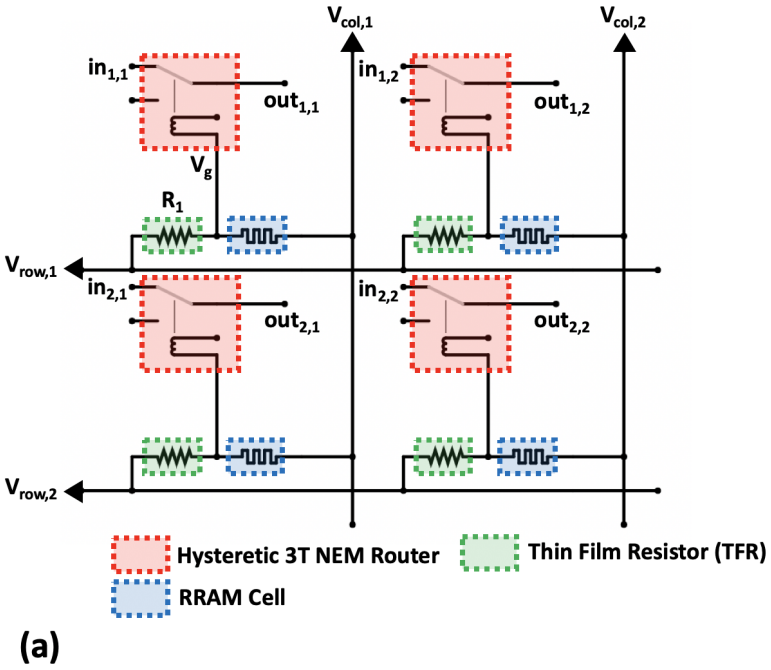
TFRs can be used to implement voltage dividers, which will be their main use in our designs.

3 Circuit design

3.1 Strategy

Here, we describe a novel architecture that uses both RRAM and NEM relays in a synergistic fashion. Ultimately, the goal is to have separate physical planes for logic and routing—the front-end-of-line (FEOL) and lower metal layers should implement the reconfigurable logic, while the upper layers in back-end-of-line (BEOL) should implement the reconfigurable routing. This design strategy mimics ASIC design in that only CLBs are implemented in FEOL and routing happens in BEOL. This paradigm should allow separate place and route of these two orthogonal elements, greatly reducing design/verification time, area overhead, and EDP. We make use of the specific device properties of both RRAM and NEM relays to enable this design—using the analog nature of the RRAM, and the sharp I-V characteristic of the NEM relay, we are able to design a 3D standard cell for a router in which the RRAM directly actuates the NEM relay with only BEOL components (no transistors).

As in [5], we use a crossbar array of hysteretic NEM relays as reconfigurable routers—however, in deciding the required device characteristics, we do take into account the effect of source voltage on the NEM relay position for 3T devices. In addition, we consider 4T devices as routers—even though these are more difficult to fabricate, they have fewer constraints on operating voltage since they are unaffected by the signals they pass. Instead of setting the NEM relay states in the crossbar fashion described in Figure 2, we have an RRAM cell that stores the NEM relay state even when the power supply is turned off. On startup, the RRAM cell's value is copied to the NEM relay (COPY mode), after which the NEM relay operates in hysteresis mode (HOLD mode). This eliminates the leakage current drawn by the RRAM cells in Figure 4. Our design does not use the same voltage divider approach taken in



Mode	Param	Value
COPY	V_{row}	V_{copy}
	V_{col}	0
HOLD	V_{row}	V_{hold}
	V_{col}	Z
SET	V_{row}	$\begin{cases} V'_{SET} = \frac{V_{SET}(R_1+R_H)}{R_H}, & \text{sel} \\ Z, & \text{unsel} \end{cases}$
	V_{col}	$\begin{cases} 0, & \text{sel} \\ Z, & \text{unsel} \end{cases}$
RESET	V_{row}	$\begin{cases} V'_{RST} = \frac{V_{RST}(R_1+R_L)}{R_L}, & \text{sel} \\ Z, & \text{unsel} \end{cases}$
	V_{col}	$\begin{cases} 0, & \text{sel} \\ Z, & \text{unsel} \end{cases}$

(b)

Figure 5: (a) 2x2 switch array using RRAM-NEM hybrid design. The difference in voltage between the row and column lines is divided using a constant resistor and the RRAM cell. The result is applied at the gate of the NEM relay which enables programmable connection between *in* and *out*. (b) Row and column voltages applied for different modes of operation. Z indicates floating, sel indicates that the row/col is selected, and unsel indicates that the row/col is unselected.

[29]. Instead of having two oppositely-programmed RRAM cells, a single RRAM cell is used, and the programming is done without a select transistor. We do not need to worry about sneak path currents, since we do not need to read the RRAM cell globally. Instead, we control the gate voltage of the NEM relay with a single RRAM cell and a constant resistor (integrated monolithically as a TFR). We control V_g such that $V_g > V_{pi}$ when the RRAM cell is in the LRS, and $V_g < V_{pi}$ when the RRAM cell is in the HRS. To SET/RESET the RRAM cell, we simply apply the SET/RESET voltage to the corresponding row of that cell and ground the corresponding column. See Figure 5 for a visual description of the architecture and the modes of operation.

3.2 Device parameters and knobs

Let us start by summarizing the device parameters:

- V_{dd}: CMOS logic supply voltage
- V_{pi}: pull-in voltage, i.e. gate voltage at which NEM relay is guaranteed to go from OFF-state to ON-state
- V_{po}: min pull-out voltage, i.e. gate voltage at which NEM relay is guaranteed to go from ON-state to OFF-state
- $V_{N,max}$: absolute maximum gate voltage for NEM relay, beyond which device failure may result
- R_L: resistance of RRAM cell in low-resistance state (LRS)
- R_H: resistance of RRAM cell in high-resistance state (HRS)
- V_{SET}: SET voltage of RRAM (positive voltage at which RRAM goes from HRS to LRS)
- V_{RST}: RESET voltage of RRAM (negative voltage at which RRAM goes from LRS to HRS)
- $V_{R,max}$: absolute maximum (positive) voltage across RRAM cell, beyond which device failure may result

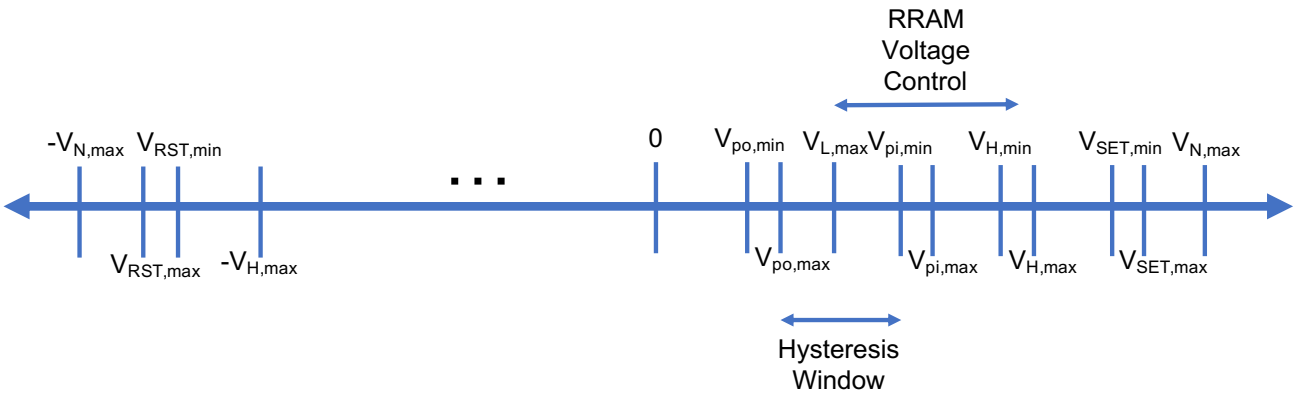


Figure 6: A number line indicating the magnitudes of different device voltage parameters relative to one another.

- $V_{R,min}$: absolute minimum (negative) voltage across RRAM cell, beyond which device failure may result
- $V_{hys,min}$: minimum NEM relay gate voltage at which the NEM relay is guaranteed to within the hysteresis window
- $V_{hys,max}$: maximum NEM relay gate voltage at which the NEM relay is guaranteed to within the hysteresis window

Our knobs are:

- V_{row}: voltage on a particular row
- V_{col}: voltage on a particular column
- R_1: counterbalancing resistor value

Now we want to determine the parameters for the case in which we implement the NEM relay with a 3T device and a 4T device. In Figure 6 number line indicates the relative positions of the different voltages and represents (some of) the relationships that need to be satisfied.

3.3 3T device constraints

Assumptions: We can assume that in COPY/SET/RESET modes that the source voltage is 0. (We cannot make this assumption during HOLD mode, so we must consider $0 \leq V_s \leq V_{dd}$)
Constraint 1: In COPY mode, NEM relay must be in ON-state when RRAM is in LRS

$$V_g = \frac{(V_{row,COPY} - V_{col,COPY})R_L}{R_1 + R_L} \geq V_{pi} \tag{1}$$

Constraint 2: In COPY mode, NEM relay must be in OFF-state and RRAM is in HRS

$$V_g = \frac{(V_{row,COPY} - V_{col,COPY})R_H}{R_1 + R_H} \leq V_{pi} \tag{2}$$

Constraint 3: In COPY mode, the voltage across the RRAM should be between the SET and RESET voltages:

$$V_{RST} \leq \frac{(V_{row,COPY} - V_{col,COPY})R_H}{R_1 + R_H} \leq V_{SET} \tag{3}$$

Constraint 4: In SET mode, the voltage across the RRAM should be between the SET voltage and the maximum RRAM voltage before device breakdown

$$V_{SET} \leq \frac{(V_{row,SET} - V_{col,SET})R_H}{R_1 + R_H} \leq V_{R,max} \tag{4}$$

Constraint 5: In SET mode, the voltage at the NEM relay gate should be less than the maximum gate voltage before device breakdown

$$\frac{(V_{row,SET} - V_{col,SET})R_H}{R_1 + R_H} \leq V_{N,max} \tag{5}$$

Constraint 6: In RESET mode, the voltage across the RRAM should be between the RESET voltage and the minimum RRAM voltage before device breakdown

$$V_{R,min} \leq \frac{(V_{row,RST} - V_{col,RST})R_L}{R_1 + R_L} \leq V_{RST} \tag{6}$$

Constraint 7: In RESET mode, the absolute voltage at the NEM relay gate should be less than the maximum gate voltage before device breakdown

$$-\frac{(V_{row,RST} - V_{col,RST})R_L}{R_1 + R_L} \leq V_{N,max} \tag{7}$$

Constraint 8: In HOLD mode, the voltage at the gate should be between $V_{hys,low}$ and $V_{hys,max}$:

$$V_{hys,low} \leq V_{row,HOLD} \leq V_{hys,max} - V_{dd} \tag{8}$$

Summary of design constraints: Constraint 8 tells us that for our 3T device, we need our hysteresis window to be at least as large as V_{dd}, otherwise we will fall outside of it for certain source voltages. We also need to make sure that we do not accidentally SET or RESET our RRAM when in COPY mode, or destroy our NEM relays when doing a SET or RESET. TODO: add device constraints for FORMing.

3.4 4T device constraints

We assume the beam is tied to ground (TODO: not for SET/RESET/FORM!). The 4T device constraints are the same as the 3T device constraints except for constraint 8, which becomes:
Constraint 8: In HOLD mode, the voltage at the gate should be between $V_{hys,low}$ and $V_{hys,max}$:

$$V_{hys,low} \leq V_{row,HOLD} \leq V_{hys,max} \tag{9}$$

This means there is no constraint on the size of our hysteresis window.

3.5 Row/col control simplification

If we tune our device parameters correctly, we can surrender our column knob as is done in Figure 5(b). By setting $V_{col} = 0$, we impose more stringent device constraints, with the benefit of having simpler column voltage controllers. The new constraint is that $R_H/R_L \geq V_{pi}/V_{po}$. The resulting row/col voltage controllers are given in Figure 7.

Ideally, we would like to use a 4T device and have the voltage levels be CMOS-compatible—this would allow us to reuse the power and ground routing for CMOS. However, if this is not possible, we can have coexisting power routing for the NEM relays in the upper metal layers.

4 Device specification

Based on the above constraints, the target application, and the device characteristics observed in literature, we develop a list of target specifications for the RRAM, TFRs, and NEM relays we would need.

4.1 TFR specification

4.1.1 Plan

Material: SiCr (high sheet resistance)
Target sheet resistance: 2000 Ω/sq.
TCR: should be ±5% for 0°C to 150°C (these are the operating conditions and ±5% should not result in too big of a voltage swing at the gate)

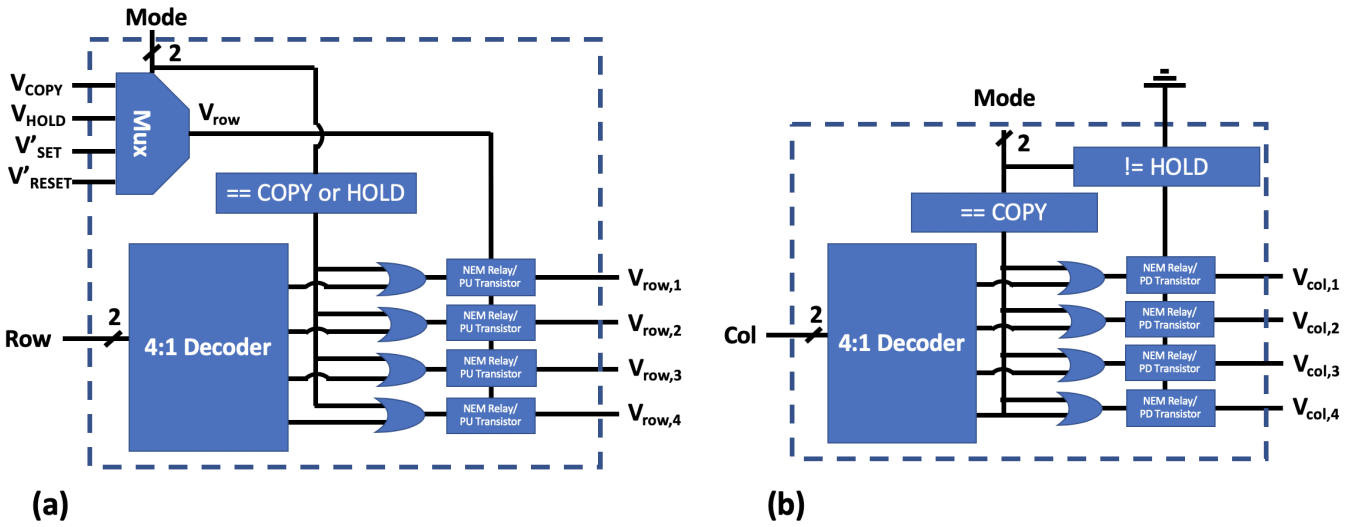


Figure 7: (a) Row voltage controller. In COPY/HOLD mode, all rows receive the same voltage. During a SET/RESET, a single row receives a voltage and the rest are floating. (b) Column voltage controller. In COPY mode, all columns are connected to ground. In HOLD mode, all columns are floating.

4.1.2 Backup 1

Material: NiCr (lower sheet resistance but still manageable with space-filling resistor)
Target sheet resistance: 200 Ω/sq.
TCR: should be ±5% for 0°C to 150°C (these are the operating conditions and ±5% should not result in too big of a voltage swing at the gate)

4.1.3 Backup 2

Material: NiCr (lower sheet resistance but still manageable with space-filling resistor at cost of increased area)
Target sheet resistance: 50 Ω/sq.
TCR: should be ±5% for 0°C to 150°C (these are the operating conditions and ±5% should not result in too big of a voltage swing at the gate)

4.2 RRAM specification

4.2.1 Plan

Material: TiN/Ti/HfO_2/TiN (available in foundry already)
Cell area: 0.01 μm^2 (100 nm side length, should be compact enough)
Speed: $<$ 1000 ns (read speed is not that important, since only happens on startup)
SET voltage: 0.8 V (almost CMOS-compatible)
RESET voltage: -0.8 V (almost CMOS-compatible)
HRS resistance: $2 \cdot 10^5$ Ω (able to match to TFR)
LRS resistance: $2 \cdot 10^4$ Ω (able to match to TFR)
Retention: $>$ 5y at RT (approximate lifetime of PLD)
Endurance: $> 10^4$ (assuming a max of 1000 writes in lifetime, should be fine)

4.2.2 Backup 1

Material: Ir/Ta_2O_5/TaO_x/TiN
Cell area: 0.01 μm^2 (100 nm side length, should be compact enough)
Speed: $<$ 1000 ns (read speed is not that important, since only happens on startup)

SET voltage: 6 V (NEM relay-compatible)
RESET voltage: -6 V (NEM relay-compatible)
HRS resistance: $2 \cdot 10^5$ Ω (able to match to TFR)
LRS resistance: $2 \cdot 10^4$ Ω (able to match to TFR)
Retention: > 5y at RT (approximate lifetime of PLD)
Endurance: $> 10^4$ (assuming a max of 1000 writes in lifetime, should be fine)

4.3 NEM relay specification

4.3.1 Plan

Device type: 4T (can operate at CMOS levels)
Material: poly-Si or Al, Pt contact (available in foundry already)
Area: 0.1 μm^2 (1 μm x 100 nm, should be compact enough)
V_{pi}**:** 0.6 V (CMOS-compatible)
V_{po}**:** 0.1 V (CMOS-compatible)
$V_{hys,max}$**:** 0.5 V (CMOS-compatible, large enough hysteresis window)
$V_{hys,min}$**:** 0.2 V (CMOS-compatible, large enough hysteresis window)
$V_{N,max}$**:** 1.1 V (CMOS-compatible, above RRAM SET voltage)
Endurance: $> 10^7$ (assuming a max of 1 million switch-ons)
R_{ds}**:** < 10 kΩ (should be much lower than transistor to get improvement)

4.3.2 Backup 1

Device type: 3T
Material: poly-Si or Al with Pt or a-C contact (BEOL compatible)
Area: 1 μm^2
V_{pi}**:** 8 V (large but still unlikely to cause problems)
V_{po}**:** 4 V (large but still unlikely to cause problems)
$V_{hys,max}$**:** 7.5 V (large but still large enough hysteresis window)
$V_{hys,min}$**:** 5 V (large but still large enough hysteresis window)
$V_{N,max}$**:** 10 V (CMOS-compatible, above RRAM SET voltage)
Endurance: $> 10^7$ (assuming a max of 1 million switch-ons)
R_{ds}**:** < 30 kΩ (should be much lower than transistor to get improvement)

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