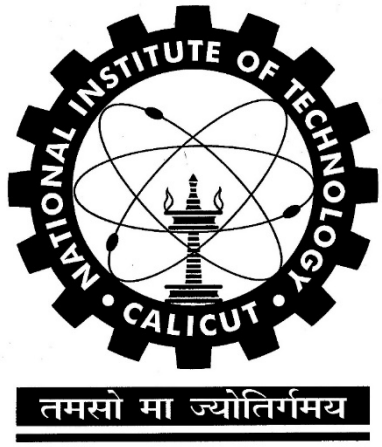
NATIONAL INSTITUTE OF TECHNOLOGY CALICUT



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL COMMUNICATION LABORATORY

EXPERIMENT NO 3

Clock Recovery From Manchester Encoded Data

Submitted by

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Aim:

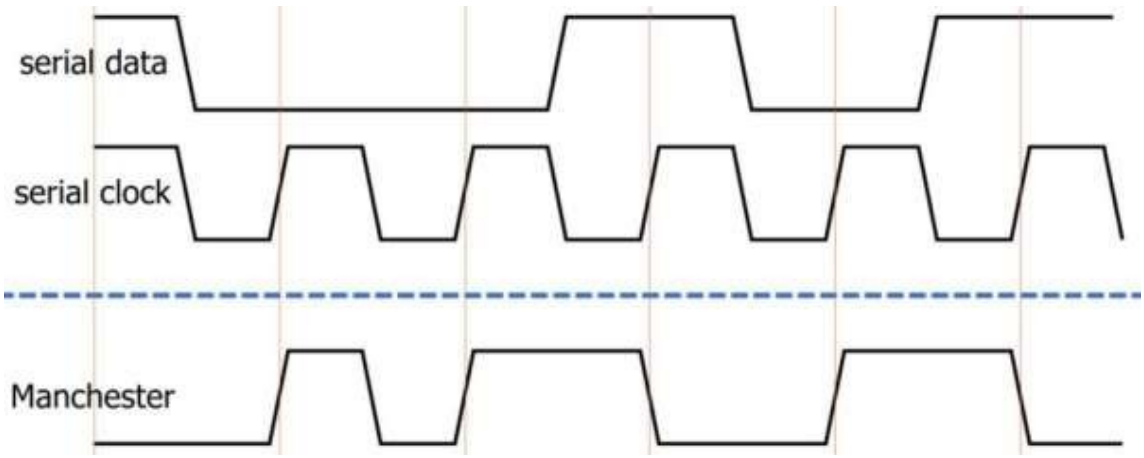
To get familiarised with Manchester Encoding and clock recovery from it and experiment it.

Theory:

Manchester encoding is a data-modulation technique that can be used in many situations but which is particularly helpful in binary data transfer based on analog, RF, optical, high-speeddigital, or long-distance-digital signals.

Despite the overwhelming advantages of standard digital communication compared to analog signaling, there are some general limitations. One is the issue of synchronization: the receiver must know when exactly to sample the incoming data. Another is the need for DC coupling. Digital data can include long, uninterrupted sequences of ones or zeros, and thus a standard digital signal used to transmit this data will remain at the same voltage for a relatively long period of time. If we attempted to AC-couple this signal using a DC-blocking capacitor, we would run into trouble since the signal decays after sometimes and reaches zero irrespective of whether the transmitted signal is one or zero. Hence it leads to ambiguity in decoding signal.

Manchester encoding offers a remedy to these two limitations. It is a simple digital modulation scheme that does two things: 1) ensures that the signal never remains at logic low or logic high for an extended period of time and 2) converts the data signal into a data-plus-synchronization signal. We can use an additional clock along with data transmitted to achieve synchronisation. But sometimes this approach is undesirable, such as when you need to minimize the number of interconnects between parts of a system, or when miniaturization demands the lowest-pincount microcontroller that can somehow provide the required functionality. In other situations, a separate clock signal is simply not an option. For example, it would be highly inefficient to include two separate RF transmitters and receivers (i.e., one for data and one for clock) in a complex wireless data link.

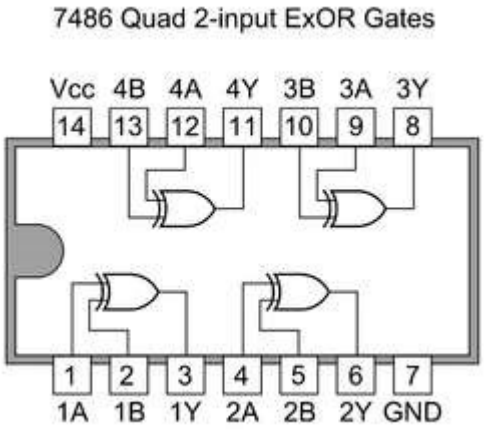


Components Required:

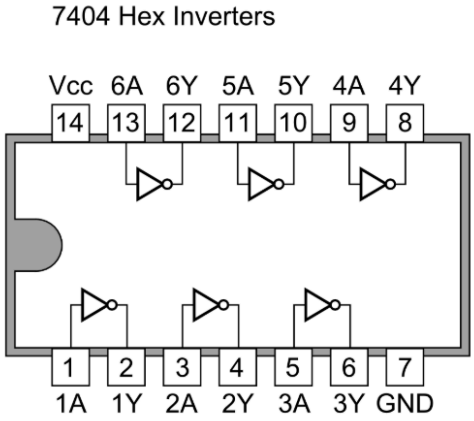
1. 7486(XOR gate)
2. 7404(NOT gate)
3. 7474(D flip flop)
4. 555 timer
5. 741 op-amp
6. Resistors
7. Capacitors

PIN Diagrams:

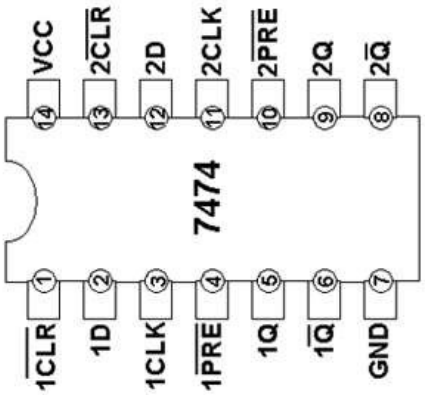
1.7486



2.7404



3.7474



Data Generation:

Data is generated using a random bit generator which comprises of array of D-Flip flops. Input to first D flip flop is XOR of 4th and 3rd delay flip flops in the array. Hence a random data is generated using D-flip flops and XOR gates.

PROCEDURE:

1.Clock of **x**Hz is given simultaneously to all D-flip flops.

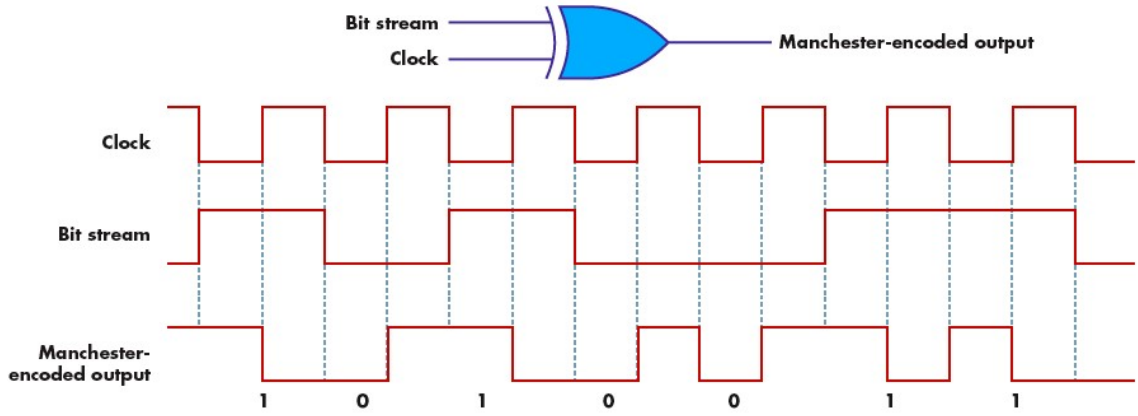
2. D-flip flops are cleared by applying LOW signal to CLR pin of all D-flip flops.

3.Then data of streams of ones and zeros are observed on oscilloscope.

Data pic

Manchester Encoding:

Manchester data encoding is typically described as the process of a logical combining of the serial data to be encoded and the clock used to establish the bit rate.



Procedure:

1. Data generated through D flip-flops is XORed with Clock signal.
2. Manchester encoded data for the generated data signal is observed on oscilloscope.

Manchester encoding pic:

Clock Recovery:

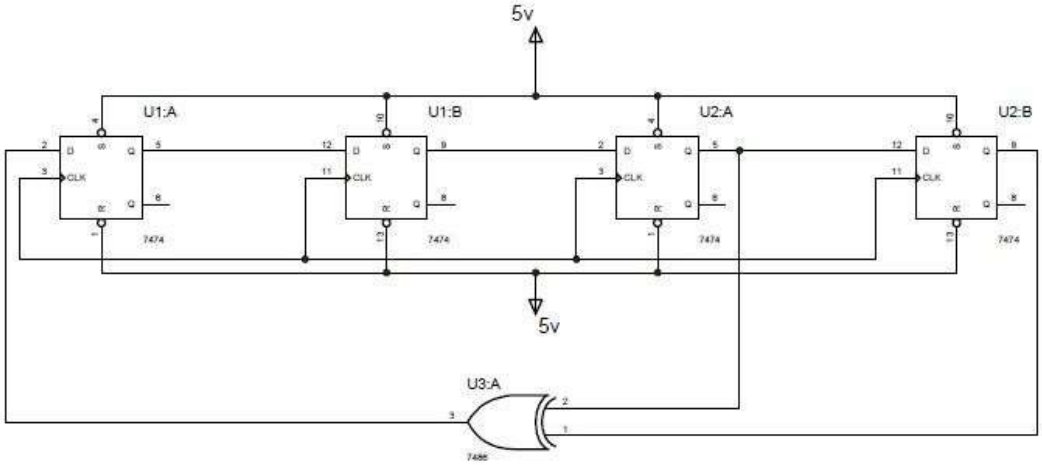
Clock recovery circuit has three stages. First the encoded data is given to a RC high pass filter which acts like a differentiator and outputs positive and negative voltage spike signals.

Then full wave rectifier circuit is used to convert positive to negative spikes and then it is given to a monostable multivibrator to generate clock signal.

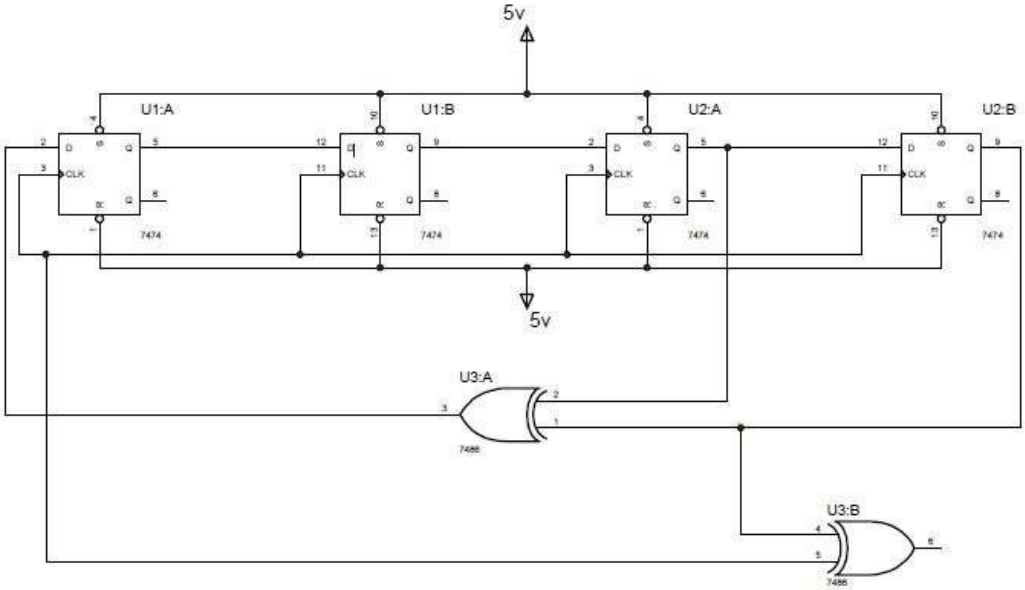
Procedure:

1. Encoded signal is inputted to high pass filter and then given to full wave rectifier.
2. Output rectified signal is observed on oscilloscope.
3. Rectified signal is given as interrupt signal monostable multivibrator and clock frequency is obtained.

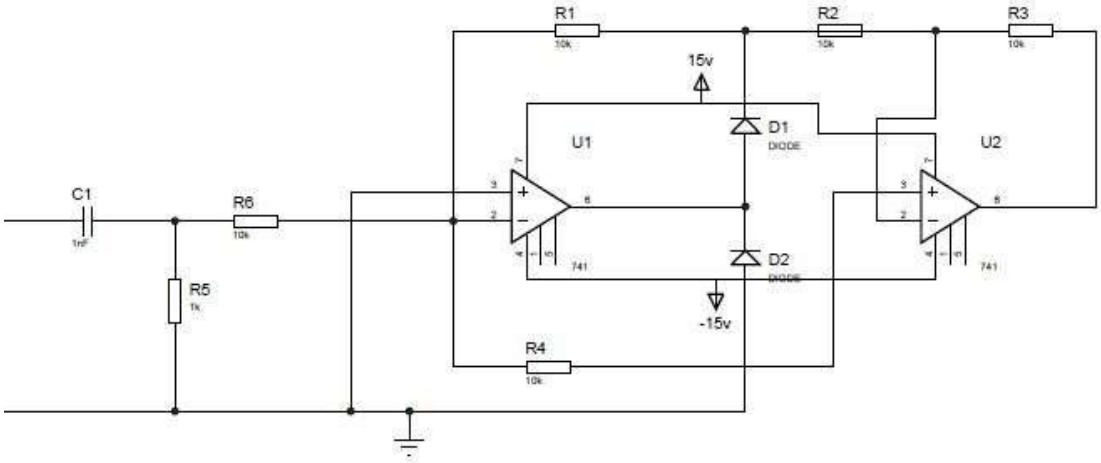
Circuit Diagrams:



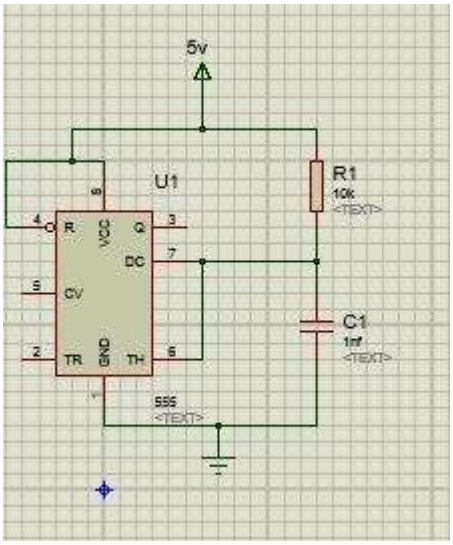
GENERATION OF MANCHESTER CODE



ENCODED MANCHESTER CODE

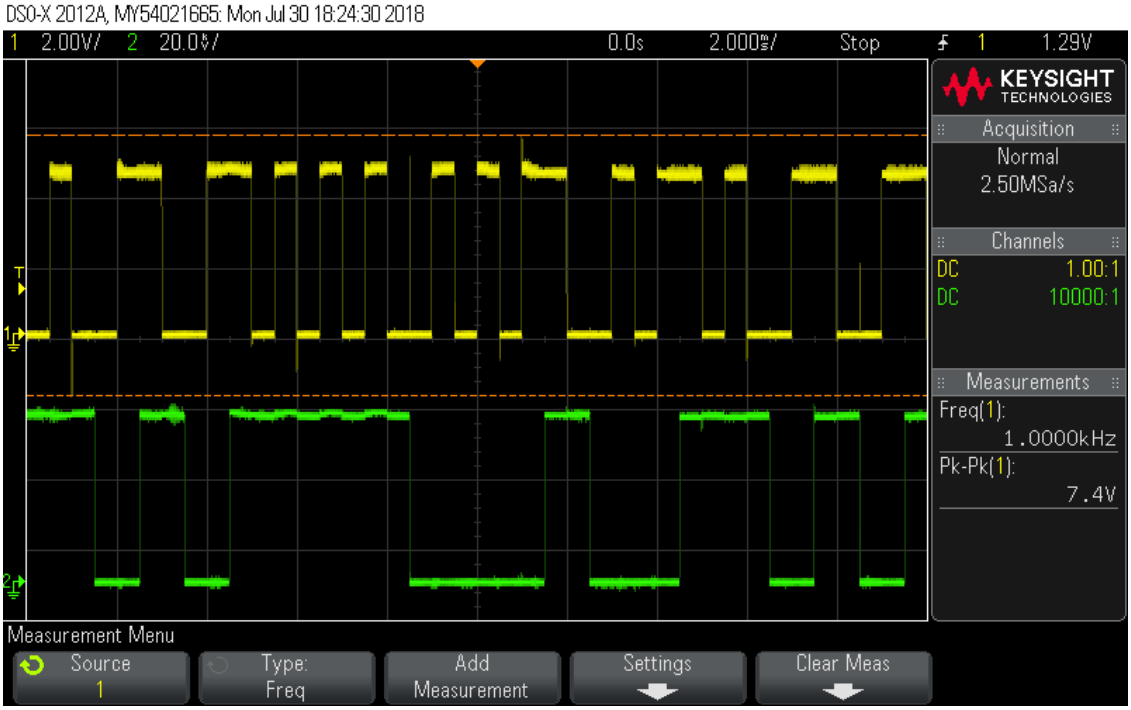


DECODING MANCHESTER CODE



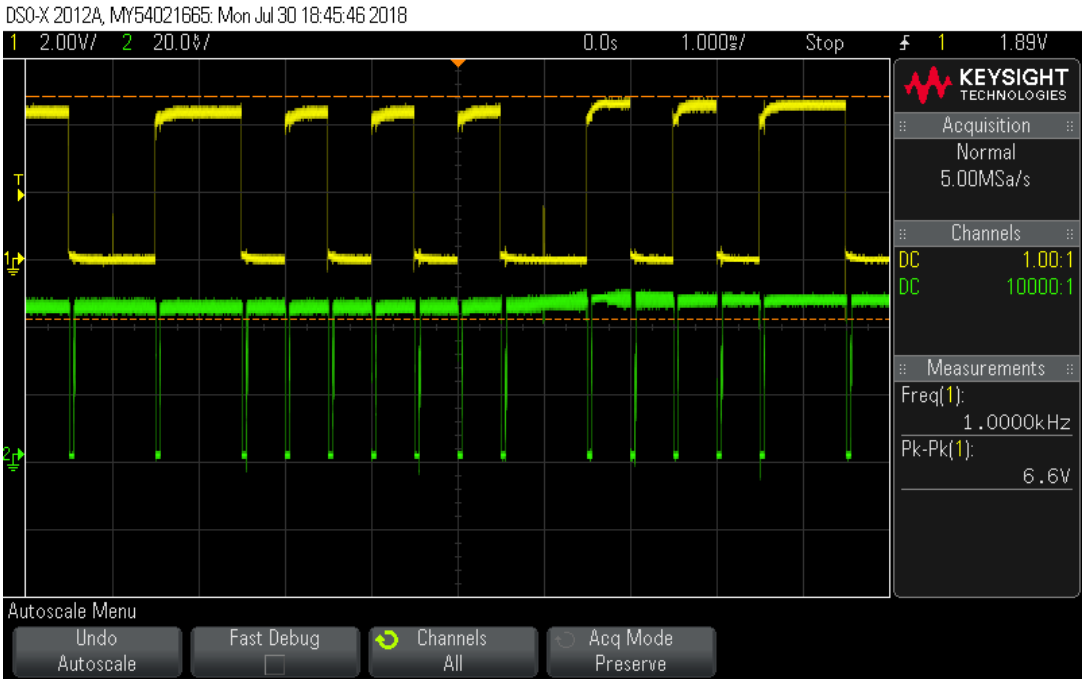
CLOCK RECOVERY CIRCUIT

GENERATED MANCHESTER CODE

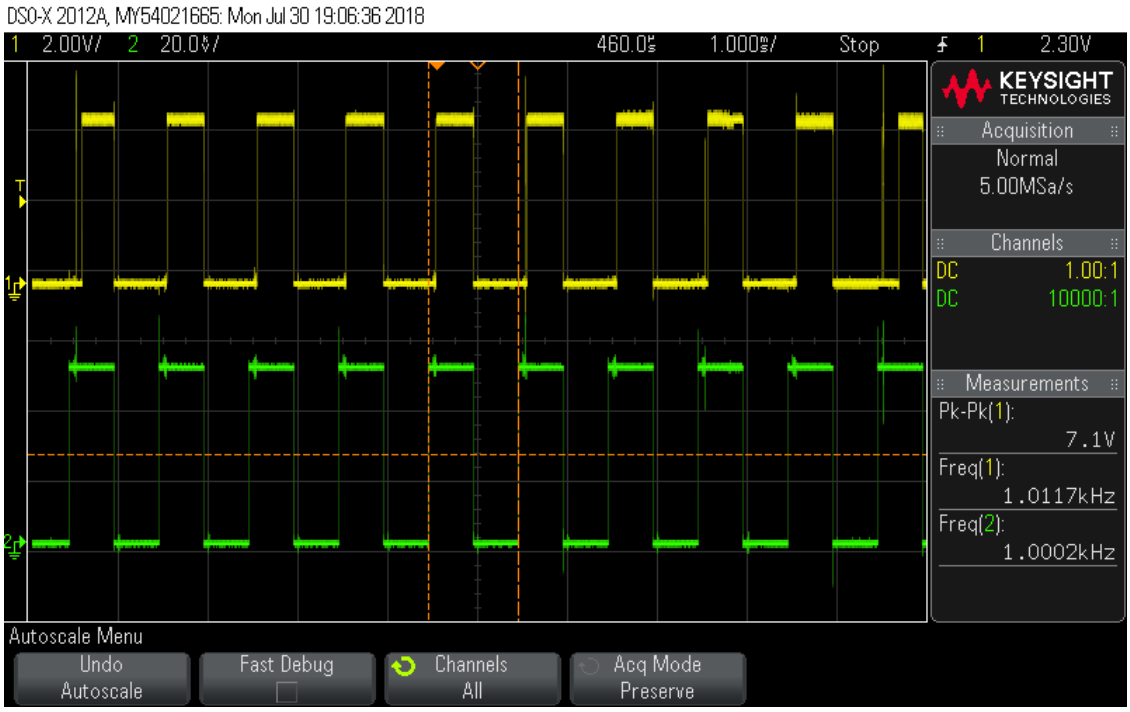


1. Signal corresponding to channel 1 is generated Manchester code.
2. Signal corresponding to channel 2 is random sequence generated from D flip flops.

OUTPUT AT FULL WAVE RECTIFIER:



OUTPUT AT 555 TIMER.



1. Signal corresponding to channel 1 is recovered clock signal.
2. Signal corresponding to channel 2 is original clock signal.

Inference:

Random data can be generated using D-flip flops. Manchester encoding can be done with XORing of data and clock signal. Since every transition in encoded signal occurs at the mid of clock signal encoded data is differentiated to get the transitions and recover clock.

Result:

Manchester Encoding is studied and realised using circuits. Advantages of Manchester encoding are understood. Clock recovery is also done from Manchester encoded signal.