Abstract:

Flash Analog-to-Digital Converters (ADCs) are essential components in high-speed data acquisition systems due to their ability to complete conversions in a single clock cycle. This makes them highly suitable for applications such as digital oscilloscopes, radar systems, and high-speed communication links. This work focuses on the design and implementation of a 3-bit Flash ADC using 90nm CMOS technology, targeting high performance, low power consumption, and compact layout. The ADC architecture is composed of a resistor ladder to generate reference voltages, a bank of seven comparators to compare the input signal with those references, and a thermometer-to-binary encoder to generate a 3-bit digital output. The ADC operates within an analog input range of 0 to 1.2V.

One of the key challenges in Flash ADC design is dealing with comparator offset, kickback noise, and input loading due to the parallel structure. To overcome these issues, dynamic latched comparators were implemented, offering faster response and lower static power compared to traditional static comparators. Input buffering was added to reduce the capacitive loading effect from the multiple comparators connected to the input node. Additionally, careful transistor sizing and layout symmetry helped minimize mismatch and offset, improving overall accuracy. The design also includes bubble error correction in the encoder logic to ensure reliable binary output even in the presence of minor glitches in comparator responses.

The complete design and simulation process was carried out using the Cadence Virtuoso design suite, utilizing the gpdk90nm process design kit (PDK). This allowed accurate modeling of the analog and digital components at the transistor level, as well as verification under various process-voltage-temperature (PVT) corners. Simulation results confirmed the functional correctness of the Flash ADC, showing sub-nanosecond conversion delay and low dynamic power consumption. The layout was optimized for minimal parasitic effects and area efficiency, with proper matching and routing techniques used to maintain signal integrity and performance.

The implemented 3-bit Flash ADC demonstrates the feasibility of high-speed, low-power analog-to-digital conversion in nanoscale CMOS technology. Its modular architecture allows easy scalability to higher resolutions by increasing the number of comparators and extending the encoder logic. Future improvements can include calibration circuits, interpolation techniques, or digital error correction to enhance resolution and linearity without significantly increasing area or power.

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CHAPTER 1
CONCEPTION OF THE PROJECT:

1.1 Introduction:

Flash Analog-to-Digital Converters (ADCs) are essential components in high-speed data acquisition systems due to their ability to complete conversions in a single clock cycle. This makes them highly suitable for applications such as digital oscilloscopes, radar systems, and high-speed communication links.

This critical function is performed by Analog-to-Digital Converters (ADCs), which act as indispensable interfaces between the continuous analog environment and discrete digital processing units. As the demand for high-speed and low-power data conversion continues to grow across a range of applications, from telecommunications and medical imaging to automotive electronics and portable devices, the performance of ADCs has become a key determinant of overall system efficiency.

Among the various ADC architectures—such as pipelined, successive approximation register (SAR), sigma-delta, and flash—the Flash ADC is distinguished by its ultra-fast conversion capability. Leveraging a fully parallel processing structure, Flash ADCs compare the input signal against a set of reference voltages simultaneously using an array of comparators. The resulting outputs are encoded into binary form within a single clock cycle, making this architecture ideally suited for time-critical and high-frequency applications.

Despite its speed advantages, the conventional Flash ADC architecture poses several challenges. The number of required comparators increases exponentially with resolution, leading to substantial power consumption, larger chip area, and layout complexity. Moreover, analog imperfections such as comparator offset, input capacitance, and resistor mismatch become more pronounced with technology scaling, adversely affecting conversion accuracy and power efficiency.

To address these limitations, recent design innovations have focused on improving power and area efficiency through techniques such as low-power comparator designs, optimized resistor ladder configurations, and layout-aware architecture planning. Furthermore, with the limitations of analog scaling in advanced CMOS technologies, digitally-assisted calibration techniques have become increasingly important. These methods enable the correction of comparator mismatches and other analog non-idealities through post-processing, thus allowing for improved performance without excessively complex analog circuitry.

1.2 Motivation:

In real-time electronic systems, such as biomedical signal monitoring, radar processing, and high-speed communication, rapid and accurate analog-to-digital conversion is essential for reliable system performance. The Flash ADC, with its parallel architecture, is well-suited for such applications due to its extremely fast conversion time. Our motivation for designing a 3-bit Flash ADC lies in understanding how this architecture can be applied to real-time data acquisition where speed is critical. By implementing the design using the Cadence design suite and 90nm CMOS technology, we aimed to optimize key performance parameters such as speed, power efficiency. The project allowed us to address practical design challenges like comparator offset, power dissipation, and input loading, thereby enhancing the ADC's suitability for integration into larger real-time processing systems. This work not only serves as a fundamental building block for high-speed ADC systems but also offers insights into how analog designs can be optimized for modern, low-power, and high-performance applications.

1.3 Literature Survey:

Sn No	Author Name	Research paper title	Summary
01.	Channakka Lakkannavar Department of E&CE SDMCET,Dharwad Shrikanth K. Shirakol Department of E&CE SDMCET,Dharwad Kalmeshwar N. Hosur Department of E&CE SDMCET ,Dharwad Year of publish: July 2012	Design,implementation and analysis of flash adc architecture with differential amplifier as comparator using custom design.	This paper presents a 4-bit Flash ADC designed using 180nm CMOS technology with a differential amplifier-based comparator to enhance noise immunity. Implemented in Cadence Virtuoso, the design includes a resistor string, 15 comparators, and a priority encoder, converting 0–1.8V analog input to digital output. The ADC achieves 3.8 GS/s speed, 49.94 mW power dissipation, and 25.84 dB SNR, occupying 0.82 μm^2, making it suitable for high-speed, low-resolution applications.
02.	Harisha Department of ECE NMAMIT, Nitte Karnataka, India Satheesh Rao Department of ECE NMAMIT, Nitte Karnataka, India Year of publish:2017	Design of 3-bit Flash ADC using Inverter Threshold Comparator in 45 nm CMOS Technology.	This paper presents a low-power, compact 3-bit Flash ADC using 45nm CMOS technology, featuring an Inverter Threshold Comparator (ITC) to replace traditional comparators and eliminate the resistor ladder. Designed in Cadence with gpdk45nm, the ADC operates at 1.1V with a 100kHz input and includes a binary encoder using Transmission Gate (TG) and Pass Transistor Logic (PTL) to minimize transistor count. Simulation results confirm accurate conversion with no missing codes, achieving average power consumption of 588.9nW (TG) and 587.3nW (PTL), and transistor counts of 44 and 36, demonstrating the design's efficiency for low-power applications.

03.	Aditi Kar Department of ETCE Tripura Institute of Technology, Agartala Alak Majumder; Abir Jyoti MandaI; Nikhil Mishra Department of ECE National Institute of Technology, Arunachal Pradesh Year of publish:2015	Design of Ultra Low Power Flash ADC using TMCC & Bit Referenced Encoder in 180nm Technology.	This paper presents a high-speed, low-power 3-bit Flash ADC using a Two-Stage Multiplying Current Conveyor (TMCC) amplifier to reduce power consumption. Implemented in 90nm CMOS using Cadence Virtuoso, the ADC operates at 2.5 Gsps with a power consumption of just 3.4 µW. The TMCC-based comparator design enables significant energy savings while maintaining high-speed performance, making it ideal for portable and wireless communication systems.
04.	Priyanka Dhage and Pradnya Jadhav Year of publish:2017	Design of Power Efficient Hybrid Flash-Successive Approximation Register Analog to Digital Converter.	This paper presents a hybrid ADC combining Flash and SAR architectures for high-speed, low-power operation. Featuring a segmented capacitive DAC and multiplexers to reduce comparator count, the design is implemented in 90nm CMOS and operates at 190 MS/s with 880 µW power consumption—33% lower than conventional designs. It balances Flash speed with SAR efficiency, reducing area and cost while ensuring robust performance across PVT variations, making it ideal for wireless and portable applications.

1.4 Problem Statement:

Design and Implement an efficient ADC architecture that minimizes power consumption and propagation delay. The focus is on optimizing the critical components of the ADC—such as comparators, reference ladder, and encoder—to achieve fast and low-power analog-to-digital conversion suitable for integration in power-constrained and high-speed digital systems.

1.5 Objectives:

- Study and analyze ADC design, its architecture, and functionality.
- Design and implement a basic ADC architecture.
- Optimize the ADC power efficiency and reduced Power-Delay Product (PDP).
- Performance and comparative analysis using key metrics against existing ADC designs.

1.6 Working:

Input Signal and Sampling:

The analog input voltage (Vin) passes through a Sample and Hold (S/H) circuit, which samples the input signal on a clock edge (clk) and holds it steady for a short period. This ensures that the signal is stable during conversion.

Reference Voltage Division:

The circuit uses a resistor ladder network (vertical column of resistors) to divide the reference voltage into a series of evenly spaced levels.

These reference voltages are applied to the inverting inputs of seven comparators.

Comparator Array:

Each of the seven comparators compares the sampled analog input with its corresponding reference voltage.

If the input voltage is higher than a given reference level, the corresponding comparator outputs a high value (1); otherwise, it outputs low (0).

This forms a thermometer code — a pattern of continuous 1s followed by 0s, based on how many reference levels the input has exceeded.

Inverters (Buffers):

The outputs of the comparators are passed through inverters. This may serve to buffer or sharpen the signal before sending it to the encoder.

Encoder Block:

The encoder receives the 7-bit thermometer code and converts it into a 3-bit binary output.

This output (labelled as Y1, Y2, and Y3) represents the digital equivalent of the analog input voltage.

1.7 Areas of Application:

1. **High-Speed Data Acquisition Systems**
Used in oscilloscopes, logic analyzers, and RF receivers where ultra-fast conversion is required.

2. **Wireless Communication Systems**
Essential in ADCs for RF front ends in 4G/5G receivers and software-defined radios due to low latency and high-speed requirements.

3. **Digital Sampling Oscilloscopes**
Flash ADCs enable real-time, high-resolution waveform capture in test and measurement equipment.

4. **Radar and Imaging Systems**
Applied in military and automotive radar systems for fast analog-to-digital conversion of reflected signals.

5. **Ultra-Fast Video and Display Interfaces**
Used in high-resolution camera systems and video digitizers where speed is prioritized over power and area.

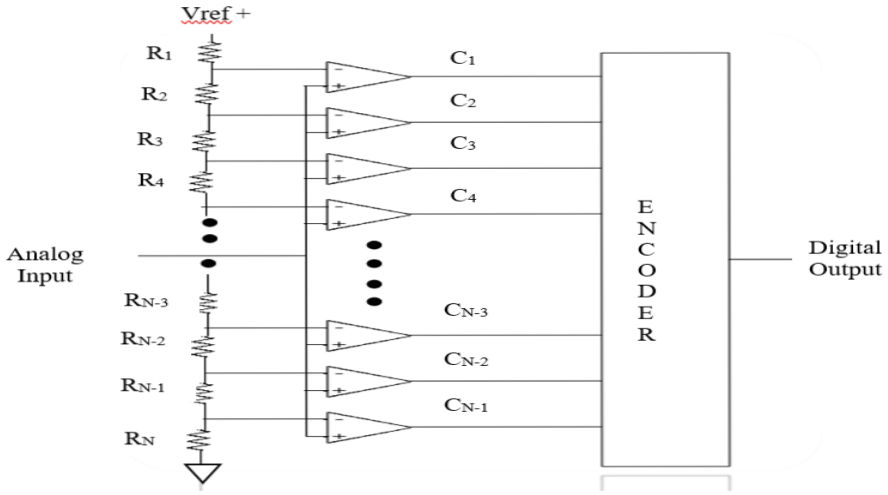
6. **Control Systems for High-Speed Industrial Automation**
Real-time conversion is crucial in applications such as servo motors, robotics, and automation controllers.

7. **Data Conversion in Mixed-Signal ICs**
Often used as a building block in mixed-signal ASICs or SoCs for applications requiring high-speed ADC front ends.

8. **Flash LiDAR Systems**
Used in autonomous vehicles and drones for fast sampling of analog returns from laser pulses.

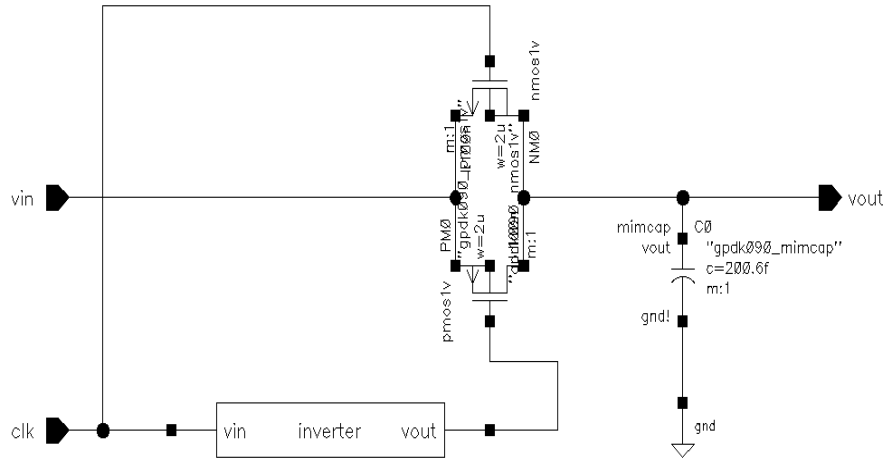
CHAPTER 2
DESIGN METHODOLOGY:

2.1 FLASH ADC ARCHITECTURE



A Flash ADC consists of a resistive ladder network, an array of comparators, a priority encoder, and a stable reference voltage source. The resistive ladder divides the reference voltage (Vref), provided by a voltage regulator, into a set of equally spaced voltages that serve as thresholds for the comparators. Each comparator compares the analog input voltage (Vin) to one of these reference levels; when Vin exceeds a given reference, the corresponding comparator outputs a high signal. As Vin increases, more comparator outputs switch to high in sequence. These outputs are fed into a priority encoder, which identifies the highest-order active comparator and generates the corresponding binary code, effectively converting the analog input into a digital output.

2.2 SAMPLE AND HOLD

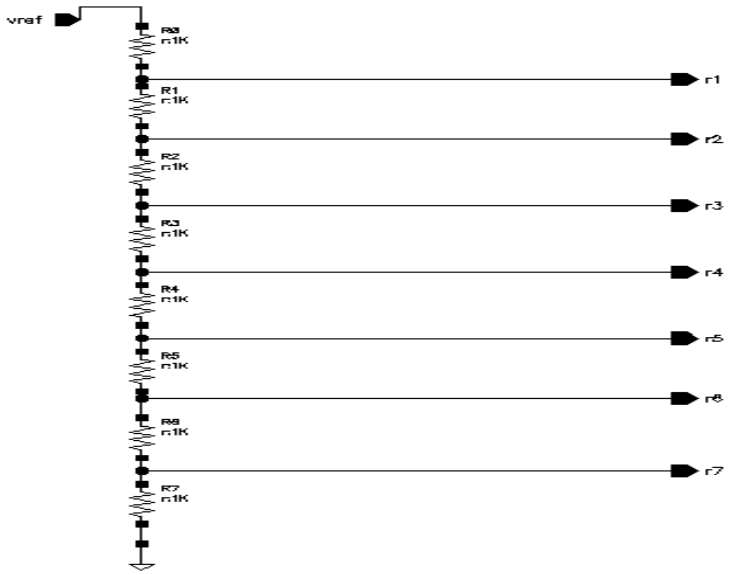


The Sample and Hold (S/H) circuit used in the proposed 3-bit Flash ADC is implemented using a CMOS transmission gate configuration, as shown in Fig. 2. This design leverages the complementary switching behavior of NMOS and PMOS transistors to efficiently sample the analog input. A clock-controlled NMOS-PMOS pair acts as the switch, with the NMOS gate driven by the clock signal and the PMOS gate controlled by its logical complement generated through an inverter. This ensures proper conduction over the full input voltage range.

During the sampling phase, when the clock signal is high, the transmission gate turns ON, allowing the analog input voltage (vin) to charge the holding capacitor. The capacitor value is 200.6 fF, chosen for its high linearity and minimal leakage characteristics. This capacitor stores the instantaneous voltage level during the hold phase. Once the clock transitions to a low state, both transistors turn OFF.

The sizing of the transistors is optimized for performance, with both NMOS and PMOS devices designed with a channel width of 2 µm to reduce on-resistance and ensure rapid charge acquisition. The overall layout achieves a trade-off between speed, accuracy, and silicon area. Simulation results confirm that the circuit maintains minimal voltage droop and negligible hold-step error, demonstrating stable operation during both sampling and holding periods. This circuit serves as a reliable interface, ensuring accurate voltage representation at the input of the comparator array in the Flash ADC architecture.

2.3 THE RESISTOR STRING



A resistor ladder in a flash ADC is made up of a chain of resistors with identical resistance values, connected between a reference voltage (Vref) and ground. This network produces a series of evenly spaced voltage levels. These voltages serve as reference points for the comparators in the ADC. Each comparator compares the input analog voltage against one of these predefined levels. For an N-bit flash ADC, the ladder consists of 2^N resistors, creating 2^N - 1 intermediate nodes, which act as reference voltages for comparison.

$Va = (M*Vref)/2^N$

M stands for the number of resistors where the voltage is divided.

N is the number of bits used in the system.

The total number of resistors needed is 2 to the power of (2^n).

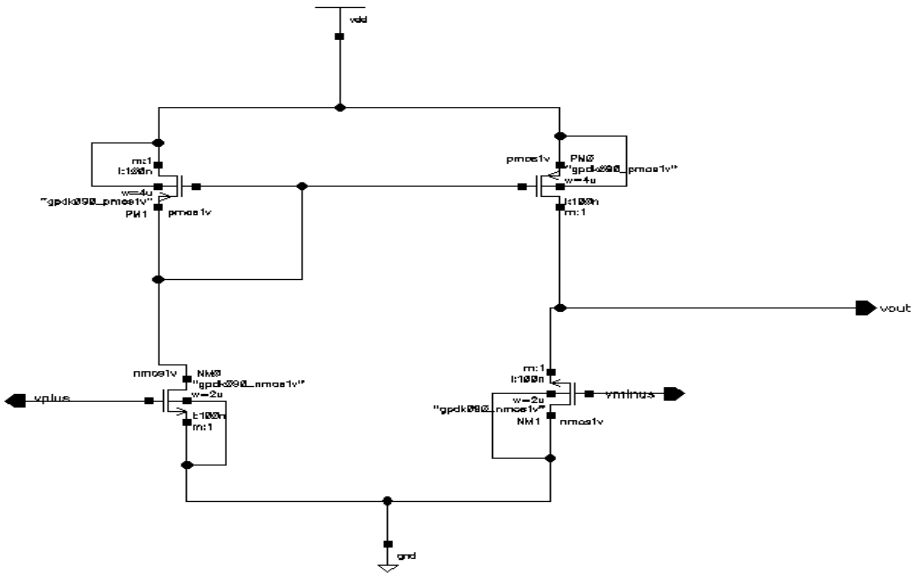
The Table 1 shows the voltage division for resistor string with reference voltage is taken to be 0.9V.

Table I: Voltage division occurs as follows

M*	**Va = (M*Vref)/2^N**
M=1	0.1125V
M=2	0.225V
M= 3	0.3375V
M=4	0.45V
M=5	0.5625V
M=6	0.675V
M=7	0.7875V
M=8	0.9V

M* =resistor tap Number and Va=Voltage of each resistor tap

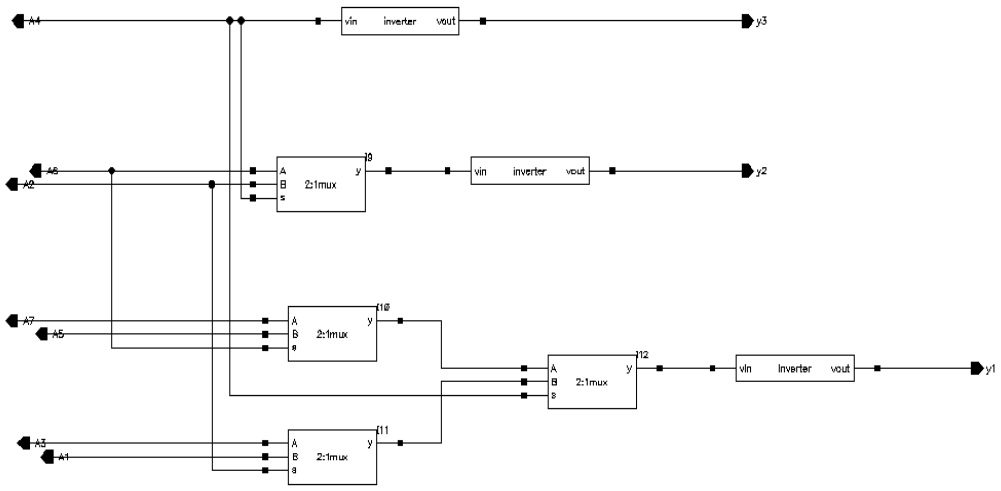
2.4 THE COMPARATOR



In a Flash ADC architecture, the comparator serves as the fundamental building block responsible for determining the digital equivalent of the input analog signal. Its primary function is to compare the analog input voltage (Vin) against a predefined reference voltage (Vref) and generate a corresponding binary output. When Vin exceeds Vref, the comparator outputs a logical high ('1'); otherwise, it produces a logical low ('0'). This decision-making process enables the generation of a thermometer code, which forms the basis for subsequent digital encoding.

For an N-bit Flash ADC, a total of 2^N - 1 comparators are required to create 2^N quantization levels. In the implemented 3-bit design, seven comparators are deployed, each receiving a unique reference voltage derived from a resistor ladder network. These comparators operate simultaneously and in parallel, ensuring high-speed performance.

2.5 ENCODER



The encoder module is designed to convert the thermometer-coded output from the comparator array into its binary equivalent. In the proposed architecture, the encoder receives seven input signals (A1–A7) generated by a static comparator array, which produces complementary thermometer codes. To perform this conversion, the design employs a logic structure based on 2:1 multiplexers. Specifically, the encoder utilizes multiplexers implemented with Transmission Gate (TG) logic, chosen over Pass Transistor Logic (PTL) due to trade-offs involving transistor count and output signal integrity. The encoding logic is derived from a truth table that maps the thermometer code inputs to corresponding 3-bit binary outputs (Y1, Y2, Y3). The logic expressions for each output bit are minimized and structured to ensure that only the highest active input influences the final binary result. This implementation achieves a compact and power-efficient design, providing accurate code conversion essential for high-speed ADC performance.

Table II. Truth table of the encoder

A7	A6	A5	A4	A3	A2	A1	Y3	Y2	Y1
0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	1	1	1	0
0	0	0	0	0	1	1	1	0	1
0	0	0	0	1	1	1	1	0	0
0	0	0	1	1	1	1	0	1	1
0	0	1	1	1	1	1	0	1	0
0	1	1	1	1	1	1	0	0	1
1	1	1	1	1	1	1	0	0	0

CHAPTER 3
IMPLEMENTATION AND RESULT OF THE PROJECT:

3.1 SOFTWARE TOOLS :

Cadence is a leading provider of Electronic Design Automation (EDA) tools that enable engineers to design, simulate, and verify complex integrated circuits and electronic systems. Its comprehensive suite includes tools like Virtuoso for analog and mixed-signal design, Spectre for circuit simulation, Innovus for digital implementation, and Allegro for PCB design. These tools are widely used in the semiconductor and electronics industries to streamline the development of high-performance, low-power chips and boards. Cadence solutions support the entire design cycle, from concept to silicon, helping accelerate innovation in areas such as AI, 5G, automotive, and IoT.

3.2 SIMULATION RESULTS:

This section presents the simulation results of the four primary components of the 3-bit Flash ADC: the Sample and Hold circuit, Resistor string, Comparator array, and Encoder. The design and simulation work was carried out using the Cadence Virtuoso platform to validate the functional performance of each block.

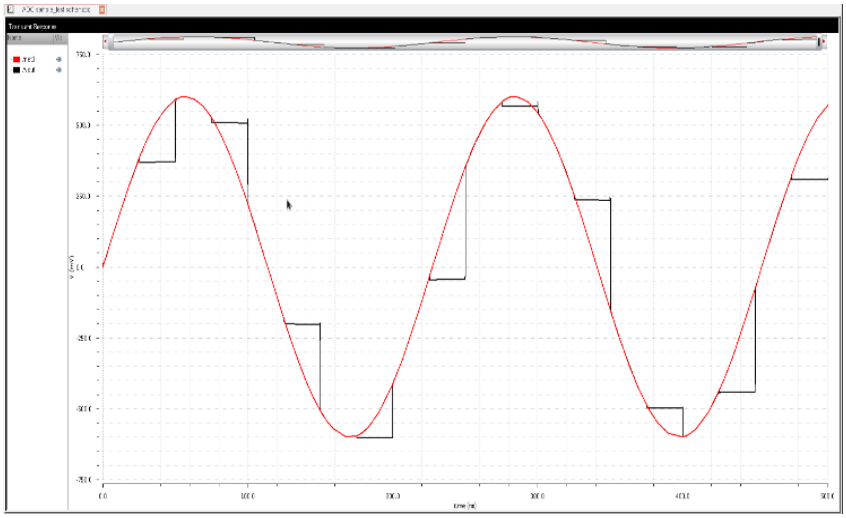


Fig.6 : Transient response of sample and hold

Fig.6 : illustrates the transient response of the complete 3-bit Flash ADC system. The red waveform represents the analog input signal, while the staircase-shaped black waveform shows the corresponding quantized digital output. As observed, the output levels change in discrete steps, accurately tracking the input signal within defined voltage ranges.

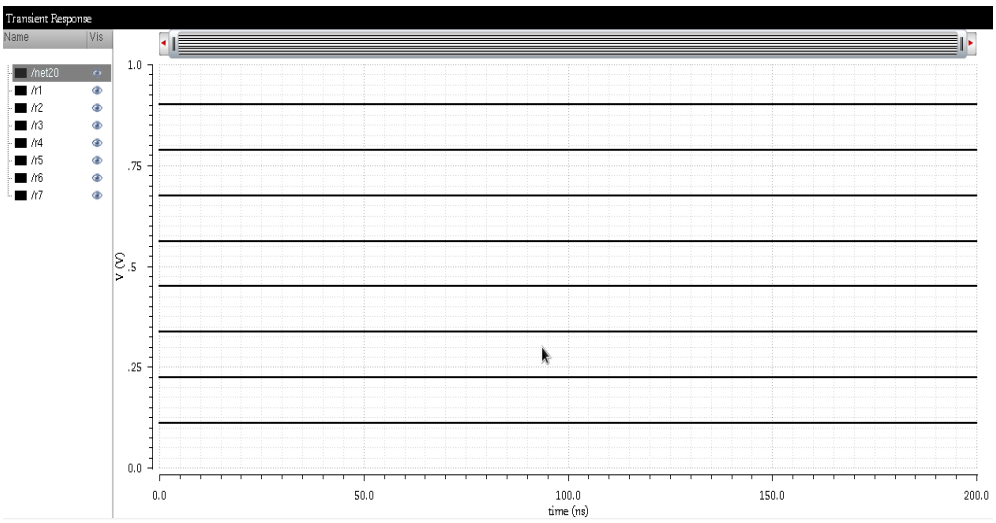


Fig.7 : Transient response of Resistor string

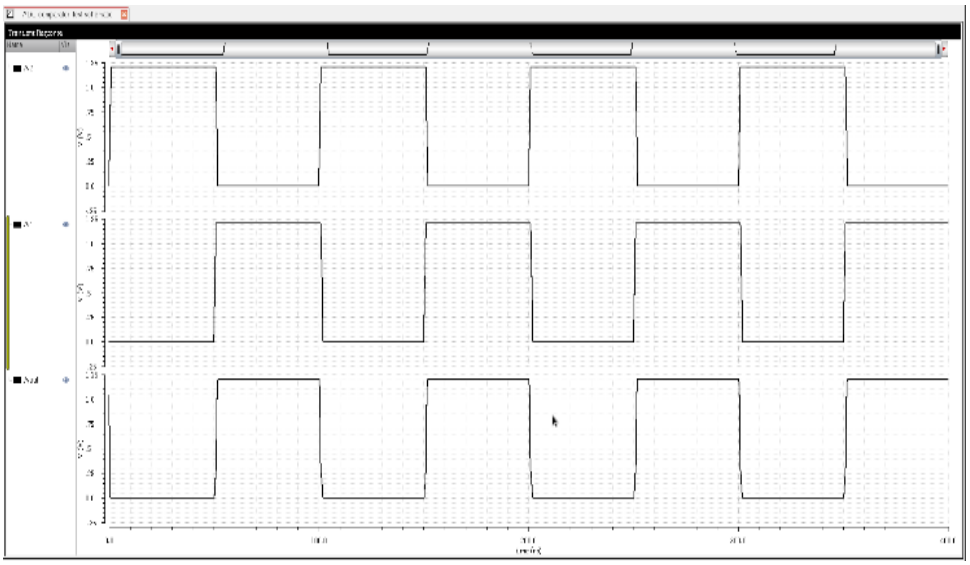


Fig.8 : Transient response of comprator

Fig.8:demonstrates the transient behavior of the comparator used in the Flash ADC design. The waveform indicates the comparison between two input voltages, labeled V1 and V2. When V1 exceeds V2, the comparator output transitions to a logic high state (‘1’), and when V1 is less than V2, the output drops to a logic low state (‘0’). For instance, during the time interval from 0 ns to 50 ns, V1 < V2, resulting in a low output. Conversely, in the interval from 50 ns to 100 ns, V1 >V2, producing a high output.

Fig.9 : Transient response of encoder

In Fig.9: signals labeled A1 to A7 represent the thermometer code inputs to the encoder, which are typically the outputs of comparators in a flash ADC. The bottom three waveforms labeled Y1, Y2, and Y3 represent the binary output of the encoder.

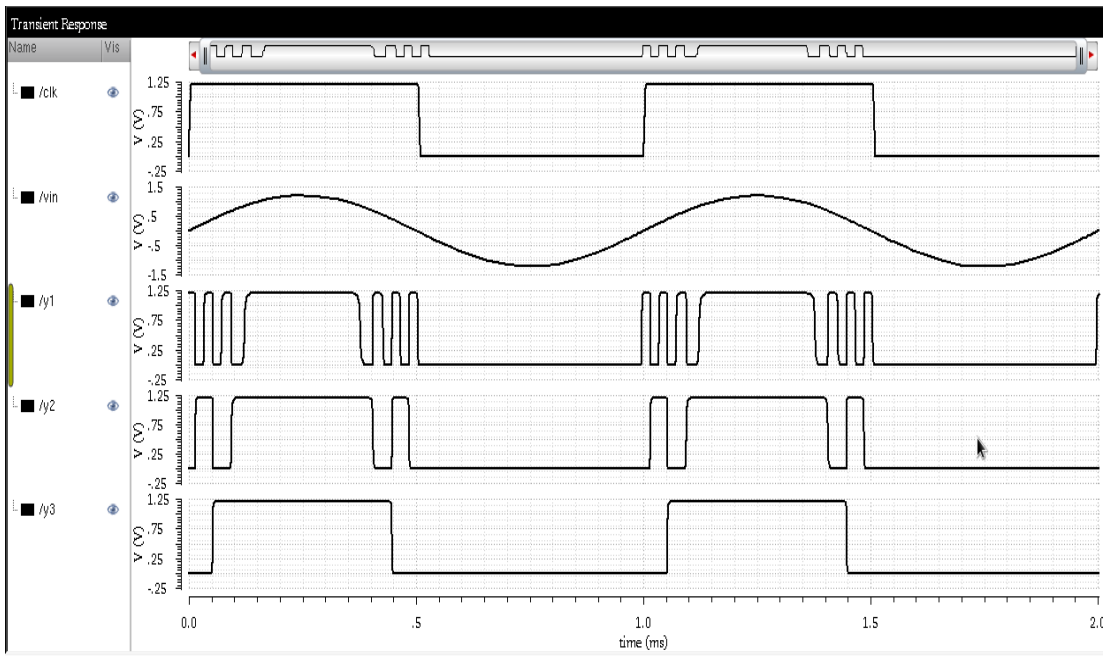


Fig.10 : Transient response of Flash ADC

Fig.10: shows outputs for analog input of 0 to 0.9V and 1K Hz input frequency using sample and hold circuit.

3.3 Performance Analysis

Table III. Specifications summary of ADC

Technology	90nm
Analog voltage, Vin	0-1.2V
Reference voltage, Vref	0.9V
Vdd	1.2V
Resolution	3-bits
Delay	363.7us
Power Dissipation	3.68mW

The table provides specifications for an ADC designed with 90nm technology. The ADC operates with an input voltage range of 0-1.2V, a reference voltage of 0.9V, and a supply voltage of 1.2V. It has a 3-bit resolution, meaning it can represent the input signal in 8 levels. The conversion delay is 363.7 microseconds, and it consumes 3.68 milliwatts of power. These specifications define the ADC's performance in terms of voltage range, resolution, speed, and power consumption.

CHAPTER 4

CONCLUSION:

The 3-bit Flash ADC architecture designed using a Sample-and-Hold circuit, resistor string, static comparators, and a MUX-based encoder offers a simple and power-efficient solution for low-resolution data conversion. The resistor string provides accurate and evenly spaced reference levels, while static comparators minimize power by avoiding clocked switching. The MUX-based encoder reduces digital logic complexity and ensures reliable output decoding. Although the design does not target high-speed operation, it effectively meets the requirements for low-power, low-speed environments where area and energy efficiency are more critical than fast conversion rates.

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