Digital Logic Design Assignment 10 - EC2016-17

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1 Question

Assume that all the digital gates in the circuit shown in the figure are ideal, the resistor $R = 10\ k\Omega$ and the supply voltage is $5\ V$. The D flip-flops D_1, D_2, D_3, D_4 and D_5 are initialized with logic values 0, 1, 0, 1 and 0, respectively. The clock has a 30% duty cycle.

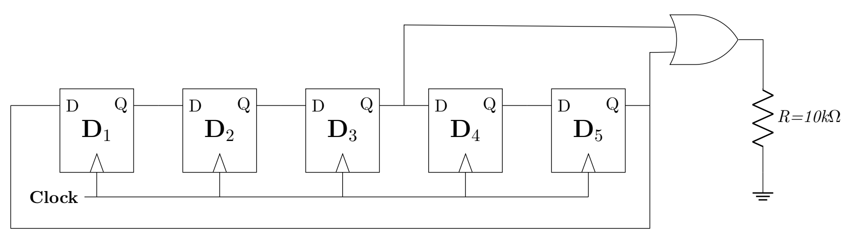

Figure 1: *Question figure*

The average power dissipated (in mW) in the resistor R is ________

2 Solution

Let the output waveform be represented by Y. Then, we can infer from the question figure that

$$Y = Q_3 + Q_5 \tag{1}$$

2.1 Truth Table

Clk	$\mathbf{Q}_1$	$\mathbf{Q}_2$	$\mathbf{Q}_3$	$\mathbf{Q}_4$	$\mathbf{Q}_5$	$\mathbf{Y = Q_3 + Q_5}$
0	0	1	0	1	0	0
1	0	0	1	0	1	1
2	1	0	0	1	0	0
3	0	1	0	0	1	1
4	1	0	1	0	0	1
5	0	1	0	1	0	0

Table 1: *Truth Table for the Circuit Diagram given in the Question Figure*

Now, using the truth table, we can make the timing diagram as given on the next page.

2.2 Timing Diagram

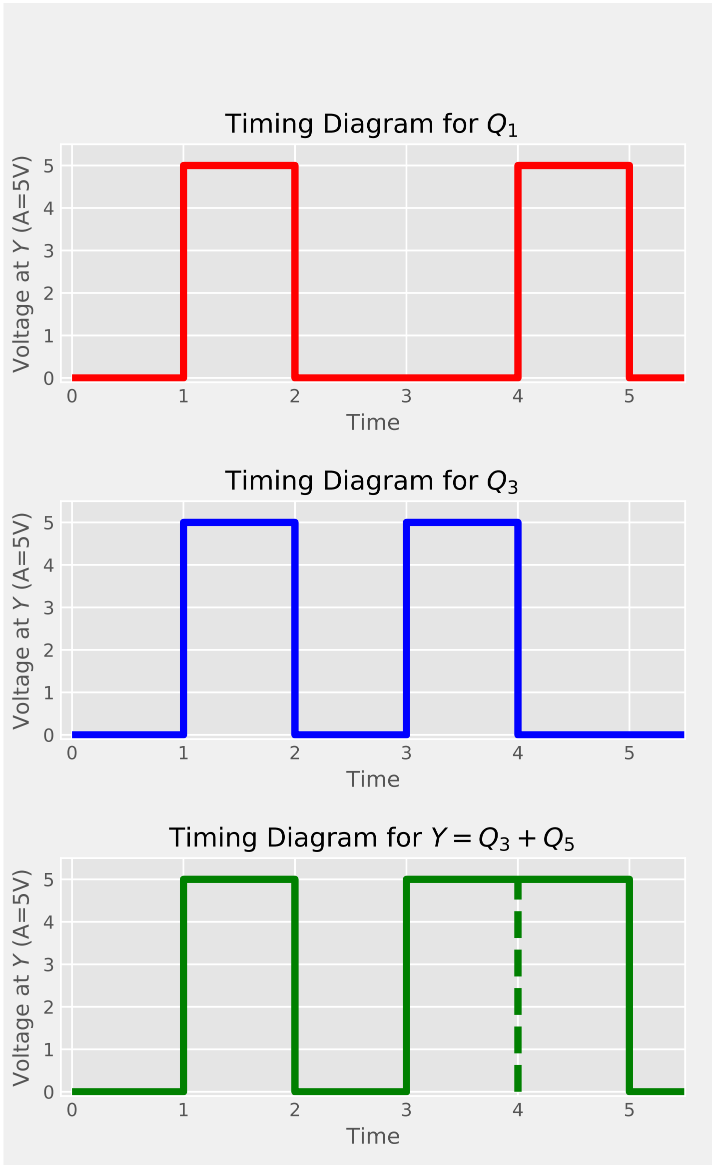

Figure 2: *Timing Diagram for the Circuit Diagram given in the Question Figure*

Here, the time 0 to 5 represent five time periods of the clock. From the timing diagram for Y, we can see that out the output voltage is non-zero for 3 time periods.

We can thus calculate the average power over time using the general formula:

$$Average\ power\ dissipated = P_{avg} = \frac{1}{T}\int_0^T VI\,dt \tag{2}$$

In the current context, we are calculating the average over 5 time periods. Hence, the equation now becomes:

$$P_{avg} = \frac{1}{5T}\int_0^{5T} VI\,dt \tag{3}$$

writing I in terms of V $(5V)$ and R $(10k\Omega)$, we get:

$$P_{avg} = \frac{1}{5T}\frac{V^2}{R}\int_0^{5T} \,dt \tag{4}$$

placing the value of integral, we get:

$$P_{avg} = \frac{1}{5T}\frac{V^2}{R}3T \tag{5}$$

finally, placing the values of V and R, we get:

$$P_{avg} = \frac{3}{5}\frac{5^2}{10000} \tag{6}$$

$$\boxed{P_{avg} = 1.5\ mW} \tag{7}$$