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Project 1

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States

1. S0
   - pc → MemA, aluA
   - +2 → aluB
   - aluC → t1
   - MemD → IR
   - t1 → pc

2. S_or
   - IR_{11-9} → RFa1
   - IR_{8-6} → RFa2
   - RFd1 → aluA
   - RFd2 → aluB
   - aluC → RFd3
   - IR_{5-3} → RFa3

3. S_or_ls
   - IR_{11-9} → RFa1
   - IR_{8-6} → RFa2
   - RFd1 → aluA
   - RFd2 → ls → aluB
   - aluC → RFd3
   - IR_{5-3} → RFa3

4. S_adi
   - IR_{11-9} → RFa1
   - RFd1 → aluA
   - IR_{5-0} → SE(6→16) → aluB
   - aluC → RFd3
   - IR_{8-6} → RFa3

5. S_lhi
   - IR_{8-0} → SE(9→16) → RFd3 (Zeros at LSB)
   - IR_{11-9} → RFa3

6. S_lb
$IR_{8-6} \rightarrow RFa_2$
$IR_{5-0} \rightarrow SE(6 \rightarrow 16) \rightarrow aluA$
$RFd2 \rightarrow aluB$
$aluC \rightarrow t2$

7. S_l
$IR_{11-9} \rightarrow RFa_1$
$t2 \rightarrow MemA$
$MemD \rightarrow RFd_1$

8. S_sb
$IR_{11-9} \rightarrow RFa_2$
$t2 \rightarrow memA$
$RFd2 \rightarrow MemD$

9. S_lm0
$IR_{11-9} \rightarrow RFa_1$
$RFd_1 \rightarrow t2$

10. S_lm1
$IR \rightarrow lsb \rightarrow t3$

11. S_lm2
$t3 \rightarrow IR$
$t1 \rightarrow aluA$
$-1 \rightarrow aluB$
$aluC \rightarrow t4$
$t4 \rightarrow t1$

12. S_lm3
$t1_{2-0} \rightarrow RFa_2$
$t2 \rightarrow MemA$
$MemD \rightarrow RFd_2$

13. S_lm4
$t2 \rightarrow aluA$
$+2 \rightarrow aluB$
$aluC \rightarrow t3$
$t3 \rightarrow t3$

14. S_sw3

$t1_{2-0} \rightarrow RFa_2$

$t2 \rightarrow MemA$

$RFd2 \rightarrow MemD$

15. S_beq0

$IR_{11-9} \rightarrow RFa_1$

$IR_{8-6} \rightarrow RFa_2$

$RFd_1 \rightarrow aluA$

$RFd_2 \rightarrow aluB$

$aluC \rightarrow t1$

16. S_beq1

$pc \rightarrow aluA$

$IR_{5-0} \rightarrow SE(6 \rightarrow 16) \rightarrow aluB$

$aluC \rightarrow pc$

17. S0_b

$pc \rightarrow aluA, memA$

$+2 \rightarrow aluB$

$MemD \rightarrow IR$

$IR_{11-9} \rightarrow RFA_1$

$aluC \rightarrow RFd_1$

18. S_jlr

$IR_{8-6} \rightarrow RFa_2$

$RFd_2 \rightarrow pc$

19. S_jal1

$IR_{11-9} \rightarrow RFa_1$

$RFd_1 \rightarrow aluA$

$IR_{8-0} \rightarrow SG(9 \rightarrow 16) \rightarrow aluB$ zero almsg

$aluC \rightarrow t1$

20. S_jal2

$t1 \rightarrow$ ~~RFdB~~ aluA

~~$RF_{03} \rightarrow aluB$~~

$pc \rightarrow aluB$

$aluC \rightarrow t2$

$t2 \rightarrow pc$

States flow

1. If OP_CODE = 0001, Last 2 bits = 00
   S0 → S_or
2. If OP_CODE = 0001, 10 S0 → if(C=1) → S_or
3. 0001 01 S0 → if(Z=1) → S_or
4. 0001 11 S0 → S_or_lr
5. 0000 S0 → S_adi
6. 0010 00 S0 → S_or
7. 0010 10 S0 → if(C=1) → S_or
8. 0010 01 S0 → if(Z=1) → S_or
9. 1111 S0 → S_lhi
10. 0111 S0 → S_lr → S_l
11. 0101 S0 → S_lr → S_s
12. 1100 S0 → S_lm0 → S_lm2 → if(t1=0) → next
    else → if(t3=0) → S_lm1
    else → S_lm3 → S_lm4 → S_lm
13. 1101 S0 → S_lm0 → S_lm2 → if(t1=0) → next
    else → if(t3=0) → S_lm1
    else → S_lm3 → S_lm4 → S_lm
14. 1000 S_beq1 → if(t1=0) → S_beq2
    else → S0
15. 1001 S0_b → S_beq1
16. 1010 S0_b → S_jlr
17. 1011 S_jri1 → S_jri2

Memory –

		State	data	write_address	read_address	we	q
①	*	S0			pc	0	IR
②		S_l			t1	0	RFd1
③	#	S_s	RFd2	t2		1	
④		S_lm3			t2	0	RFd2
③	#	S_sm3	RFd2	t2		1	
①	*	S0_b			pc	0	IR

Register File

	State	data	write_address	read_address	we	q	
S_ar, S_ar_ls, S_adi, S_lhi, S_jri	2, 3, 4, 15, 19			IR_{11-9}	001	0	aluA ①
S_ar, S_ls, S_br,	2, 6, 15			IR_{8-6}	010	0	aluB ②
S_ar, S_ar_ls	2,3	aluC	IR_{5-3}		0101	1	③
S_ar_ls	3			IR_{8-6}	010	0	→ls ④
S_adi	4	aluC	IR_{8-6}		0110	1	③
S_lhi	5	IR_{8-0} →SE ⟷	IR_{11-9}		0111	1	③
S_l	7	MemD	IR_{11-9}		010	1	①
S_s	8			IR_{11-9}	011	0	MemD ②
S_lm0	9			IR_{11-9}	011	0	t2 ①
S_lm3	12	MemD	$t1_{2-0}$		100	1	②
S_sm3	14			$t1_{2-0}$	101	0	MemD ④
S0_b	17	aluC	IR_{11-9}		100	1	①
S_jlr	18	pc	IR_{8-6}		110	1	②
S_jri2	20	t1	aluB		100	1	③

		t2	+2	t3	
Slm 4		~~t3~~	~~t4~~		
Slm 2		t1	-1	t4	
		ALU A	ALU B	ALU C.	
①. ALU →	S_0:	pc	+2	t1	D
	S_ar	RF_d1	RF_d2	RF_d3.	②
	S_ar_ls	RF_d1	RF_d2 → ls	RF_d3.	③
	S_adi	RF_d1	IR 5-0 → SE	RF_d3.	④
	~~S_ls~~ S_ls	ID5-0 - SE	RF_d1	mem A.	⑤
	S_beq0	RF_d1	Rf_d2	t1	⑥
*	S_beq1	pc	ID5-0 → SE	pc t1	⑨
	S_ob	pc	+2	RFd1	⑦
*	~~S_jal1~~	~~pc~~	~~ID5-0 → SE~~	pc.	
	~~S_jtr~~				
	S_jri1	RF_D1	ID8-0 → SE	RF_D3.	⑧
*	S_jri2	RF_D3	pc	pc t1	⑩

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⇒ **Program Counter**

pc → MemA S0, S0_b
aluA S_bool, S0, S0_b

t1 → pc S0
aluC → S_bool, S_jri2
RFd2 → S_jlr

⇒ **t1**

t1 → pc S0
~~MemA~~
aluA S_lm2
RFd3 S_jri2
$t1_{2-0}$ → RFa2 S_lm3, S_sm3

aluC → t1 S0, S_bool0
t4 S_lm2

⇒ **t2**

t2 → memA S_l, S_s, S_lm3, S_sm3
aluA S_lm4

aluC → t2 S_ls
RFd1 S_lm0
t3 S_lm4

⇒ **Shifter (ls)**

S_ar_ls	RFd2	aluB
S_lm1	IR	t3

⇒ **t3**

t3 → IR S_lm2
t2 S_lm4

ls → t3 S_lm1
aluC → S_lm4

⇒ **t4**

aluC → t4 S_lm2

t4 → t1 S_lm2