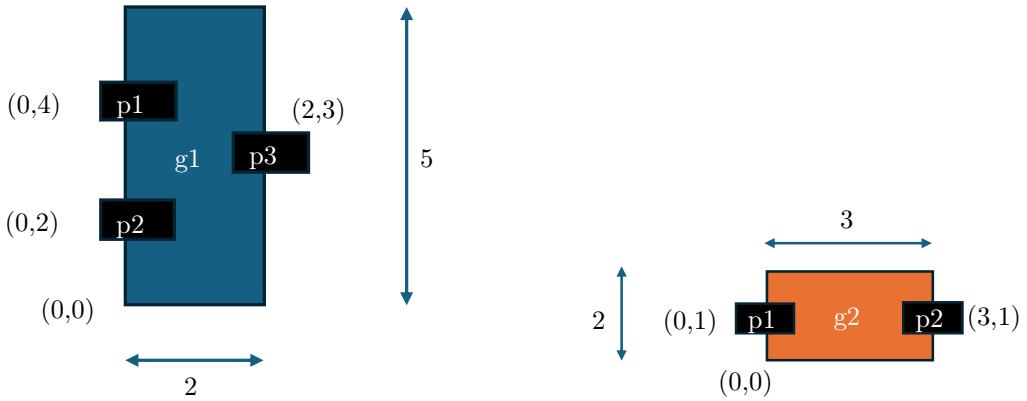
# COL215 Software Assignment 2: Wiring-aware Gate Positioning

Deadline: 1st October 2024

## 1 Introduction

Extending on the gate packing assignment, the gates will contain pins locations as shown in Figure 1. Objective is to minimize the total wire length of the circuit.




(a) Gate 1 (b) Gate 2

Figure 1: Gate pin specification example

## 2 Problem Statement

Given:

- a set of rectangular logic gates $g_1, g_2 ... g_n$
- ***width*** and ***height*** of each gate $g_i$
- the input and output pin locations ($x$ and $y$ co-ordinates) on the boundary of each gate $g_i.p_1, g_i.p_2, ..., g_i.p_m$ (where gate $g_i$ has $m$ pins)
- the pin-level connections between the gates

write a program to assign locations to all gates in a plane so that:

- no two gates are overlapping
- the ***sum of estimated wire lengths*** for all wires in the whole circuit is ***minimised***.

### 2.1 Notes

- Assume that the gates cannot be re-oriented (rotated, etc.) in any way.
- Assuming that all wiring is horizontal and vertical
- Possible estimate for the wire length for a set of connected pins uses the ***semi-perimeter method***: form a rectangular bounding box of all the pin locations; the estimated wire length is half the perimeter of this rectangle.

## 3 Mathematical Formulation

Consider a structure consisting of gates and $m$ wires, each connecting a pair of pins. Let the coordinates of the pins connected by wire $w_i$ be $(x_i^{(1)}, y_i^{(1)})$ and $(x_i^{(2)}, y_i^{(2)})$.

The length of each wire is measured using the Manhattan distance between its coordinates, which can be expressed as:

$$f(w_i) = |x_i^{(1)} - x_i^{(2)}| + |y_i^{(1)} - y_i^{(2)}|$$

The total objective function is the sum of the areas of the gates and the weighted sum of the wiring lengths. Let $A_{\text{total}}$ denote the total area of the gates, and let $\bar{d}$ represent the mean width of the wires. The full objective function is:

$$\text{Objective Function} = A_{\text{total}} + \bar{d} \cdot \sum_{i=1}^{m} f(w_i)$$

Since $A_{\text{total}}$ and $\bar{d}$ are constants, minimizing the objective function reduces to minimizing the total Manhattan distance between the pins, which is:

$$\sum_{i=1}^{m} f(w_i) = \sum_{i=1}^{m} \left( |x_i^{(1)} - x_i^{(2)}| + |y_i^{(1)} - y_i^{(2)}| \right)$$

Therefore, the task is to minimize the total Manhattan distance between the connected pins to achieve the optimal wiring configuration. Estimating wire length using Manhattan distance is known as **Semi Perimeter Method**.

## 4 Formats

### 4.1 Input file format

For each gate, the input file contains the width and height and the corresponding pins co-ordinates. Referring to Figure 1, **g1.p1 is at (0,2), g1.p2 is at (0,4), g1.p3 is at (2,3) with respect to the bottom left corner of g1** and **g2.p1 is at (0,1), g2.p2 is at (3, 1) with respect to the bottom left corner of g2**. Then each wire connections in the following format (see Figure 2) :

```
<name of gate> <width> <height>
<pins> <name of gate> <x_1, y_1> ... <x_m, y_m>
<wire> <g_x.p_x> <g_y.p_y>
```

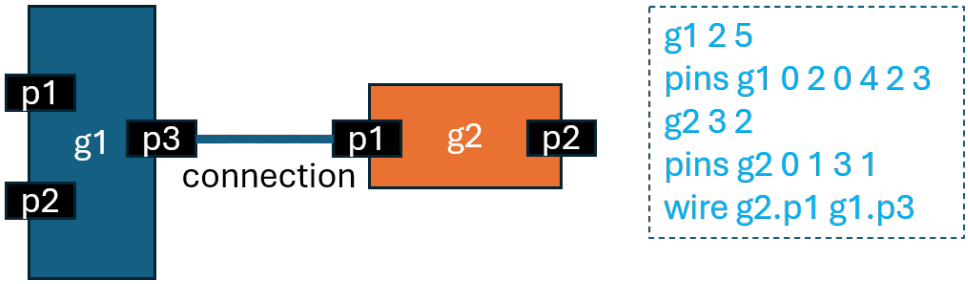



Figure 2: Input file format

### 4.2 Output file format

The output file begins with a specification of the bounding box, of the form:

```
bounding_box <width> <height>
wire_length <wire_length>
```

Following the bounding box line, each line of the output file from your program should have the location of the gate, specified as the $x$- and $y$-co-ordinates of the bottom left corner as follows:

```
<name of gate> <x co-ordinate> <y co-ordinate>
```

## 5 Test Case format

The Figure 3 shows input specifications for sample test. We are given 3 gates, $g1$, $g2$, $g3$ and pins $p_{11}, p_{12}, p_{21}, p_{22}, p_{31}, p_{32}$, where $p_{ij}$ denotes the $j^{th}$ pin of $i^{th}$ gate.

```
g1 2 3
pins g1 0 1 0 2
g2 3 2
pins g2 0 0 3 1
g3 2 2
pins g3 0 1 2 1
wire g1.p1 g2.p1
wire g2.p2 g3.p1
wire g1.p2 g3.p2
```

Figure 3: Gate and pin input specifications

Please note that coordinates of a pin are relative to the bottom-left corner of that gate, which is assumed to be at (0, 0) to determine the position of pins for that gate. The Table 1 shows the height, width, and pin position relative to gates.

Figure 4 shows the gates with the position of pins. The height and width are also shown to avoid confusion. Figure 5 shows 4 different configurations of placing the gates shown in Figure 4. Both optimal and sub-optimal wires/gates placement are shown.

Table 1: Gate and pin parameters

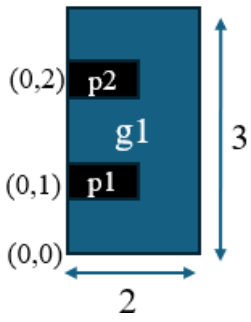
| Gate | Width | Height | Pin-Coordinates relative to bottom left corner (0, 0) of gate $g_i$ |
|---|---|---|---|
| $g_1$ | 2 | 3 | (0, 1), (0, 2) |
| $g_2$ | 3 | 2 | (0, 0), (3, 1) |
| $g_3$ | 2 | 2 | (0, 1), (2, 1) |

In our case, for the 4 configurations shown, configuration 1 is the most optimal configuration for minimizing the wire length using semi-perimeter method. For this, `"output.txt"` would be as follows:

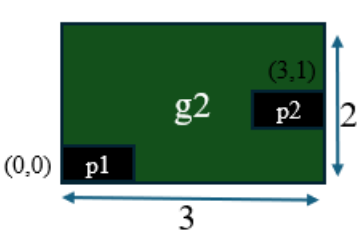
```
bounding_box 7 3
g1 0 0
g2 2 0
g3 5 0
wire_length 11
```

We can connect the wires in different ways. As you can see in 5, the wires can be connected through solid and dotted paths. However, the dotted paths don't use the semi-perimeter method and hence would not give the minimized wire length. The solid path uses the semi-perimeter method and would provide a minimal length.

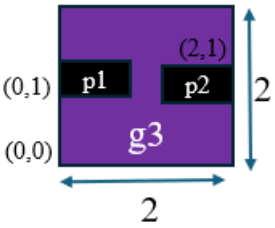
**Note:** There are other ways too, to optimize the wire length, but we are using the semi-perimeter method in this assignment.




(a) g1




(b) g2




(c) g3

Figure 4: Sample test gate specifications

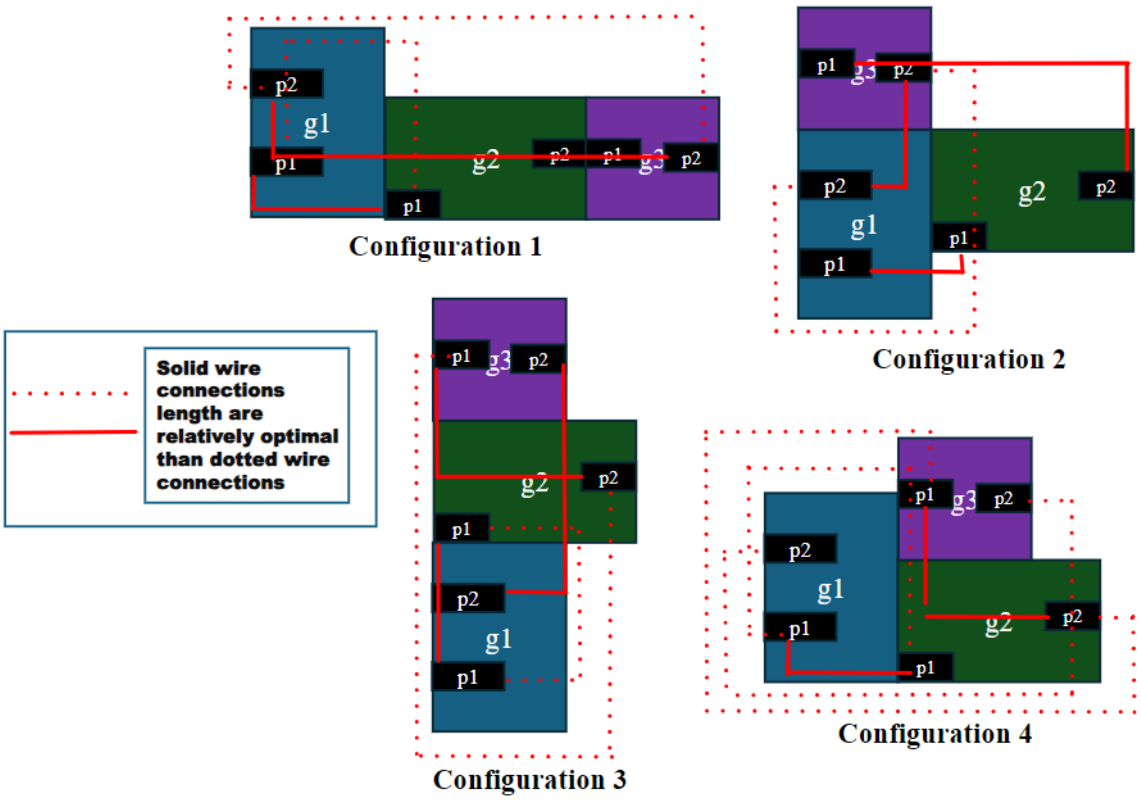



Figure 5: Different Configurations for Sample Case of Figure 4

# 6 Testing instructions

Initial sample test cases will be uploaded on moodle. Additionally, you are required to generate your own test cases to verify the implementation. You need to provide justification (in report) for the generated test cases.

Following are the input constraints:

- **Corners of gate have integral coordinates**
- **Pins will have integral coordinates relative to the corresponding gate**
- **0 $<$ Number of gates $\leq$ 1000**
- **0 $<$ Width of gate $\leq$ 100**
- **0 $<$ Height of gate $\leq$ 100**
- **0 $<$ Number of pins on one side of a gate $\leq$ Height of Gate**
- **0 $<$ Total Number of pins $\leq$ 40000**
- **There is atleast 1 wire connecting a gate**

# 7 Assignment Submission Instructions

General assignment instructions that need to be followed for all assignments: only one partner needs to submit. Mention all team member names and entry IDs during the submission.

1. Name the submission file as entryNumber1_entryNumber2.zip or entryNumber1.zip
2. Go to Gradescope via moodle and upload the file under Software Assignment 2.
3. Only one submission per group is required. Gradescope will allow you to select the group partner.
4. The following files should be part of the zip folder:
    - Source files
    - Report as a .pdf file (handwritten report will be rejected). The report needs to state:
        - your design decisions
        - time complexity analysis
        - test cases