COL215 Assignment 1 - Lorem Ipsum Dolor

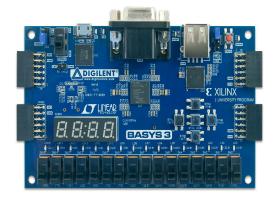
Submission By:

Yash Rawat Priyanshi Gupta 2023CS50334 2023CS10106

Department of Computer Science and Engineering Indian Institute of Technology, Delhi

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1 Design Philosophy

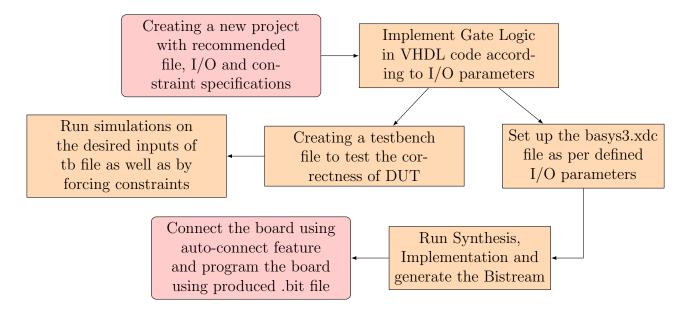
1.1 I/O Terminals

Implementing a 2 input AND gate, 2 input OR gate and 1 input NOT gate required us to define 5 inputs and three outputs. The mapping of ports to the constraint file are as give below :

SNo.	Port Name	Board Contstraint	I/O
1	a_and_in	V17	IN
2	b_and_in	V16	IN
3	c_{and_out}	U16	OUT
4	d_or_in	W16	IN
5	e_or_in	W17	IN
6	f_or_out	E19	OUT
7	g_not_in	W15	IN
8	h_not_out	U19	OUT

Table 1: Mapping of Ports and Constraints in Basys3.xdc

1.2 Desgin Process Flow Chart - Week 1



2 Lab Work

3 To Do: Complete This Doc