

COL215: Common Vivado Errors

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Error overview

- Error 1: Poor placement for routing between an IO pin and BUFG
- Error 2: Rule violation (MDRV-1) Multiple Driver Nets
- Error 3: Rule violation (LUTLP-1) Combinatorial Loop

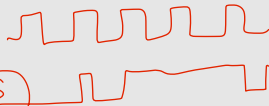
Error: Poor placement

```
1  entity poor_placement is
2      Port (
3          clk: IN std_logic;
4          sw: IN std_logic_vector(13 downto 0);
5          led: OUT std_logic_vector(1 downto 0)
6      );
7  end poor_placement;
8
9  architecture Behavioral of poor_placement is
10     signal i: integer := 0;
11 begin
12     led <= std_logic_vector(to_unsigned(i, 2));
13     sample: process (clk, sw(0))
14     begin
15         if (rising_edge(sw(0))) then
16             i <= i + 1;
17         end if;
18         -- if (rising_edge(clk)) then
19         --     if (sw(0) = '1') then
20         --         i <= i + 1;
21         --     end if;
22         -- end if;
23     end process;
24 end Behavioral;
```

*input pin
synchron*

1

→



Error: Poor placement

Implementation (3 errors)

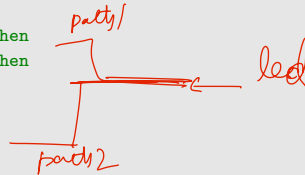
Place Design (3 errors)

- ❌ **Place 30-574** Poor placement for routing between an IO pin and BUFQ. If this sub optimal condition is acceptable for this design, you may use the CLOCK_DEDICATED_ROUTE constraint in the .xdc file to demote this message to a WARNING. However, the use of this override is highly discouraged. These examples can be used directly in the .xdc file to override this clock rule.
< set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets sw_BUF[0]] >

sw_BUF[0].inst (BUFQ) is locked to IOB_X0Y11
and sw_BUF_BUFQ[0].inst (BUFQ) is provisionally placed by clockplacer on BUFQCTRL_X0Y0

Error: Multiple Driver nets

```
1  architecture Behavioral of poor_placement is
2
3  signal i: integer := 0;
4  begin
5      led <= std_logic_vector(to_unsigned(i, 2));
6      sample: process (clk, sw(0))
7      begin
8          if(rising_edge(clk)) then
9              if (sw(0) = '1') then
10                 i <= i + 1;
11             end if;
12         end if;
13     end process;
14     sample2: process (clk)
15     begin
16         if(rising_edge(clk)) then
17             i <= i + 2;
18         end if;
19     end process;
20 end Behavioral;
```



Error: Multiple driver net

Net (1 error)

[DRC MDRV-1] Multiple Driver Nets: Net led_OBUF[1] has multiple drivers: i_reg[1]_0/Q, and i_reg[1]/Q.

[Vivado_Tcl 4-78] Error(s) found during DRC. Opt_design not run.

Error: Combinatorial Loop

```
1 architecture Behavioral of poor_placement is
2 signal i: integer := 0;
3 signal j, k: std_logic := '0';
4 begin
```

```
5     j <= sw(0) and sw(1) and j;
6     led(0) <= j;
7     --j <= sw(0) and sw(1);
```

```
8
9
10    --sample3: process(clk)
11    --begin
12    --    if (rising_edge(clk)) then
13    --        k <= j;
14    --    end if;
15    --end process;
16    --led(0) <= j and k
17 end Behavioral;
```

in → indeterminate

0 → 1



Error: Combinatorial Loop

