COL215 Software Assignment 1: Gate Packing

Deadline: 25 August 2024

1 Introduction

In this assignment we will attempt to automatically generate a compact physical layout of a gate-level circuit. Assume that all gates are rectangular, and the final layout is also rectangular. In a compact layout, blank space is minimised. See Figure 1 below.

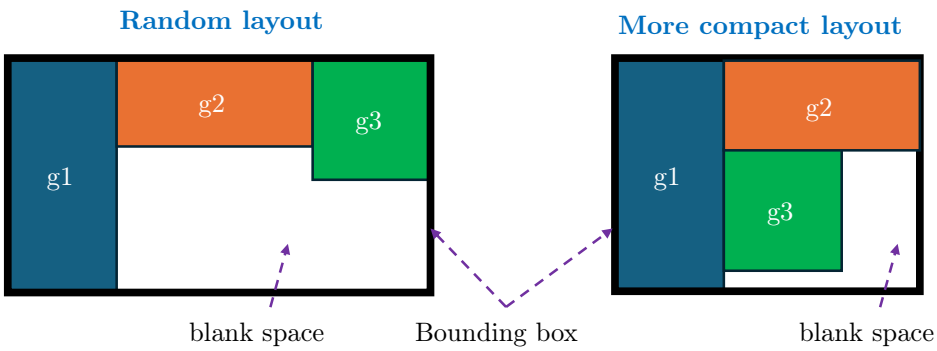

Figure 1: Gate packing example

2 Problem Statement

Given:

- a set of rectangular logic gates $g_1, g_2 ... g_n$
- ***width*** and ***height*** of each gate g_i

write a program to assign locations to all gates in a plane so that:

- no two gates are overlapping
- the ***bounding box*** of the entire circuit (smallest rectangle that encloses all gates) has minimum area.

2.1 Notes

- Assume that the gates cannot be re-oriented (rotated, etc.) in any way.
- In this simplified problem statement, we ignore connections between gates.

3 Formats

3.1 Input file format

Each line of the input file contains the width and height of each gate in the following format (see Figure 2) :

```
<name of gate> <width> <height>
```

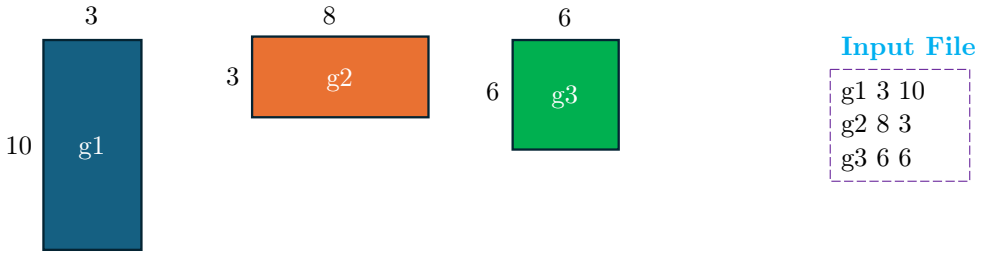

Figure 2: Input file format

3.2 Output file format

The output file begins with a specification of the bounding box, of the form:

```
bounding_box <width> <height>
```

Following the bounding box line, each line of the output file from your program should have the location of the gate, specified as the x- and y-co-ordinates of the bottom left corner as follows (see Figure 3):

```
<name of gate> <x co-ordinate> <y co-ordinate>
```

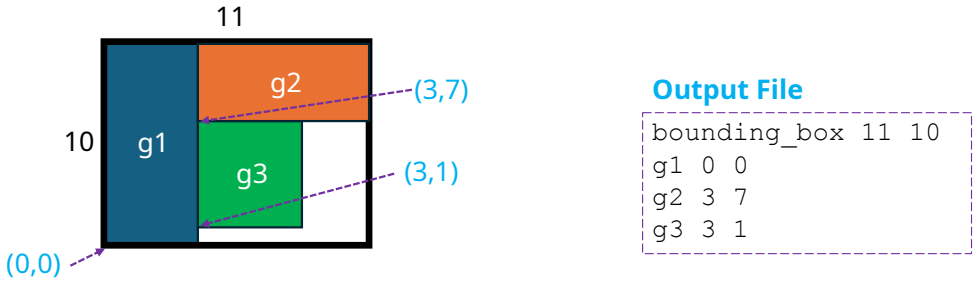

Figure 3: Output file format

4 Visualisation of the circuit

An utility to visualise the gate packing shall be provided, it will take arguments as specified in Section 3.2.

5 Testing instructions

Sample test cases will be uploaded on moodle. Additionally, you are required to generate your own test cases to verify the implementation.

6 Assignment Submission Instructions

General assignment instructions that need to be followed for all assignments: only one partner needs to submit. Mention all team member names and entry IDs during the submission.

1. Name the submission file as entryNumber1_entryNumber2.zip or entryNumber1.zip
2. Go to Gradescope via moodle and upload the file under Software Assignment 1.
3. Only one submission per group is required. Gradescope will allow you to select the group partner.
4. The following files should be part of the zip folder:
    - Source files
    - Report as a .pdf file (handwritten report will be rejected). The report needs to state:
        - your design decisions
        - time complexity analysis
        - test cases