LOW POWER VLSI DESIGN

(EC365TDA)

The Power Problem

- High frequency and chip density lead to high power
  - Today's microprocessors consume 100-150 W
  - Future microprocessors may consume over 200 W
- Power has an impact on:
  - System performance (battery life)
  - Chip performance (circuit speed)
  - Packaging and cooling (cost)
  - Signal integrity: Inductive kick (Ldi/dt), IR drop, noise, etc.
  - Physical reliability: Electromigration, hot-carriers, etc.
- Power is a problem in both portable & fixed equipment

Impact on Performance

- Power dissipation affects chip speed in two ways:
  - Power supply (voltage) variations (IR drop, Ldi/dt drop)
  - Temperature variations
- Power supply reduction causes a circuit to slow down
  - A 5% reduction in Vdd may cause a 15% increase in gate delay
- Increased temperature has a complex effect on speed
  - Traditionally: slow down
  - Today: gates speed-up, wires slow down

Impact on Chip Reliability

- ICs are subject to a variety of physical failure mechanisms:
  - Electromigration (EM)
  - Hot-carrier degradation (HC)
- Reliability is worse under:
  - High switching activity
  - High temperature
- Result: chip MTF is reduced under high power conditions

MTF: Median Time to Failure: Is defined to occur when 50% devices have failed so that half of the failure happens prior to time(t50) and remaining half after t50. (where t50 is the failure distribution)

Introduction to Low-Power Design

Low power design is a collection of techniques and methodologies for reducing the overall dynamic and static power consumption of an Integrated Circuit (IC).

➢ **Low-power is a current need in VLSI design.**

- **Transistor scaling has been a highly successful method for Silicon technology**
- **CMOS technology scaling has now moved to a power constrained condition.**
- **Circuit techniques to reduce chip standby leakage has become a key enabler**
- **Scaling is a trading off performance and leakage**
- **Different circuit design techniques to optimize the delay and leakage**

Low Power Techniques

- General Good Design Practices
- Transistor sizing
- Voltage scaling
- Power down testability blocks when not in the test mode
- Clock gating (Power down the functional blocks)
- Minimize sequential elements
- Downsize all non-critical path circuits
- Reduce loading on the clock
- Adiabatic circuits

Unit – I

Introduction: Need for Low Power VLSI Design, Sources of power dissipation, Power dissipation in CMOS circuits: Short Circuit dissipation, Dynamic dissipation, load capacitance Charging and Discharging, Static Power: Leakage Currents, Static Currents, Emerging low power approaches and limits.

Physics of Power Dissipation in CMOS devices, MIS structure, long channel effect, sub-micron MOSFET, Gate induced drain leakage.

Unit – II

Power Estimation: Signal Modeling and probability calculation, Probabilistic techniques for signal activity estimation, statistical techniques, Estimation of glitching power, power estimation using input vector compaction, power estimation at circuit level, information theory-based approach.

Unit – III

•**Device and Technology Impact on Low Power Electronics:** Introduction, Dynamic Dissipation in CMOS, Effects of VDD and Vt on speed, Constraints on Vt Reduction, Transistor and Gate Sizing, Transistor Sizing and Optimal Gate Oxide Thickness (Quantitative analysis only) Impact of Technology Scaling.

•Equivalent Pin Ordering, Network Restructuring and Reorganization, Technology and Device Innovations, Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Pre-computational Logic, Power gating Techniques, Clock Gating Techniques.

Unit – IV

•**Low Power Circuit Techniques:** Introduction, Power consumption in circuits, Circuit design styles, Analysis of adders, multipliers, Flip-Flops and Latches, Low Power Cell Library.

•**Low power SRAM architectures:** SRAM organization, MOS SRAM cells-4T and 6T, Banked organization of SRAMs, Reducing voltage swings on bit-lines, Reducing power in write driver circuits, Reducing power in sense amplifier circuits.

Unit – V

Synthesis for Low Power: Behavioral level transforms: Architecture-Driven Voltage Scaling, Power reduction using Operation Reduction and Substitution, **logic level optimizations:** circuit level transforms, CMOS gates, **Power Reduction in Clock Networks:** power dissipation in clock distribution, single driver Vs distributed buffers, zero skew Vs tolerable skew, CMOS Floating Nodes, Low Power Bus, Delay Balancing, Energy recovery CMOS and Adiabatic computation.

Course Outcomes:

- **CO1**: Acquire the knowledge with regard to the physical principles, analysis and the characteristics of the low power designs.
- **CO2**: Identify, formulate, and solve engineering problems in the area of low power VLSI designs.
- **CO3**: Use the techniques and skills in system designing through modern engineering tools such as logic works SPICE and description languages such as VHDL and Verilog.
- **CO4**: Design a digital system, components or process to meet desired needs of low power within realistic constraints.

Reference Books

1. Kaushik Roy and Sharat Prasad, "Low-Power CMOS VLSI Circuit Design", John Wiley, 2000. ISBN 13 9788126520237
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, ISBN 978-1-4613-7778-8, 2002.
3. Jan M. Rabaey and Massoud Pedram, "Low Power Design Methodologies" Kluwer Academic Publishers, 5th reprint, ISBN 978-1-46 13-5975-3, 2002.
4. Anantha Chandrakasan and Robert W. Brodersen, Low Power CMOS design,, 1998, Wiley-IEEE press, ISBN: 0-7803-3429-9.
5. Ajit Pal, "Low-Power VLSI Circuits and Systems," Springer publications, ISBN: ISBN 978-81-322-1936-1, 2015
6. Robert Aitken, Alan Gibbons, Kaijian Shi, Michael Keating, David Flynn, Michael Keating, "Low Power Methodology Manual For System-on-Chip Design" Springer, ISBN 978-0-387-71818-7, 2007.

Continuous Internal Evaluation (CIE): Total marks: 100

Scheme of Continuous Internal Evaluation (CIE); Theory (100 Marks)

QUIZZES: Quizzes will be conducted in online/offline mode. **Two quizzes** will be conducted & Each Quiz will be evaluated for 10 Marks. The sum of two quizzes **(20 Marks)** will be the Final Quiz marks.

TESTS: Students will be evaluated in test, descriptive questions with different complexity levels (Revised Bloom's Taxonomy Levels: Remembering, Understanding, Applying, Analyzing, Evaluating, and Creating). **Two tests** will be conducted. Each test will be evaluated for 50 Marks, adding upto 100 Marks. Final test marks will be reduced to **40 Marks**.

EXPERIENTIAL LEARNING: Students will be evaluated for their creativity and practical implementation of the problem. **Case study-based teaching learning (10), Program specific requirements (10), Video based seminar/presentation/demonstration (20) Phase 2 will be done in the exhibition mode (Demo/Prototype/any outcome). ADDING UPTO 40 MARKS**.

Semester End Evaluation (SEE): Total marks: 100

Scheme of Semester End Examination (SEE) for 100 marks:

RUBRIC FOR SEMESTER END EXAMINATION (THEORY)		
Q. NO.	**CONTENTS**	**MARKS**
	PART A	
1	Objective type questions covering entire syllabus	20
	PART B (Maximum of TWO Sub-divisions only)	
2	Unit 1: (Compulsory)	16
3 & 4	Unit 2: Question 3 or 4	16
5 & 6	Unit 3: Question 5 or 6	16
7 & 8	Unit 4: Question 7 or 8	16
9 & 10	Unit 5: Question 9 or 10	16
	TOTAL	**100**

Power Consumption of VLSI Chips

Why is it a concern?

➢ **Business & technical needs**

The industry for low power consumer electronic products is booming with a rapidly expanding market.

➢ **Semiconductor processing technology**

Increased device density, speed and complexity

NEED FOR LOW POWER

- **More transistors are packed into the chip.**
- **Increased market demand for portable devices.**
- **Environmental concerns**

- As more and more no. of transistors are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation.
- Increased market demand for portable consumer electronics powered by batteries. The smaller, lighter and more durable electronic products indirectly translates to low power requirements.
- Another major demand for low power chips and systems comes from environmental concerns.
  - Electricity generation is a major source of air pollution, inefficient energy usage in computing equipment indirectly contributes to environmental pollution.

- **Battery lifetime will increase at a smaller rate even with the use of new battery technologies such as rechargeable lithium or polymers .**
- **If low-power design techniques are not adopted, the current and future portable devices will suffer from:**
  - **Either very short battery life or**
  - **Heavy battery packs.**

In addition, there is an issue of reliability. High power systems tend to run hot, and high temperature tends to several silicon failure mechanisms. Every 10 °C increase in operating temperature roughly doubles a component's failure rate.

Figure illustrates relationship between temperature and the various failure mechanisms such as electromigration, junction fatigue(weakness), and gate dielectric breakdown.

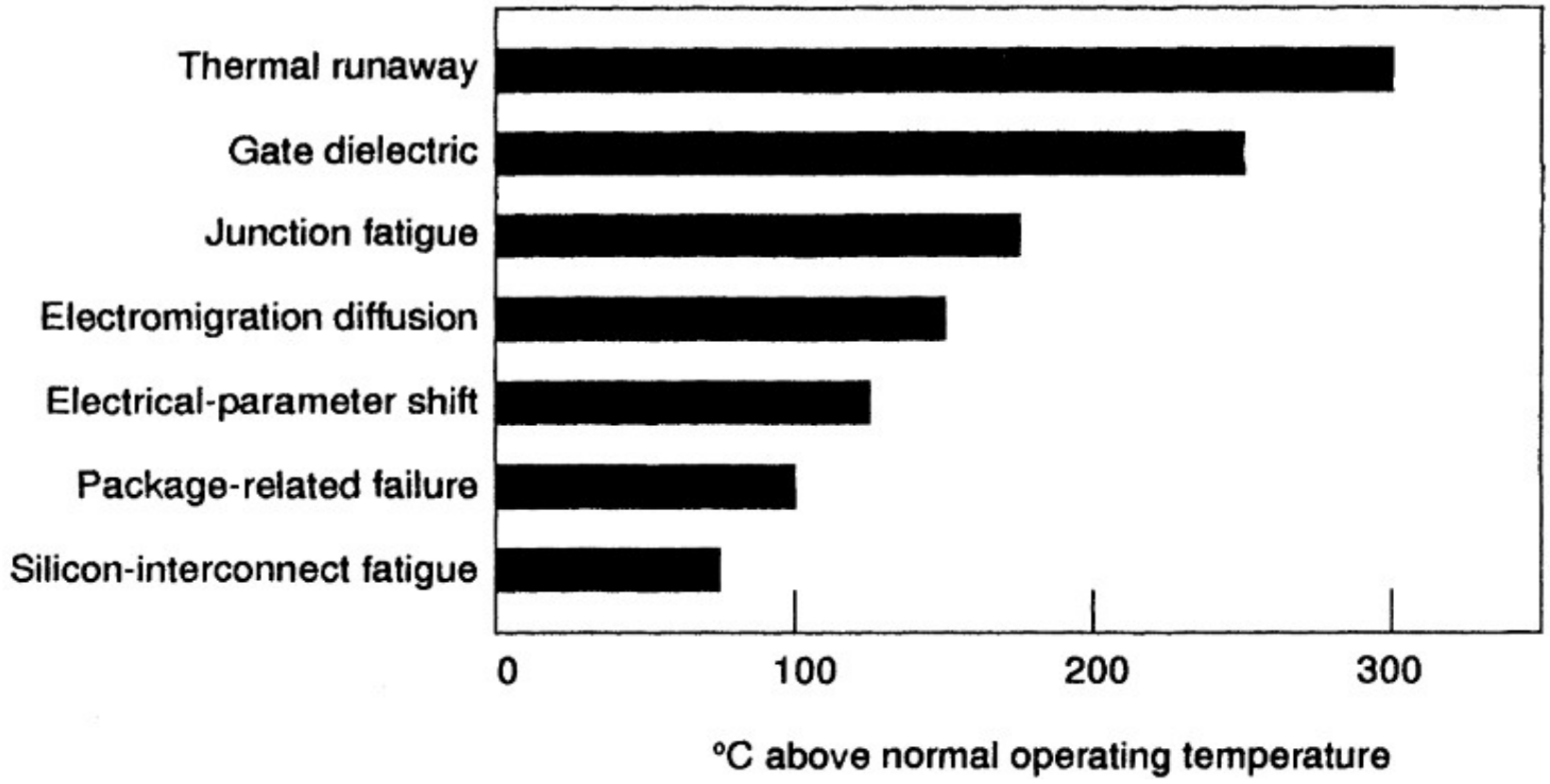
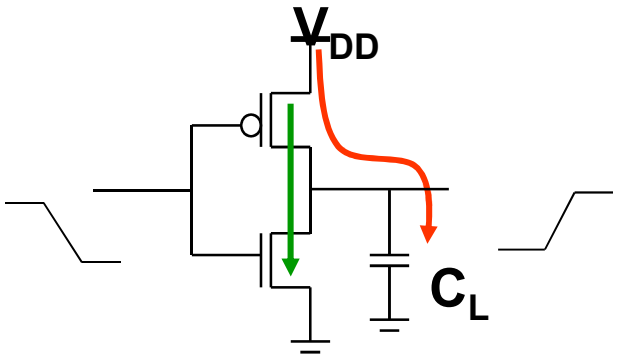


Fig: Onset temperatures of various failure mechanisms

Sources of power dissipation on Digital Integrated circuits

The average power dissipation in conventional CMOS digital circuits can be classified into three main components :

- **The dynamic (switching) power dissipation**
- **The short-circuit power dissipation and**
- **The Static (leakage) power dissipation.**



Dynamic Power Consumption

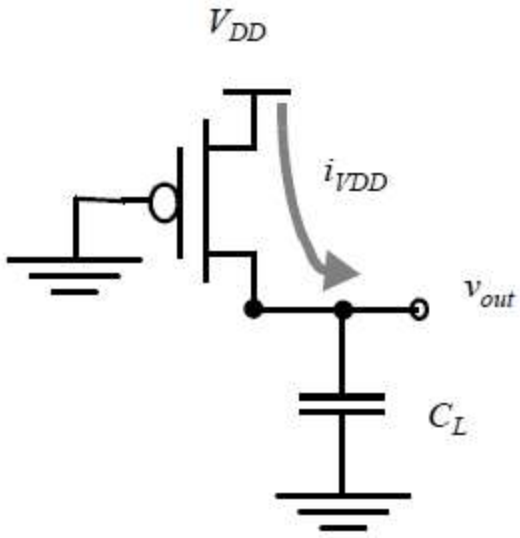
Dynamic Dissipation is due to Charging and Discharging Capacitances.

Each time the capacitor *CL gets charged through the PMOS transistor, its voltage rises* from 0 to *VDD*,

***Certain amount of energy is drawn from the power supply. Part of this* energy is dissipated in the PMOS device, while the remainder is stored on the load capacitor.**

During the high-to-low transition, this capacitor is discharged, and the stored energy is dissipated in the NMOS transistor.

The values of the energy *EVDD, taken from the supply during the transition, as* well as the energy *EC, stored on the capacitor at the* end of the transition, can be derived by integrating the instantaneous power over the period



The energy *EVDD, taken from the supply*

$$E_{VDD} = \int_0^{\infty} i_{VDD}(t) V_{DD} dt = V_{DD} \int_0^{\infty} C_L \frac{dv_{out}}{dt} dt = C_L V_{DD} \int_0^{V_{DD}} dv_{out} = C_L V_{DD}^2$$

The energy *EC, stored on the capacitor at the* end of the transition

$$E_C = \int_0^{\infty} i_{VDD}(t) v_{out} dt = \int_0^{\infty} C_L \frac{dv_{out}}{dt} v_{out} dt = C_L \int_0^{V_{DD}} v_{out} dv_{out} = \frac{C_L V_{DD}^2}{2}$$

This means that only half of the energy supplied by the power source is stored on *CL. The* other half has been dissipated by the PMOS transistor.

During the discharge phase, the charge is removed from the capacitor, and its energy is dissipated in the NMOS device.

Each switching cycle (consisting of an L→H and an H→L transition) takes a fixed amount of energy, This is for one cycle of the clock.

In order to compute the power consumption, we have to take into account how often the device is switched per second.

$$P_{dyn} = \frac{1}{T} C_{load} V_{DD}^2 = C_{load} V_{DD}^2 f$$

Note the average switching power dissipation of a CMOS gate is essentially independent of all transistor characteristics and transistor sizes.

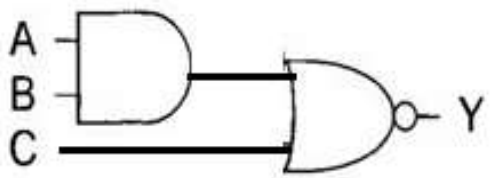
The analysis of switching power dissipation presented above is based on the assumption that the output node of a CMOS gate faces one power-consuming transition (0 to-VDD transition) in each clock cycle.

This assumption, however, is not always correct; the node transition rate can be smaller than the clock rate, depending on the circuit topology, logic style and the input signal statistics.

To better represent this behavior, we will introduce αf (node transition factor), which is the effective number of power-consuming voltage transitions experienced per clock cycle. Then, the average switching power dissipation becomes

(i.e.Most of gates do not switch every clock cycle, it is often more convenient to express switching frequency *f* as an *activity factor* times the clock frequency *f*)

$$P_{switching} = \alpha C V_{DD}^2 f$$



Prob. 1 A 32 bit off-chip bus operating at 5V and 66MHz clock rate is driving a capacitance of 25pF/bit. Each bit is estimated to have a toggling probability of 0.25 at each clock cycle. What is the power dissipation in operating the bus?

Soln:

$$C = 32 \times 25 = 800\text{pF}$$
$$V = 5.0\text{V}$$
$$f = 0.25 \times 66 = 16.5\text{MHz}$$
$$P = 800\text{pF} \times 5^2\text{V}^2 \times 16.5\text{MHz} = 330\text{mW}$$

Prob. 2

The chip size of a CPU is 15mm × 25mm with clock frequency of 300MHz operating at 3.3V. The length of the clock routing is estimated to be twice the circumference of the chip. Assume that the clock signal is routed on a metal layer with width of 1.2um and the parasitic capacitance of the metal layer is 1fF/um^2. What is the power dissipation of the clock signal?

Circumference of a rectangle=2(L+W)

Soln:

$$C = 4(15 + 25)\,\text{mm} \times 1.2\text{um} \times 1\text{fF/um}^2 = 192\text{pF}$$
$$V = 3.3\text{V}$$
$$f = 300\text{MHz}$$
$$P = CV^2f = 192\text{pF} \times 3.3\text{V}^2 \times 300\text{MHz} = 627\text{mW}$$

Dissipation Due to Direct-Path Currents(Short-Circuit Power Dissipation)

The input signal causes a direct current path between *VDD* and *GND for a short period of time during switching, while the NMOS and the PMOS* transistors are conducting simultaneously as shown in Figure.

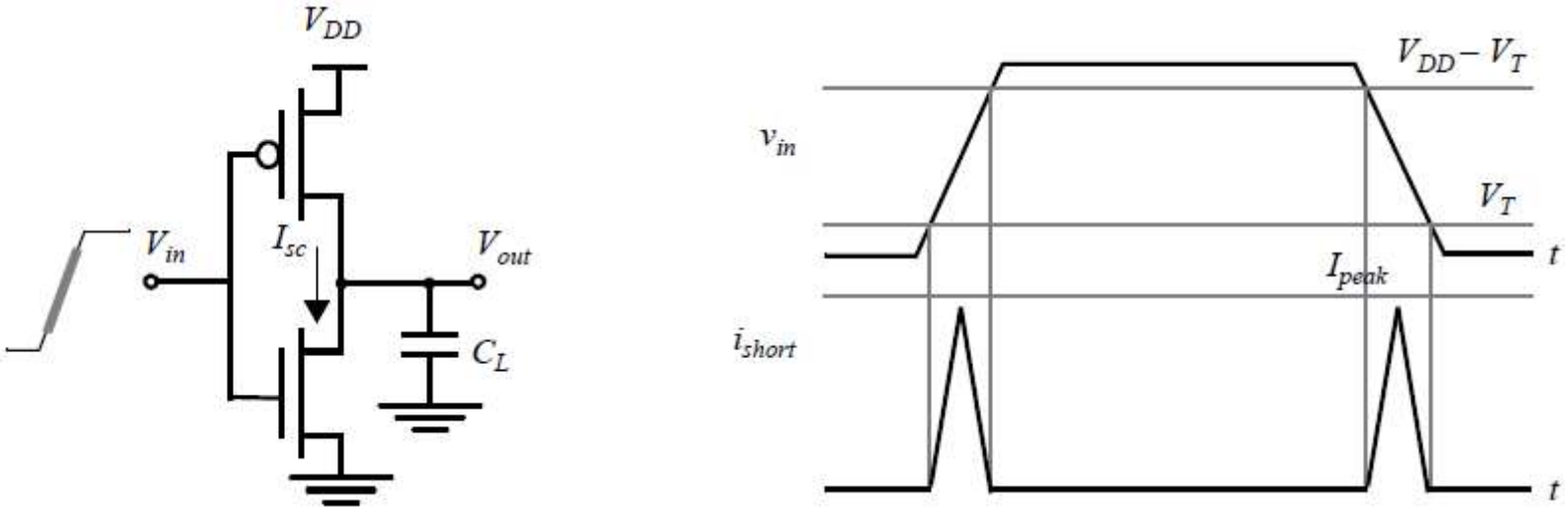


Figure: Short-circuit currents during transients

we can compute the **energy consumed per switching period(i.e. for one cycle),**

$$E_{dp} = V_{DD}\frac{I_{peak}t_{sc}}{2} + V_{DD}\frac{I_{peak}t_{sc}}{2} = t_{sc}V_{DD}I_{peak}$$

The average power consumption for a total period due to direct-path is

$$P_{dp} = t_{sc}V_{DD}I_{peak}f$$

short-circuit current can be reduced by lower the supply voltage

Short-circuit Current Variation with Output Load

Short-circuit current exhibits some interesting characteristic with respect to the output loading capacitance and the input signal slope of a CMOS inverter.

The duration of short-circuit current depends on the transition period of the input signal.

Consider the case when the input voltage is falling and the output voltage is rising. The short circuit current is non-zero only when the input level is between Vtn and Vtp.

If the output capacitance is large, the output voltage rises above zero and the voltage across the source and drain of the N transistor is slightly above zero. The low source-drain potential difference results in small short-circuit current.

If the output capacitance is small the output voltage rises faster and the source-drain voltage is much higher, causing a larger short-circuit current.

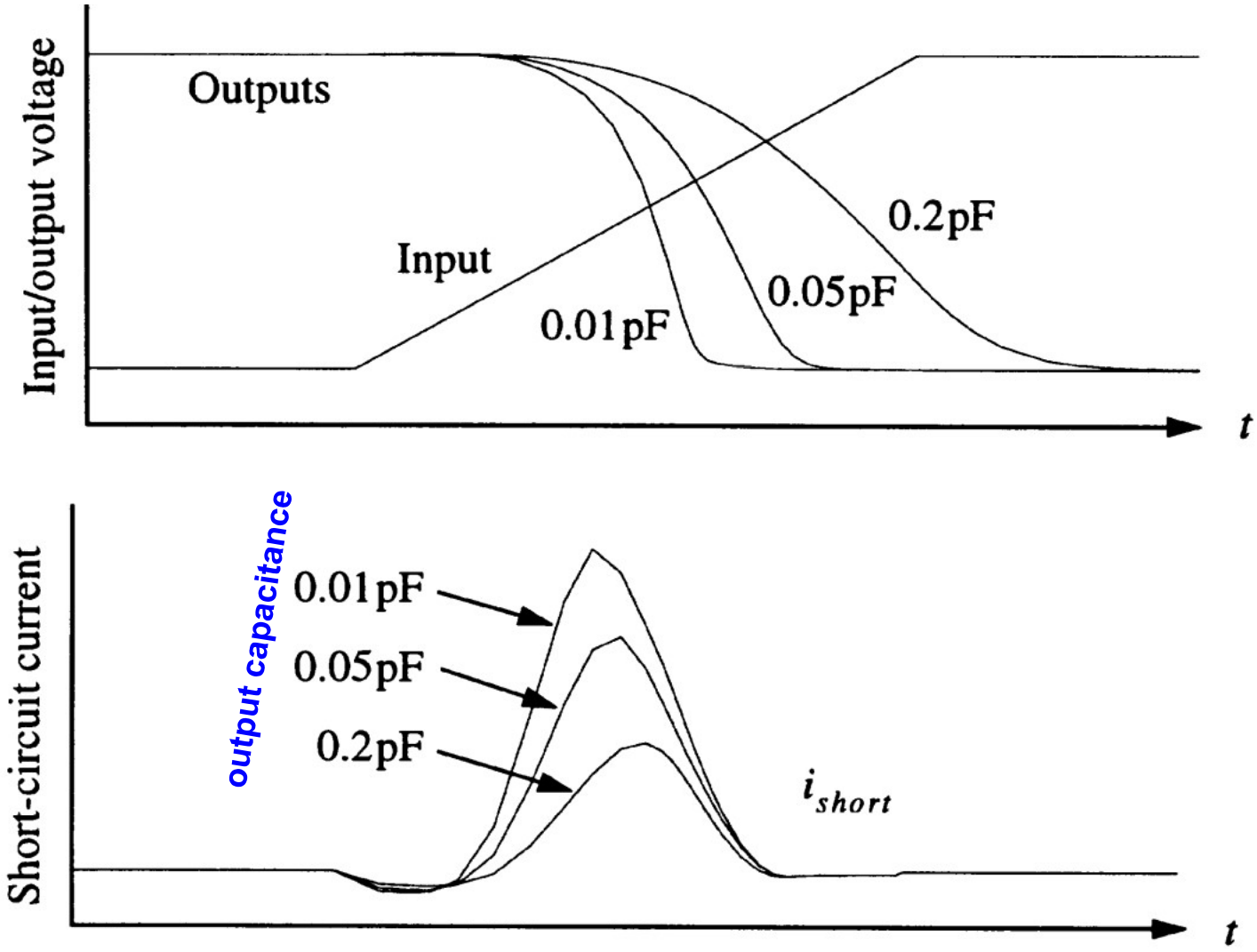


Fig: Short-circuit current under varying output capacitance.

If all conditions are kept identical, increasing the output loading capacitance has the effect of reducing the short-circuit energy per transition.

When the output capacitance is increased, the total current always increases in peak as well as time duration of charging/discharging. This means that increasing the output capacitance decreases the short-circuit power dissipation but the sum of capacitive and short-circuit power increases. Therefore, capacitance is always the enemy of power efficiency and a low power digital design should always strive to reduce loading capacitance.

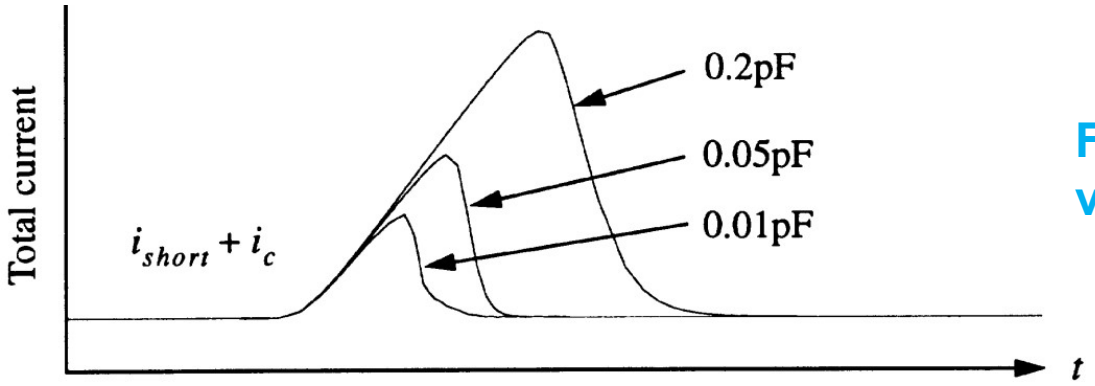


Fig: Total current under varying output capacitance

Table: Effects of increasing output loading capacitance_

Current envelope	Width of short ciruit pulse	Peak Current
Shortcircuit Current(Isc)	Unchanged	Decrease
Load Cap Current(Ic)	Increase	Increase
Total Current(Isc+Ic)	Increase	Increase

Short-circuit Current Variation with Input Signal Slope

If the input signal rise time increses (longer signal transition time), the short-circuit current peak and time duration increase. For the total current, i.e., short-circuit plus capacitance current, the time duration increases but the peak decreases.

Table: Effects of increasing Input signal slope

Current envelope	Width of short ciruit pulse	Peak Current
Shortcircuit Current(Isc)	Increase	Increase
Cap Current(Ic)	Increase	Decreases
Total Current(Isc+Ic)	Increase	Decreases

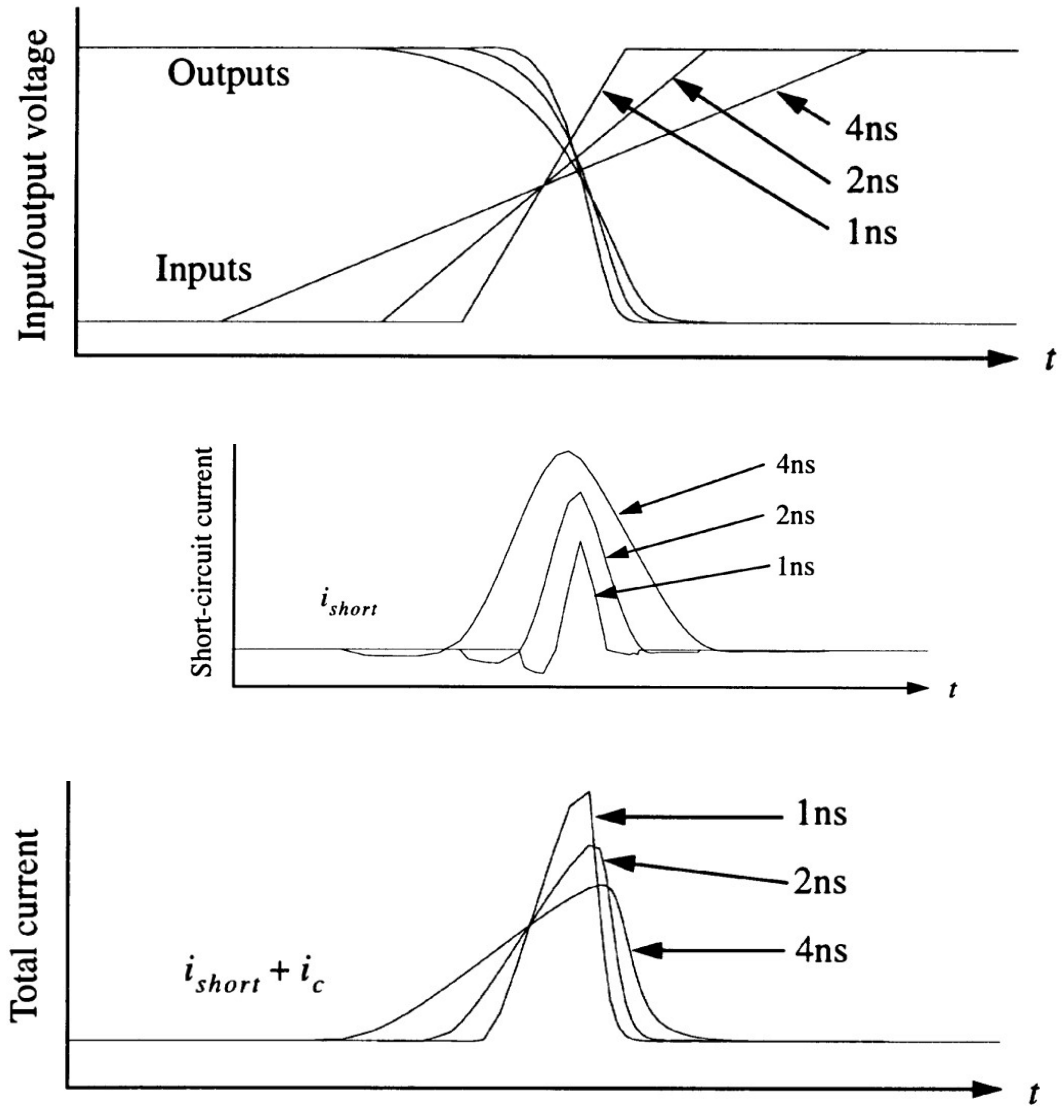


Fig: Short-circuit and total current under different input signal slopes.

Static (Leakage) Power Consumption

The static (or steady-state) power dissipation of a circuit is, where *the current that flows between the supply rails in the absence of switching activity*

$$P_{stat} = I_{stat} V_{DD}$$

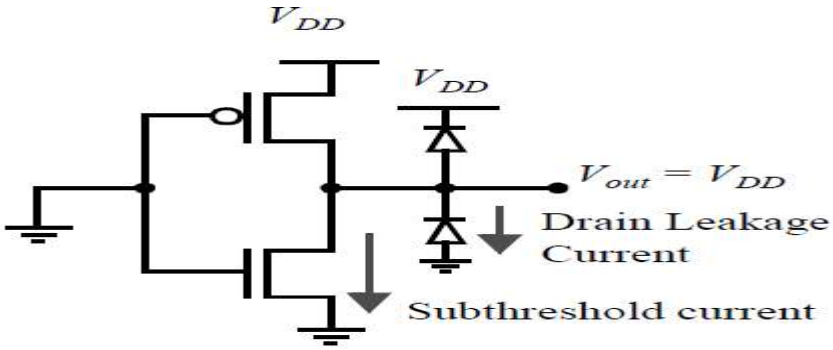
Ideally, the static current of the CMOS inverter is equal to zero, as the PMOS and NMOS devices are never on simultaneously in steady-state operation.

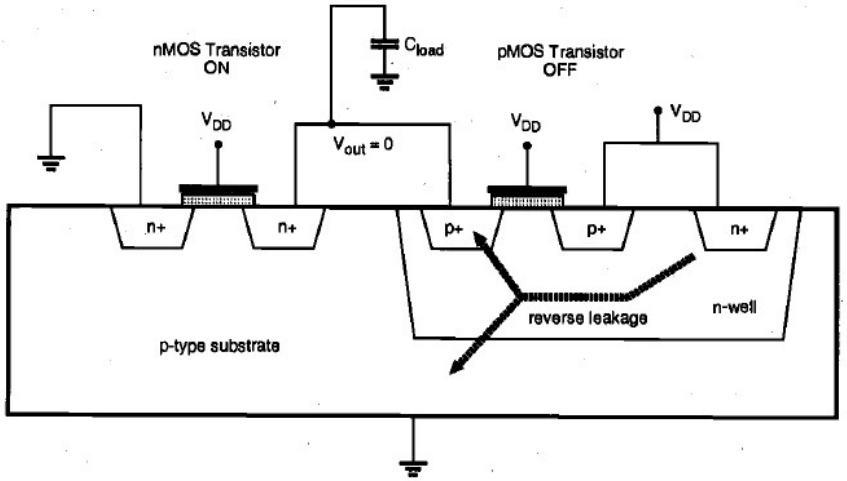
Two main leakage current components found in a MOSFET are

(1) Reverse diode leakage current

(2) Sub threshold leakage current

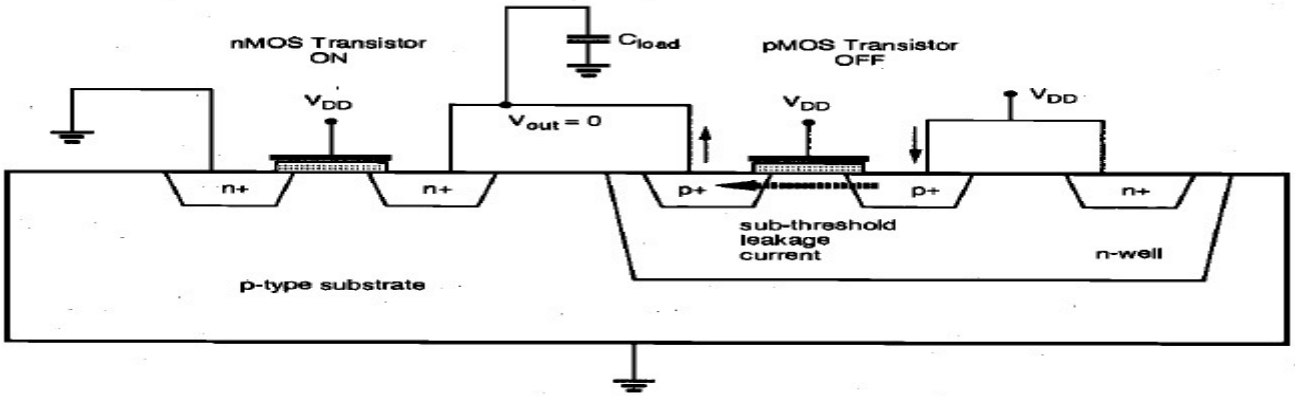
The reverse diode leakage occurs when the pn-junction between the drain and the bulk of the transistor is reversely biased. The reverse-biased drain junction then conducts a reverse saturation current which drawn from the power supply.





Subthreshold leakage current:

Another component of leakage currents which occur in CMOS circuits is the subthreshold current, which is due to carrier diffusion between the source and the drain region of the transistor in weak inversion. The subthreshold leakage current is shown in Fig. below.



Subthreshold leakage current path in a CMOS inverter with high input voltage.

The total power consumption of the CMOS inverter is now expressed as the sum of its three components:

$$P_{tot} = P_{dyn} + P_{dp} + P_{stat}$$

$$P_{tot} = (C_L V_{DD}^2 + V_{DD} I_{peak} t_s) f + V_{DD} I_{leak}$$

Where :

$$P_{dyn} = \frac{1}{T} C_{load} V_{DD}^2 = C_{load} V_{DD}^2 f$$

$$P_{dp} = t_{sc} V_{DD} I_{peak} f$$

$$P_{stat} = I_{stat} V_{DD}$$

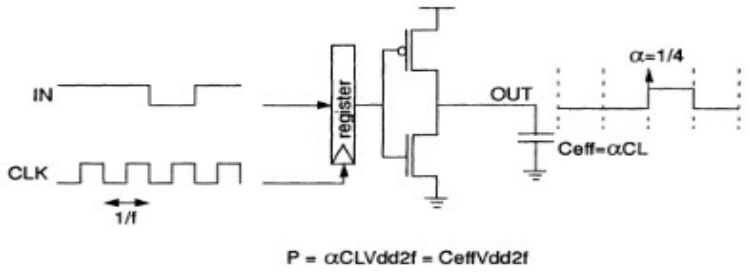
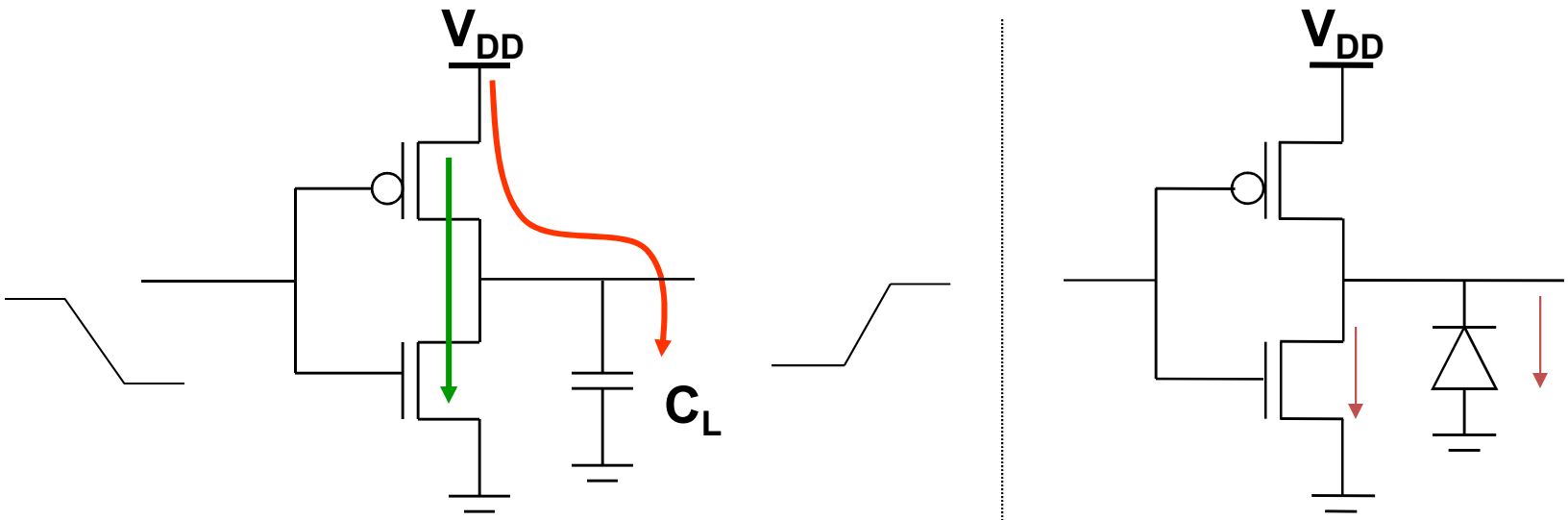


Fig: Interpretation of switching activity in synchronous systems

Power Dissipation in CMOS Logic (0.25µ)

$$P_{total} = (C_L V_{DD}^2 + t_{sc} V_{DD} I_{peak} + V_{DD} I_{leakage}) \text{ for one cycle}$$



The power dissipation caused by a single capacitor *CL* *is given by*

$$P = C_L V^2 f$$

In general, the total power should be summed over each capacitance Ci in a circuit, i.e.

$$P = \sum_i C_i V_i^2 f_i$$

where *Vi is the voltage swing across the capacitor* Ci switching at frequency *fi. For* CMOS circuits, *V is typically the same for all capacitance Ci*. One simple approximation is to assume that *fi is constant, for example, by taking the average of all fi 's*. This gives

$$P = V^2 f \sum_i C_i = C_{total} V^2 f$$

in which *Ctotal is the sum of all capacitance*, *f is the average frequency and V is the* voltage swing. Some of the basic principles of low power design includes: Reduce Switching Voltage, Reduce Capacitance, Reduce Switching Frequency, Reduce Leakage and Static Current

Basic Principles of Low Power Design

Low power considerations should be applied at all levels of design abstraction and design activities. No single low power technique is applicable to all situations. Design constraints should be viewed from all angles within the bounds of the design specification.

Early design decisions have higher impact to the final results and therefore, power analysis should be initiated early in the design cycle.

Some of the basic principles of low power design includes: Reduce Switching Voltage, Reduce Capacitance, Reduce Switching Frequency, Reduce Leakage and Static Current

1) Reduce Switching Voltage

The dynamic power of digital chips expressed by Equation: $P=CV^2f$ consist of three terms: voltage, capacitance and frequency. Due to the quadratic effect of the voltage term, reducing the switching voltage can achieve dramatic savings. The easiest method to achieve this is to reduce the operating voltage of the CMOS circuit.

There are many trade-offs to be considered in voltage reduction. Performance is lost because MOS transistors become slower at lower operating voltages. The threshold voltages of the transistors do not scale accordingly with the operating voltage to avoid excessive leakage current.

Noise immunity is also a concern at low voltage swing. Special level converters are required to interface low-swing signals to the full-swing ones.

2 Reduce Capacitance

Reducing parasitic capacitance in digital design has always been a good way to improve performance as well as power. However, a blind reduction of capacitance may not achieve the desired result in power dissipation. The real goal is to reduce the product of capacitance and its switching frequency. Signals with high switching frequency should be routed with minimum parasitic capacitance to conserve power. Conversely, nodes with large parasitic capacitance should not be allowed to switch at high frequency.

Capacitance reduction can be achieved at most design abstraction levels: material, process technology, physical design (floorplanning, placement and routing), circuit techniques, transistor sizing, logic restructuring, architecture transformation and alternative computation algorithms.

3 Reduce Switching Frequency

Frequency reduction is best applied to signals with large capacitance. Reduction of switching frequency effect the reliability of a chip as some failure mechanism is related to the switching frequency. One effective method of reducing switching frequency is to eliminate logic switching that is not necessary for computation(Clock gating). Other methods involve alternate logic implementation since there are many ways to design a logic network to perform an identical function.

The use of different coding methods(Gray coding has less switching than binary), number representation systems, counting sequences and data representations can directly alter the switching frequency of a design.

Binary code		Gray code	
Sequence	No. toggles	Sequence	No. toggles
000	3	000	1
001	1	001	1
010	2	011	1
011	1	010	1
100	3	110	1
101	1	111	1
110	2	101	1
111	1	100	1

4 Reduce Leakage and Static Current

Leakage current, through reverse biased junction or sub-threshold current, is generally not very useful in digital design. However, designers often have very little control over the leakage current of the digital circuit. Fortunately, the leakage power dissipation of a CMOS digital circuit is several orders of magnitude smaller than the dynamic power. The leakage power problem mainly appears in very low frequency circuits or ones with "sleep modes" where dynamic activities are suppressed.

Most leakage reduction techniques are applied at low-level design abstraction such as process, device and circuit design. Memory chips that have very high device density are most susceptible to high leakage power. Static current can be reduced by transistor sizing, layout techniques and careful circuit design. Circuit modules that consume static current should be turned off if not used. Sometimes, static current depends on the logic state of its output and we can consider reversing the signal polarity to minimize the probability of static current flow.

Emerging Low Power Approaches

The low power digital design requires optimization at all levels of the design hierarchy which includes:

- **Technology, Devices,**
- **Circuits, Logic,**
- **Architecture (Structure),**
- **Algorithm (Behavior) and**
- **System Levels, as is illustrated in Figure**

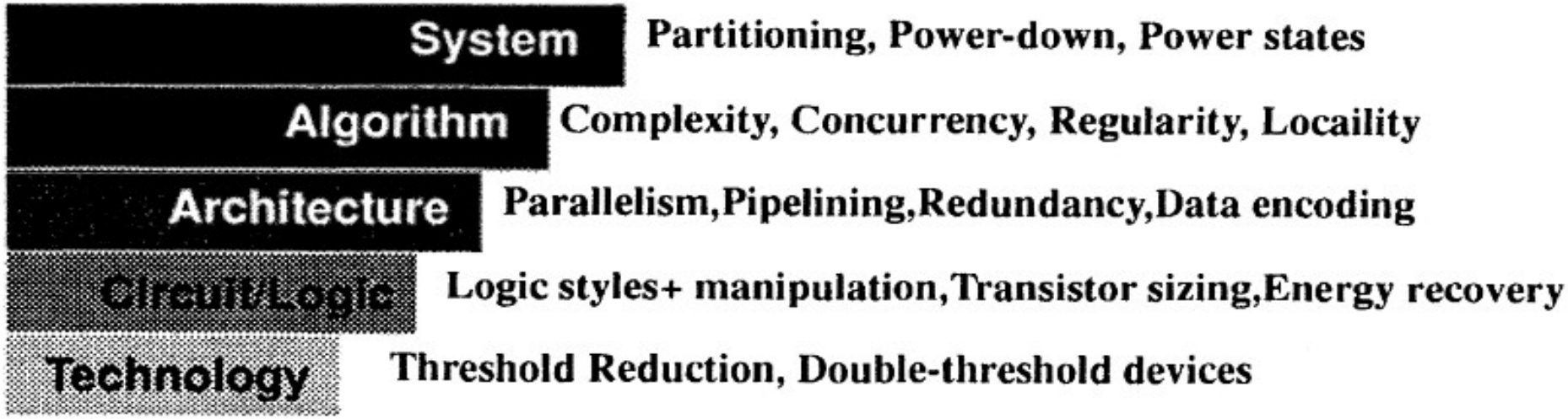


Fig: An integrated low-power methodology requires optimization at all design abstraction layers.

- **Silicon CMOS technology, Technology Scaling, GaAs, SOI.**

  SOl is an attractive evolutionary new technology that reduces capacitance and increases current.

- **The main parameters controlling circuit power consumption CMOS circuit techniques, complementary pass transistor logic, static logic, dynamic flip-flops, double-edge-triggered flip-flops.**

Other Circuit and gate level methods includes:

- **Reduced supply voltage**
- **Adiabatic switching**
- **Logic design for reduced activity**
- **Transistor sizing**
- **Pass-transistor logic**
- **Pseudo-nMOS logic**
- **Multi-threshold gates**

The power analysis and minimization at the logic and module levels includes:

- Dynamic power reduction techniques
- Leakage power reduction

Low-power implementation techniques can be considered at all steps in the design hierarchy including power management at the system level and architectural level.

System level methods

- Microprocessors
- Arithmetic circuits
- Low power memory technology

Functional and architectural methods

- Clock suppression
- Clock frequency reduction
- Supply voltage reduction
- Power down
- Algorithmic and Software methods

The presented techniques and approaches ultimately all come down to a fundamental set of concepts like: dissipation is reduced by lowering either the supply voltage, the voltage swing, the physical capacitance, the switching activity or a combination of the above.

Physics of power dissipation in CMOS devices

MOS structure

Consider an ideal Metal Insulator Semiconductor (MIS) structure shown in figure1 . When the insulator is an oxide layer (typically thermal oxide) then this becomes a MOS structure.

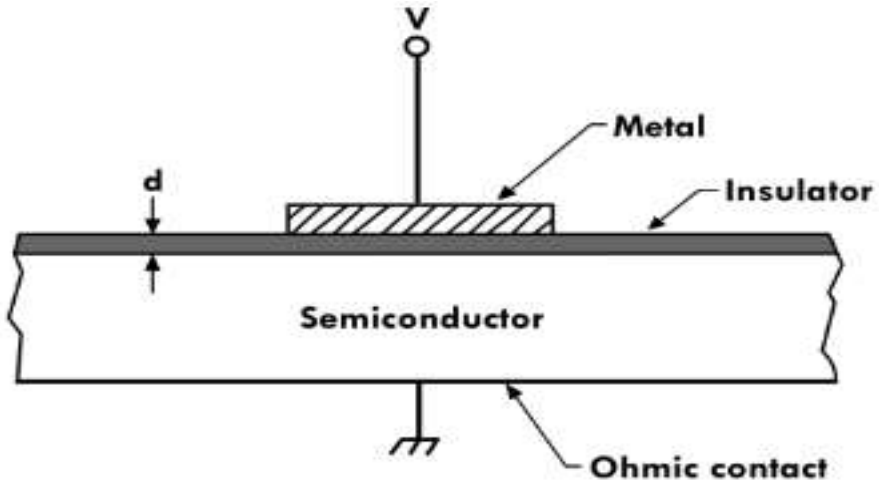


Fig1: Metal insulator semiconductor structure.

The energy-band diagram of an ideal un-biased MIS structure is shown in figure 2. for both n-type and p-type semiconductors.

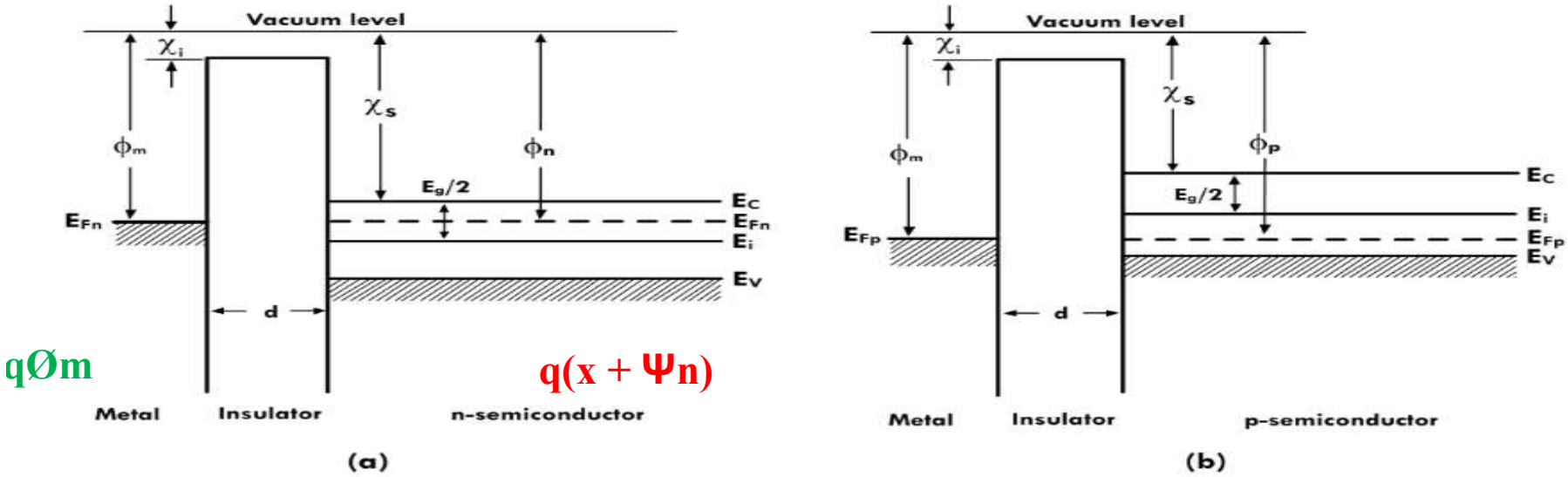


Fig 2: Energy bands in an unbiased MIS Structure (a) n and (b) p type semiconductor.

For an ideal MOS device the work functions of the metal and semiconductor are equal. i.e. The energy difference Øms between the metal work function(Øm) and s/c work function is zero.

$$\phi_{ms} \equiv \phi_m - \left(\chi + \frac{E_g}{2q} + \psi_B \right) = 0$$

where χ is the semiconductor electron affinity,[2] E_g the band gap, ϕ_B the potential barrier[3] between the metal and the insulator, and ψ_B the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i.

In an ideal MIS diode, the insulator has infinite resistance and not having charge carriers , so the Fermi level in the metal lines up with the Fermi level in the s/c.

So the Fermi levels line up at equilibrium, without any band bending or charge accumulation or depletion at the semiconductor interface.

The work function is the energy difference between the vacuum level and the Fermi level. This quantity is denoted by qØm for the metal, and is equal to q(x + Ψn) in the semiconductor, where qx is the electron affinity measured from the bottom of the conduction band Ec, to the vacuum level, and qΨn *is the energy difference between Ec* and the Fermi level, intrinsic Fermi level *Ei*.

When an ideal MIS Structure is biased with positive or negative voltages, basically three cases may exist at the semiconductor surface (Fig. 3). Consider the p-type semiconductor first. When a negative voltage ($V < 0$) is applied to the metal plate, the valence-band edge Ev, bends upward near the surface and is closer to the Fermi level (Fig. 3a). For an ideal MIS structure, no current flows in the structure, so the Fermi level remains flat in the semiconductor. This band bending causes an accumulation of majority carriers (holes) near the semiconductor surface. This is the accumulation case.

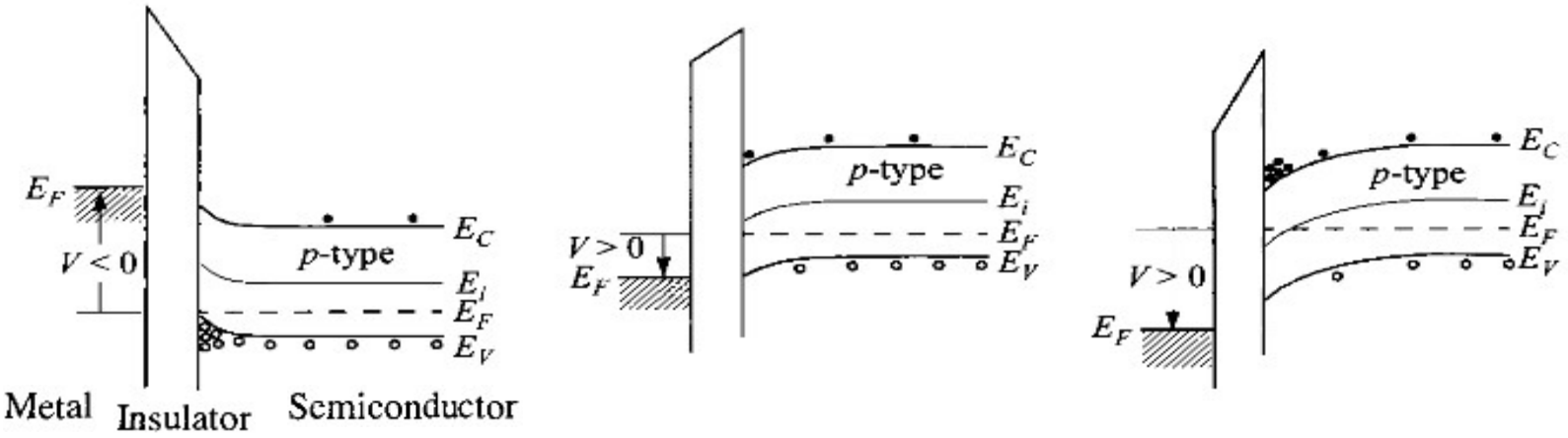
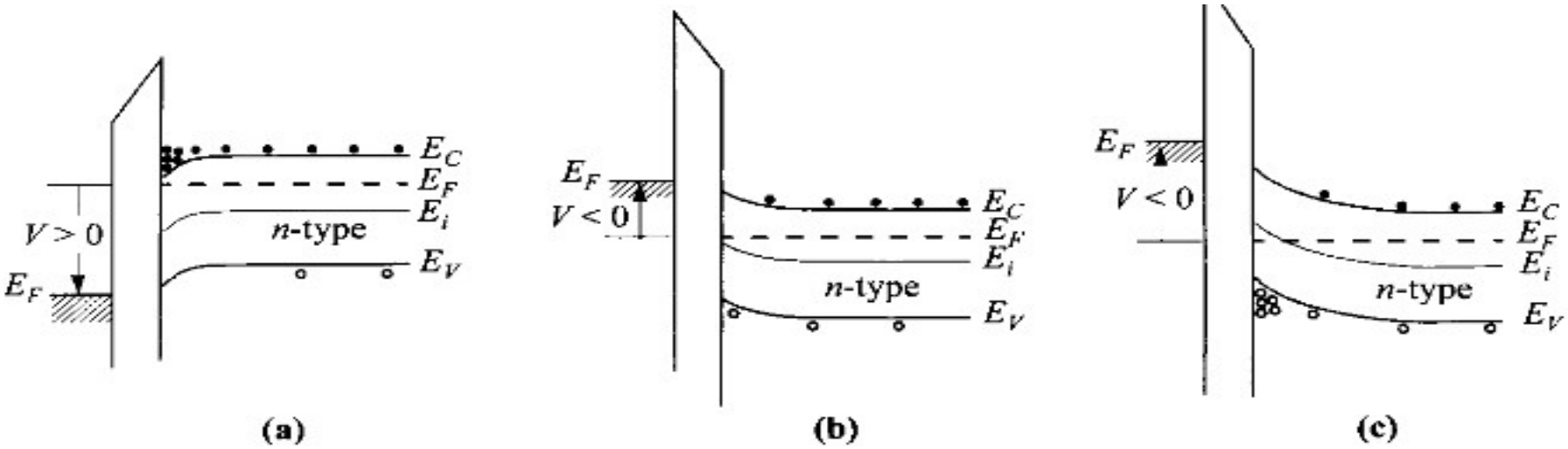


Fig3: Energy-band diagrams for ideal MIS capacitors under different bias, for the conditions of: (a) accumulation, (b) depletion, and **(c) inversion** for p-type semiconductor substrates

When a small positive voltage (V>0) is applied, the bands bend downward, and the majority carriers are depleted The depletion region extending from surface into the s/c (Fig. 3b). This is the depletion case. The positive voltage on gate attracts electrons in the s/c to surface. The surface is said to be inverting from the original p-type to n-type. This is called weak inversion condition.

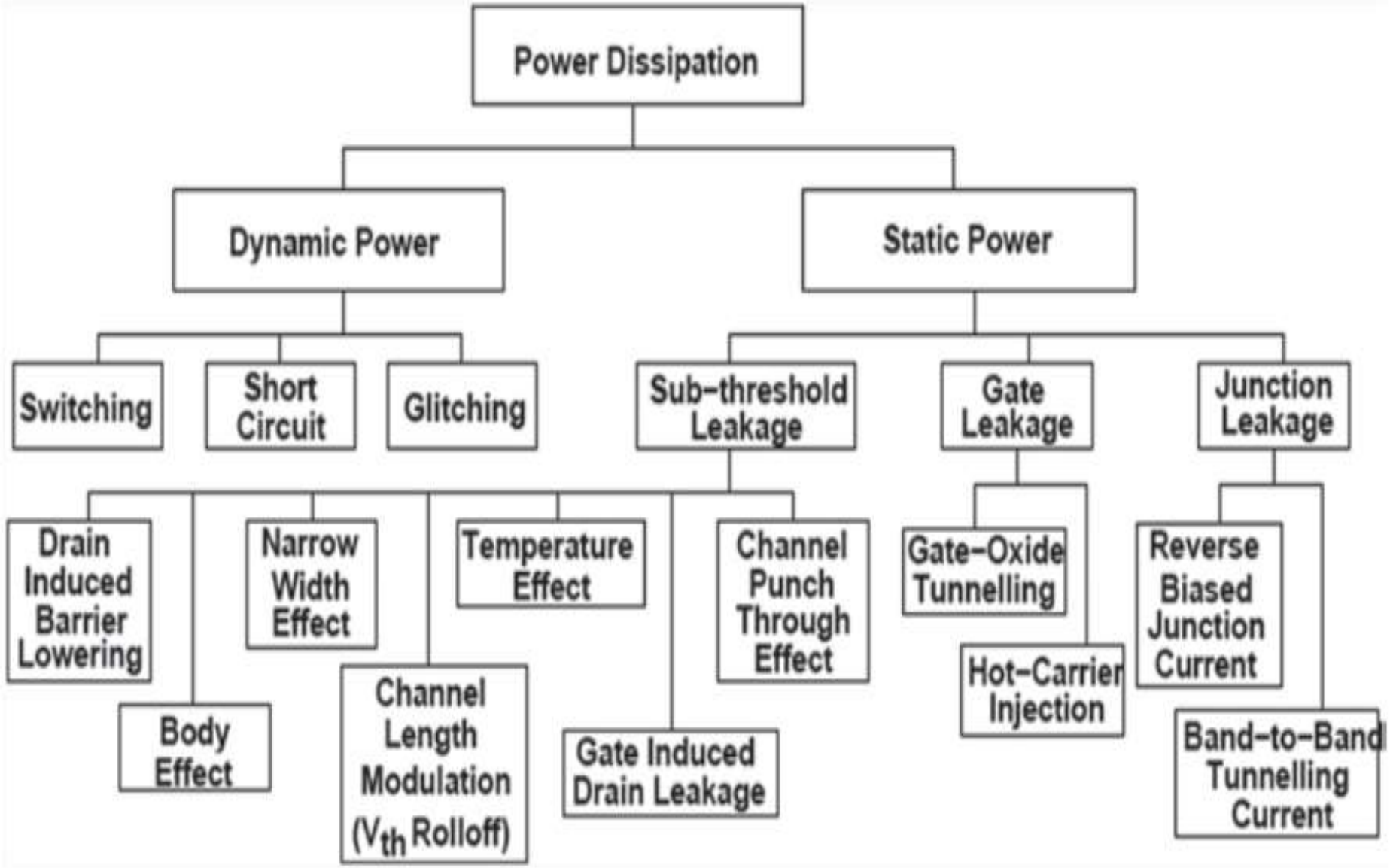
When the applied positive voltage is increased sufficiently, the bands bend even more downward so that the intrinsic level Ei at the surface crosses over the Fermi level EF (Fig. 3c). At this point the number of electrons (minority carriers) at the surface is larger than that of the holes, the surface is thus inverted and this is the *inversion case*.

Similar results can be obtained for the n-type semiconductor. The polarity of the voltage, however, should be changed for the n-type semiconductor.



Energy-band diagrams for ideal MIS capacitors under different bias, for the conditions of: (a) accumulation, (b) depletion, and (c) inversion for n-type semiconductor substrates

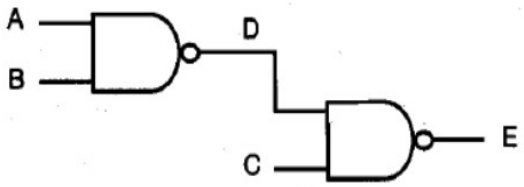
Types of power dissipation

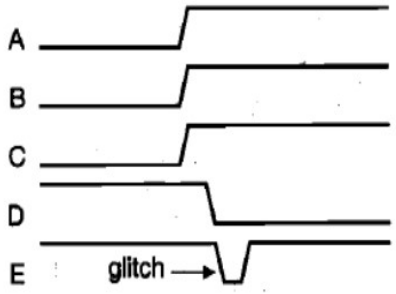


Glitching Power Dissipation

Glitches occur because the input signals to a particular logic block arrive at different times, causing a number of intermediate transitions to occur before the output of the logic block stabilizes. These additional transitions result in power dissipation, which is categorized as the glitching power.

Since the dynamic power is directly proportional to the number of output transitions of a logic gate, glitching can be a significant source of signal activity.





Signal glitching in multi-level static CMOS circuits

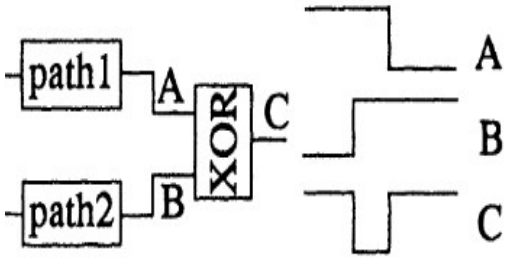


Fig: CMOS XOR Gate

Static Power

Static power dissipation takes place as long as the device is powered on, even when there are no signal changes. Normally in CMOS circuits, in the steady state, there is no direct path from *Vdd* to GND and so there should be no static power dissipation, but there are various leakage current mechanisms which are responsible for static power dissipation. Since the MOS transistors are not perfect switches, there will be leakage currents and substrate injection currents, which will give rise to static power dissipation in CMOS.

Leakage currents are also normally negligible, in the order of nano-amps, compared to dynamic power dissipation. But with deep submicron technologies, the leakage currents are increasing drastically.

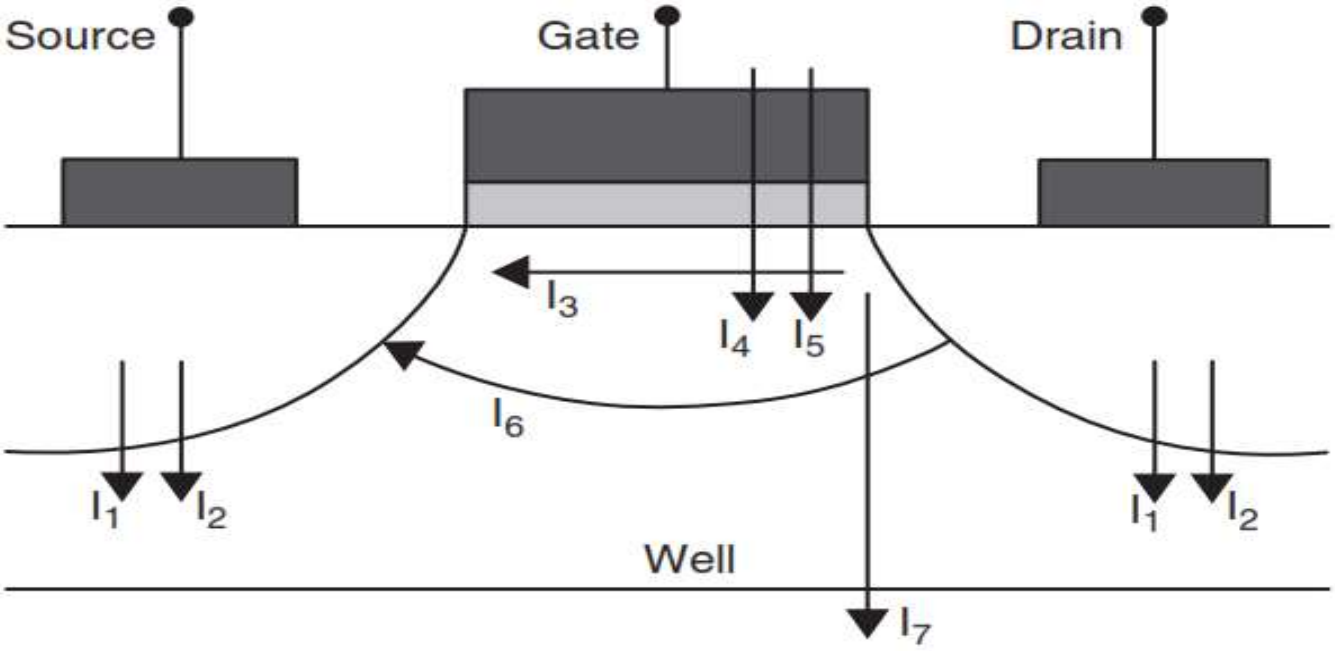


Fig: Leakage currents in an MOS transistor.

Figure shows several leakage mechanisms that are responsible for static power dissipation. Here:

I1 is the reverse-bias p–n junction diode leakage current,

I2 is the reverse-biased p–n junction current due to tunneling of electrons from the valence band of the p region to the conduction band of the n region

I3 is the sub-threshold leakage current between the source and the drain when the gate voltage is less than the threshold voltage (*Vt*),

I4 is the oxide tunneling current due to reduction in the oxide thickness,

I5 is the gate current due to hot carrier injection of electrons (I4 and I5 are commonly known as IGATE leakage current),

I6 is the gate-induced drain leakage current due to high field effect in the drain junction, and

I7 is the channel punch through current due to close proximity of the drain and the source in short-channel devices.

Gate Oxide Tunneling/Leakage Current

In short channel devices, a thin gate oxide results in high electric fields across the SiO_2 layer. Low oxide thickness with high electric fields results in electrons tunneling from the substrate to the gate and from the gate to the substrate through the gate oxide, resulting in gate oxide tunneling current

Gate current due to hot carrier injection of electrons :

In short channel devices, the high electric field near the substrate-oxide interface energizes the electrons or holes and they cross the substrate-oxide interface to enter the oxide layer. This phenomenon is known as hot carrier injection.

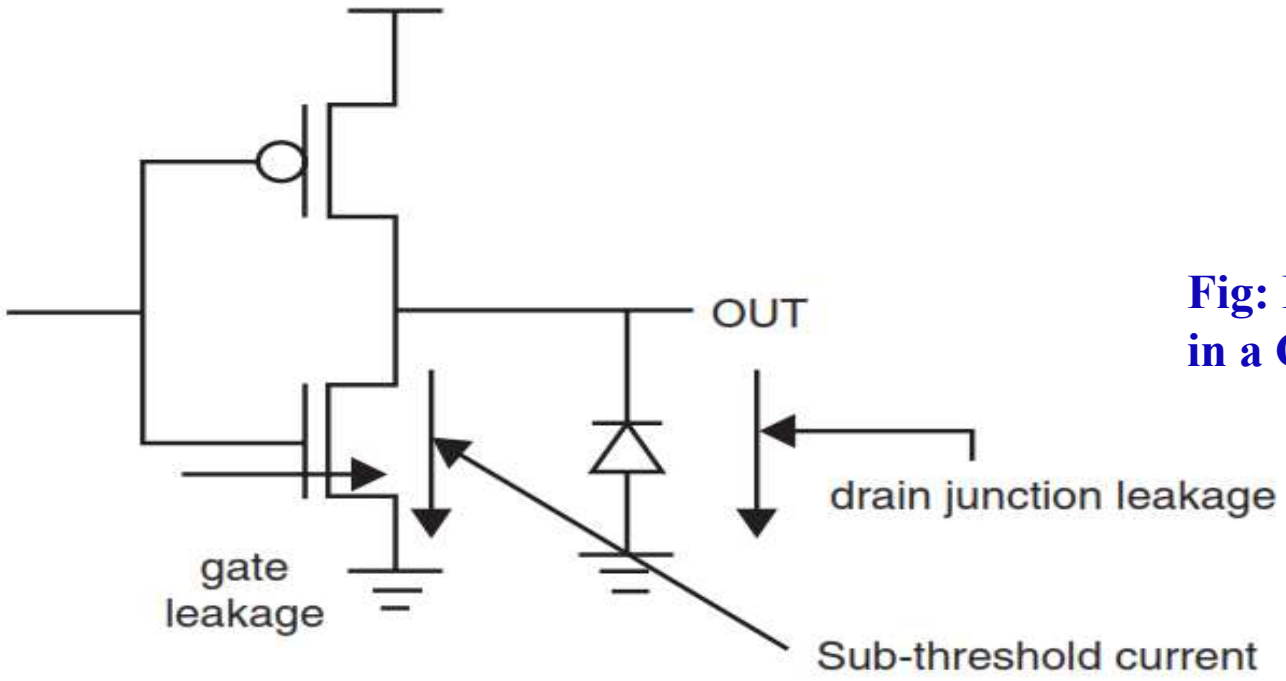


Fig: Leakage currents in a CMOS inverter.

These are generally categorized into four major types:

i) Sub-threshold leakage, ii) gate leakage,

iii) gate-induced drain leakage, and

iv) junction leakage as shown in Fig.

1) Body Effect (Substrate bias effect)

The variation of threshold voltage due to source to substrate voltage is called body effect.

We have considered a transistor to be a three-terminal device with gate, source, and drain.

However, the body is an implicit fourth terminal. The potential difference between the source and body Vsb affects the threshold voltage.

The threshold voltage can be modeled as

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

where Vt0 is the threshold voltage when the source is at the body potential(i.e source & substrate are shorted),

Φs is the surface potential at threshold and is given by

$$\phi_s = 2v_T \ln\frac{N_A}{n_i}$$

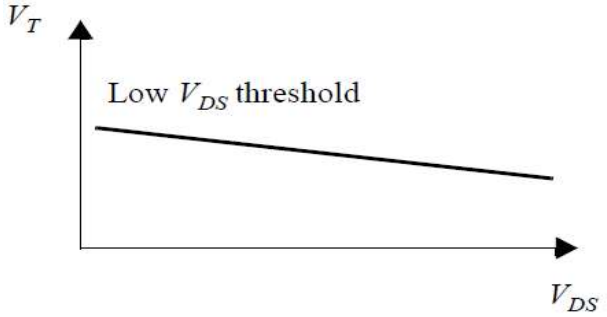
γ is the body effect coefficient, typically in the range 0.4 to 1

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

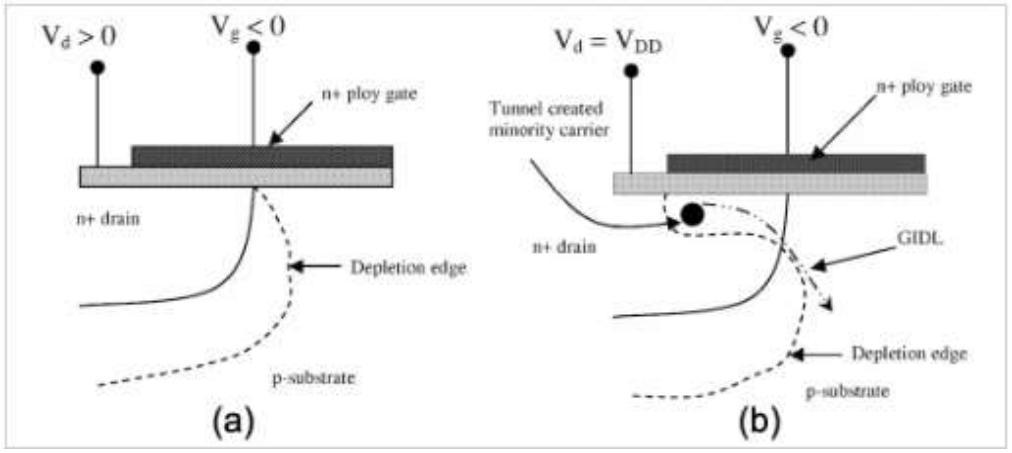
Thus, the variation of threshold voltage due to source to substrate voltage is called body effect.

2) Drain - induced Barrier Lowering (DIBL)

Increasing the drain to source (Vds) voltage leads to increase the width of the drain-junction depletion region. Consequently, the threshold voltage decreases with increasing *VDS*. This effect, called the drain-induced barrier lowering (DIBL)



3)Gate Induced Drain leakage



a)Formation of thin depletion region at the drain-substrate interface (b) flow of GIDL current due to carriers generated

Consider an NMOS transistor with a p-type substrate. When there is a negative/zero voltage at the gate terminal, positive charges accumulate just at the oxide-substrate interface. Due to the accumulated holes at the substrate, the surface behaves as a p-region more heavily doped than the substrate.

This results in a thinner depletion region at the surface along the drain-substrate interface (when compared to the thickness of the depletion region in the bulk).

Due to a thin depletion region and higher electric fields, the minority carriers in the drain region underneath the gate are generated and are pushed into the substrate by the negative gate voltage. This adds to the leakage current.