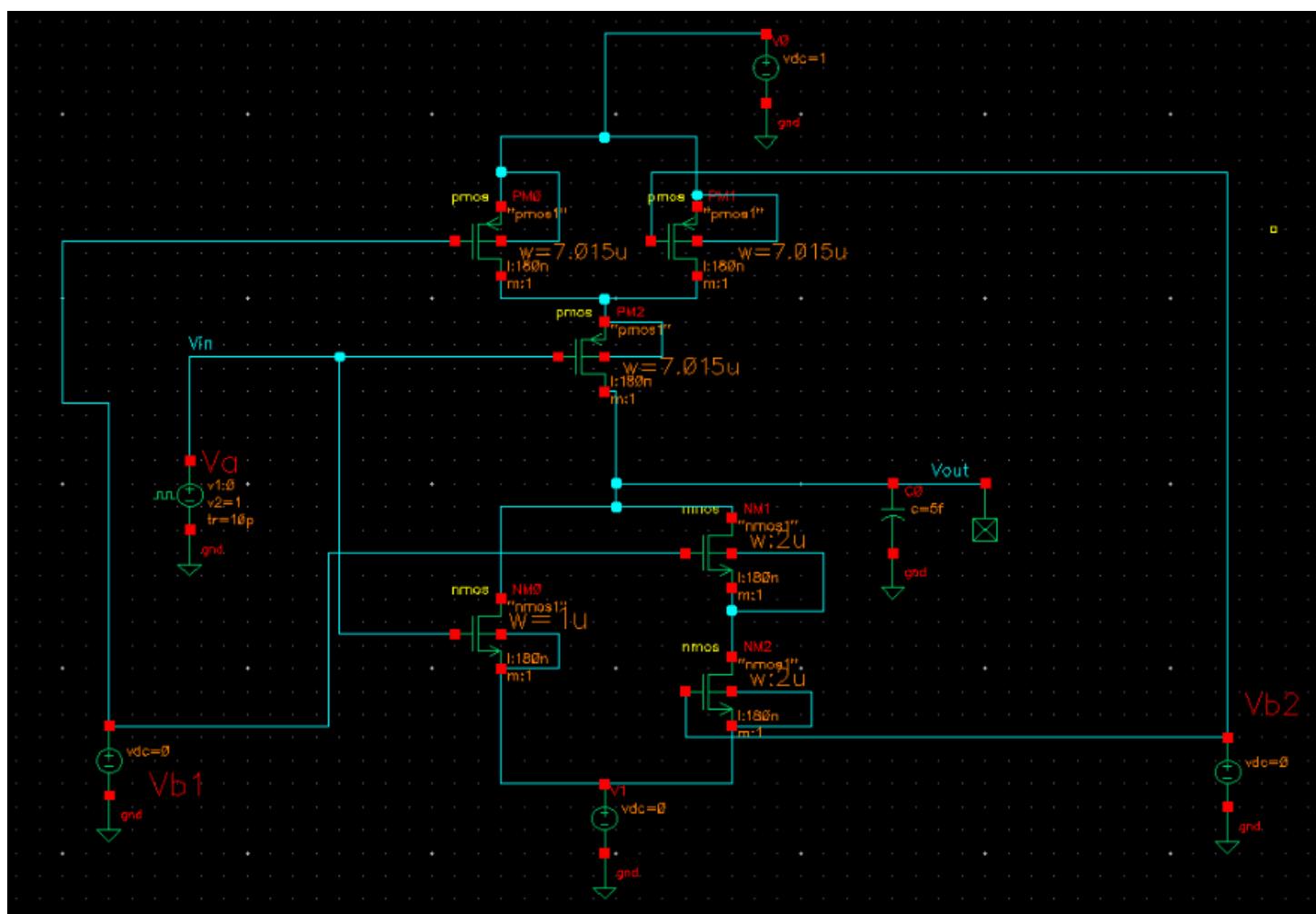


EE619- Project -3

Team SUPERKINGS

AOI21 schematic 1

Priyansh Singh , Anand Gaurav

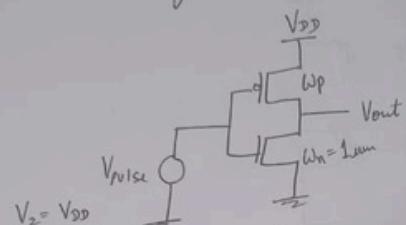


^{a. Power} \rightarrow steady state power $P_{avg} = \frac{V_{DD}^2}{R}$ [All current consumption now used at output node]

AOI21 ($F = A + B_1 B_2$) (schematic)

first reference inverter is designed and β is calculated taking

$$W_n = 1 \mu m \text{ using } t_{PHL} = t_{PLH}.$$



$$V_2 = V_{DD}, V_1 = 0.$$

$$T = 2.0 \mu s, \text{ sufficient time.}$$

Pulsewidth = $10\mu s$

trise + tfall = $10\mu s$. for worst case delay.

for AOI21 ($F = A + B_1 B_2$)

for PMOS (schematic 1).

$$\frac{R}{K_a} + \frac{R}{K_b} = R$$

$$K_a = 2$$

$$\therefore K_b = 2B_1 \text{ (Sizing of all PMOS)}$$

NMOS

$$K_a = R$$

$$K_b = 1$$

NMOS sized at 1 with input A

$$\frac{R}{K_b} + \frac{R}{K_b} = R$$

$$K_b = 2$$

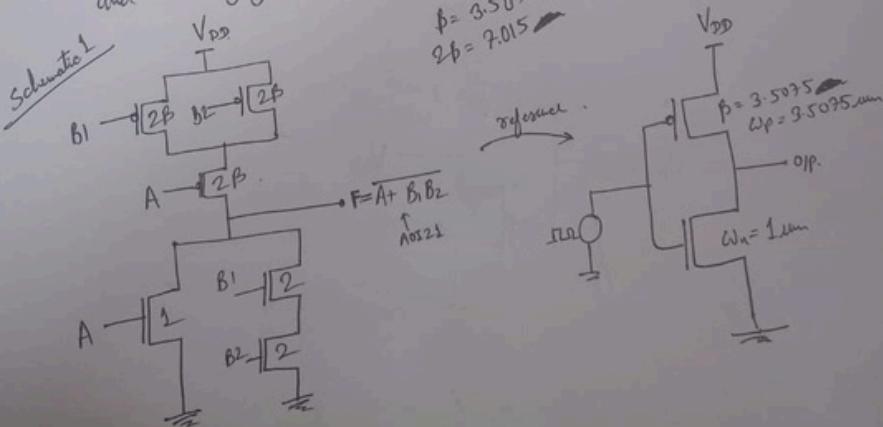
$$B_1 \& B_2 \text{ sized at 2.}$$

B By plotting t_{PHL} and t_{PLH} , we found their intersection point at

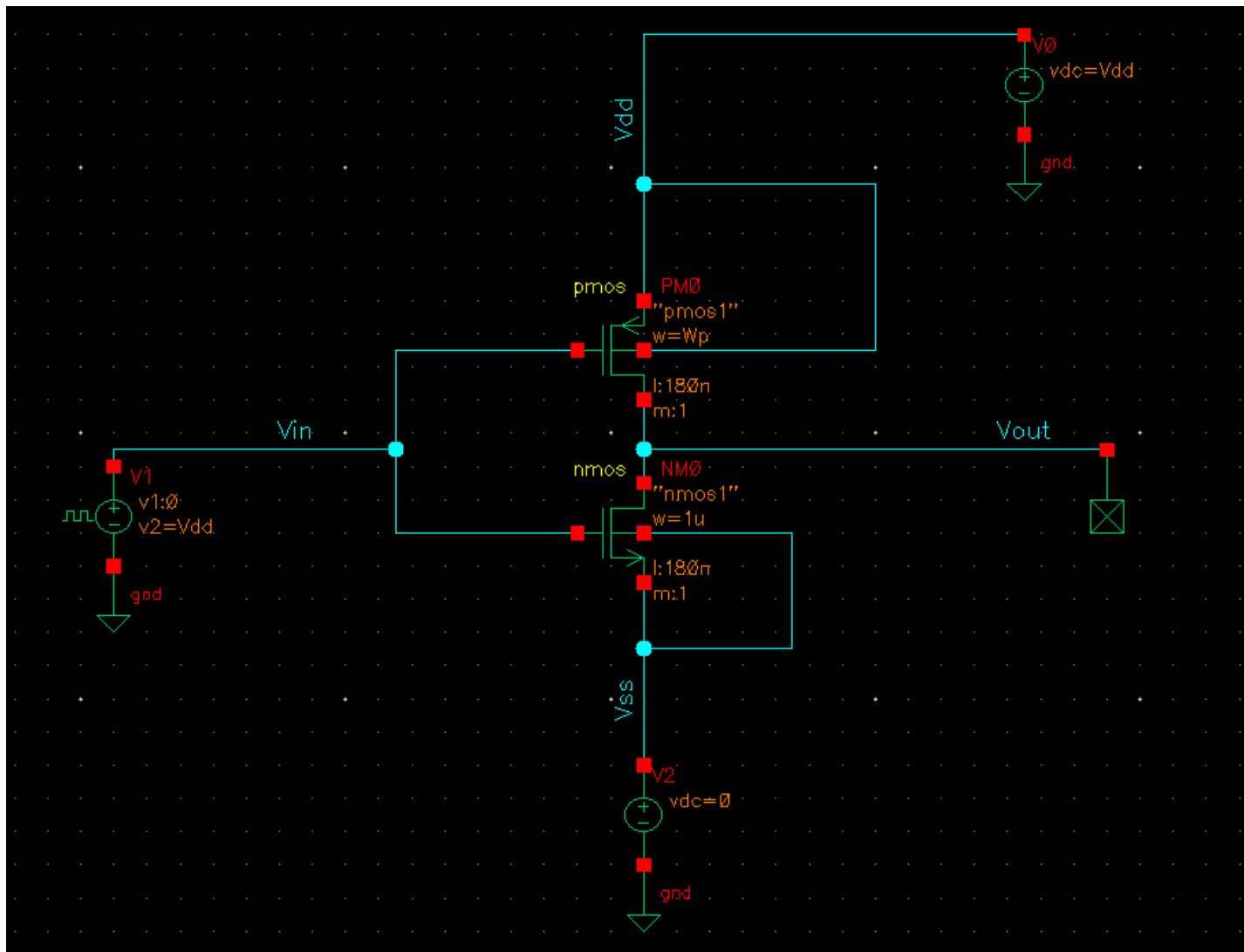
$$W_p = 3.5075 \mu m.$$

$$\text{Thus, } \beta = \frac{W_p}{W_n} = \frac{3.5075 \mu m}{1 \mu m} = 3.5075.$$

Using β we have done sizing of Txors in the AOI21 & OAII21, given for sizing, we have considered worst case delay / charging path / discharging path and made sure that worst case delay was equal for both charging and discharging.



Sizing(above)



reference CMOS inverter

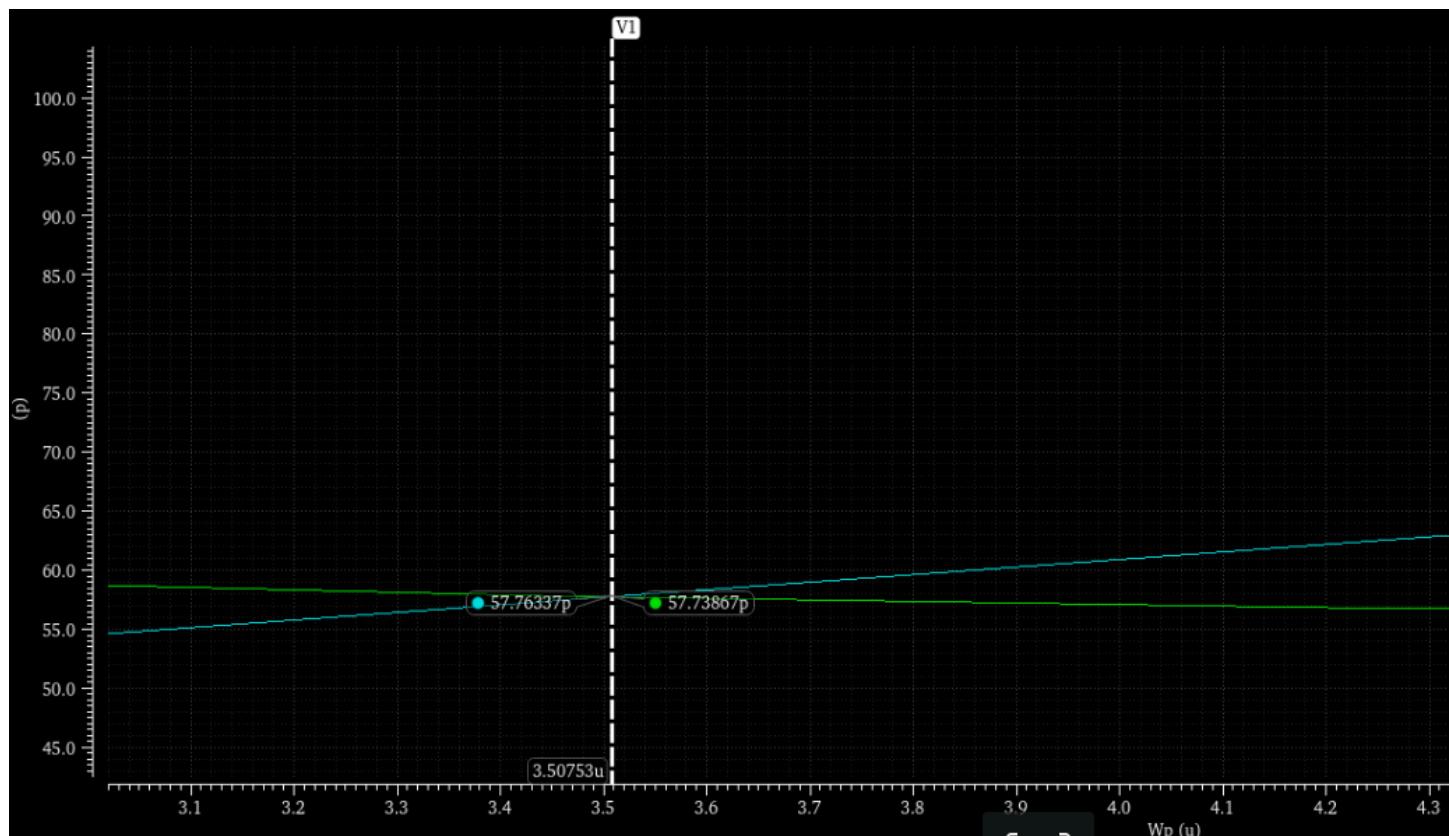


Table with propagation delays from schematic simulation

$\beta = 3.5075 \mu\text{m}$

$2\beta = 7.015 \mu\text{m}$

Delays of schematic 1 (All values are in ps)

AOI21 ($F = \frac{1}{A + B_1 B_2}$)

t_{pHl} from A to F ($B_1 = 0, B_2 = 0$)			t_{pLH} from A to F ($B_1 = 0, B_2 = 0$)		
Load capacitance	5 fF	50 fF	Load capacitance	5 fF	50 fF
Input transition			Input transition		
10 ps	80.8	208.17	10 ps	57.28	108.7
100 ps	101.15	231.31	100 ps	79.12	180.42

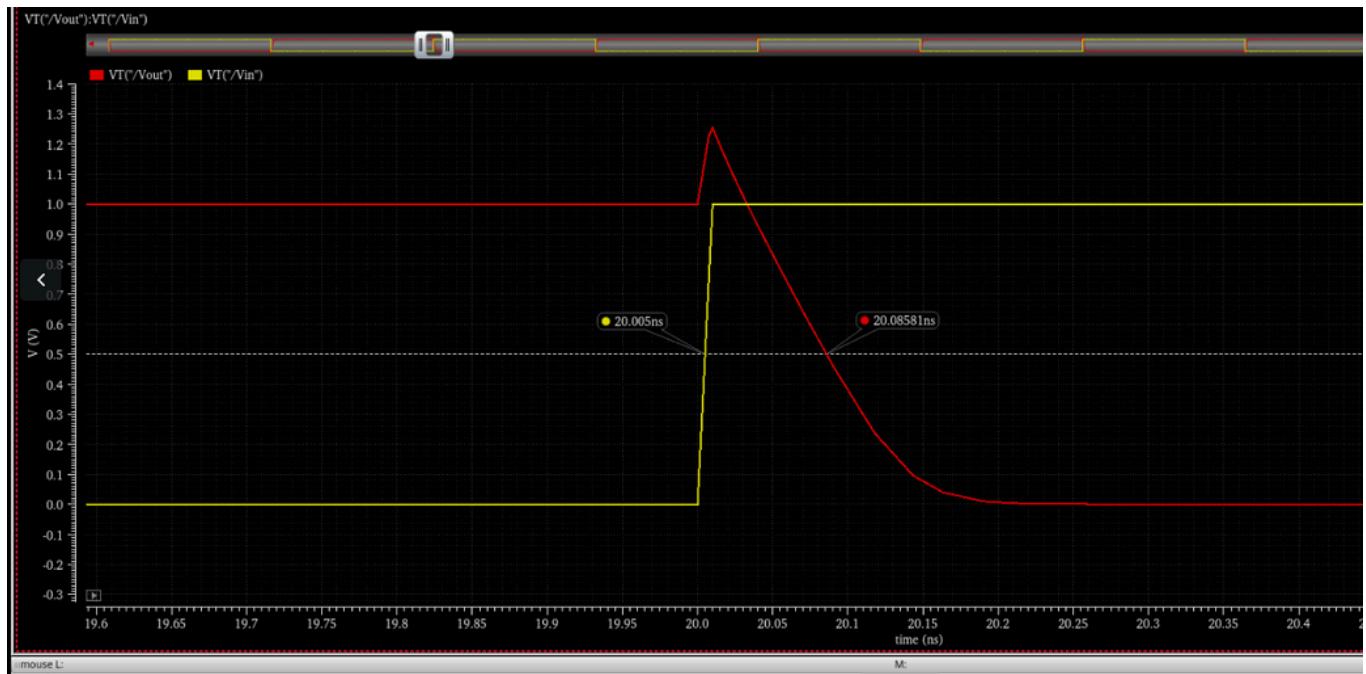
t_{pHl} from A to F ($B_1 = 0, B_2 = 1$)			t_{pLH} from A to F ($B_1 = 0, B_2 = 1$)		
Load capacitance	5 fF	50 fF	Load capacitance	5 fF	50 fF
Input transition			Input transition		
10 ps	81.63	209.3	10 ps	74.48	207.94
100 ps	102.69	233.25	100 ps	92.67	227.27

t_{pHl} from A to F ($B_1 = 1, B_2 = 0$)			t_{pLH} from A to F ($B_1 = 1, B_2 = 0$)		
Load capacitance	5 fF	50 fF	Load capacitance	5 fF	50 fF
Input transition			Input transition		
10 ps	81	208.31	10 ps	82.73	218.02
100 ps	101.7	232.5	100 ps	101.3	237.26

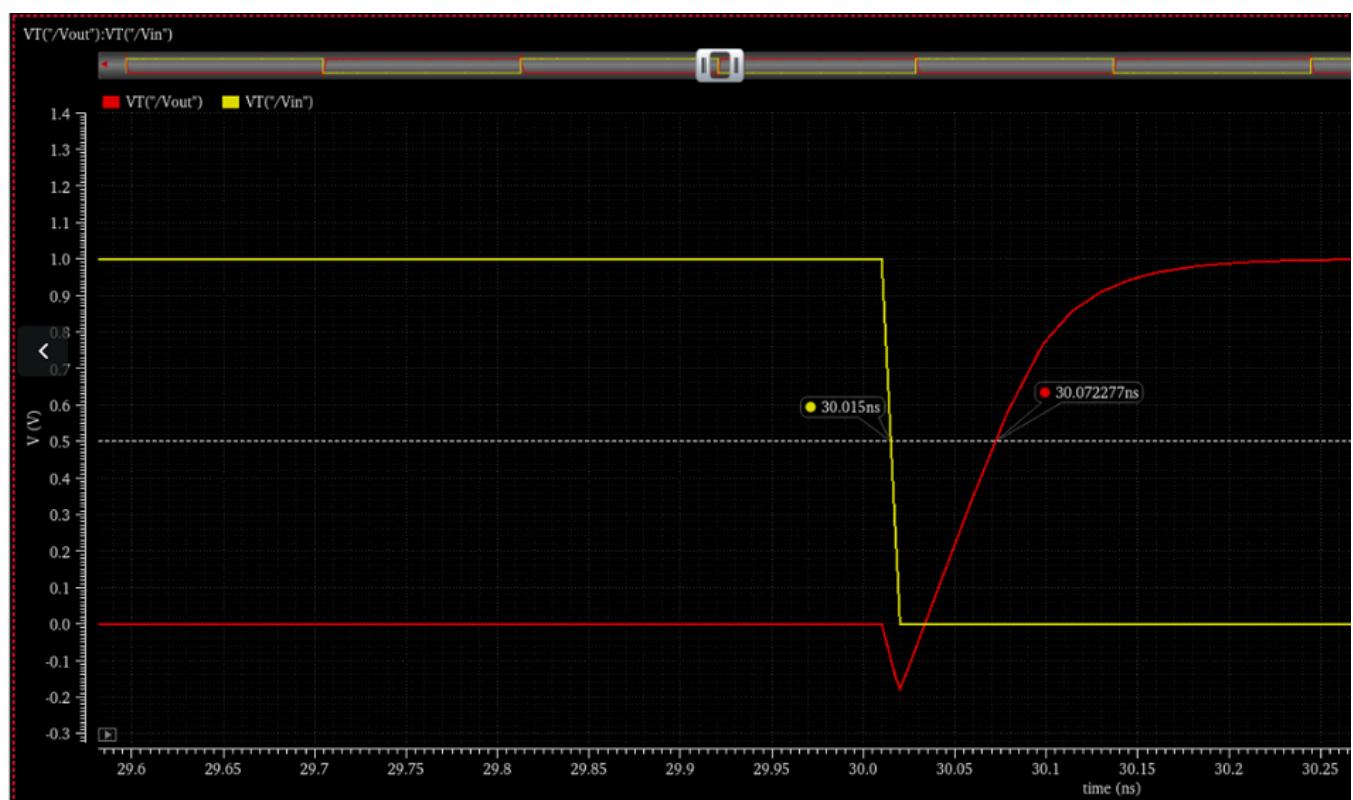
Table 1: Propagation delay from A to F in AOI21 based on schematic simulations.

Transient analysis waveforms of input and output from schematic (For B1=0 B2=0 and rise/fall=10ps , C=5fF)

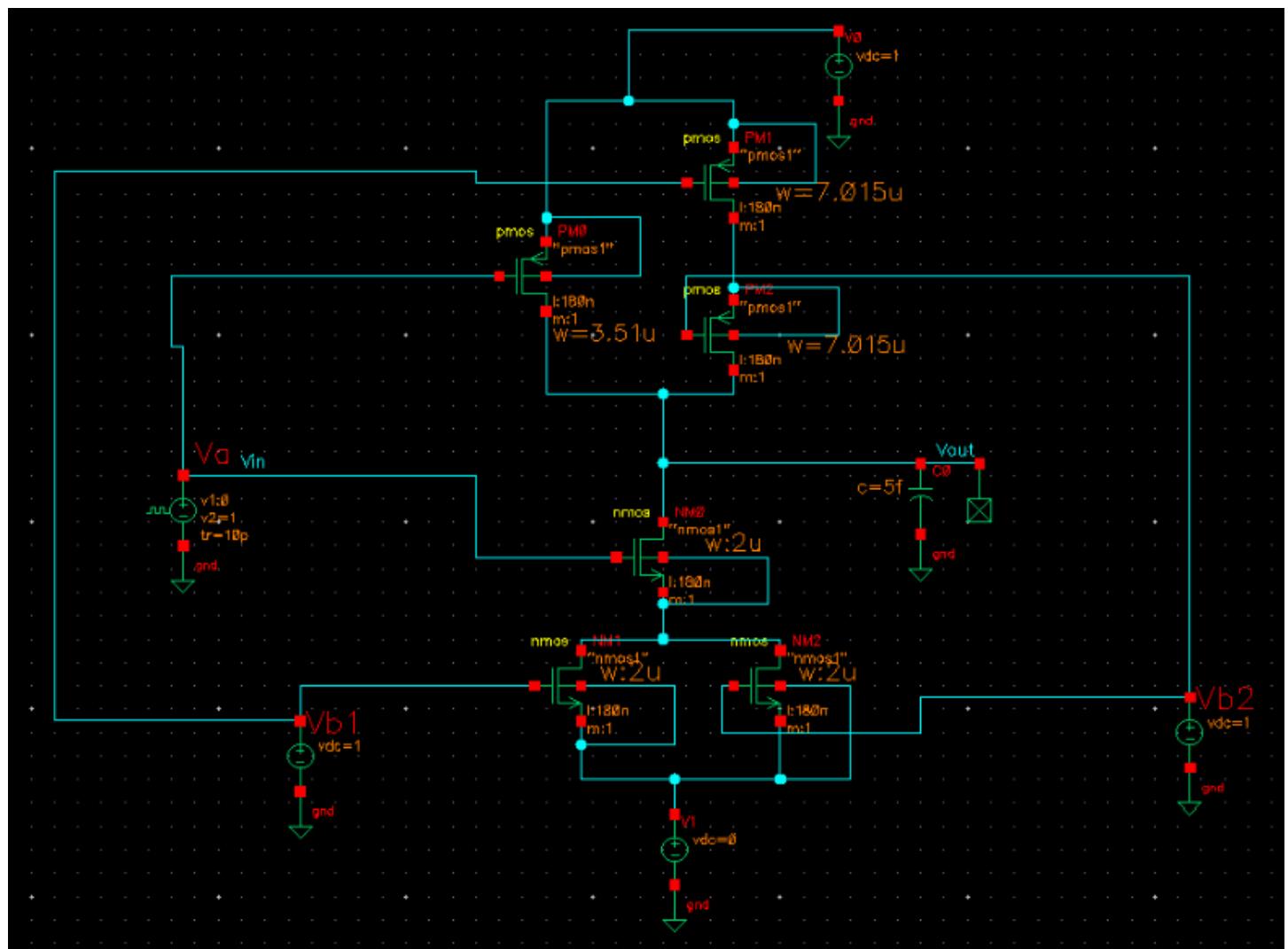
TpHL



tpLH

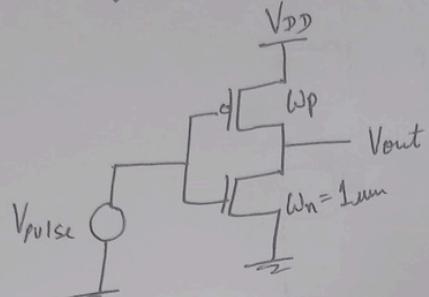


OAI21 schematic 2



first reference inverter is designed and β is calculated taking

$$W_n = 1 \text{ mm} \text{ using } t_{PHL} = t_{PLH}$$



$$V_2 = V_{DD}$$

$$V_1 = 0.$$

$$T = 20 \text{ ns}$$

Pulsewidth = 10 ns } sufficient time.

$$t_{rise} = t_{fall} = 10 \text{ ps. for worst case delay.}$$

By plotting t_{PHL} and t_{PLH} , we found their intersection point at

$$W_p = 3.5075 \text{ mm.}$$

$$\text{Thus, } \beta = \frac{W_p}{W_n} = \frac{3.5075 \text{ mm}}{1 \text{ mm}} = 3.5075.$$

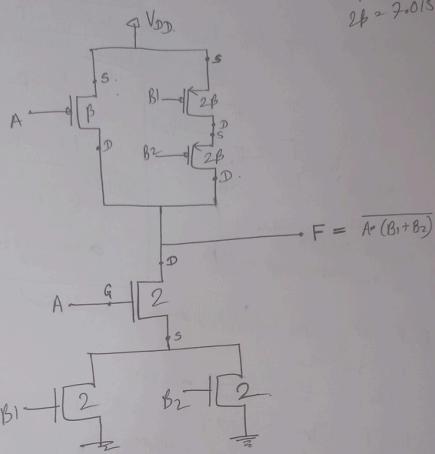
Using β we have done sizing of Txers in the AOI21 & OAI21, given.
for sizing, we have considered worst case delay / charging path / discharging path
and made sure that worst case delays are equal for both charging
and discharging.

OA121

$$F = \overline{A \cdot (B_1 + B_2)}$$

(Schematic)

$$\begin{aligned} \beta &= 3.5075 \\ 2\beta &= 7.015 \end{aligned}$$



$$\text{Sizing for OA121: } F = \overline{A \cdot (B_1 + B_2)}$$

PMOS :-

$$\frac{R}{K_A} = R$$

$$K_A = 1$$

$A \rightarrow 1 \times B \rightarrow A$ is sized at β .

$$\frac{R}{K_B} + \frac{R}{K_B} = R$$

$$K_B = 2$$

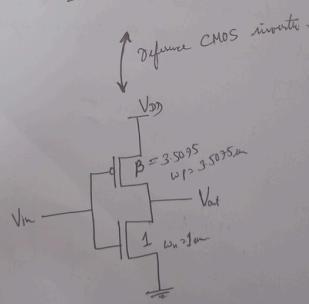
B_1 & B_2 PMOS Trans are sized as $K_B = 2\beta = 2 \cdot 7.015 \mu m$.
 B_1, B_2 are β led at $2\beta = 7.015 \mu m$.

NMOS :-

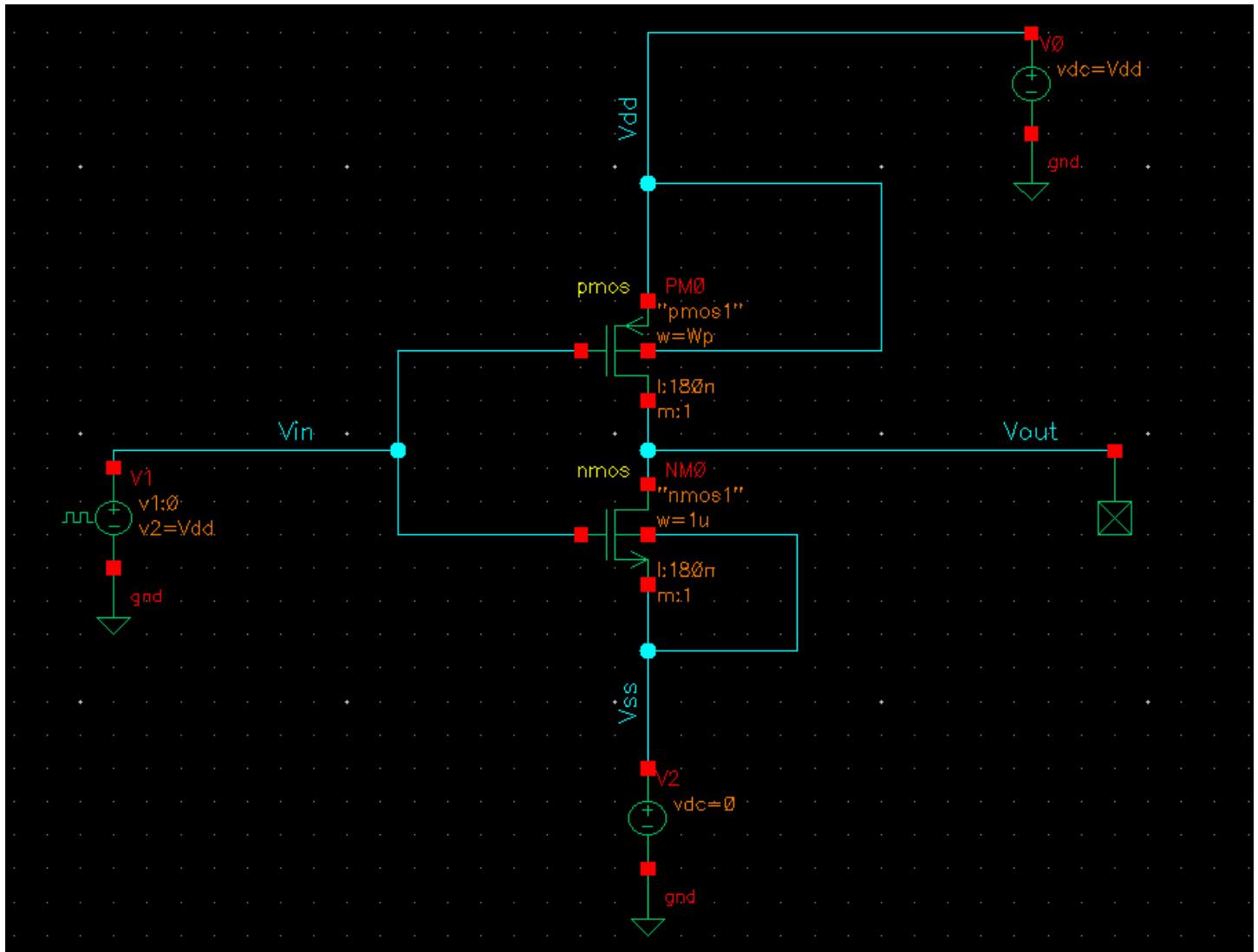
$$\frac{R}{K} + \frac{R}{K} = R.$$

$$K = 2$$

all NMOS sized at 2



sizing is explained above.



above is ref cmos inverter and below is the diagram for getting Beta.

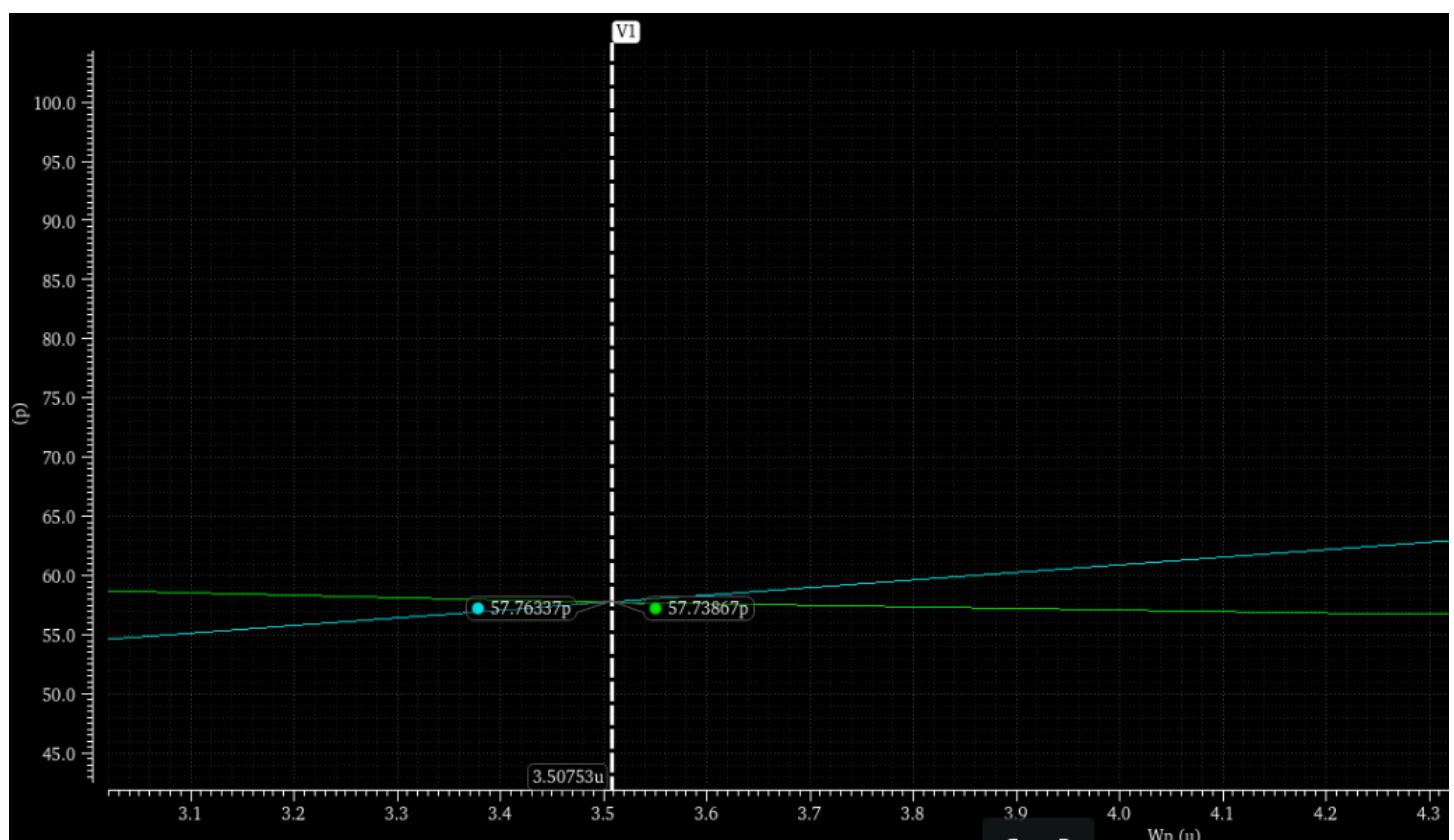


Table with propagation delays from schematic simulation

$B_1 = 3.507 \mu m$
 $2B_2 = 7.015 \mu m$

(All values are in pico seconds)
 Delay of schedule 2

$OAI21 (F = \overline{A} \cdot (\overline{B}_1 + B_2))$

t_{pHL} from A to F ($B_1 = 0, B_2 = 0$)		
	5 fF	50 fF
Input transition		
10 ps	56.2	144.53
100 ps	79.73	168.53

t_{pHL} from A to F ($B_1 = 0, B_2 = 1$)		
	5 fF	50 fF
Input transition		
10 ps	75.7	191.76
100 ps	97.37	213.29

t_{pHL} from A to F ($B_1 = 1, B_2 = 0$)		
	5 fF	50 fF
Input transition		
10 ps	93.9	215.07
100 ps	116	237.8

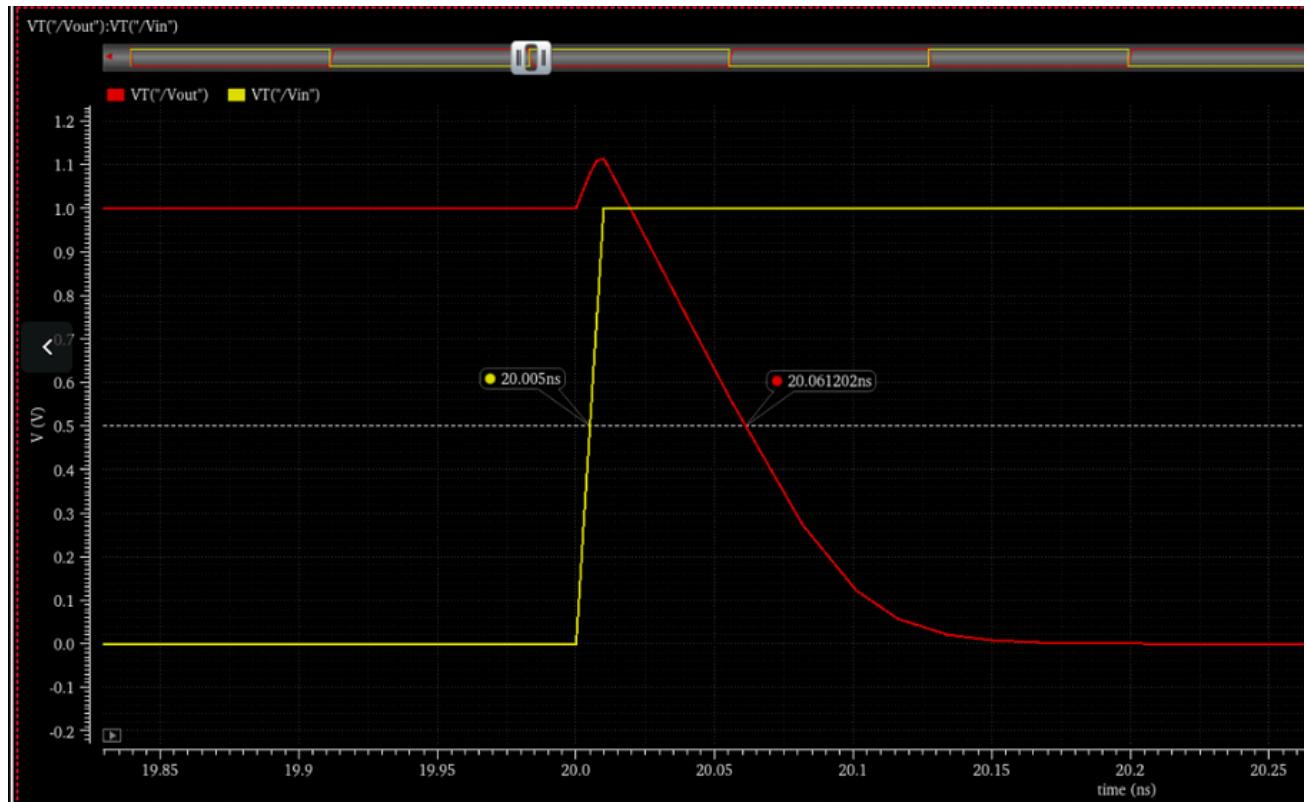
t_{pLH} from A to F ($B_1 = 0, B_2 = 0$)		
	5 fF	50 fF
Input transition		
10 ps	79.6	215.4
100 ps	104.16	242.47

t_{pLH} from A to F ($B_1 = 0, B_2 = 1$)		
	5 fF	50 fF
Input transition		
10 ps	84.17	226.4 ps
100 ps	109.3	248.33

t_{pLH} from A to F ($B_1 = 1, B_2 = 0$)		
	5 fF	50 fF
Input transition		
10 ps	80.35	216.99
100 ps	106	241.74

Transient analysis waveforms of input and output from schematic (For B1=1 B2=1 and rise/fall=10ps , C=5fF)

tpHL



tpLH

