EE619 - Project 3

Standard Cells designed:

- AOI21 [F = ~(A + B1.B2)]
- OAI21 [F = ~(A.(B1 + B2))]

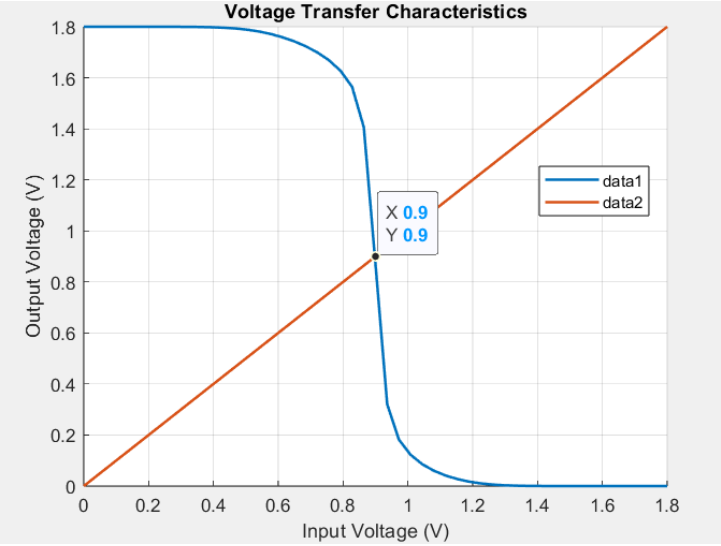
Sizing of Reference Inverter:

Firstly, we size a reference inverter, and then size the transistors of the OAI21 gate. For sizing the reference inverter, we use the condition that $V_M = V_{DD} / 2$ (same PUN & PDN driving strength). We use the results of Assignment – 2, where the inverter sizes was found to be:
$L_n = L_p = 180$ nm

$W_n = 400$ nm

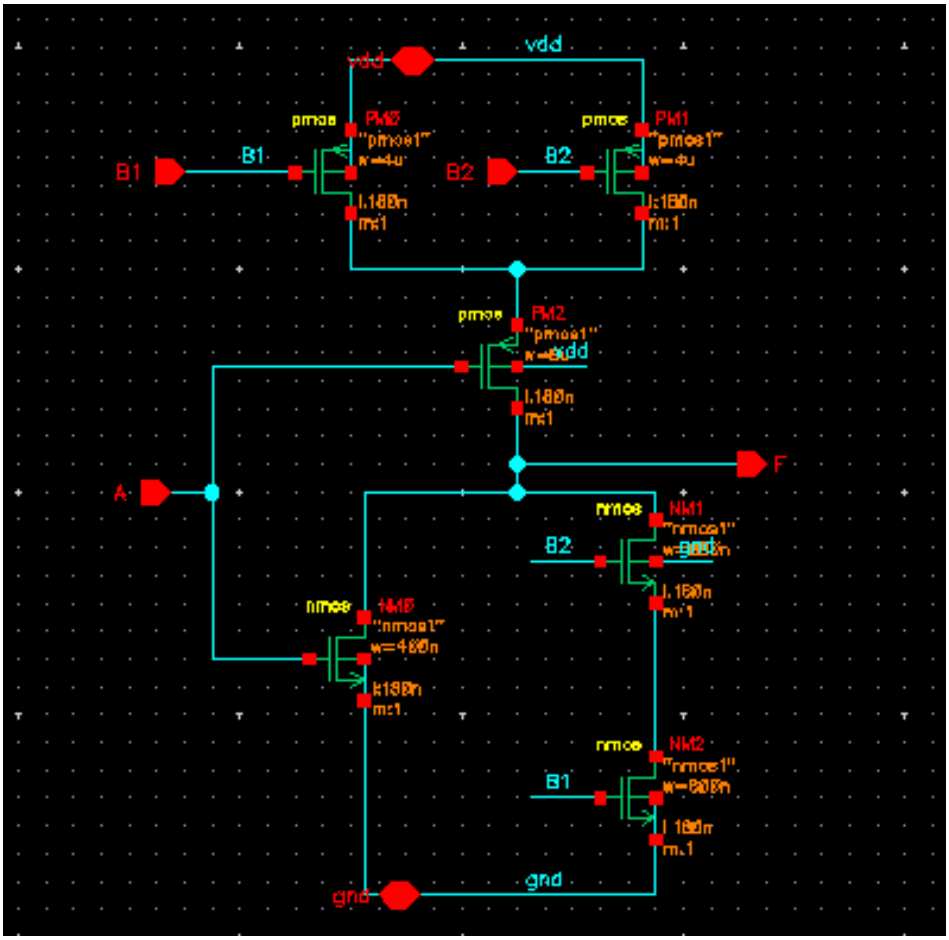
$W_p = 2000$ nm.

The graph of Vout vs Vin for this inverter is:

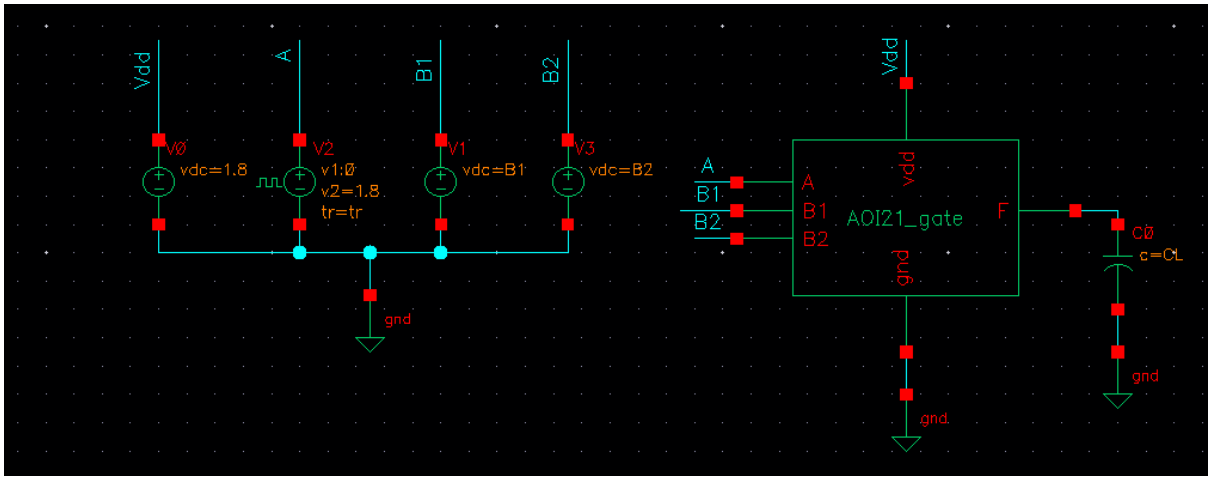


AOI21 Gate

Circuit Schematic



Test Bench Schematic



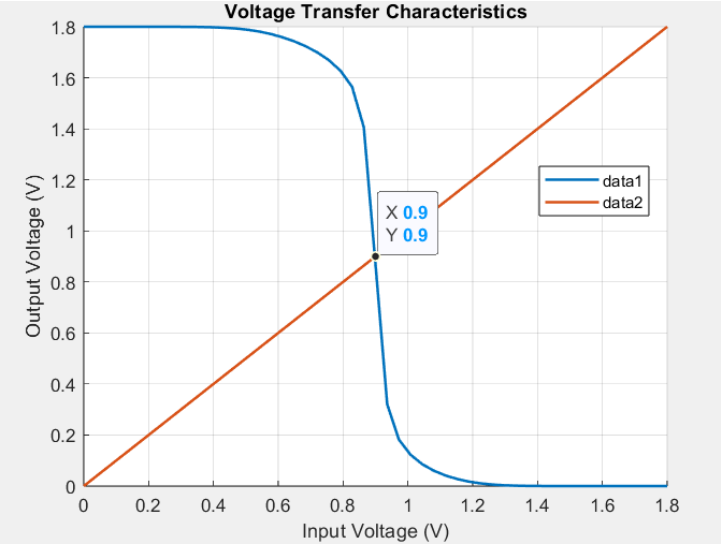
Sizing of transistors

Firstly, we size a reference inverter, and then size the transistors of the AOI21 gate. For sizing the reference inverter, we use the condition that $V_M = V_{DD} / 2$ (same PUN & PDN driving strength). We use the results of Assignment – 2, where the inverter sizes was found to be:
$L_n = L_p = 180$ nm

$W_n = 400$ nm

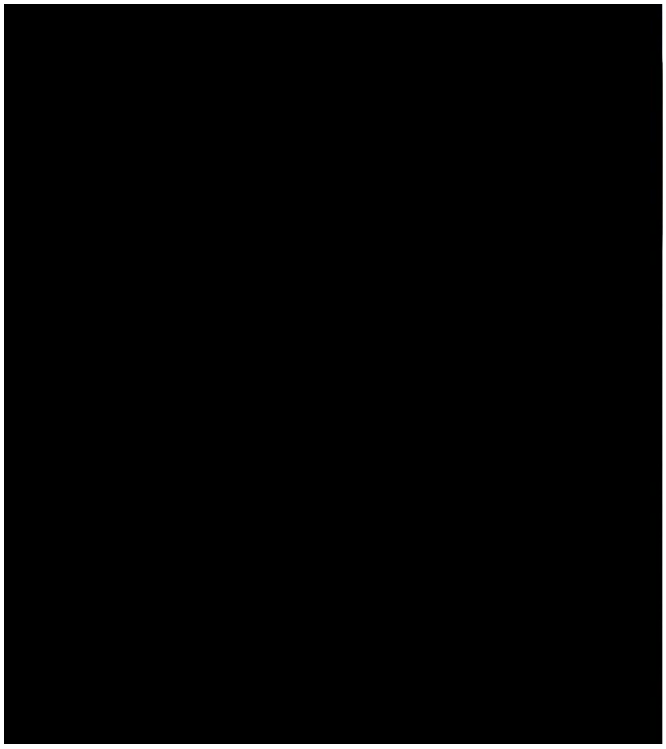
$W_p = 2000$ nm.

The graph of Vout vs Vin for this inverter is:

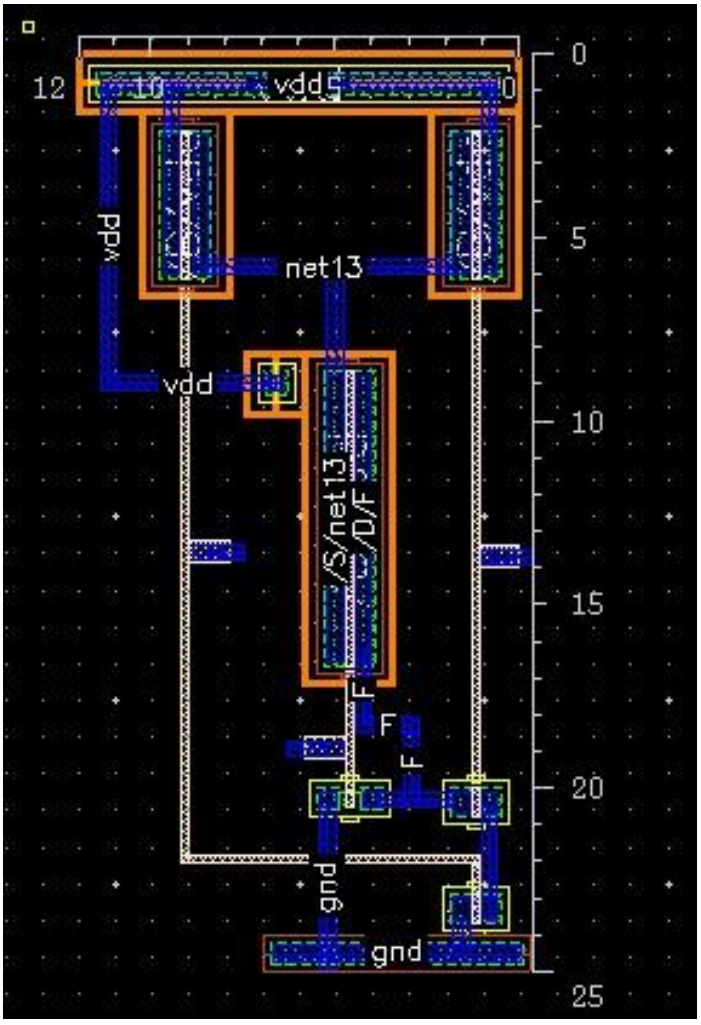


With this, the sizing of the transistors in the AOI21 gate are done to match the drive strength of the reference inverter.

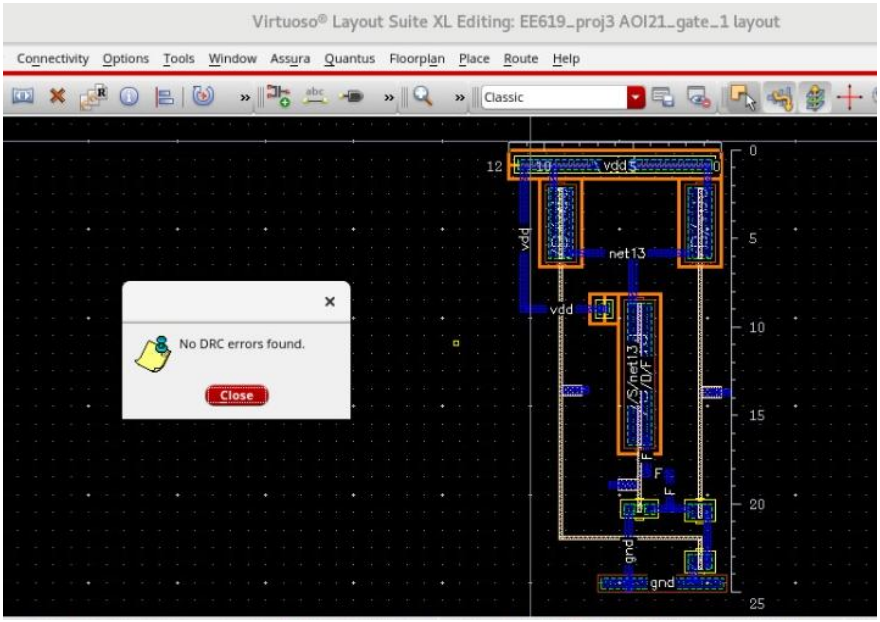
Hence, the size finally chosen is:



Layout Screenshot:

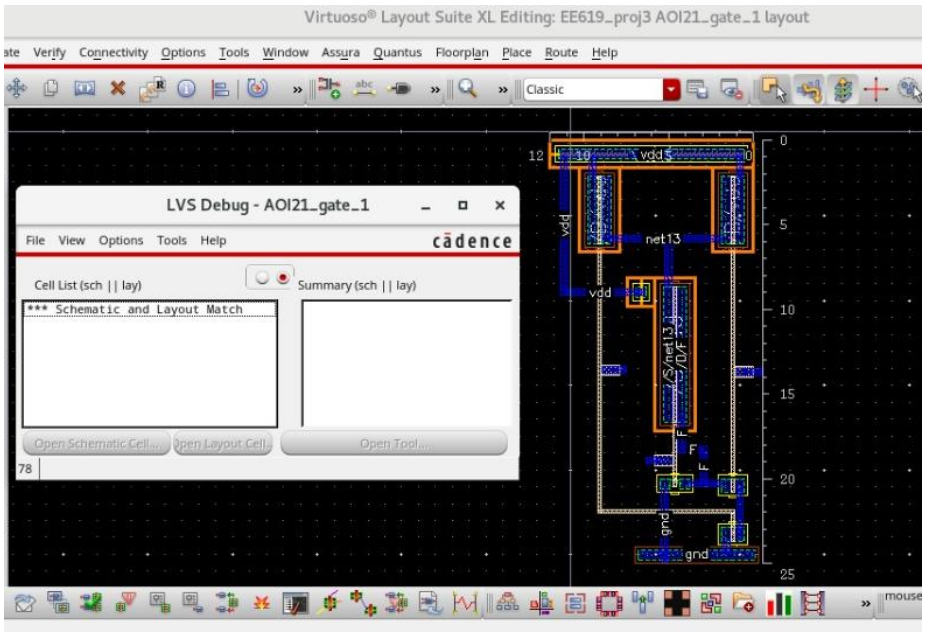


DRC Check:



Screenshot of the layout with the DRC log – AOI21 gate

LVS Check



Screenshot of the layout with the LVS log – AOI21 gate

Propagation delay values from the **Schematic simulation**

T_{pHL} from A to F ($B_1 = 0$, $B_2 = 0$)			T_{pLH} from A to F ($B_1 = 0$, $B_2 = 0$)	
Load capacitance	5 fF	50 fF	5 fF	50 fF
Input transition				
10 ps	102.279 ps	257.548 ps	23.6118 ps	69.8883 ps
100 ps	105.046 ps	265.151 ps	37.972 ps	85.1956 ps

T_{pHL} from A to F ($B_1 = 0$, $B_2 = 1$)			T_{pLH} from A to F ($B_1 = 0$, $B_2 = 1$)	
Load capacitance	5 fF	50 fF	5 fF	50 fF
Input transition				
10 ps	102.582 ps	256.785 ps	30.938 ps	96.3784 ps
100 ps	106.56 ps	266.028 ps	45.4516 ps	109.339 ps

T_{pHL} from A to F ($B_1 = 1$, $B_2 = 0$)			T_{pLH} from A to F ($B_1 = 1$, $B_2 = 0$)	
Load capacitance	5 fF	50 fF	5 fF	50 fF
Input transition				
10 ps	103.129 ps	257.322 ps	31.0496 ps	101.752 ps
100 ps	108.224 ps	267.672 ps	46.0696 ps	115.305 ps

Propagation delay values from the **Post Layout Simulations:**

T_{pHL} from A to F ($B_1 = 0$, $B_2 = 0$)			T_{pLH} from A to F ($B_1 = 0$, $B_2 = 0$)	
Load capacitance	5 fF	50 fF	5 fF	50 fF
Input transition				
10 ps	108.327 ps	262.331 ps	26.5071 ps	72.813 ps
100 ps	111.119 ps	270.543 ps	41.1895 ps	88.0867 ps

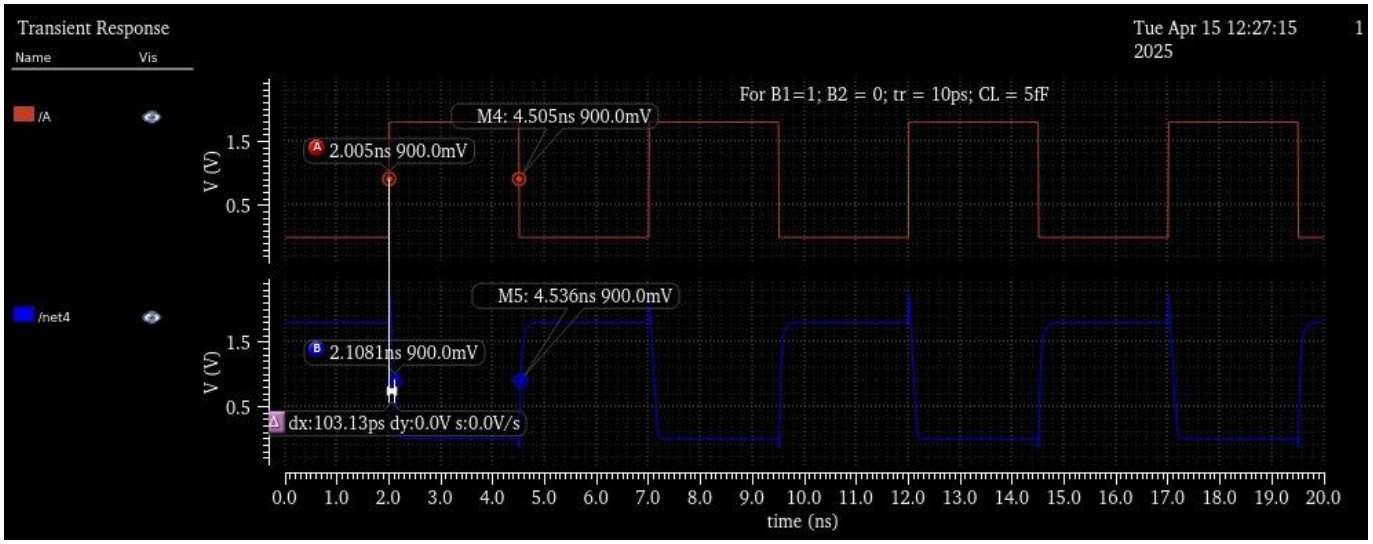
T_{pHL} from A to F ($B_1 = 0$, $B_2 = 1$)			T_{pLH} from A to F ($B_1 = 0$, $B_2 = 1$)	
Load capacitance	5 fF	50 fF	5 fF	50 fF
Input transition				
10 ps	110.56 ps	265.791 ps	39.4776 ps	110.776 ps
100 ps	115.976 ps	277.196 ps	54.1432 ps	124.582 ps

T_{pHL} from A to F ($B_1 = 1$, $B_2 = 0$)			T_{pLH} from A to F ($B_1 = 1$, $B_2 = 0$)	
Load capacitance	5 fF	50 fF	5 fF	50 fF
Input transition				
10 ps	109.095 ps	263.143 ps	33.8222 ps	104.667 ps
100 ps	114.471 ps	274.374 ps	48.8546 ps	117.881 ps

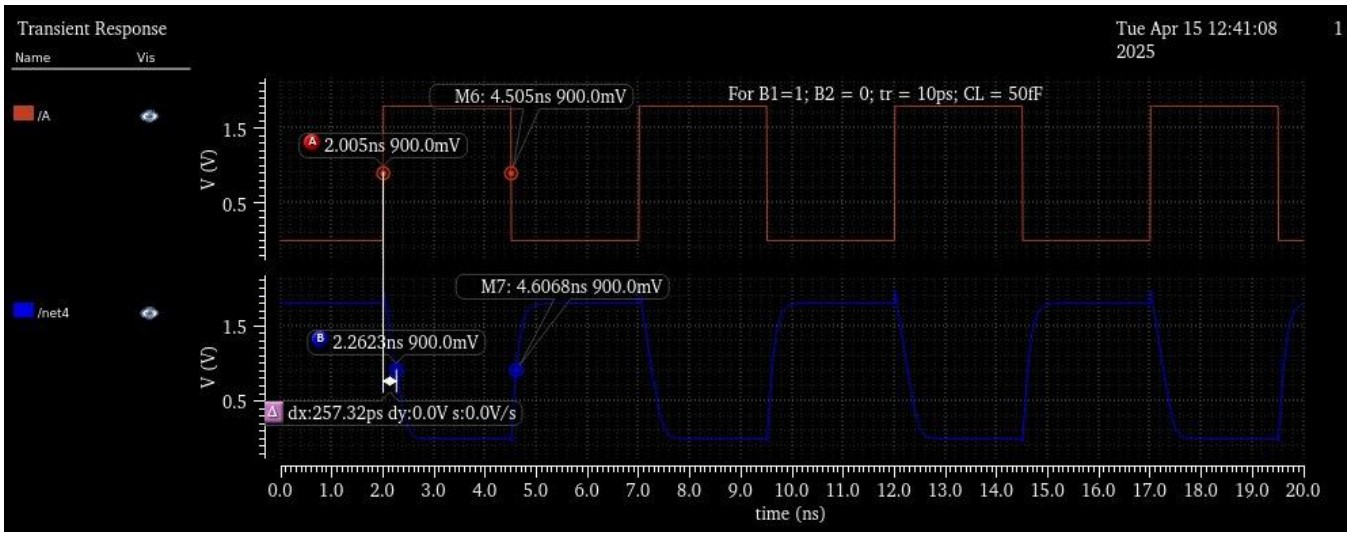
Waveform from transient analysis:

For Input transition: (B1 = 1; B2 = 0; A -> F)

Schematic Simulations:

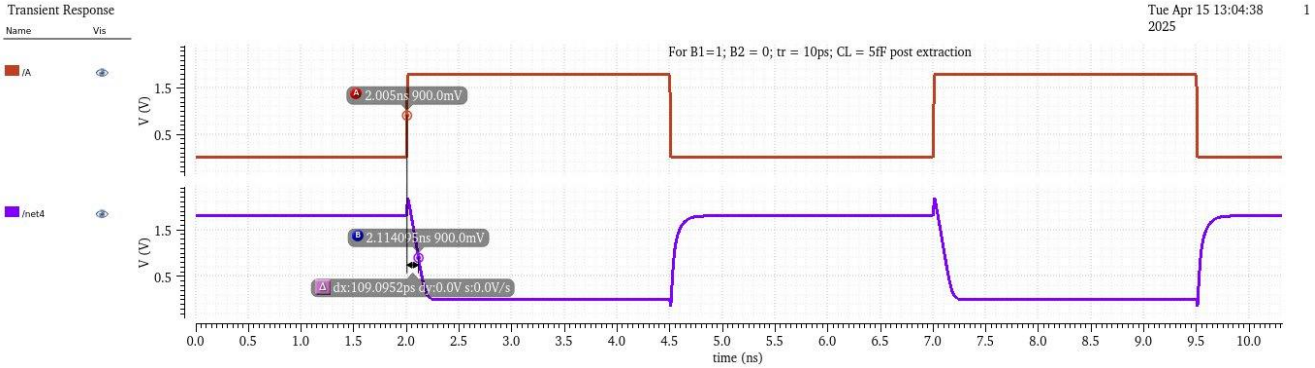


For 5 fF fanout capacitance, for 10 ps input transition time. (B1 = 1; B2 = 0)

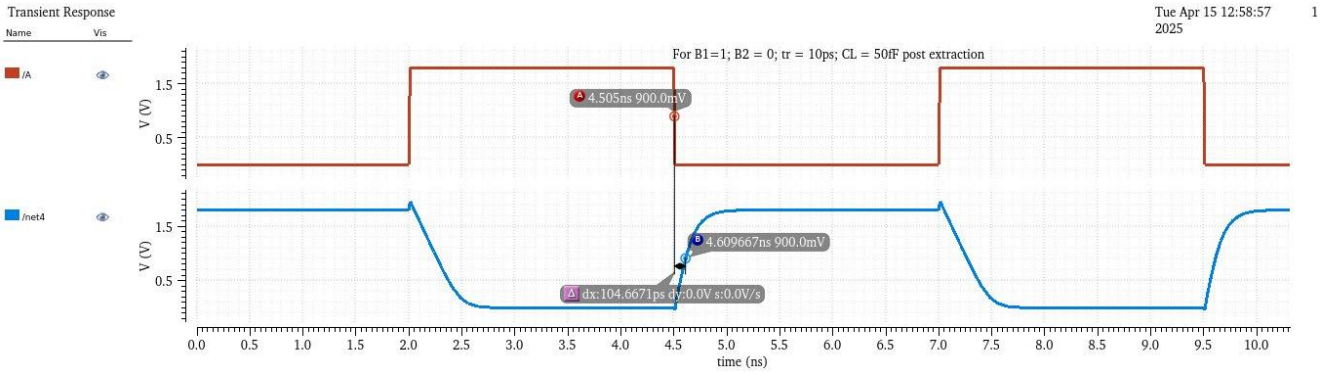


For 50 fF fanout capacitance, for 10 ps input transition time. (B1 = 1; B2 = 0)

Post Layout Simulations



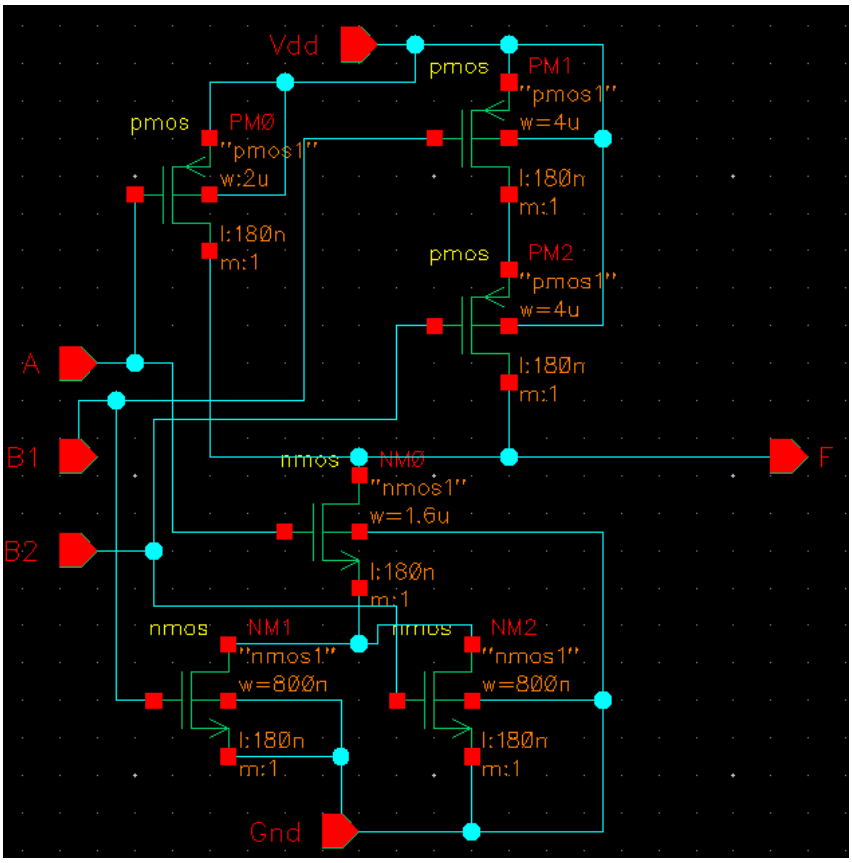
For 5 fF fanout capacitance, for 10 ps input transition time. (B1 = 1; B2 = 0)_Post layout



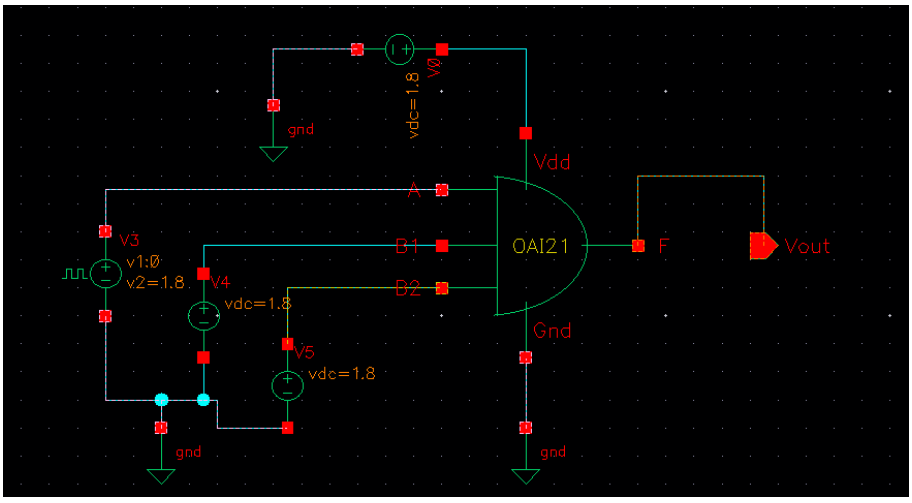
For 50 fF fanout capacitance, for 10 ps input transition time. (B1 = 1; B2 = 0)_Post layout

OAI21 Gate

Circuit Schematic



Test Bench Schematic



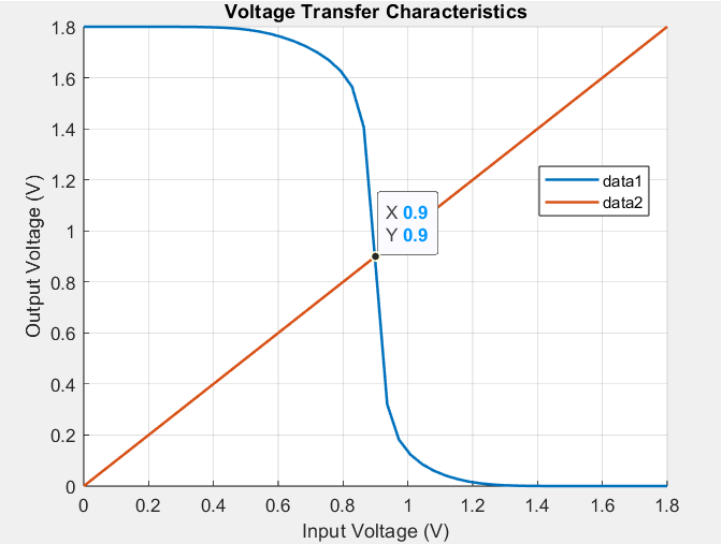
Sizing of transistors

Firstly, we size a reference inverter, and then size the transistors of the OAI21 gate. For sizing the reference inverter, we use the condition that $V_M = V_{DD} / 2$ (same PUN & PDN driving strength). We use the results of Assignment – 2, where the inverter sizes was found to be:
$L_n = L_p = 180$ nm

$W_n = 400$ nm

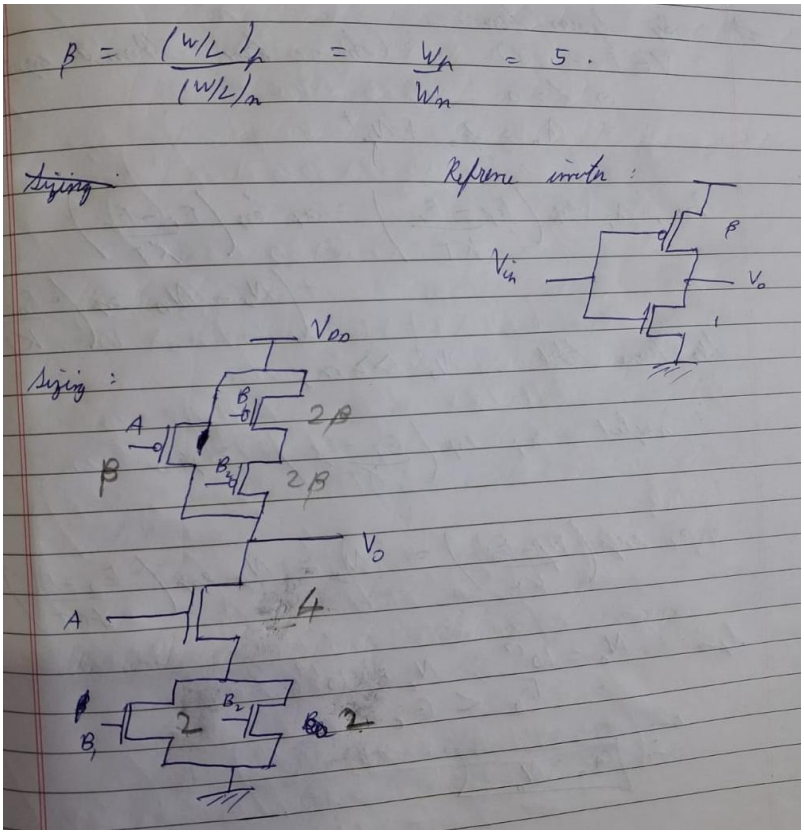
$W_p = 2000$ nm.

The graph of Vout vs Vin for this inverter is:

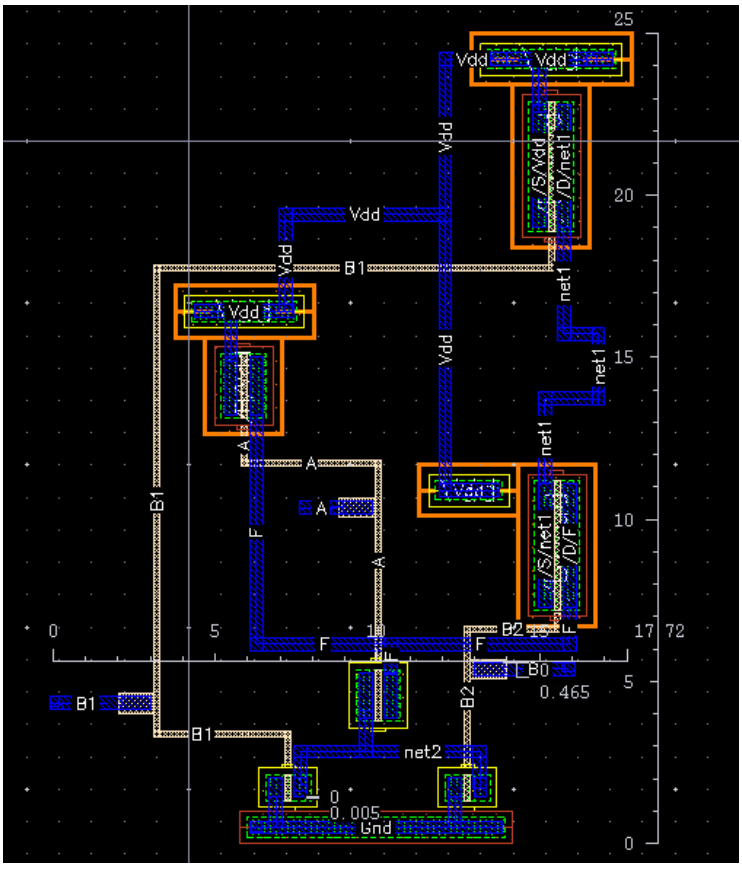


With this, the sizing of the transistors in the OAI21 gate are done to match the drive strength of the reference inverter.

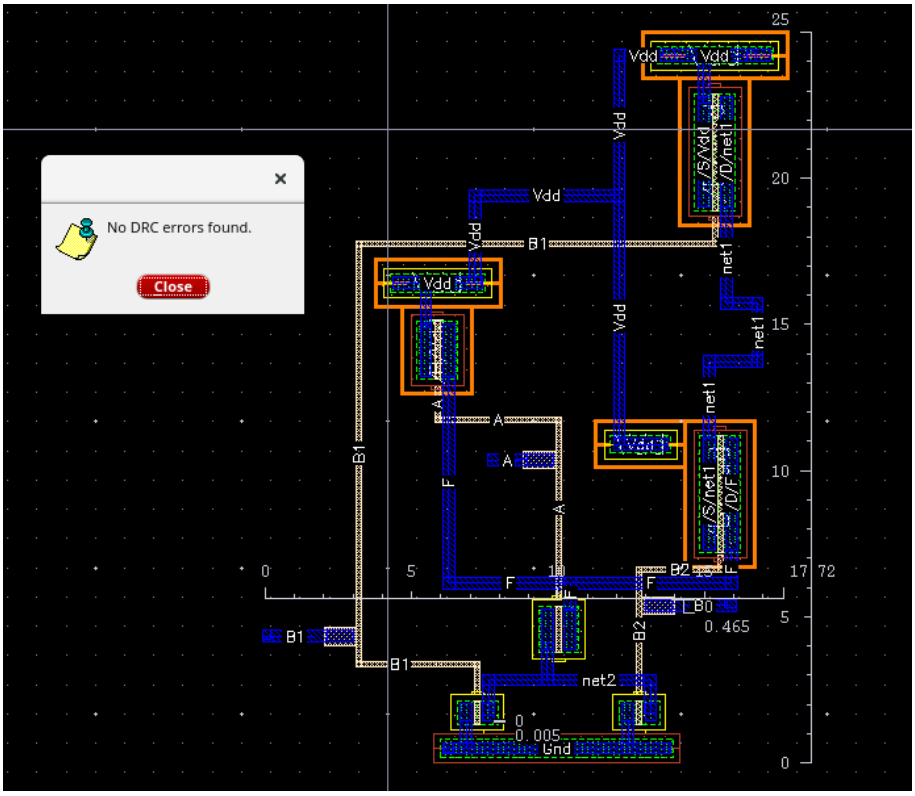
Hence, the size finally chosen is:



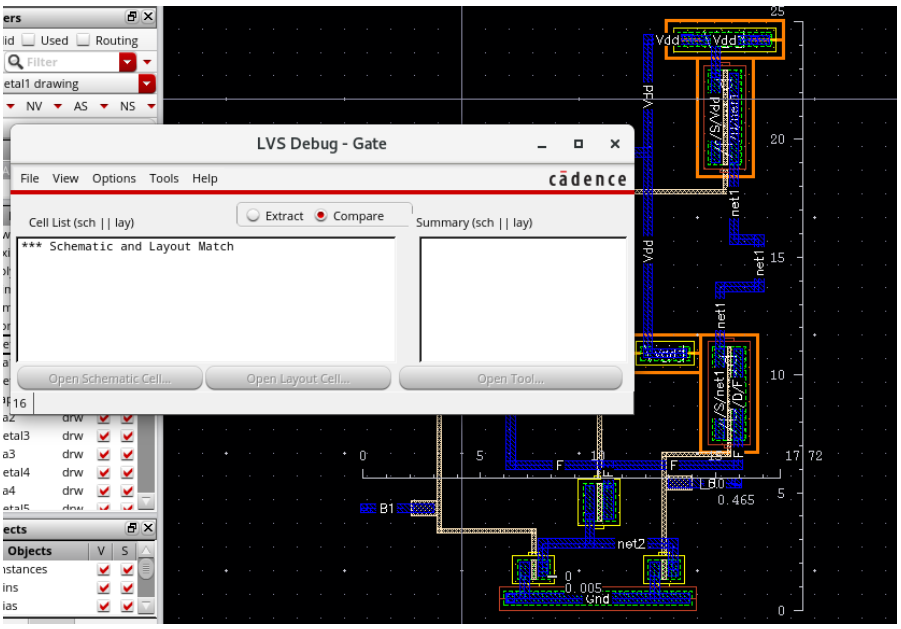
Layout



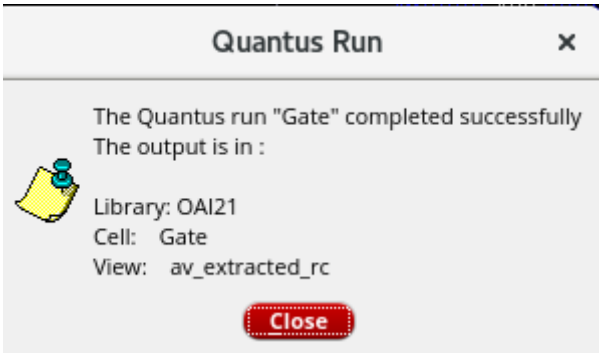
DRC Check



LVS Check



Parasitic Extraction



Schematic Simulations

T_{pHL} from A to F (B_1 = 1, B_2 = 1)		
Load capacitance Input transition	5 fF	50 fF
10 ps	22.44 ps	75.68 ps
100 ps	31.04 ps	87.01 ps

T_{pLH} from A to F (B_1 = 1, B_2 = 1)		
Load capacitance Input transition	5 fF	50 fF
10 ps	36.17 ps	130.63 ps
100 ps	54.22 ps	148.04

T_{pHL} from A to F (B_1 = 1, B_2 = 0)		
Load capacitance Input transition	5 fF	50 fF
10 ps	43.78 ps	128.18 ps
100 ps	51.85 ps	135.37 ps

T_{pLH} from A to F (B_1 = 1, B_2 = 0)		
Load capacitance Input transition	5 fF	50 fF
10 ps	41.78 ps	136.37 ps
100 ps	59.83 ps	154.44 ps

T_{pHL} from A to F ($B_1 = 0$, $B_2 = 1$)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	32.29 ps	114.61 ps
100 ps	39.60 ps	121.93 ps

T_{pLH} from A to F ($B_1 = 0$, $B_2 = 1$)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	37.00 ps	132.42 ps
100 ps	54.86 ps	149.60 ps

Post Layout Simulations

T_{pHL} from A to F ($B_1 = 1$, $B_2 = 1$)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	35.76 ps	101.08 ps
100 ps	48.77 ps	114.31 ps

T_{pLH} from A to F ($B_1 = 1$, $B_2 = 1$)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	48.10 ps	142.70 ps
100 ps	64.87 ps	159.17 ps

T_{pHL} from A to F ($B_1 = 1$, $B_2 = 0$)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	84.38 ps	187.63 ps
100 ps	94.72 ps	198.31 ps

T_{pLH} from A to F ($B_1 = 1$, $B_2 = 0$)		
Load capacitance	5 fF	50 fF

Input transition		
10 ps	49.93 ps	143.29 ps
100 ps	66.36 ps	161.11 ps

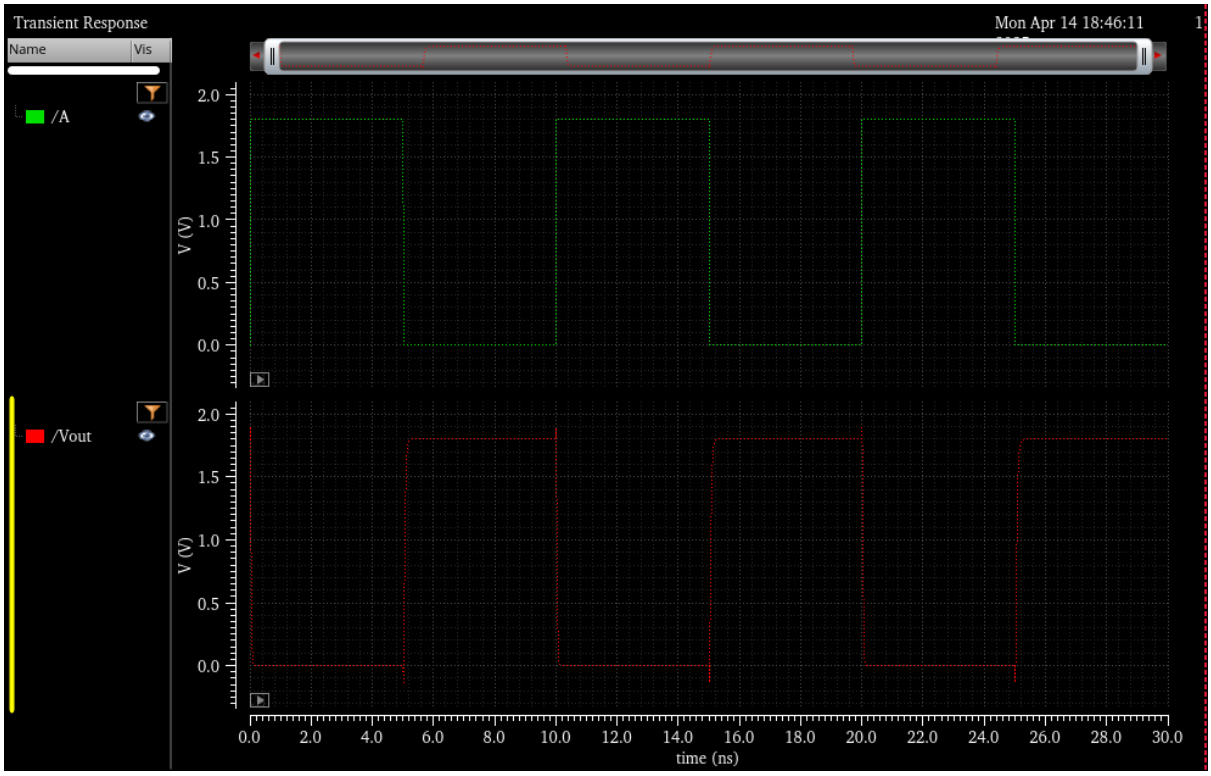
T_{pHL} from A to F (B_1 = 0, B_2 = 1)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	50.15 ps	148.58 ps
100 ps	60.10 ps	159.24 ps

T_{pLH} from A to F (B_1 = 0, B_2 = 1)		
Load capacitance	5 fF	50 fF
Input transition		
10 ps	48.62 ps	143.60 ps
100 ps	65.40 ps	159.49 ps

Schematic Output

Transient Analysis (B1 = B2 = 1)

Transient Analysis (post parasitic extraction)



Comparison with schematic simulation

(zoomed in)

Red is the old output without parasitic extraction (schematic simulation). The blue graph is the output post extraction.