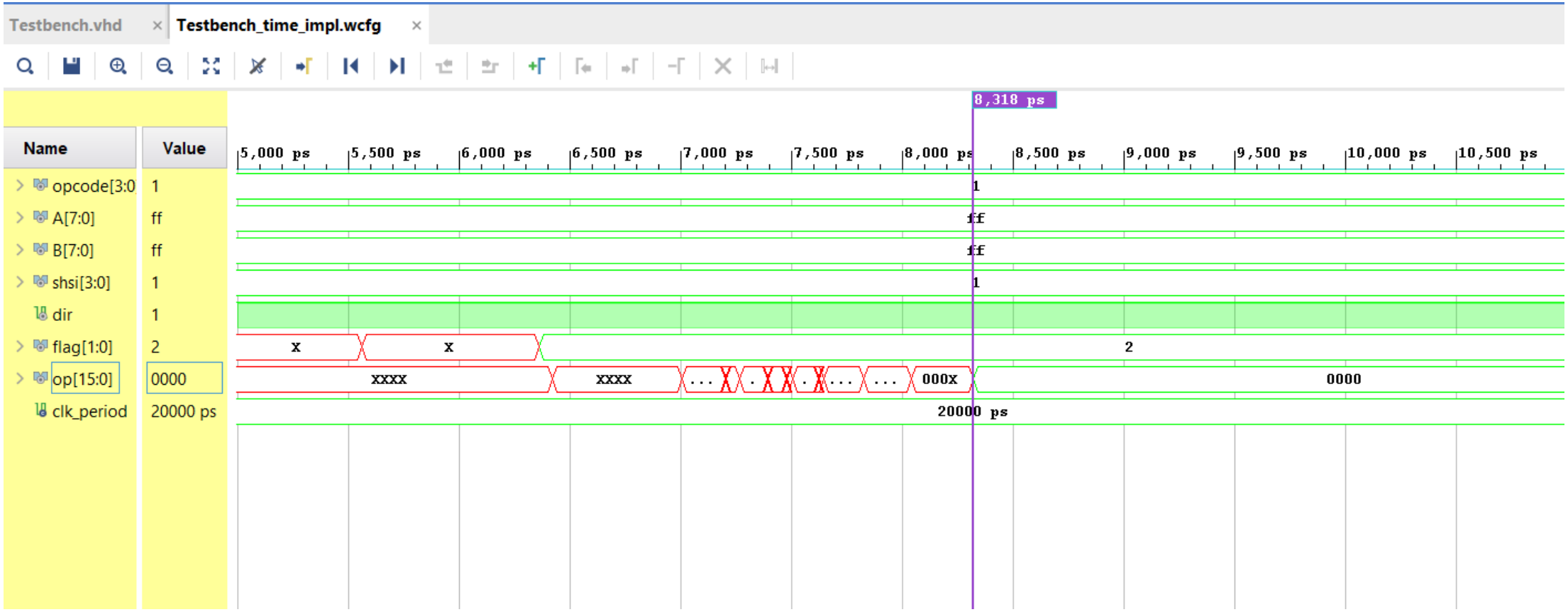
# Timing Analysis:

- Same Input for all Operations. A=FF, B=FF, shsi(as per operation), dir(as per operation)
- Example for opcode:0001(Increment/Decrement)



# Timing Analysis:

- Same Input for all Operations. A=FF, B=FF, shsi(as per operation), dir(as per operation)

| Opcode | Operation | Delay (ns) |
|---|---|---|
| 0001 | Increment/Decrement | 8.318 |
| 0010 | Parity | 9.059 |
| 0011 | Hamming Weight | 28.372 |
| 0100 | Rotate | 8.765 |
| 0101 | Reverse | 8.518 |
| 0110 | Shift | 8.765 |
| 0111 | Not | |
| 1000 | Or | |
| 1001 | And | |
| 1010 | Xor | |
| 1011 | Summation | |
| 1100 | Subtraction | |

# Timing Analysis:

- Same Input for all Operations. A=FF, B=FF, shsi(as per operation), dir(as per operation)

| Opcode | Operation | Delay (ns) |
|---|---|---|
| 1101 | Multiplication | 10.593 |
| 1110 | Concatenate | |
| 1111 | Compare | 9.126 |

# Present And Future Scope:

- This ALU project demonstrates VHDL design and simulation techniques.
- The ALU is multi-purpose and can be used in processor cores, embedded systems, and other learning or development platforms.
- The design is scalable and can be extended to support 32-bit or more operations.
- Limitation: The current version does not support floating-point arithmetic, which may be considered for future development.