Binary Ripple Counter

Priya Rajammal R
Department of Electronics and Communication Engineering
College of Engineering, Guindy
Anna University
Email:priyarajammal.r@gmail.com

***Abstract*—A register that goes through a prescribed sequence of states upon the application of input pulses is called a counter.The input pulses may be clock pulses,or they may originate from some external source and may occur at a fixed interval of time or at random.The sequence of states may follow the binary number sequence or any other sequence of states.In this paper,the hardware implementation of Binary Ripple Counter is discussed.**

***Index Terms*—asynchronous,ripple counter**

I. Introduction

A binary ripple counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the C input of the next higher order flip-flop.The flip-flop holding the least significant bit receives the incoming count pulses. A complementing flip-flop can be obtained from a JK flip-flop with the J and K inputs tied together or from a T flip-flop.A third possibility is to use a D flip-flop with the complement output connected to the D input.In this way,the D input is always the complement of the present state,and the next clock pulse will cause the flip-flop to complement.The counter constructed with complementing flip-flops of the D type is used here.

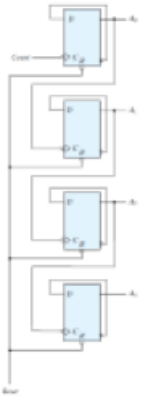

Fig. 1. Four bit Binary Ripple Counter.

Operation: The count starts with binary 0 and increments by 1 with each count pulse input. After the count of 15, the counter goes back to 0 to repeat the count. The least significant bit, A0, is complemented with each count pulse input. Every time that A0 goes from 1 to 0, it complements A1. Every time that A1 goes from 1 to 0, it complements A2. Every time that A2 goes from 1 to 0, it complements A3,and so on for any other higher order bits of a ripple counter.The flip-flops change one at a time in succession, and the signal propagates through the counter in a ripple fashion from one stage to the next.

II. Design Implementation

The elaborated design view of the modules included within the Verilog code for the implementation of Binary Ripple Counter is shown.

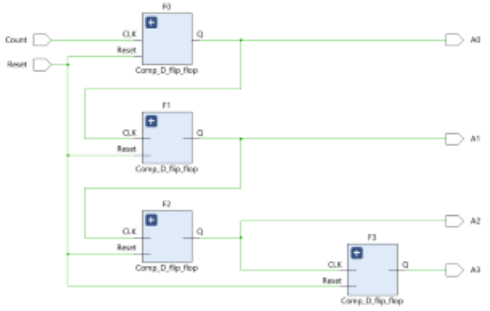

Fig. 2. Elaborated Design.

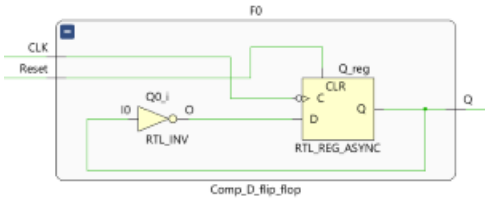

Fig. 3. Complementing flip-flop.

III. Simulation

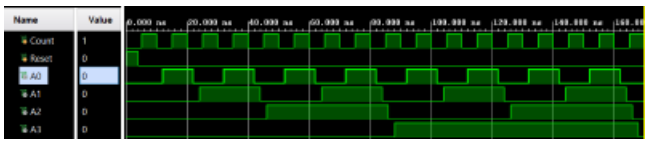

Fig. 4. Simulation results.

References

[1] M. Morris Mano and Michael D. Ciletti, 'Digital Design', Pearson, 5th Edition, 2013.