PRIYESH SHUKLA

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RESEARCH INTERESTS

Domain-specific, efficient hardware accelerators - devices, circuits, systems and co-designed algorithms for artificial intelligence (AI), Disruptive computing paradigm for nano-robotics and augmented/virtual reality (AR/VR), Probabilistic hardware, Probabilistic AI (on-device trusted, uncertainty-aware AI), Compute-in-memory, and Audio deep learning and acceleration.

EDUCATION

University of Illinois at Chicago, United States ***August 2018 - Present***
Doctor of Philosophy in Electrical and Computer Engineering

Birla Institute of Technology and Science, Pilani, India ***August 2015 - May 2017***
Master of Engineering in Microelectronics

Birla Institute of Technology and Science, Pilani, India ***August 2011 - May 2015***
Bachelor of Engineering (Hons.) in Electrical and Electronics

RESEARCH EXPERIENCE

AEON Lab, UIC, Chicago, Illinois ***August 2018 - Present***
Advisor: *Amit Ranjan Trivedi*

- *Thesis title:* Breaking the energy cage of insect-scale autonomous drones: The interplay of probabilistic hardware and co-designed algorithms.
- Exploring and designing in-memory computing based ultra-low-power hardware accelerators and co-designed algorithms for prediction uncertainty aware intelligent systems, targeted for deployment at edge platforms such as area/power constrained insect-sized drones, bio-surgical robots, augmented/virtual reality (AR/VR) devices and IoT.

Oyster Lab, BITS-Pilani, India ***August 2013 - May 2017***
Mentors: *Anu Gupta, Subhash Chandra Bose, Navneet Gupta, Abhijit Asati*

- Designed mixed-signal circuits and processor architectures focussing on co-optimizing power, area and throughput. Implemented MEMS switches and interfaces for accelerometers targeting motion sensing.

PROFESSIONAL EXPERIENCE

BOSE Corporation, Framingham, Massachusetts, United States ***Jan 2022 - Present***
Machine Learning Research Engineer Co-op

- Investigating state-of-the-art neural network accelerators and platforms to deploy deep learning models for efficient inference at the edge (concept wearables).
- Audio deep learning research: data collection and exploration, model training, optimization and deployment.

QUALCOMM Inc., San Diego, CA, United States ***May 2020 - Aug 2020***
Engineering Intern, RF Analog and Digital SoC IP

- Developed a prototype of Machine Learning tool to predict SoC level SRAM leakage based on device level leakage data across sub-10 nm technology nodes and PVTs. The tool is leveraged for Silicon-accurate SoC power estimation across several Digital IP teams.

QUALCOMM Inc., Bengaluru, India ***July 2017 - June 2018***
Engineer, IP Library Division

· Characterized Standard Cells IP libraries at sub-10nm technology nodes for high density, high power and gated architectures targeting modem chipsets; Explored machine learning tools for IC characterization.

CSIR-CEERI, Pilani, India ***July 2014 - December 2014***
Research Intern, Cyber Physical Systems Group

· Implemented reconfigurable interface between wireless sensor network (WSN) nodes and centralized monitoring station for structural health monitoring.

PATENT

- Amit Ranjan Trivedi, Theja Tulabandhula, **Priyesh Shukla**, Ahish Shylendra and Shamma Nasrin, ***"Integrated memory system for high performance bayesian and classical inference of neural networks,"*** **US Patent US 2021037936A1**

PUBLICATIONS AND SELECTED PRESENTATIONS

- Ahish Shylendra, **Priyesh Shukla**, and Amit Ranjan Trivedi, ***"Non von-Neumann Anomaly Detection in Multi-Channel Time-Series using Charge Trap Transistor Crossbars,"*** **IEEE International Symposium on Circuits and Systems (ISCAS), 2022**.
- **Priyesh Shukla** and Amit Ranjan Trivedi, ***"Breaking the energy cage of insect-scale autonomous drones: Interplay of probabilistic hardware and co-designed algorithms,"*** **In 2021 58th ACM/IEEE Design Automation Conference (DAC), 2021**.
- **Priyesh Shukla**, Ankith Muralidhar, Nick Iliev, Theja Tulabandhula, Sawyer Fuller, and Amit Ranjan Trivedi, ***"Ultra-low-Power Localization of Insect-Scale Drones: Interplay of Probabilistic Filtering and Compute-in-Memory,"*** **IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021**.
- **Priyesh Shukla**, Shamma Nasrin, Nastaran Darabi, Wilfred Gomes, and Amit Ranjan Trivedi, ***"MC-CIM: Compute-in-Memory with Monte-Carlo Dropouts for Bayesian Edge Intelligence,"*** **arXiv preprint arXiv:2111.07125 (2021)**.
- **Priyesh Shukla**, Shamma Nasrin, and Amit Ranjan Trivedi ***"Sub-mW-power Positioning of Autonomous Pico-drones,"*** **IBM IEEE CAS/EDS AI Compute Symposium, 2021**.
- Shamma Nasrin, **Priyesh Shukla**, Shruthi Jaisimha, and Amit Ranjan Trivedi ***"Compute-in-Memory Upside Down: A Learning Operator Co-Design Perspective for Scalability,"*** **Design, Automation & Test in Europe Conference & Exhibition (DATE), 2021**.
- **Priyesh Shukla**, Ahish Shylendra, Theja Tulabandhula, and Amit Ranjan Trivedi, ***"MC^{2}RAM: Markov Chain Monte Carlo Sampling in SRAM for Fast Bayesian Inference,"*** **IEEE International Symposium on Circuits and Systems (ISCAS), 2020**.
- Shamma Nasrin, Justine Drobitch, **Priyesh Shukla**, Theja Tulabandhula, Supriyo Bandyopadhyay, and Amit Ranjan Trivedi, ***"Bayesian Reasoning Machine on a Magneto-tunneling Junction Network,"*** **Nanotechnology, 2020**.
- Ahish Shylendra, **Priyesh Shukla**, Saibal Mukhopadhyay, Swarup Bhunia, Amit Ranjan Trivedi, ***"Low Power Unsupervised Anomaly Detection by Nonparametric Modeling of Sensor Statistics,"*** **IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020**.
- Ahish Shylendra, Sina Haji Alizad, **Priyesh Shukla**, Amit Ranjan Trivedi, ***"Non-parametric Statistical Density Function Synthesizer and Monte Carlo Sampler in CMOS,"*** **International Conference on VLSI Design (VLSID), 2020**.

- Ahish Shylendra, **Priyesh Shukla**, Swaroop Bhunia, Amit Ranjan Trivedi, ***"Fault attack detection in AES by monitoring power side-channel statistics,"*** **International Symposium on Quality Electronic Design (ISQED), 2020**.

TECHNICAL SKILLS

Programming	Python, R, C/C++, Verilog/VHDL (RTL coding), Embedded C, and Matlab
Tools	HSPICE, Cadence, TCAD, Xilinx EDK, Scikit-learn, PyTorch, Tensorflow, Vuforia

RELEVANT COURSEWORKS

VLSI (ASIC) design, Computer architectures, Machine learning, Statistics and Probability, Linear algebra, Augmented/Virtual/Mixed reality, Nanoelectronics, Robotics, Object oriented programming, Reconfigurable computing, Data Mining, Deep learning, Graphical models and Reinforcement learning.

HONORS AND AWARDS

Peter and Deborah Wexler Award, The University of Illinois System, **2018-19**

Graduate Tuition Scholarship, The University of Illinois System, **2018-present**

BITSAA Research Scholarship travel grants by BITS-Pilani, **2016-17**

Award for outstanding merit in 10+2 by Krishna Group of Institutions and Chhattisgarh State Government of India, **2010**

AFFILIATIONS AND SERVICES IN RESEARCH COMMUNITY

Graduate Student Member, IEEE, 2019-present

Student Member, ACM SIGDA, 2020-present

Student Member, IEEE Robotics and Automation Society, 2021-present

Reviewer: IEEE Internet of Things Journal, IEEE Journal of Selected Areas in Communication, IEEE Transactions on Intelligent Transportation Systems, VLSID

REFERENCES

Dr. Amit Ranjan Trivedi
Assistant Professor, Department of Electrical and Computer Engineering
University of Illinois at Chicago, Illinois, United States (Email: amitrt@uic.edu)

Dr. Sawyer Fuller
Assistant Professor, Department of Mechanical Engineering
University of Washington, Seattle, Washington, United States (Email: minster@uw.edu)

Dr. Theja Tulabandhula
Assistant Professor, Department of Information and Decision Sciences
University of Illinois at Chicago, Illinois, United States (Email: theja@uic.edu)

Dr. Animesh Datta
Senior Custom Cell Design Engineer, Apple Inc., San Diego, CA, United States
(Email: anidatta@gmail.com)

Dr. Chuan-Che (Jeff) Huang
Research Software Engineer, Bose Corporation, Framingham, MA United States
(Email: Chuan-Che_Huang@bose.com)