컴 퓨 터 특 강 중 간 발 표

Computer Architecture

숙 명 여 자 대 학 교 전 자 공 학 과 1 8 1 0 8 1 8 김 상 은

Question 1

#Q1. Explain why you have to learn the topic every week?

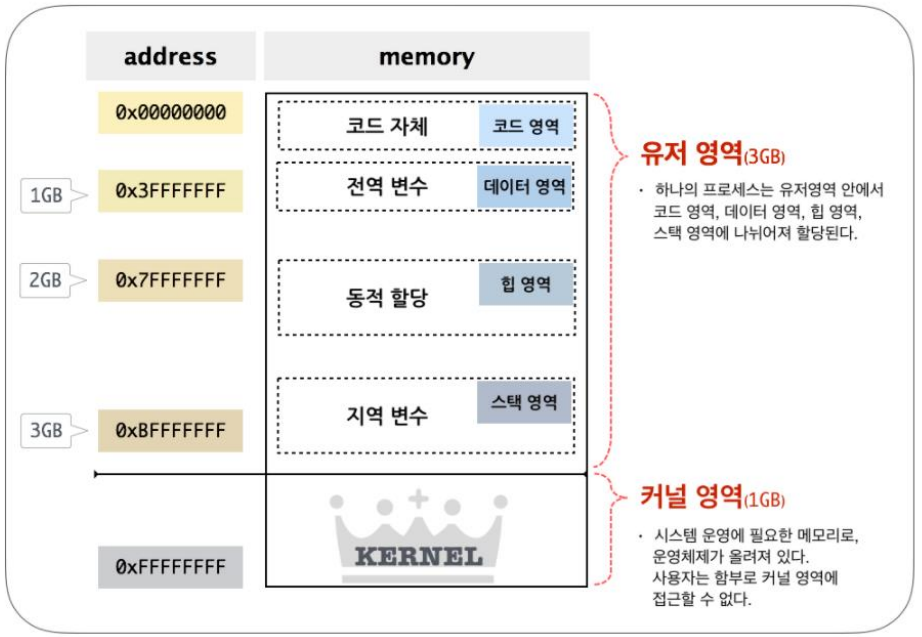
Question 2

#Q2. Explain what's the most important thing in each topic and why it is the most important.

1) Introduction to Memory
2) Basis and Theory for Digital Circuits
3) Introduction to CPU
4) Physical Implementation

#Q1. Explain why you have to learn the topic every week?

컴퓨터 구조를 안 이후



어? 프로그램이 안 돌아가네,,,

디버깅 해봐야겠군

0xbfffe1fc 이건 뭐지?

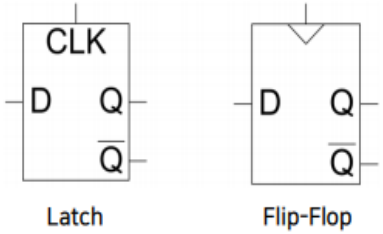
16진수로 표현된 메모리 주소구나!

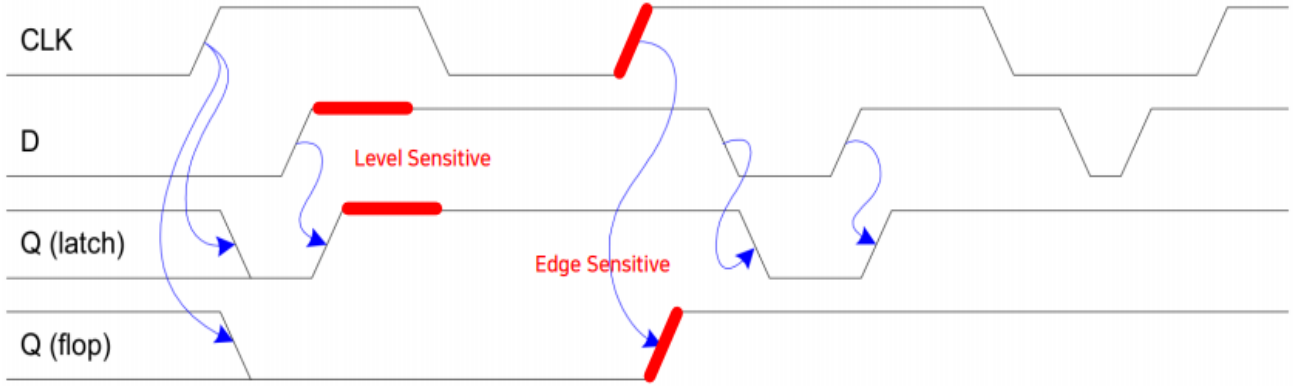
CLK

#Q1. Explain why you have to learn the topic every week?

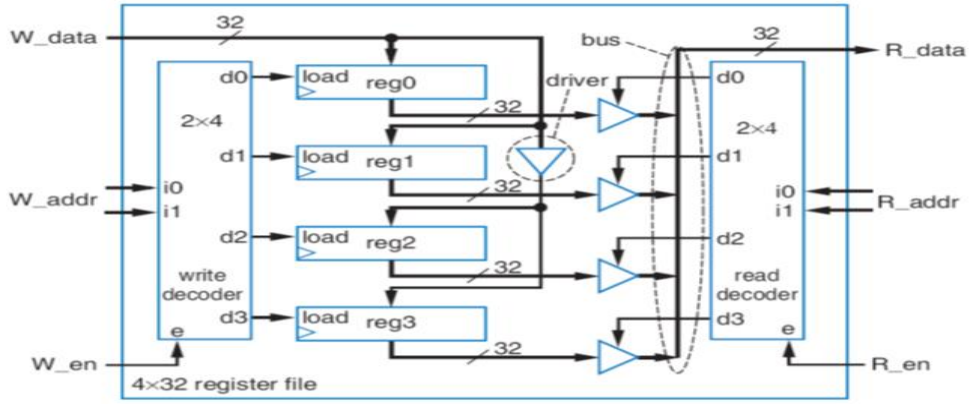
1. CLK으로 인해 더 정교한 동기화를 할 수 있게 되었고, 이는 인간이 복잡한 회로를 제어하기 쉽게 만들어주었다.

- **Latch**
  - Level Sensitive
- **Flip-Flop**
  - Edge Sensitive

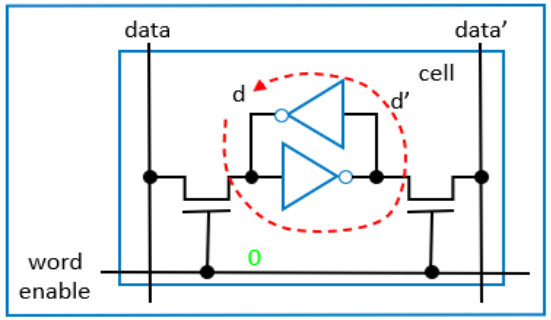




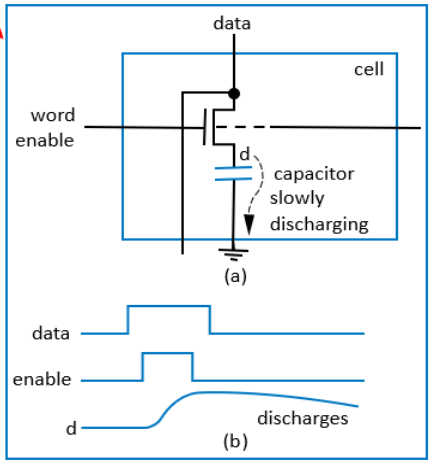
Register



SRAM cell



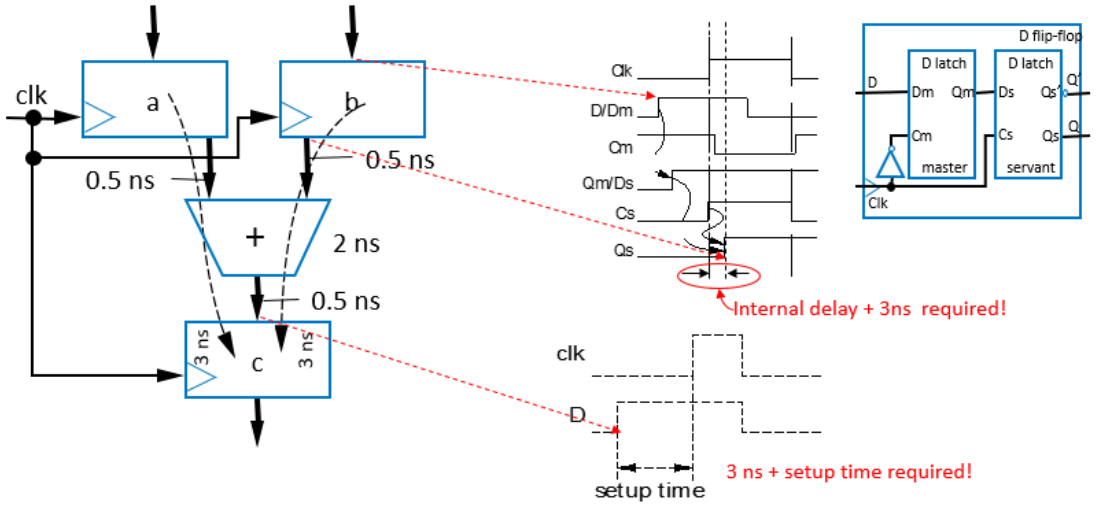
DRAM cell



CLK

#Q1. Explain why you have to learn the topic every week?

2. CLK은 디지털회로가 안정적으로 동작할 수 있게 도와주는 기준이 되고 기술의 성능을 분석하는 역할도 가능하다.



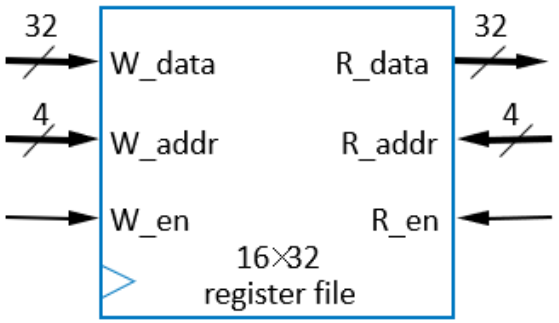
$$\text{Operating frequency} = \frac{1}{\textit{Critical path}}$$

Type \ Analysis	Cycle Counts	Critical Path Delay /Operating Frequency	Execution Time (Cycle Count x Critical Path Delay)	Speed-Up (SW Ex' Time / HW EX' Time)
Software	3915	10 ns / 100 MHz	3915 x 10 ns = 39150 ns	-
Hardware	111	12 ns / 83 MHz	111 x 12 ns = 1332 ns	29.4 X Faster (= 39150 ns / 1332 ns)

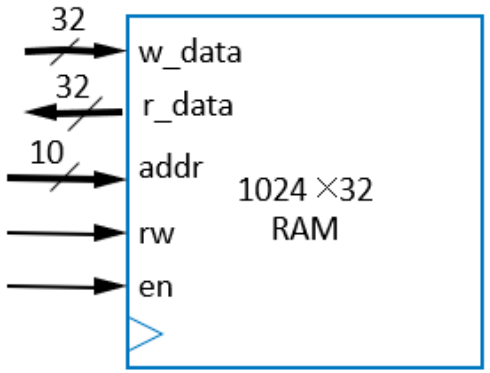
Critical path = wire_delay (1ns) + logic delay (2 ns)
+ setup time (0.1ns) + internal delay (0.05 ns) = 3.15 ns.

#Q2. Explain what's the most important thing in each topic and why it is the most important.

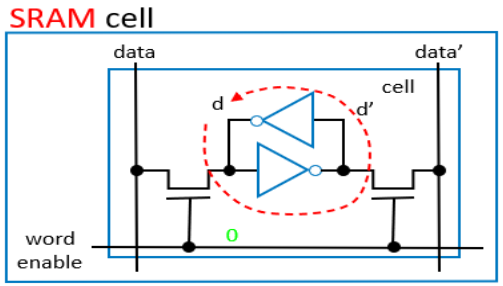
1) Introduction to Memory

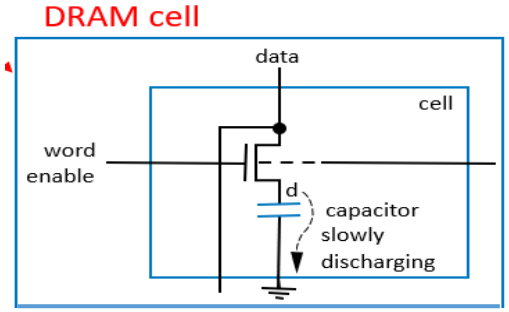


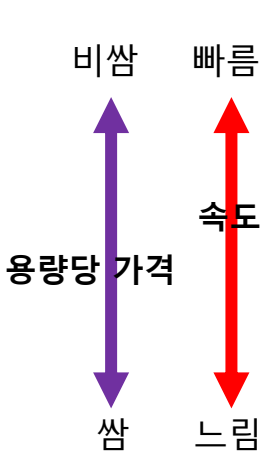
Register file from Ch. 4

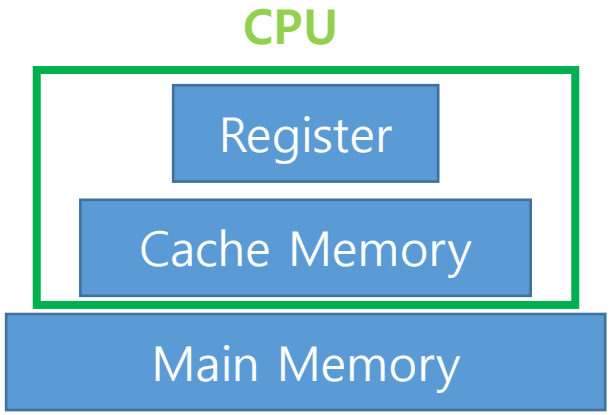


RAM block symbol









Register : 38 Transistor for 1bit

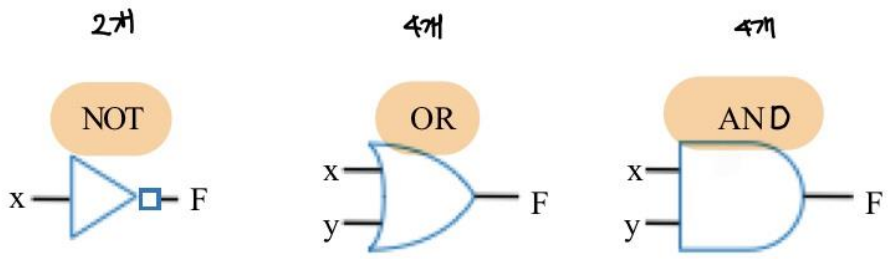
SRAM : 6 Transistor for 1bit

DRAM : 1 Transistor for 1bit

#Q2. Explain what's the most important thing in each topic and why it is the most important.

2) Basis and Theory for Digital Circuits

Symbol



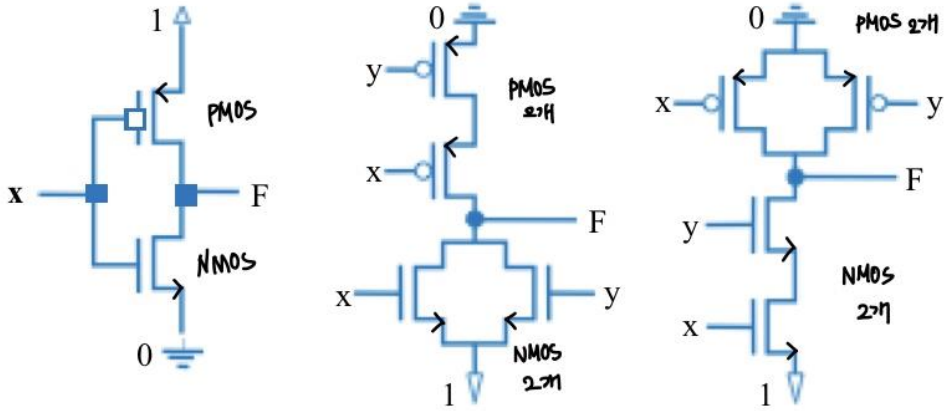
Truth table

x	F
0	1
1	0

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

CMOS Transistor circuit



- Boolean Algebra
  - Boolean Identities

x + 0 = x x · 1 = x	Identity Law	x + (y + z) = (x + y) + z x(yz) = (xy)z	Associative Law
x + 1 = 1 x · 0 = 0	Domination law	x(y + z) = xy + xz x + yz = (x + y) (x + z)	Distributive Law
x + x = x x · x = x	Idempotent Law	(x y)' = x' + y' (x + y)' = x' y'	De Morgan's Law
(x')' = x	Complementation Law	x + xy = x x (x + y) = x	Absorption Law
x + y = y + x xy = yx	Commutative Law	x + x' = 1 x x' = 0	Complement Law

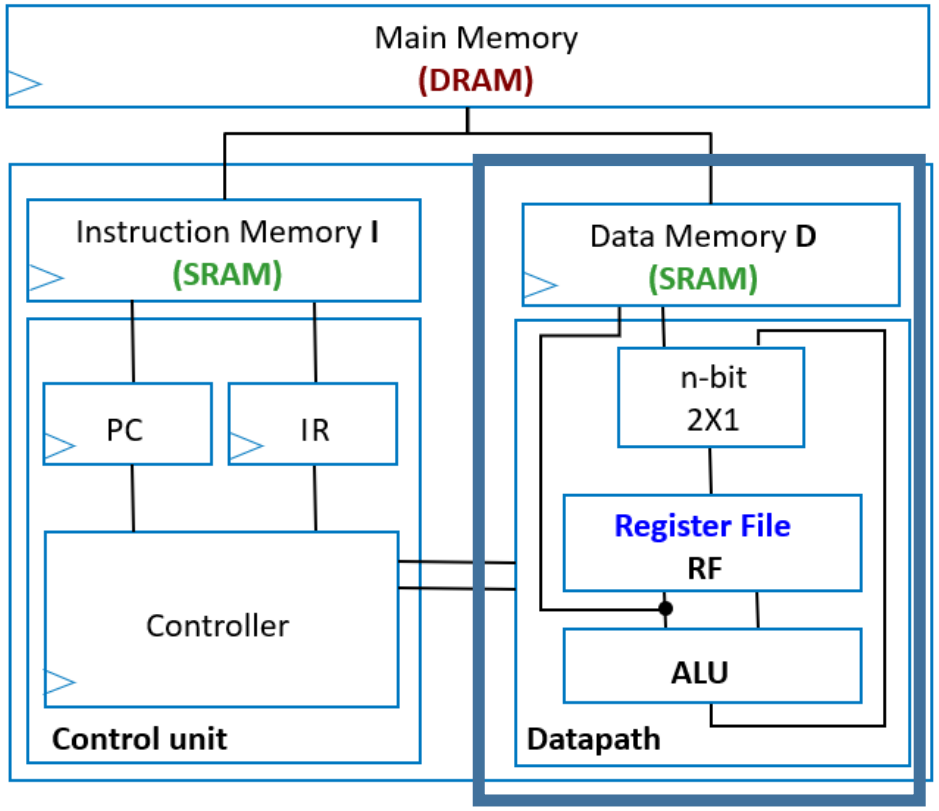
강대원 박사님

Claude Shannon

#Q2. Explain what's the most important thing in each topic and why it is the most important.

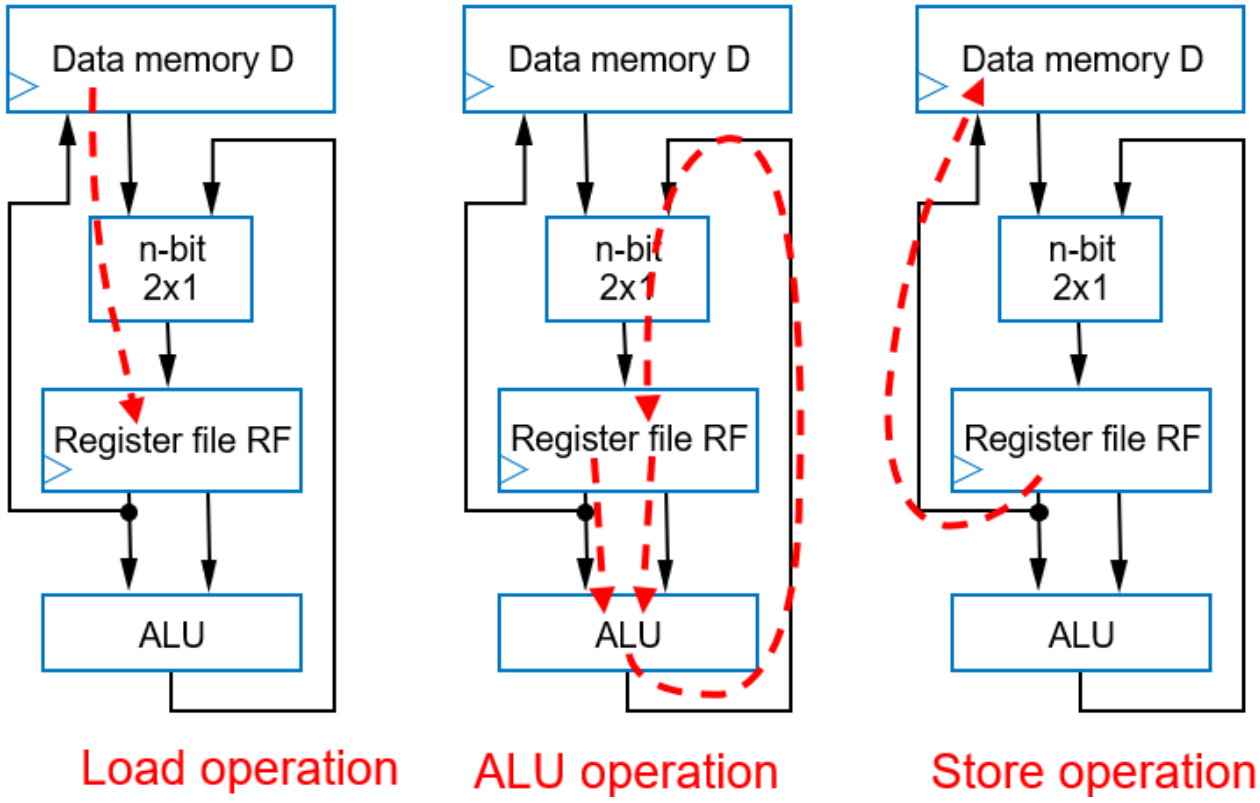
3) Introduction to CPU

***메모리 관점에서 단순화 시킨 GPP**



Data Path

*** Data Path 관점에서 본 동작**



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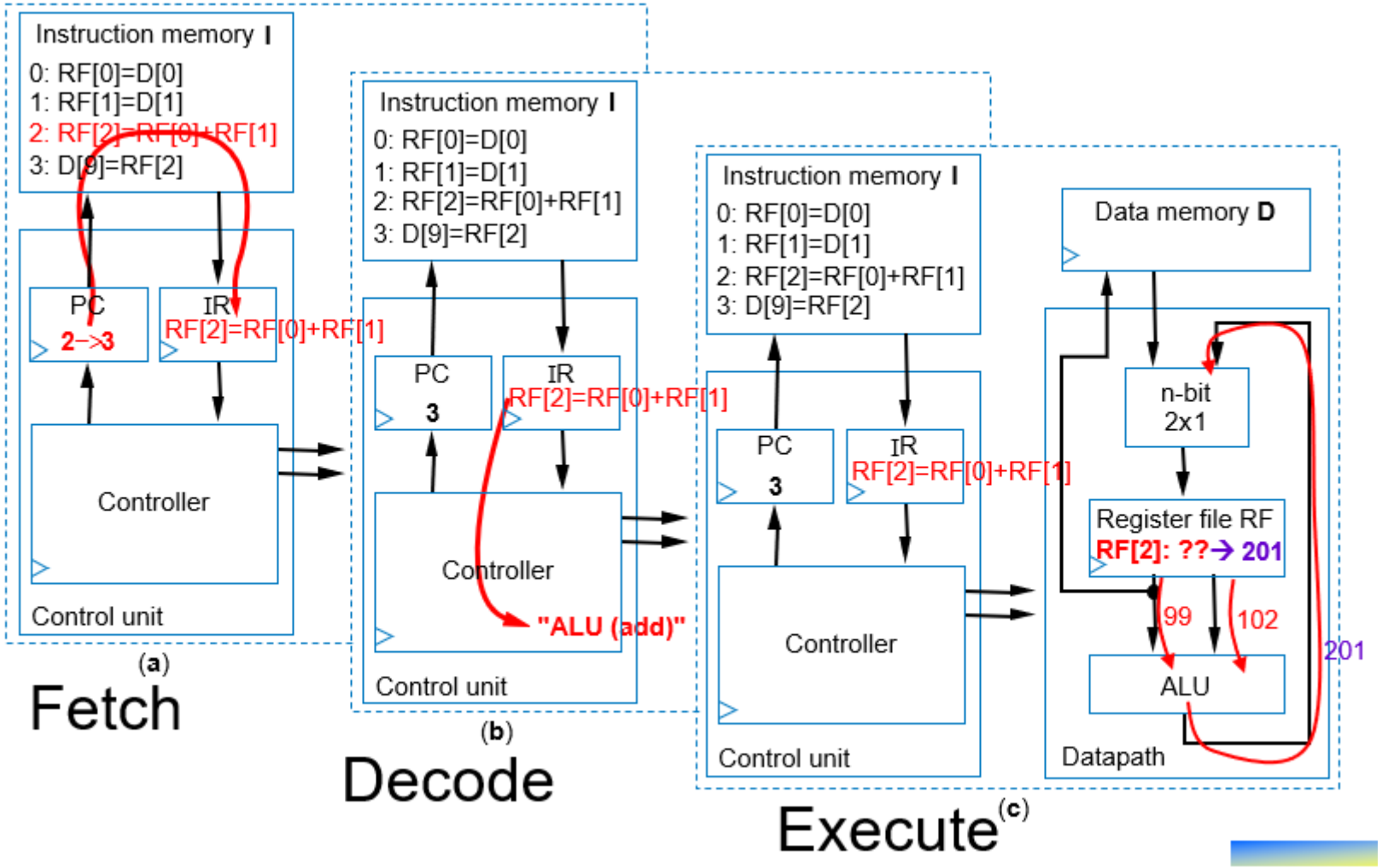
3) Introduction to CPU



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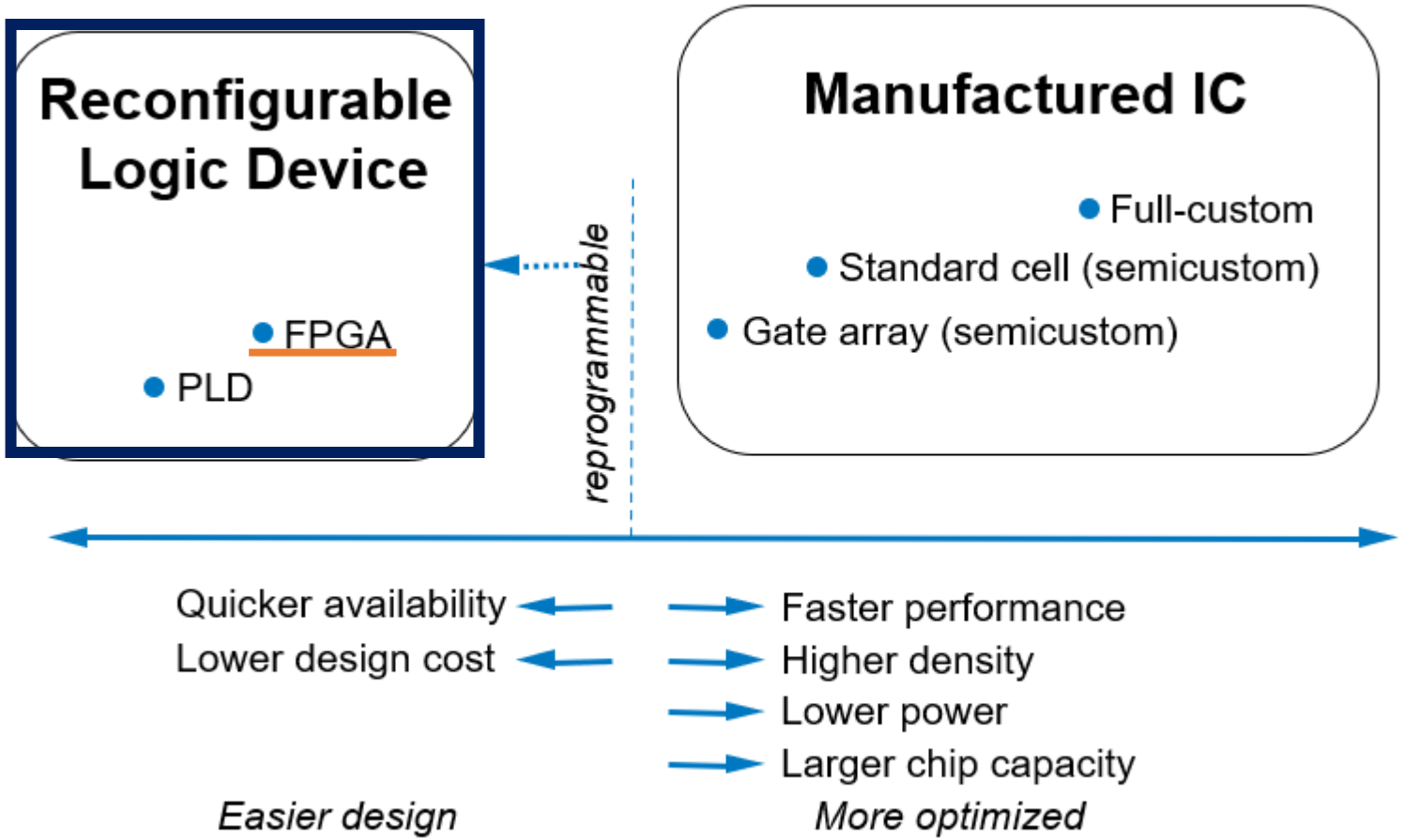
4) Physical Implementation



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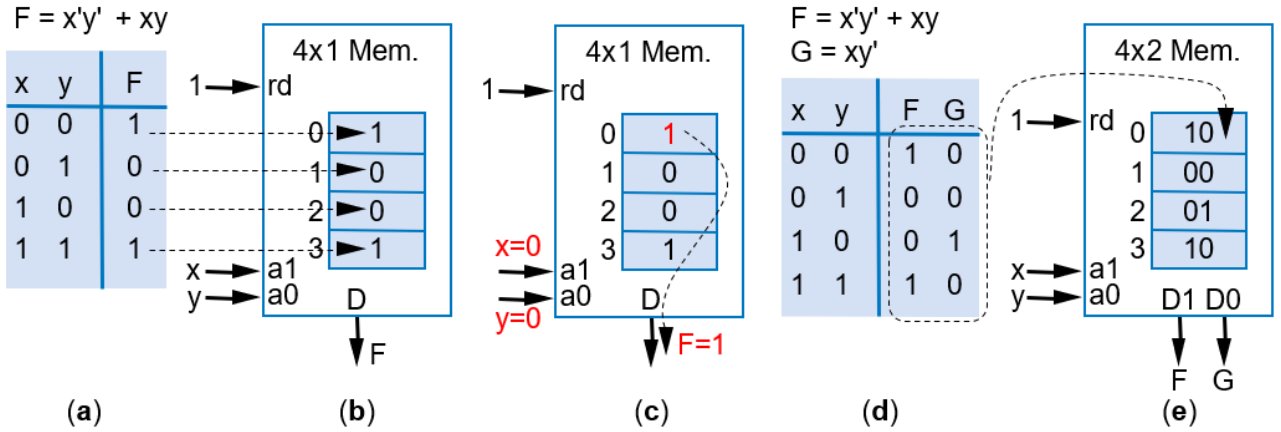
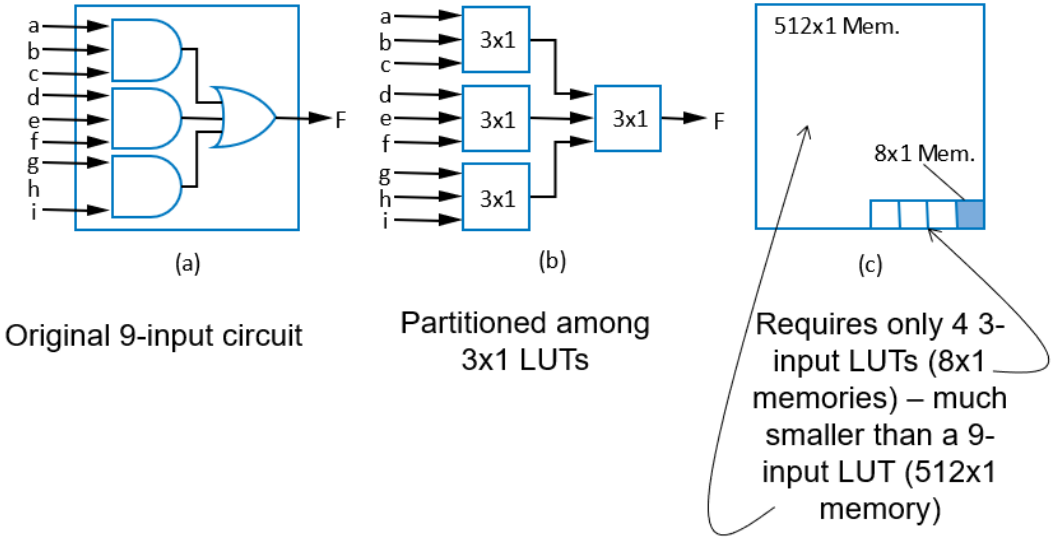
4) Physical Implementation

FPGA

- Such memory in FPGA known as Lookup Table (LUT)





감사합니다.