Advanced Topics for Micro-Architecture of CPU

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Outline

ex) 애플
ex) intel + 삼성
(위키) 어떻게 분류하는지 알아볼 것임.

- Commerical CPU products classification ⇒ 상용 CPU 제품 분류

- Selected Commercial CPU products
  ↳ 교수님이 선택한 제품 (⇒ cache의 예와 같음)

- $\boxed{\text{Key factors}}$ for analyzing micro-architecture of commercial CPU products
  ↳ 중요 point를 볼 것임.
  야두위한 것임

- Introduction to $\boxed{\text{ILP}}$ (Instruction Level Parallelism)
  ↳ 명령어 level의 병렬화

- What is VLIW (Very Long Instruction Word) processor?
  ↳ VLIW 보다 superscalar는 훨씬더 많이 씀.
  (0.1xx%) (99.9..%)

- Comparison between superscalar processor and VLIW processor
  ↳ 어떤차이 때문에 superscalar를 더 많이 쓰는가!?. 왜 실패했는가 !?

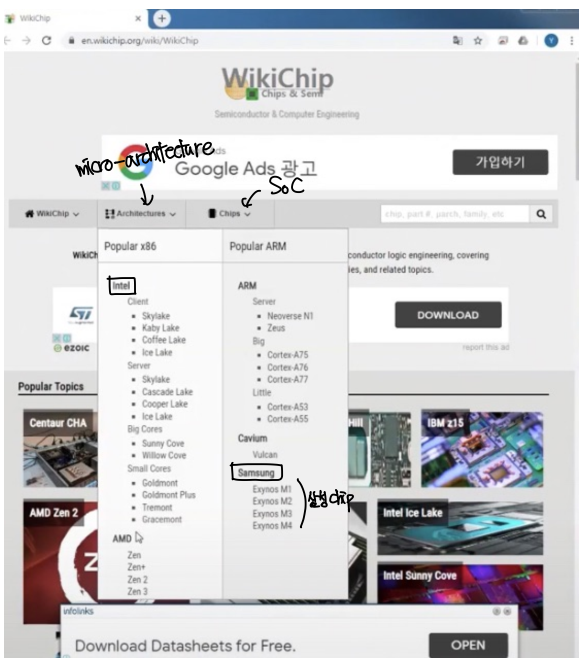
- Performance-power consumption metrics for evaluating commercial CPUs
  ↳ 12주차 추가된내용

컴퓨터 Architecture
VLIW processor
superscalar processor
역순 ····> CISC
(명령이 다양하고 단계가 간단한 구조)
⇒ 오늘날 많이쓰는 구조

- Relationship among fabrication technology, micro-architecture, no. of cores and cache memory
  ⇒ 공정, micro-architecture, core의 개수, cache memory의 관계

Commercial CPU Products Classification

https://en.wikichip.org/wiki/WikiChip



↳ 여기에 정보가 많음. (WikiChip)

Selected Commercial CPU Products

Group#1

Clk주파수 pipeline depth 비례하기일기.

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators: Fab. Tech	Power	Name	CPU: Micro-architecture	Bit-Width	Clock Freq.	ISA	No. of Cores	L1 Cache	L2 Cache	L3 Cache
Embedded Computer Systems	Smart Phone	iPhone 4	2010. 06	45 nm	?	Apple A4	ARM Cortex-A8	32	800 MHz	ARM v7-A	1	Per-core: I-32KB, D-32KB	512KB	None
		iPhone 4s	2011. 03	32 nm	?	Apple A5	ARM Cortex-A9	32	1 GHz	ARM v7-A	2	Per-core: I-32KB, D-32KB	1MB shared	None
		iPhone 5s	2013. 09	28 nm	2~3 W	Apple A7	Apple Cyclone	64	1.3 GHz	ARM v8.0-A	2	Per-core: I-64KB, D-64KB	1MB shared	4MB shared by the entire SoC
		iPhone 6s	2015. 09	16 nm	?	Apple A9	Apple Twister	64	1.85 GHz	ARM v8.0-A	2	Per-core: I-64KB, D-64KB	3MB shared	4MB shared by the entire SoC
		iPhone 7	2016. 09	16 nm	?	Apple A10 Fusion	2 x **Hurricanes** for high performance	64	2.34 GHz	ARM v8.1-A	4	Per-core: I-64KB, D-64KB	3MB shared	4MB shared by the entire SoC
							2 x **Zephyr** for energy efficiency		pipeline depth			Per-core: I-32KB, D-32KB	1MB shared	
		Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x **Mongoose2 (M2)** for high performance	64	13 2.3 GHz	ARM v8-A	8	Per-core: I-64KB, D-32KB	2MB shared	None
							4 x **Cortex-A53** for energy efficiency		8 1. 7 GHz			Per-core: I-32KB, D-32KB	256KB shared	
		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x **Monsoon** for high performance	64	2.39 GHz	ARM v8.2-A	6	Per-core: I-64KB, D-64KB	8MB shared	None
							4 x **Mistral** for energy efficiency		1.42 GHz			Per-core: I-32KB, D-32KB	1MB shared	
		iPhone XS	2018. 09	7 nm	?	Apple A12	2 x **Vortex** for high performance	64	2.49 GHz	ARM v8.3-A	6	Per-core: I-128KB, D-128KB	8MB shared	None
							4 x **Tempest** for energy efficiency		1.52 GHz			Per-core: I-32KB, D-32KB	2MB shared	
		iPhone 11 Pro	2019. 09	7 nm	?	Apple A13	2 x **Lightning** for high performance	64	2.66 GHz	ARM v8.4-A	6	Per-core: I-128KB, D-128KB	8MB shared	None
							4 x **Thunder** for energy efficiency		1.82 GHz			Per-core: I-32KB, D-48KB	4MB shared	
	Tablet PC	HP x2 210 G2 3ML39PA	2018. 02	14 nm	2W	Intel Atom® Processor x5-Z8350	Airmont	64	1.44 ~ 1.92 GHz	x86 -64	4	Per-core: I-32KB, D-24KB	2MB (1MB shared by 2 cores)	None

Selected Commercial CPU Products

Group#2

발상의 시도

Type	Sub Type	Product Name	Release date (Year. Month)	Fab. Tech	Power	Name	SoC (System-on-Chip) = CPU + GPU + HW Accelerators — CPU: Micro-architecture	Bit-Width	Clock Freq.	ISA	No. of Cores	L1 Cache	L2 Cache	L3 Cache
Embedded Computer Systems	Smart Phone	Galaxy S9	2018. 03	10 nm	?	Exynos 9810	4 x **Meerkat (M3)** for high performance	64	2.9 GHz	ARM v8-A	8	Per-core: I-64KB, D-64KB	Per-core: 512KB	4MB shared
							4 x **Cortex-A55** for energy efficiency		1. 9 GHz	ARM v8.2-A		Per-core: I-32KB, D-32KB	256KB Shared	
		Galaxy Note10	2019. 08	7 nm	?	Exynos 9825	2 x **Cheetah (M4) for** high performance	64	2.73 GHz	ARM v8.2-A	8	Per-core: I-64KB, D-64KB	Per-core: 512KB	4MB shared
							2 x **Cortex-A75** for moderate performance		2.4 GHz			Per-core: I-64KB, D-64KB	Per-core: 256KB	
							4 x **Cortex-A55** for energy efficiency		1.95 GHz			Per-core: I-32KB, D-32KB	Per-core: 128KB	
General PC	Laptop	SAMSUNG NT900X3N-K59SS	2015. 03	14 nm	15W	Intel® Core™ i5-7200U	7th Gen. Kaby Lake	64	2.5 ~ 3.1 GHz	x86-64	2	Per-core: I-32KB, D-32KB	Per-core: 256KB	3MB shared by 2 cores and GPU
		LG GRAM 17ZD90N-VX70K	2019. 12	10 nm	15W	Intel® Core™ i7-1065G7	변화가 일어남 10th Gen. Ice Lake	64	1.3 ~ 3.9 GHz	x86-64	4	Per-core: I-32KB, D-48KB	Per-core: 512KB	8MB shared by 4 cores and GPU
	Desktop	SAMSUNG DB400T6B	2015. 03	14 nm	65W	Intel® Core™ i7-6700	6th Gen. Skylake	64	3.4 ~ 4 GHz	x86-64	4	Per-core: I-32KB, D-32KB	Per-core: 256KB	8MB shared by 4 cores and GPU
		Danawa 190721	2019. 07	14 nm	95W	Intel® Core™ i7-9700K	9th Gen. Coffee Lake	64	3.6 ~ 4.9 GHz	x86-64	8	Per-core: I-32KB, D-32KB	Per-core: 256KB	12MB shared by 4 cores and GPU
Server/ Workstation	Floating License/ Data Sever	TYAN KFT46	2011. 09	32 nm	80W	Intel® Xeon® E5606	Westmere / WikiChip / Block diagram	64	2.13 GHz	x86-64	4	Per-core: I-32KB, D-32KB	Per-core: 256KB	8MB shared by 4 cores
	High performance Workstation	Lenovo ThinkStation P500TW 850W	2015. 07	22 nm	140W	Intel® Xeon® E5-1630 v3	Haswell	64	3.7 ~ 3.8 GHz	x86-64	4	Per-core: I-32KB, D-32KB	Per-core: 256KB	10MB shared by 4 cores
		TYAN TAKO KQT44	2020. 04	14 nm	150W	Intel® Xeon Gold 6226R	Cascade Lake	64	2.9 ~ 3.9 GHz	x86-64	16	Per-core: I-32KB, D-32KB	Per-core: 1MB	22MB shared by 16 cores

예전 것.

core가 많아지면
L3 캐시도 무조건 커야함 (클수록 좋다 가정)

미유효.
→ 효과가 어떤지는 모르겠음.

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators										
				Fab. Tech	Power	Name	CPU							
							Micro-architecture	Bit-Width	Clock Freq.	ISA	No. of Cores	L1 Cache	L2 Cache	L3 Cache

★★★

이안으로 들어가볼 것임.

4가지보다 더 있을 수 있는데 핵심적인 것은 위주로 볼것임.

4가지로 나뉘어서 볼 수 있음. → 성능을 분석해볼 것임.
(스펙을 볼때)

L1 캐시가 seperate일때 I, D로 나뉘는데 그때 pipeline이 가능해서 된다,
연속명령이 fetch가 가능함.

Micro-architecture							
Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor				Pipeline depth
			No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	

연도도 중요함
→ 순서는 아는것이 중요함.
→ 어떤것이 개발되었는지 비교하기가 좋아서

VLIW
or
superscalar
교수님이 선택하신 것

pipeline의 길이 depth는 다를 것임.

6가지를 기준으로
중요히 성능을 분석할 수 있음.
(의미, 차이, cache의 구성과 연관하여 설명할 수 있으면 좋음)

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products

모두 Yes

다양한 숫자

(숫자가 높을수록 높은 성능)

낮을수록 성능이 낮다는것은 아님.

모두 superscalar

6가지 질문으로 살펴보기

이에 대해 자세히 볼 것임

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators: Fab. Tech	Power	Name	CPU: Micro-architecture: Name	Intro' date (Year. Month)	① Type	Spec. of Superscalar processor: ② No. of Issues (Decodes)	③ Out of order execution	④ Branch prediction (speculation)	⑤ No. of Execution ports	⑥ Pipeline depth
Embedded Computer Systems	Smart phone	iPhone 4	2010. 06	45 nm	?	Apple A4	ARM Cortex-A8	2005. ?	Super scalar	2	No	Yes	2	13
		iPhone 4s	2011. 03	32 nm	?	Apple A5	ARM Cortex-A9	2007. ?	Super scalar	2	Yes	Yes	3	11
		iPhone 5s	2013. 09	28 nm	2~3 W	Apple A7	Apple Cyclone	2013. ?	Super scalar	6	Yes	Yes	9	16
		iPhone 6s	2015. 09	16 nm	?	Apple A9	Apple Twister	2015. ?	Super scalar	6	Yes	Yes	9	16
		iPhone 7	2016. 09	16 nm	?	Apple A10 Fusion	2 x **Hurricanes** for high performance	2016. ?	Super scalar	6	Yes	Yes	9	16
							2 x **Zephyr** for energy efficiency	2016. ?		3	Yes	Yes	5	12
		Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x **Mongoose2 (M2)** for high performance	2017. 02	Super scalar	4	Yes	Yes	8	13
							4 x **Cortex-A53** for energy efficiency	2012. 10		2	No	Yes	2	8
		iPhone X	2017. 11	10 nm	?	오른쪽에있음. ← cache와 architecture Apple A11 Bionic	2 x **Monsoon** for high performance	2017. ?	Super scalar	7	Yes	Yes	13	16
							4 x **Mistral** for energy efficiency	2017. ?		3	Yes	Yes	5	12
		iPhone XS	2018. 09	7 nm	?	Apple A12	2 x **Vortex** for high performance	2018. ?	Super scalar	7	Yes	Yes	13	16
							4 x **Tempest** for energy efficiency	2018. ?		3	Yes	Yes	5	12
		iPhone 11 Pro	2019. 09	7 nm	?	Apple A13	2 x **Lightning** for high performance	2019. ?	Super scalar	7	Yes	Yes	13	16
							4 x **Thunder** for energy efficiency	2019. ?		3	Yes	Yes	5	12
	Tablet PC	HP x2 210 G2 3ML39PA	2018. 02	14 nm	2W	Intel Atom® Processor x5-Z8350	Airmont	2015. ?	Super scalar	2	Yes	Yes	5	12-14

고사양이 숫자가 저사양에 비해 더 높음.

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products

Group#2

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators										
				Fab. Tech	Power	Name	CPU							
							Micro-architecture							
							Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor				Pipeline depth
										No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	
Embedded Computer Systems	Smart Phone	Galaxy S9	2018. 03	10 nm	?	Exynos 9810	4 x **Meerkat (M3)** for high performance	2018. ?	Super scalar	6	Yes	Yes	12	15
							4 x **Cortex-A55** for energy efficiency	2017. 05		2	No	Yes	2	8
		Galaxy Note10	2019. 08	7 nm	?	Exynos 9825	2 x **Cheetah (M4) for** high performance	2019. ?	Super scalar	6	Yes	Yes	12	15
							2 x **Cortex-A75** for moderate performance	2017. 05		3	Yes	Yes	8	11-13
							4 x **Cortex-A55** for energy efficiency	2017. 05		2	No	Yes	2	8
General PC	Laptop	SAMSUNG NT900X3N-K59SS	2017. 07	14 nm	15W	Intel® Core™ i5-7200U	7th Gen. Kaby Lake	2016. 08	Super scalar	5	Yes	Yes	8	14-19
		LG GRAM 17ZD90N-VX70K	2019. 12	10 nm	15W	Intel® Core™ i7-1065G7	10th Gen. Ice Lake	2019. 05	Super scalar	5	Yes	Yes	10	14-19
	Desktop	SAMSUNG DB400T6B	2015. 12	14 nm	65W	Intel® Core™ i7-6700	6th Gen. Skylake	2015. 08	Super scalar	5	Yes	Yes	8	14-19
		Danawa 190721	2019. 07	14 nm	95W	Intel® Core™ i7-9700K	9th Gen. Coffee Lake	2017. 10	Super scalar	5	Yes	Yes	8	14-19
Server/ Workstation	Floating License/ Data Sever	TYAN KFT46	2011. 09	32 nm	80W	Intel® Xeon ® E5606	Westmere WikiChip Block diagram	2010. 01	Super scalar	4	Yes	Yes	6	14-19
	High performance Workstation	Lenovo ThinkStation P500TW 850W	2015. 07	22 nm	140W	Intel® Xeon ® E5-1630 v3	Haswell	2013. 06	Super scalar	4	Yes	Yes	8	14-19
		TYAN TAKO-KQT44	2020. 04	14 nm	150W	Intel® Xeon Gold 6226R	Cascade Lake	2019. ?	Super scalar	5	Yes	Yes	8	14-19

pipelining은 무엇인가!?

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – What is Pipeline (Pipelining)?

Group#2

Type	Sub Type	Product Name	Release date (Year.	Fab.	Power	Name	System-on-Chip / CPU / Micro-architecture / Spec. of Superscalar processor: …nch …ction …lation)	No. of Execution ports	Pipeline depth
							s	12	15
							s	2	8
							s	12	15
							s	8	11-13
							s	2	8
							s	8	14-19
							s	10	14-19
							s	8	14-19
							s	8	14-19
							s	6	14-19
							s	8	14-19
							s	8	14-19

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	System-on-Chip: Fab. Tech	Power	Name	CPU / Micro-architecture: Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor: No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	Pipeline depth
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		Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x **Mongoose2 (M2)** for high performance	2017. 02	Super scalar	4	Yes	Yes	8	13
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특이

pipelining 이란 !?

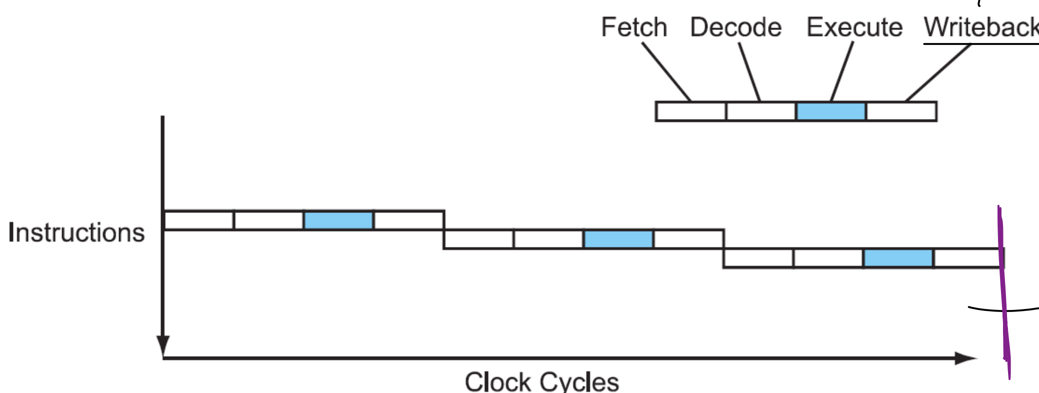
Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – What is Pipeline (Pipelining)?

- **Instruction flow of sequential processor**

(순차적인 processor)

이전과정에서 하나가 추가됨.
(메모리에 다시 쓰는 과정)

→ 4 stage로 읽다고 보면됨



→ 4 stage가 그냥 순서대로 돌아감. (비효율적임)

- **Instruction flow of pipelined processor**

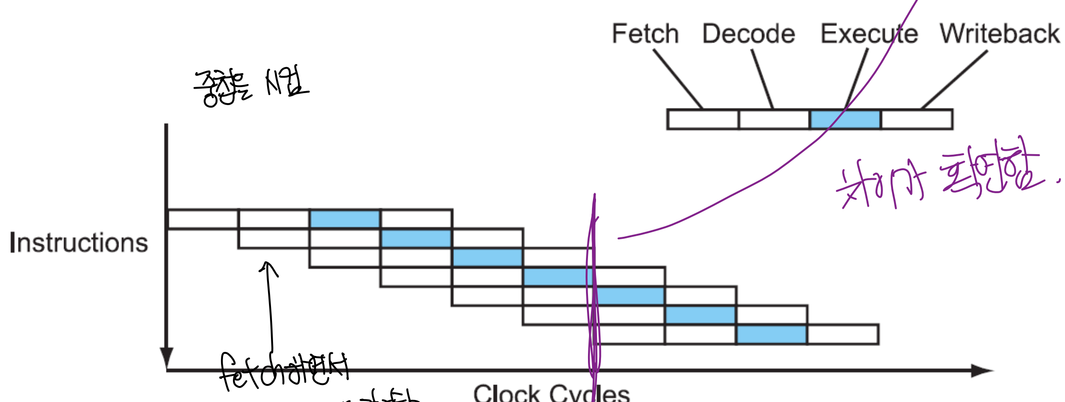
→ clk cycle을 줄일수 있음
Sequential processor에 비해

⇓

성능향상을 위해 pipelining을 사용함.

중첩을 시킴

차이가 확연함.

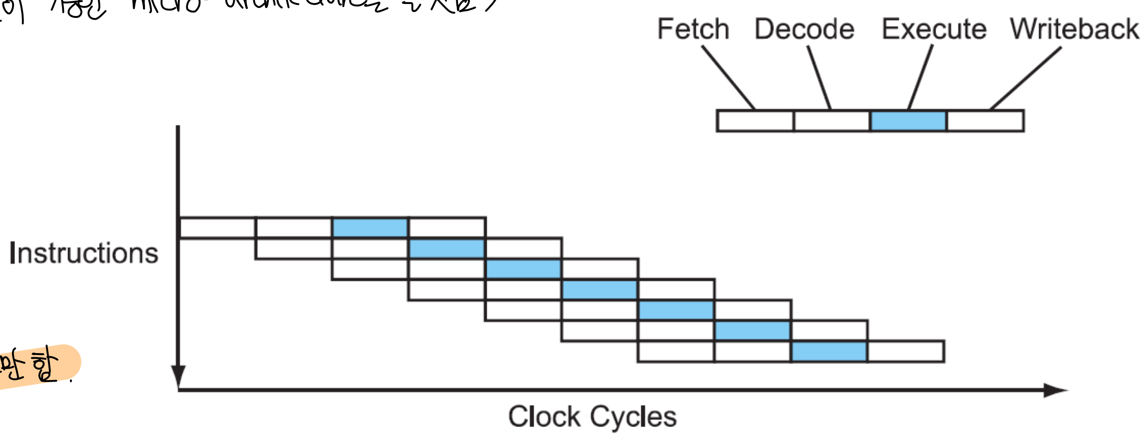


fetch하면서 decode도 같이함.

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products *– What is Pipeline (Pipelining)?*

- **Pipelined micro-architecture**

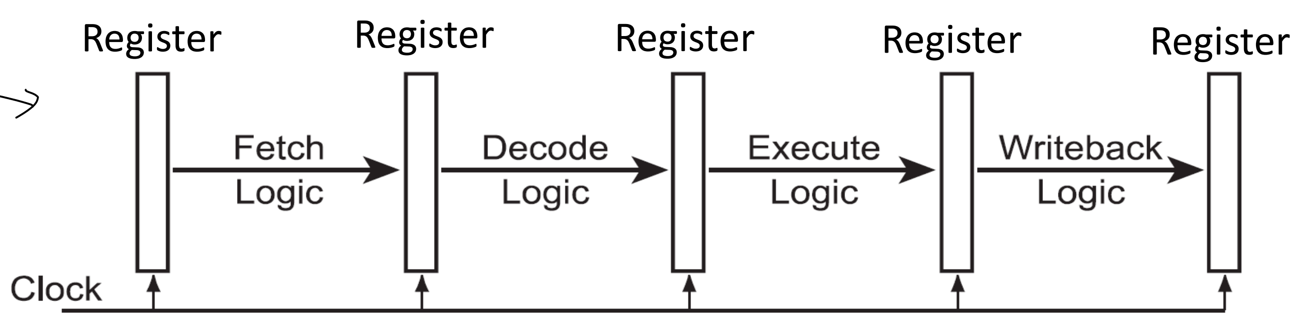
(pipelining이 가능한 micro-architecture를 볼 것임)



Register가 나뉘어 배치되어야만 함.

* architecture가 다음과 같이 생겨야만 pipelining이 가능함.

명령을 (시간적, 공간적)으로 확장할 수 있어야 함.



Critical path delay (Register to Register 중에 가장 긴 path delay)

- **Deeper Pipelines – Superpipelining**
  - The clock speed is limited by the delay length of the longest, slowest stage in the pipeline.
  - The logic gates that make up each stage can be subdivided for converting the pipeline into a deeper super-pipeline with a larger number of shorter stages.
  - Then the whole processor can be run at a higher clock speed.

⇒ 그 결과, 더 빠른 clk으로 동작시킬 수 있음.

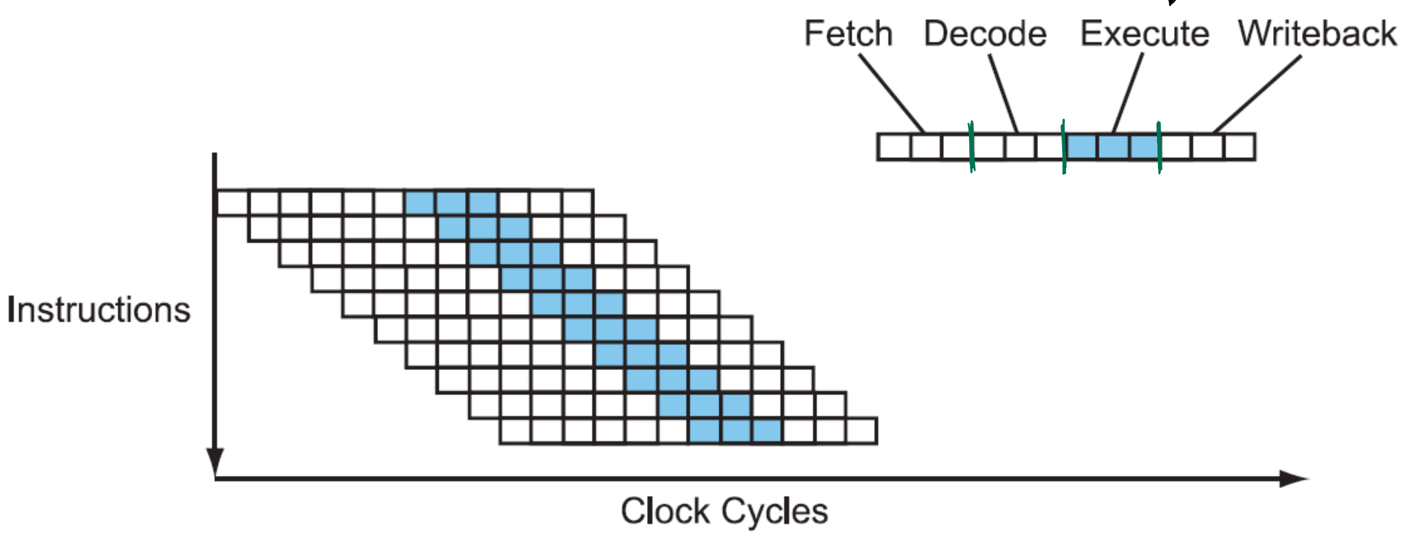
동작 clk을 더 높여주기 위해 (⇒ critical path delay를 더 줄이기 위해)

fetch, decode, execute, writeback 동작을 또 3등분해줌.

subdivided

high performance

- **Instruction flow of superpipelined processor**



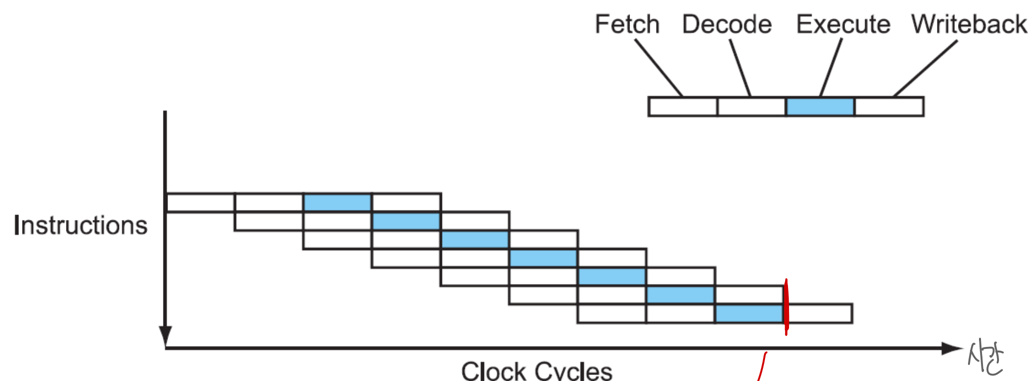
Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – What is Pipeline (Pipelining)?

이런 issue는 매우 많음.
(여기서는 안다룸)

- **Pipeline depth**
  - Number of pipeline stages
  - For example,

Pipeline depth: 4

→ 그냥 pipeline



실행시간 = (cycle cnt × cycle period)

높은수록 많이 나눠졌고
동작 clk주파수가 더 높으니
고성능이 될 수 있겠구나

몇 개로 쪼개졌는지를 나타냄. (한가지 명령어를 수행완료하는 동안)

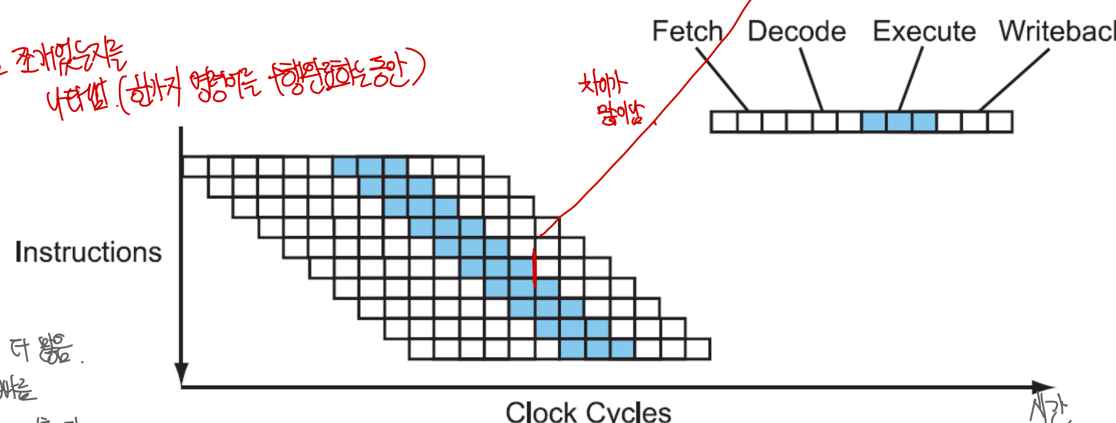
차이가 많이남.

이것을 사용함.

Pipeline depth: 12

→ super pipeline

↳ cycle cnt는 더 많음.
↳ speed는 훨씬 빠름
↳ 전체 실행(수행) 시간이 단축됨.



1:17:52

Superscalar는 무엇인가? (scalar processor와 비교해서 생각해보기)

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – What is Superscalar Processor?

Group#2

ntro' date Year. Ionth)	Type	No. of Issues (Decodes)
'018. ?	Super scalar	6
'017. 05		2
'019. ?	Super scalar	6
'017. 05		3
'017. 05		2
'016. 08	Super scalar	5
'019. 05	Super scalar	5
'015. 08	Super scalar	5
'017. 10	Super scalar	5
'010. 01	Super scalar	4
'013. 06	Super scalar	4
'019. ?	Super scalar	5

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	Fab. Tech	Power	System-on-Chip Name	CPU Micro-architecture Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor: No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	Pipeline depth
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		iPhone 4s	2011. 03	32 nm	?	Apple A5	ARM Cortex-A9	2007. ?	Super scalar	2	Yes	Yes	3	11
		iPhone 5s	2013. 09	28 nm	2~3 W	Apple A7	Apple Cyclone	2013. ?	Super scalar	6	Yes	Yes	9	16
		iPhone 6s	2015. 09	16 nm	?	Apple A9	Apple Twister	2015. ?	Super scalar	6	Yes	Yes	9	16
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							2 x Zephyr for energy efficiency	2016. ?		3	Yes	Yes	5	12
		Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x Mongoose2 (M2) for high performance	2017. 02	Super scalar	4	Yes	Yes	8	13
							4 x Cortex-A53 for energy efficiency	2012. 10		2	No	Yes	2	8
		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x Monsoon for high performance	2017. ?	Super scalar	7	Yes	Yes	13	16
							4 x Mistral for energy efficiency	2017. ?		3	Yes	Yes	5	12
		iPhone XS	2018. 09	7 nm	?	Apple A12	2 x Vortex for high performance	2018. ?	Super scalar	7	Yes	Yes	13	16
							4 x Tempest for energy efficiency	2018. ?		3	Yes	Yes	5	12
		iPhone 11 Pro	2019. 09	7 nm	?	Apple A13	2 x Lightning for high performance	2019. ?	Super scalar	7	Yes	Yes	13	16
							4 x Thunder for energy efficiency	2019. ?		3	Yes	Yes	5	12
	Tablet PC	HP x2 210 G2 3ML39PA	2018. 02	14 nm	2W	Intel Atom® Processor x5-Z8350	Airmont	2015. ?	Super scalar	2	Yes	Yes	5	12-14

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – What is Superscalar Processor?

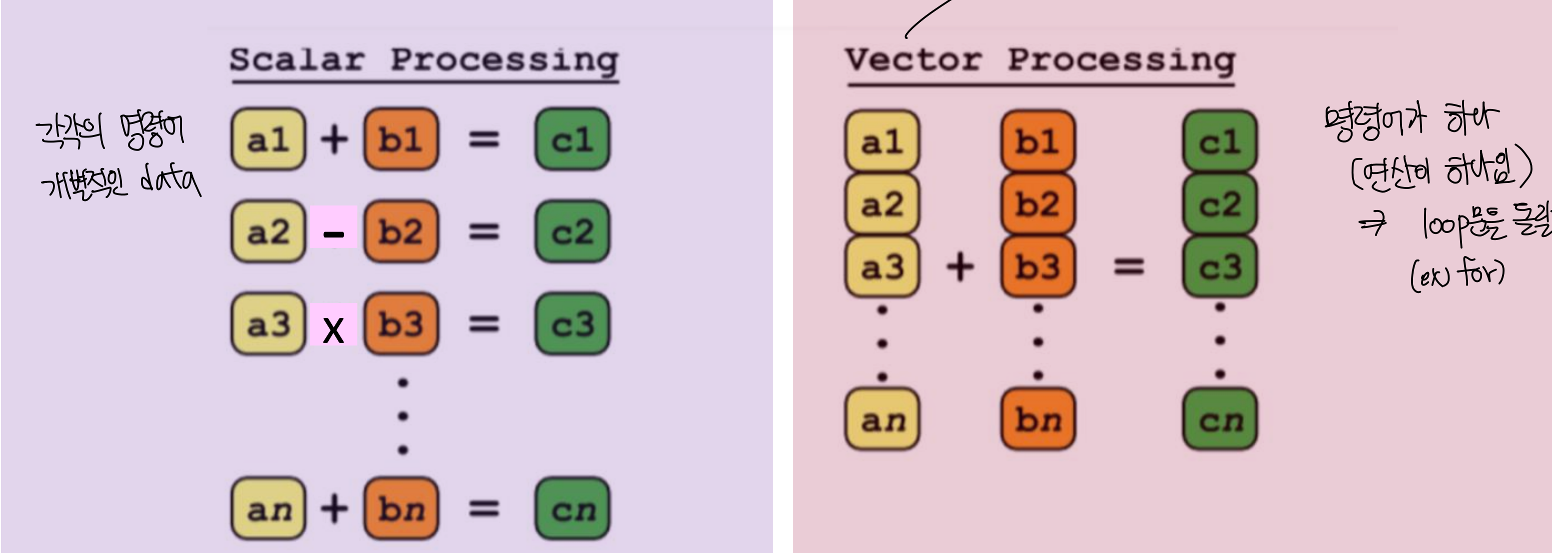
- **Scalar processor versus Vector processor** 둘이 비교해 보면서 특징 알아보기

Instruction과 Data를 가지고 정의된 단어
→ SISD, SIMD 등

Scalar Vs Vector Processing

단일값이 아닌 여러 성분으로
이루어진 종합체 (방향성을 가지고있음)
세부 성분을 더하고 빼기등 연산하는 것이 의미있음

각각의 명령어
개별적인 data



명령어가 하나
(연산이 하나임)
→ loop문을 돌릴때 사용
(ex) for)

그냥 영어 그대로읽음.

→ **SISD (Single Instruction Single Data)**

→ 1개의 명령어를 가지고 1개의 data를 처리하는 것

→ 개별적인 명령을 나열하는 것

SIMD (Single Instruction Multiple Data) 심드

→ 명령어는 하나, 데이터는 여러개

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – What is Superscalar Processor?

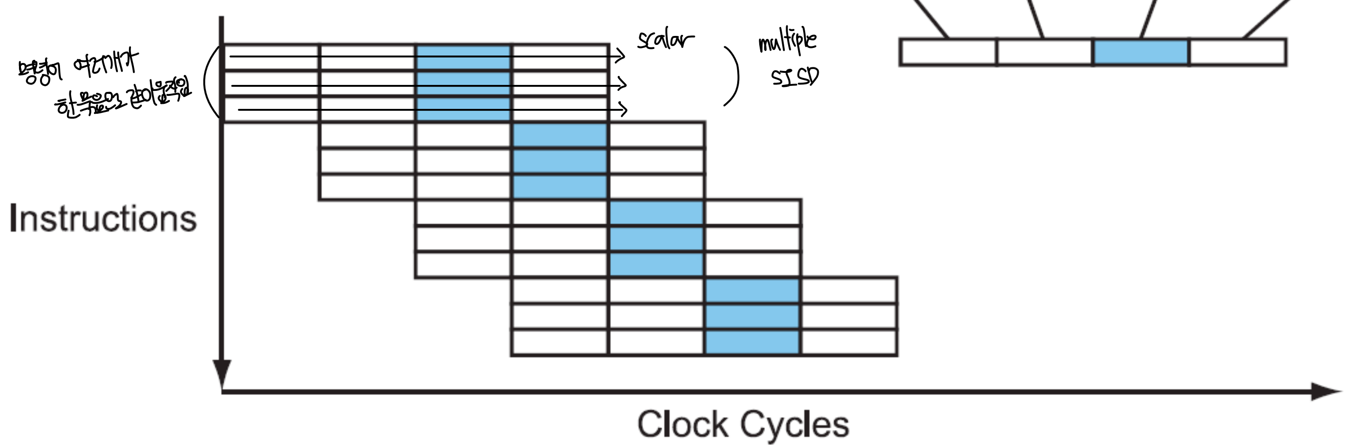
- **Superscalar processor** clk당 instruction 여러개를 끄집어낸다.
  - Issues multiple instructions per clock cycle from a sequential stream
  - Dynamic scheduling of execution units (**scheduling done in hardware**)
    ⇒ 실행 unit의 순서는 H·W가 scheduling함.

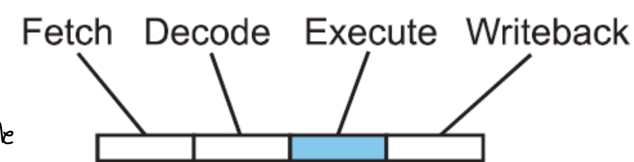
    현재 돌아가는 상황을 보고 판단
    Runtime에 HW가 scheduling함.
    (VLIW와 다른점)
  - Single-core superscalar processor is classified as an SISD (Single Instruction Single Data) processor even though it peforms multiple SISDs. ⇒ single core superscalar에서 쓰는말
    - Multi-core superscalar processor is classified as an MIMD (Multiple Instruction Multiple Data) processor.
      ⇒ multi-core일 때만 이렇게 부름.

- **Instruction flow of superscalar processor**

(Superscalar의 가장 이상적인 pipelining)

명령어 여러개가 한 묶음으로 같이 움직임

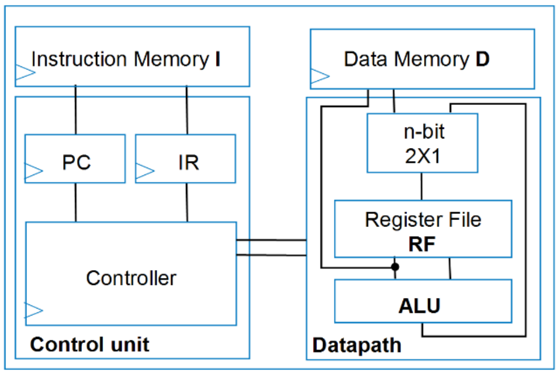




Key Factors for Analyzing Micro-Architecture of Commercial CPU Products *– What is Superscalar Processor?*

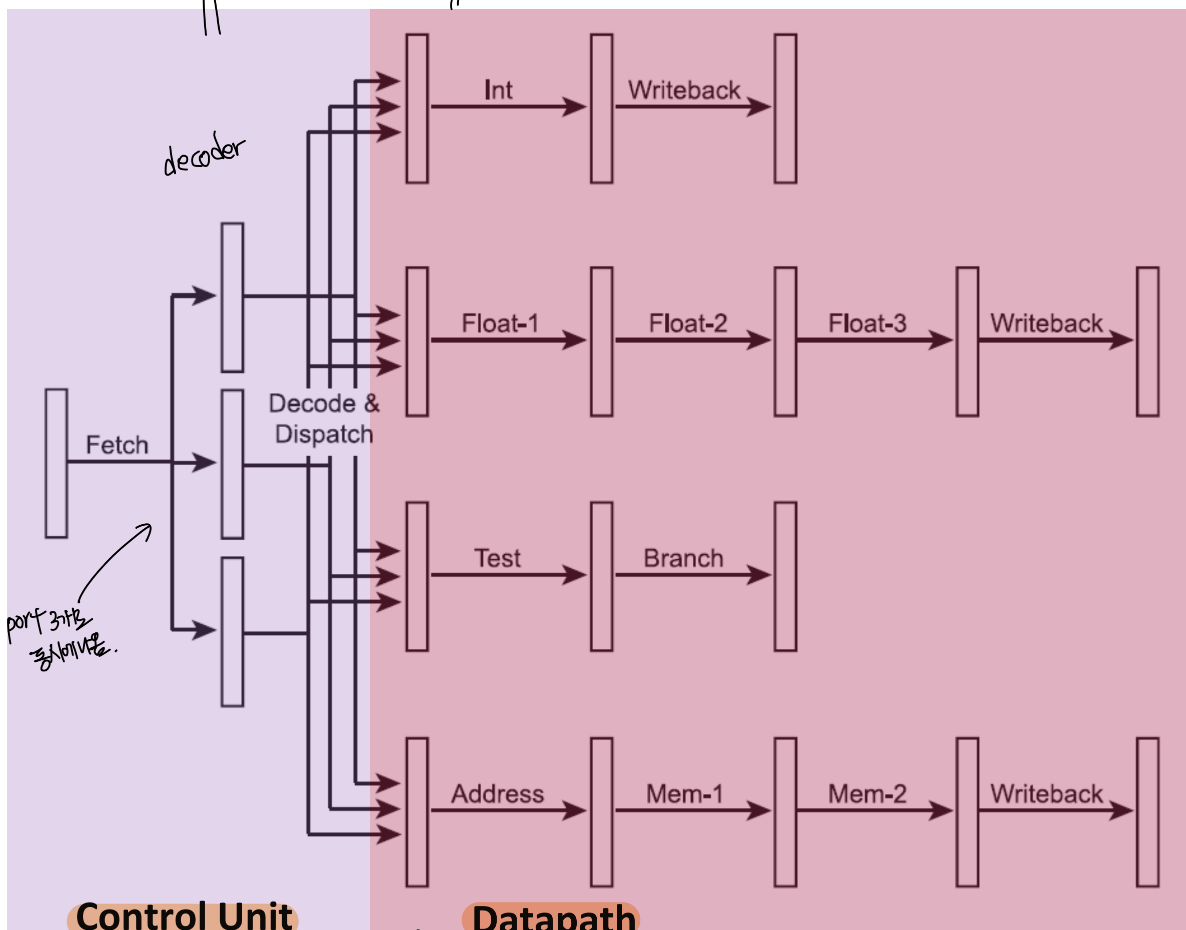
- **Superscalar micro-architecture**

(이전에 배운 단순한 architecture)



No. of Issue
(= decodes)

No. of execution ports

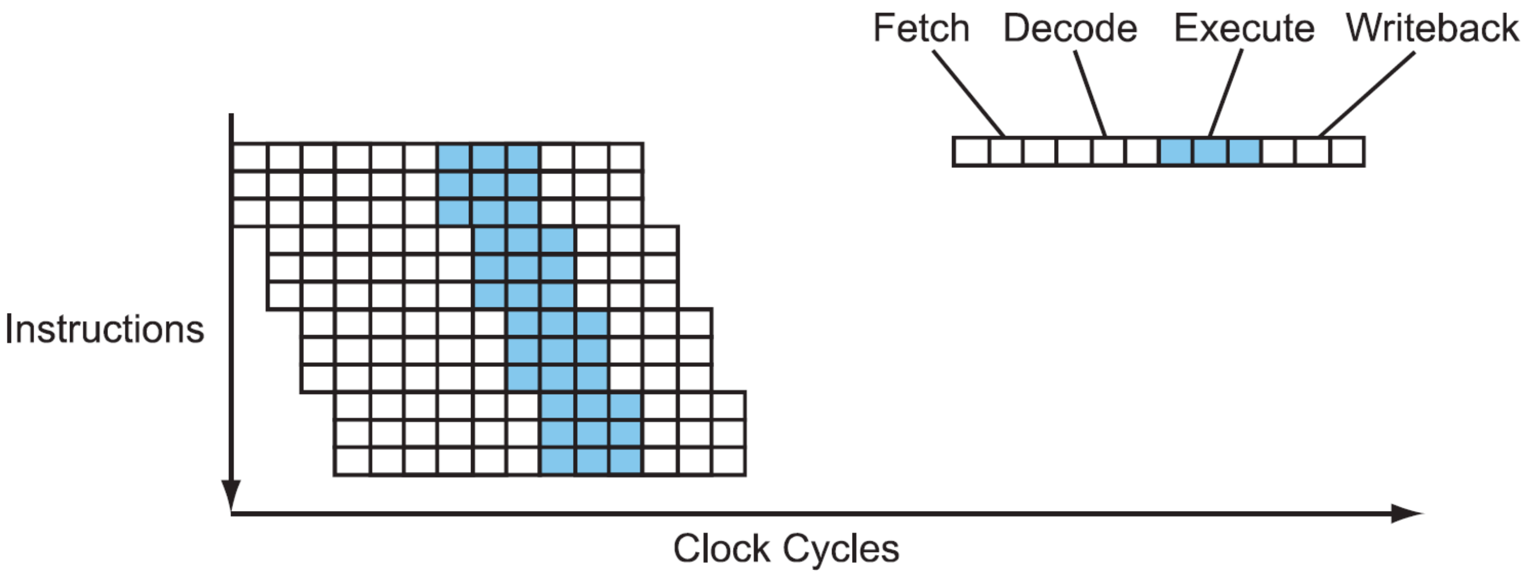


종류가 많은 유닛 있음 ⇒ cost 때문에
무작정 늘릴수만은 없음.

- **Instruction flow of superpipelined-superscalar processor**

  ↳ superscalar processor에서 super pipeline 에서

  ↳ 최근 기기들은 이 기술을 상용화됨.



Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – Spec. of Superscalar Processor

- **No. of Issues (decodes), No. of execution ports ?**

↳ 몇개의 execute를 동시에 수행할 수 있는가?

적은 high performance core
+ 적은 전력

Group#2

Type	Sub Type	Product Name	Release date (Year. Month)	Fab. Tech	Power	Name	Name	Intro' date (Year. Month)	Type	No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports
				System-on-Chip			CPU: Micro-architecture			Spec. of Superscalar processor			
								2018. ?	Superscalar	6	Yes	Yes	12
								2017. 05		2	No	Yes	2
								2019. ?	Superscalar	6	Yes	Yes	12
								2017. 05		3	Yes	Yes	8
								2017. 05		2	No	Yes	2
								2016. 08	Superscalar	5	Yes	Yes	8
								2019. 05	Superscalar	5	Yes	Yes	10
								2015. 08	Superscalar	5	Yes	Yes	8
								2017. 10	Superscalar	5	Yes	Yes	8
								2010. 01	Superscalar	4	Yes	Yes	6
								2013. 06	Superscalar	4	Yes	Yes	8
								2019. ?	Superscalar	5	Yes	Yes	8

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	Fab. Tech	Power	Name	Name	Intro' date (Year. Month)	Type	No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports
				System-on-Chip			CPU: Micro-architecture			Spec. of Superscalar processor			
Embedded Computer Systems	Smart phone	iPhone 4	2010. 06	45 nm	?	Apple A4	ARM Cortex-A8	2005. ?	Superscalar	2	No	Yes	2
		iPhone 4s	2011. 03	32 nm	?	Apple A5	ARM Cortex-A9	2007. ?	Superscalar	2	Yes	Yes	3
		iPhone 5s	2013. 09	28 nm	2~3 W	Apple A7	Apple Cyclone	2013. ?	Superscalar	6	Yes	Yes	9
		iPhone 6s	2015. 09	16 nm	?	Apple A9	Apple Twister	2015. ?	Superscalar	6	Yes	Yes	9
		iPhone 7	2016. 09	16 nm	?	Apple A10 Fusion	2 x Hurricanes for high performance	2016. ?	Superscalar	6	Yes	Yes	9
							2 x Zephyr for energy efficiency	2016. ?		3	Yes	Yes	5
		Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x Mongoose2 (M2) for high performance	2017. 02	Superscalar	4	Yes	Yes	8
							4 x Cortex-A53 for energy efficiency	2012. 10		2	No	Yes	2
		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x Monsoon for high performance	2017. ?	Superscalar	7	Yes	Yes	13
							4 x Mistral for energy efficiency	2017. ?		3	Yes	Yes	5
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							4 x Tempest for energy efficiency	2018. ?		3	Yes	Yes	5
		iPhone 11 Pro	2019. 09	7 nm	?	Apple A13	2 x Lightning for high performance	2019. ?	Superscalar	7	Yes	Yes	13
							4 x Thunder for energy efficiency	2019. ?		3	Yes	Yes	5
	Tablet PC	HP x2 210 G2 3ML39PA	2018. 02	14 nm	2W	Intel Atom® Processor x5-Z8350	Airmont	2015. ?	Superscalar	2	Yes	Yes	5

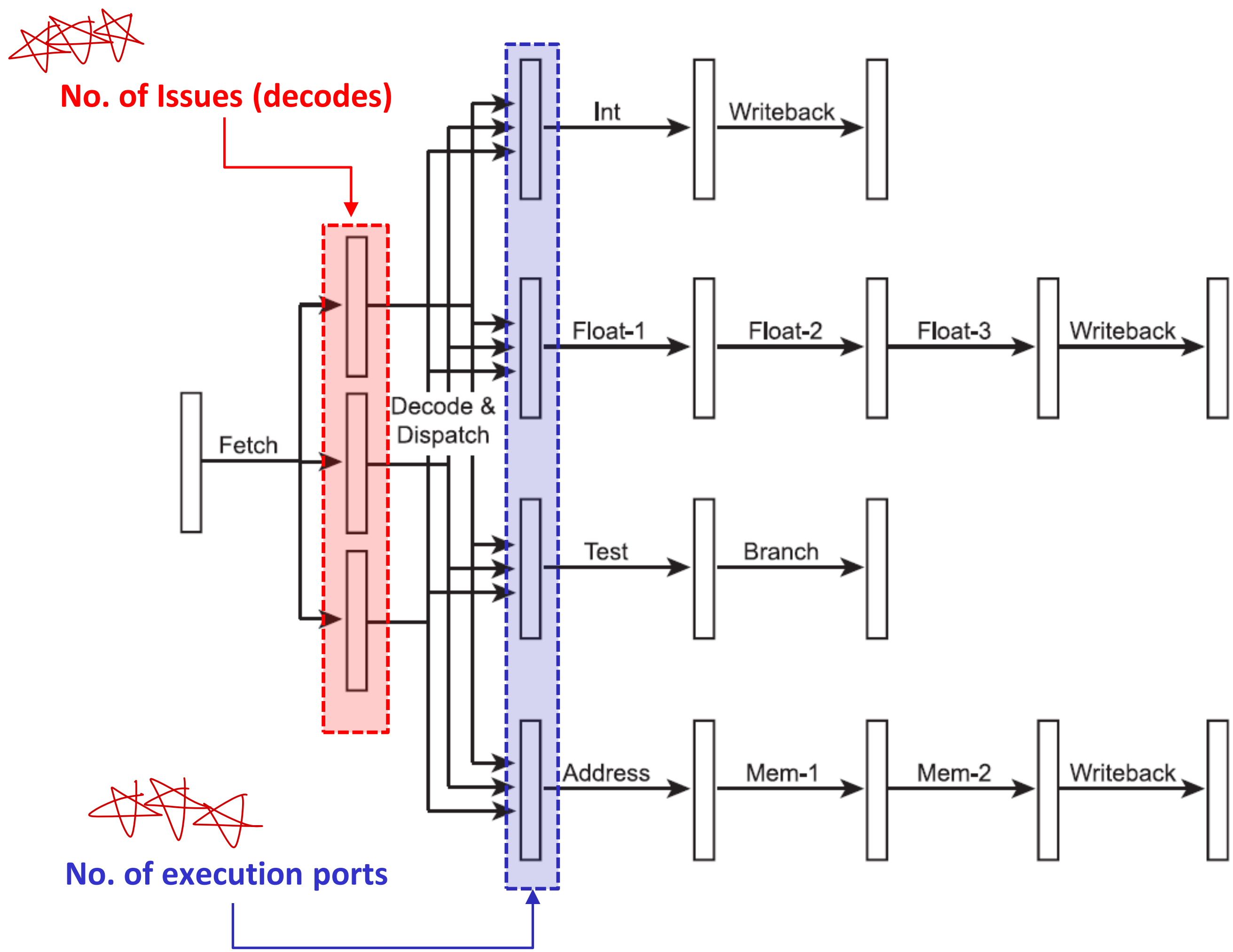
10 개가 넘어감

모바일보다 적음 ...
✗ why?

그래도 기본적인 성능이 더 좋은데 + core도 큼
⇒ 기본동작 freq가 매우 큼.

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – Spec. of Superscalar Processor

- **No. of Issues (decodes), No. of execution ports ?** → 숫자가 크면 클수록 high performance.



#CPU 1
(11주차)

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – Spec. of Superscalar Processor

- **Out of order execution?**

Yes가 좋은 것임.

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	Fab. Tech	Power	Name (System-on-Chip)	Name (CPU Micro-architecture)	Intro' date (Year. Month)	Type	No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	Pipeline depth
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Group#2

Out of order execution	Branch prediction (speculation)
Yes	Yes
No	Yes
Yes	Yes
Yes	Yes
No	Yes
Yes	Yes
Yes	Yes
Yes	Yes
Yes	Yes
Yes	Yes
Yes	Yes
Yes	Yes

single core에서는 pipeline과 관련없음
multi core에서는 〃 관련있음.

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – Spec. of Superscalar Processor

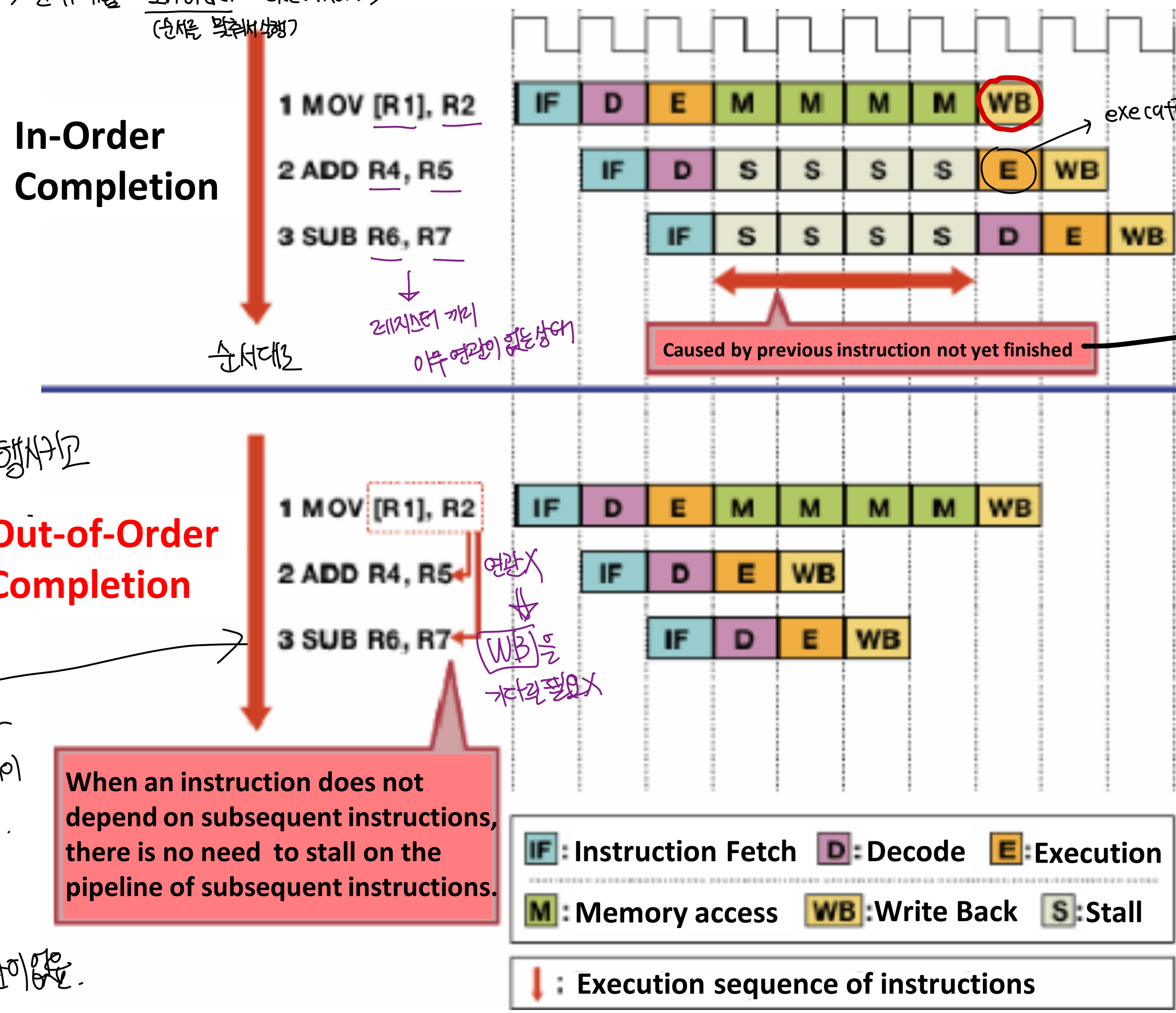
이것을 판단하기 위한 H.W logic이 필요.
(But, energy를 많이 먹음)

(순서를 안 맞춰서)

- **Out of order execution?**

(↔ 반대 개념 In order execution)
(순서를 맞춰서 실행)

⊕ single-core 기준



execution에서 Memory에 write back된 결과를 사용할 수도 있기 때문에 기다리는 것.

아직 끝나지 않은 이전 명령어 때문에 다음 명령어가 기다리는 상황.
(pipeline 없이도 더이상 진행하지 않음)

순서대로

레지스터 끼리 아무 연관이 없는 상태

순서가 상관없는 애들은 동시 다발적으로 수행시키고 끝나는 것도 그냥 내비둠

연관X ⇓ WB를 기다릴 필요X

시작순서도 out-of-order completion이 가능함.
⇓
어떤 명령어부터 fetch하든 상관이 없음.

→ 5 stage의 pipelining

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – Spec. of Superscalar Processor

분기점에 대한 예측

- **Branch prediction (speculation)?** ⇒ All "Yes" ····> 개념만 알기.

Group#1

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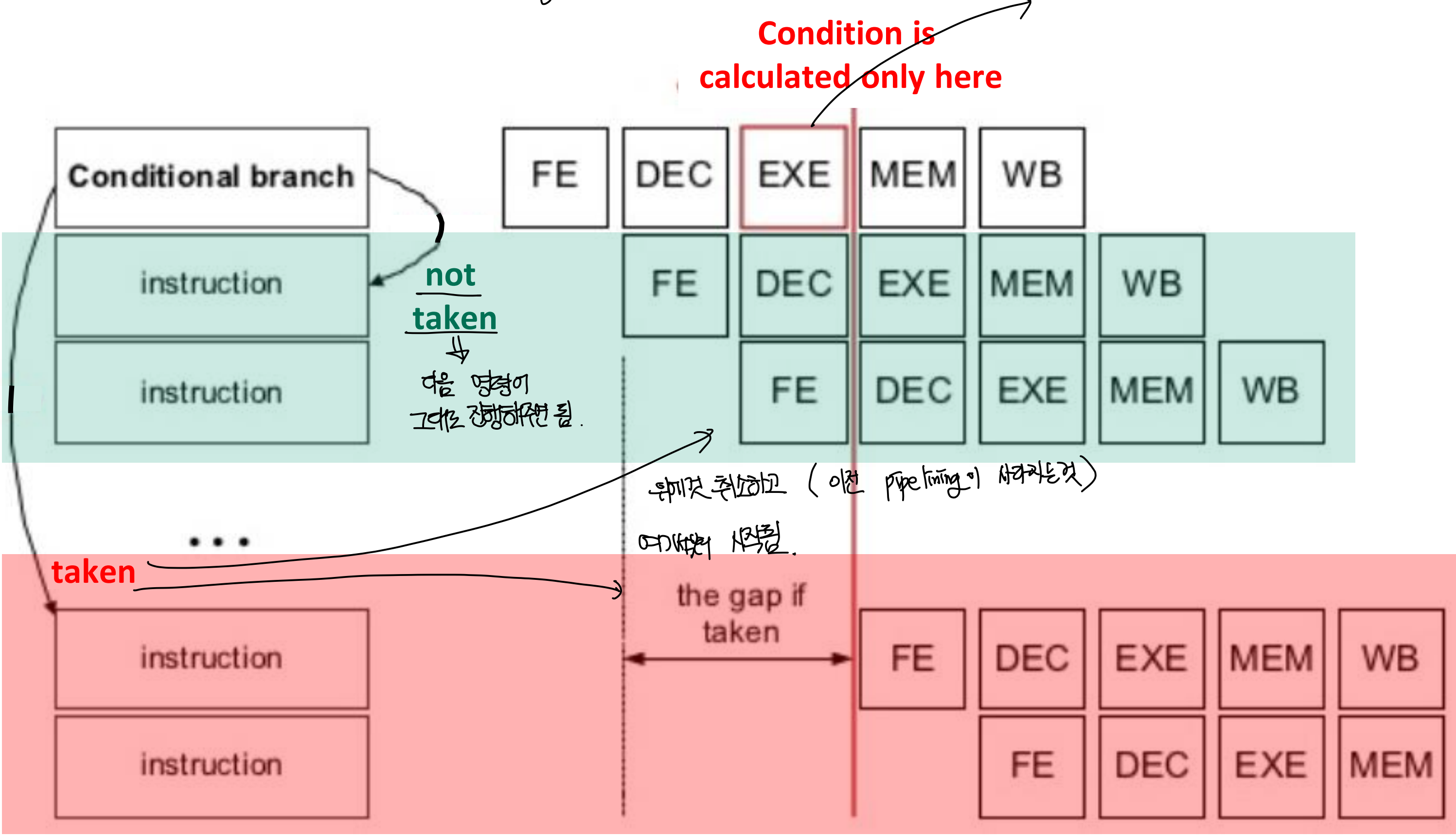
Group#2

System-on-Chip / CPU / Micro-architecture / Spec. of Superscalar processor: Out of order execution	Branch prediction (speculation)
Yes	Yes
No	Yes
Yes	Yes
Yes	Yes
No	Yes
Yes	Yes
Yes	Yes
Yes	Yes
Yes	Yes
Yes	Yes
Yes	Yes
Yes	Yes

- **Branch prediction (speculation)?** → Branch 예측이 왜 필요한가?
  - Why need?: in order not to stall pipelining
    → pipelining을 하기 때문에 반드시 필요함.

exe 에서 branch가 어디로 갈지 결정됨.



오늘날에는 기본이상함.
(이미 다 개발되어 들어간 기술)

Key Factors for Analyzing Micro-Architecture of Commercial CPU Products – Spec. of Superscalar Processor

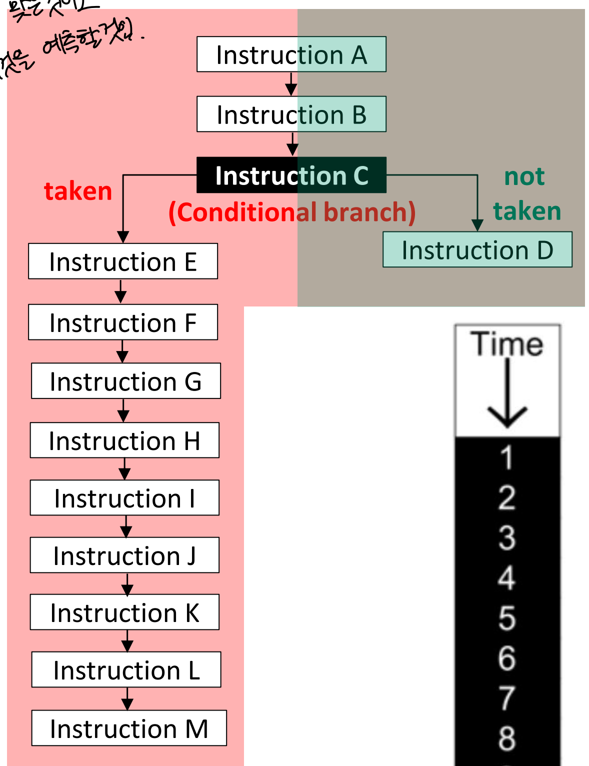
H·W 또는 SW로
이것을 예측하는
알고리즘이 있음.

- **Branch prediction (speculation)?**
  - For example

pipeline 하는 경우
pipeline 안하는 경우

stall O
(not taken)
stall X
(taken)
경우

taken이 맞는 것이고
└> 이것을 예측할 것임.



pipeline 안하는 경우

'taken' selected in instruction C

pipeline 하는 경우

'taken' selected in instruction C

성능극대화
(단, predicted 가 맞아야함)

predicted with 'taken'

Time	Conventional				Pipelined				Pipelined with branch prediction			
	Fetch	Decode	Process	#	Fetch	Decode	Process	#	Fetch	Decode	Process	#
1	A			0	A	*	*	0	A	*	*	0
2		A		0	B	A	*	0	B	A	*	0
3			A	1	C	B	A	1	C	B	A	1
4	B			1		C	B	2	E	C	B	2
5		B		1		GAP	C	3	F	E	C	3
6			B	2	E			3	G	F	E	4
7	C			2	F	E		3	H	G	F	5
8		C		2	G	F	E	4	I	H	G	6
9			C	3	H	G	F	5	J	I	H	7
10	E			3	I	H	G	6	K	J	I	8
11		E		3	J	I	H	7	L	K	J	9
12			E	4	K	J	I	8	M	L	K	10

stall

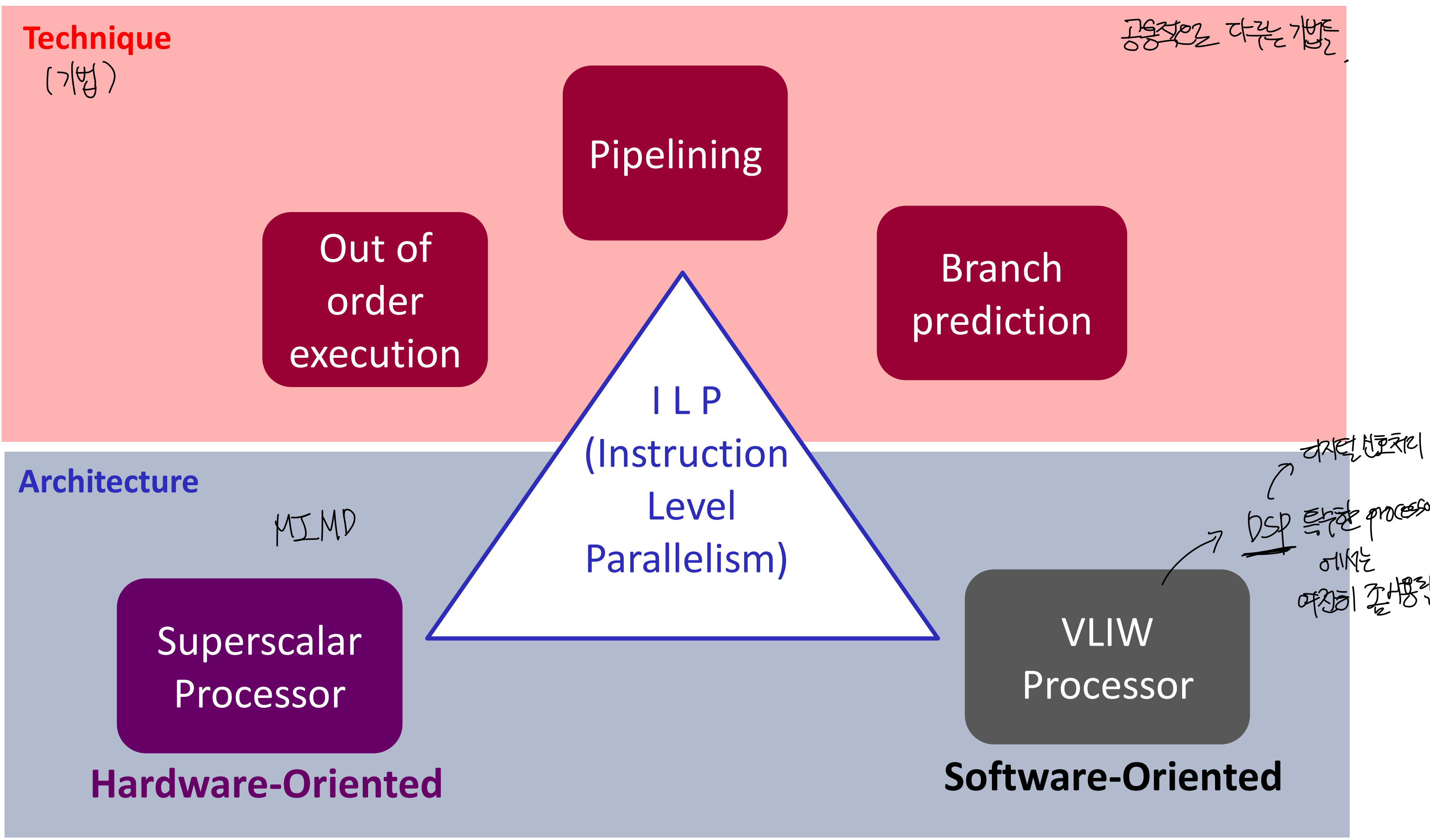
예측이 맞은 경우

instruction 표시

최대한 많은 명령을 병렬로 동시 다발적으로 처리하면 성능이 향상됨.

Introduction to ILP (Instruction Level Parallelism)

Multi-core ⇒ TLP (Threads Level Parallelism) → 공정기술의 발달로 개발됨 ...



What is VLIW (Very Long Instruction Word) Processor?

복잡한 명령어

- **VLIW (Very Long Instruction Word) processor**
  - Issues one very 'wide' instruction per clock cycle; this instruction contains multiple operations

    scheduling을 compiler가 함. (프로그램 실행전에 반영

  - Static scheduling of execution units (**done by compiler**).
  - Single-core VLIW processor may be classified as a SISD (Single Instruction Single Data) processor.

    명령어가 다 다를 경우 (+, −, ×, ÷ 등)

    - If the multiple operations in an instruction are different.
  - Single-core VLIW processor may be classified as a SIMD (Single Instruction Multiple Data) processor.

    명령어가 다 같을 경우 (모두 × 이다 등)

    - If the multiple operations in an instruction are same.

WLIW는 둘다 될수있다.

↓

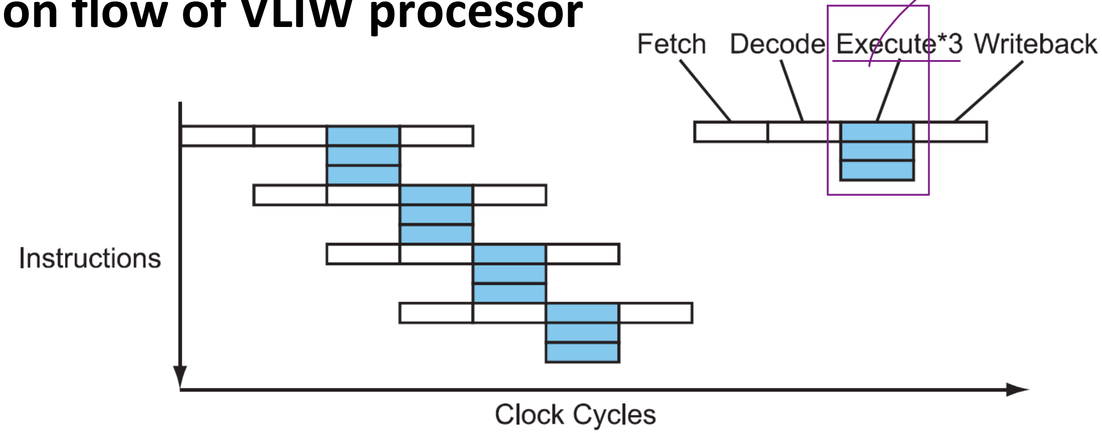
"VLIW를 그냥 SIMD다" 라는 것은 잘못된 명제임.

- **Instruction flow of VLIW processor**

독립적으로 수행해도 무방한 명령어가 같이 들어가 있는 것.

↓

포장한 1개의 명령어임.



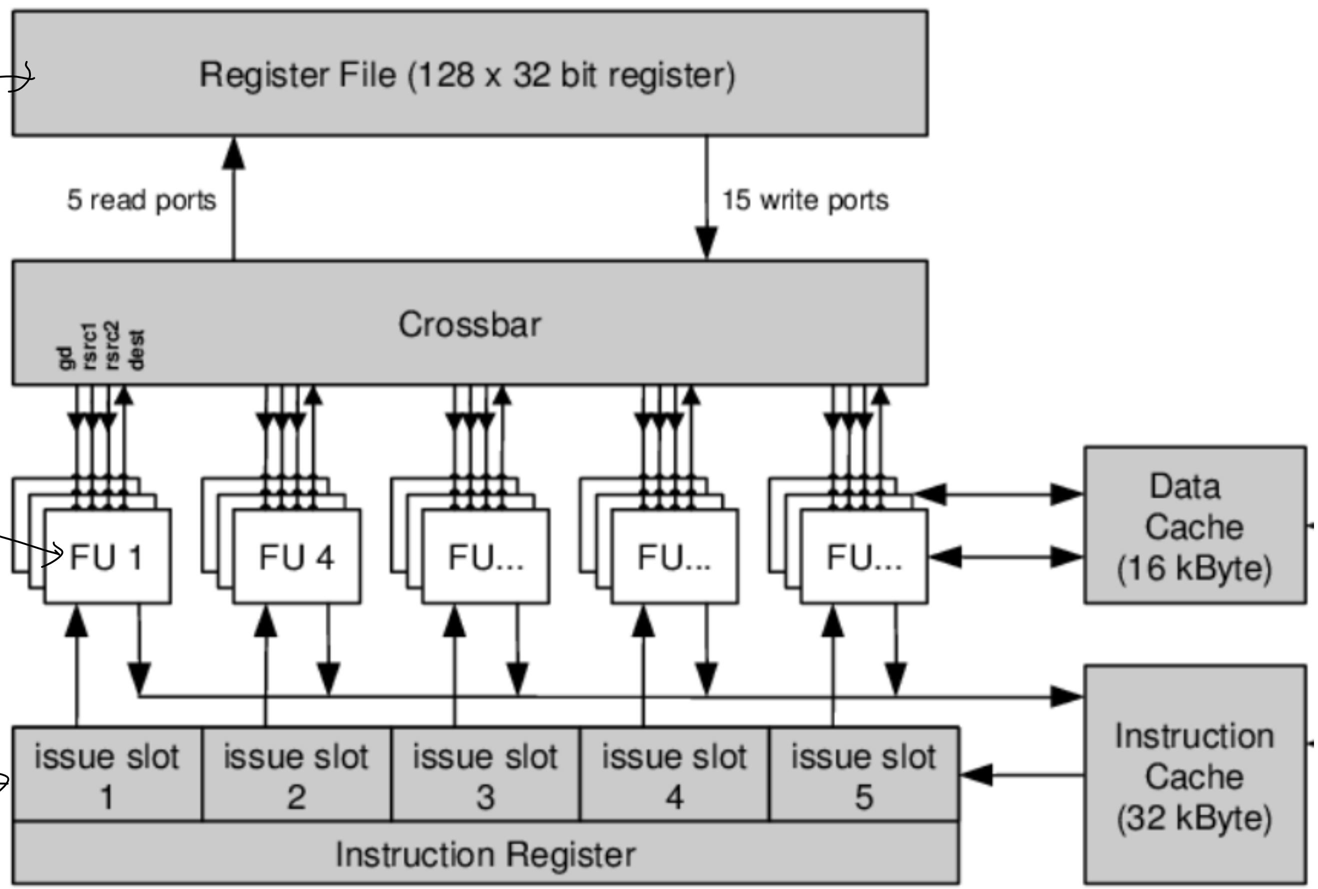
What is VLIW (Very Long Instruction Word) Processor?

- **VLIW micro-architecture** (옛날 VLIW 모델)

중앙한 Register file을 공유하면서 동작함.

Function unit (+, -, ×, ÷ 등)

독립적으로 제각각 수행될 수 있는 것들



Comparison between superscalar processor and VLIW processor

win

Superscalar Processor

power를 많이 먹음.

(in Runtime)

- Hardware finds parallelism
  주체가 H.W, HW가 병렬성을 발견함.
- More complex hardware
  복잡한 HW
- More power consumption
  power 많이 요구함
- Works even with lousy compiler
  compiler 가 안좋아도 잘 동작함.

공정기술이 발전하면서 복잡한 HW가 큰 문제가 아니게 됨.

VS

lose

VLIW Processor

성능향상에 한계가 있음

- Compiler finds parallelism
  컴파일러가 프로그램 실행전에 병렬성을 찾아 놓음.
- Simpler hardware
  단순한 HW
- Less power consumption
  power 요구 감소
- Works only if compiler has done the right things
  아주 좋은 compiler가 필요함.
  실제로는 predict 한 것이 비효율적일 수 있음.

Comparison between superscalar processor and VLIW processor

- **Why have the superscalar processor become the norm in today's commerical CPUs, not VLIW processor?**

  ↳ 왜 superscalar가 오늘날 상용 CPU에 범용적 표준이 되었는가?

  – https://namu.wiki/w/%EC%9D%B8%ED%85%94%20%EC%95%84%EC%9D%B4%ED%83%9C%EB%8B%88%EC%97%84%20%EC%8B%9C%EB%A6%AC%EC%A6%88

    ↳ 나무위키 링크

    ↳ "인텔 아이테니엄 시리즈" (ITANIUM)

      ↳ "VLIW" architecture 을 선택한 core였음 (20세기 → 21세기) 1999 ~ 2000정도 ← AMD에게 밀린시기

      ↳ x86을 버리고 새로운 core를 만듦

      ↳ 완전 망함...

AMD Intel

뿌리가 같음 (instruction이 같음)

전력소모

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

지표 , 기준 (= guidline)

증가시킨 확률이 높은.

- **Prerequisite** = 선수체계
  └→ 미리 알아야하는 체계

성능향상을 위한 Technique

단일 core 성능향상

private 캐시가 뒷받침이 되어야 함.

코어의 개수증가

코어들이 공유하는 캐시가 증가해야함. critical path delay를 줄이는것.

Techniques for Improving Performance	**Synergy Effect (① and ②)**		**Synergy Effect (③ and ④)**		⑤ Increase of Clock Frequency
	① Improvement of Micro-Architecture	② Increase of Private Cache Size	③ Increase in the Number of Cores	④ Increase of Shared Cache Size	
고려해야하는 문제점들. **Problems**	Increasing **Power** Consumption	Increasing **Much Power** Consumption	Increasing **Power** Consumption	Increasing **Much Power** Consumption	Increasing **Power** Consumption
	Maybe Increasing Delay				

power 비교

power 비교

power가 증가하겠지만 단일 core 성능을 향상시키려고 해서 큰 power가 필요한 것은 아님.

캐시크기를 늘리면 2~3배 늘림. (32KB → 64KB) 이렇게

이때 많은 power를 먹음

① < ③ 필요한 power

power 소모가 엄청남.

(4MB → 8MB 이렇게 크게증가 시킴)

이에 대한 power 변화

1G → 1.2G 이렇게 조금씩 변화.

Improvement of Fabrication process Technology
(For example: 14nm process → 10nm process)

Effect	Reduction of Delay and Power Consumption in CMOS

Relieving/Reducing the problems

||

문제들 완화 / 경감 시켜줄 수 있음.

공정기술의 발전영향

└→ 특히 임베디드에 영향이 큼

① ② ⑤ ⇒ 같이보기

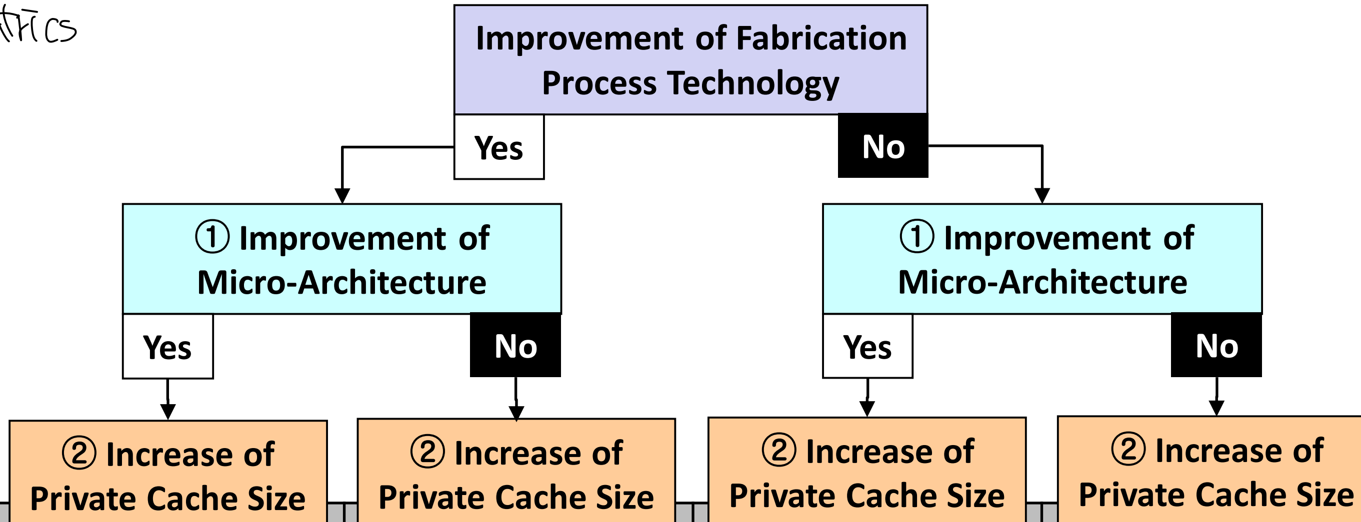
③ ④ ⑤ ⇒ 같이보기

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

* 동일회사에서 만든 동일 architecture

- Metrics for ① embedded CPU and ② non-embedded CPU in laptop (general PC)

2가지 case에 대한 Matrics



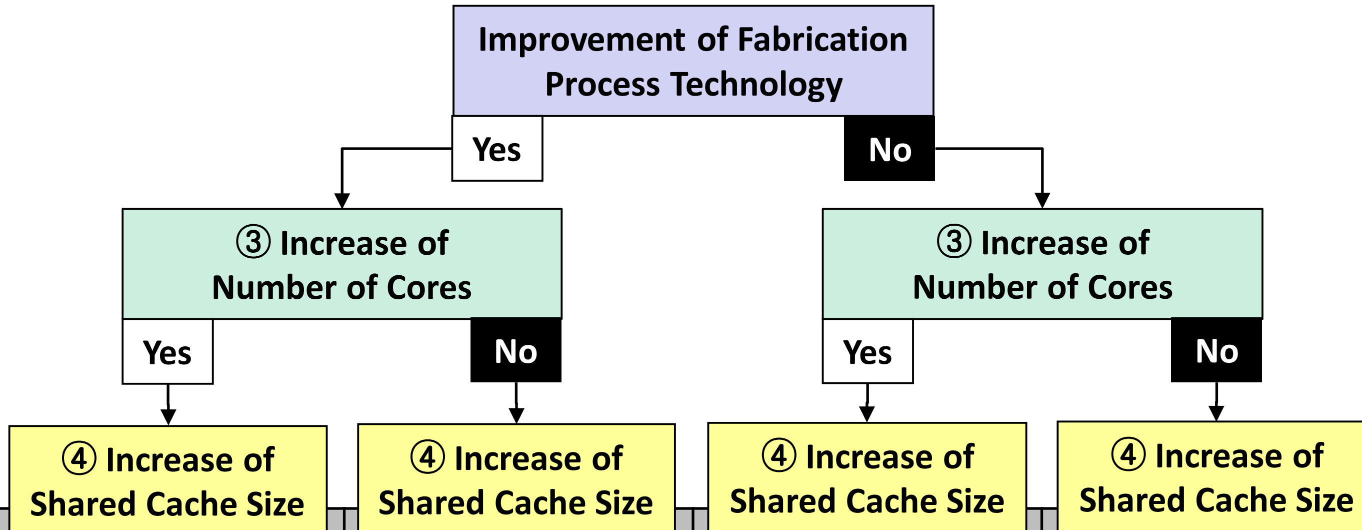
⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid =	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid $\xrightarrow{\text{개선영향}}$	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High $\xrightarrow{\text{개선영향}}$	Low	Low	성능향상X	High	Low	Low	-
	Power Consumption	Low $\xrightarrow{\text{개선영향}}$	Very Low	Low	Lowest	High	Mid	High	-

공정이 발전해서

성능이 같음, but power 또한 더 좋음.

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Metrics for embedded CPU and non-embedded CPU in laptop (general PC)**



⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Metrics for non-Embedded CPU in desktop, server and workstation**

→ 이 종류 구분하기

단일 core의 향상

① Improvement of Micro-Architecture

Yes → ② Increase of Private Cache Size

No → ② Increase of Private Cache Size

⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low
No	Performance Improvement	High	Low	Low	-

power를 볼 필요가 없음
→ desktop이여서
→ 성능만 보면 됨.
→ power, 발열에서
⇓
cooling을 이미 잘함

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Metrics for non-Embedded CPU in desktop, server and workstation**

→ core의 개수

		③ Increase in the Number of Cores: Yes		③ Increase in the Number of Cores: No	
⑤ Increase of Clock Freq.	Case / Effect	④ Increase of Shared Cache Size: Yes	④ Increase of Shared Cache Size: No	④ Increase of Shared Cache Size: Yes	④ Increase of Shared Cache Size: No
Yes	Performance Improvement	Very High	Mid	Mid	Low
No	Performance Improvement	High	Low	Low	-

성능향상은
① ②
③ ④
이렇게 묶어서
정리해야함.

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#1 (laptop)

intel vs intel 비교가능
intel vs AMD 비교불가

cache

Group#2

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators										
				Fab. Tech	Power	Name	CPU							
							Micro-architecture	Bit-Width	Clock Freq.	ISA	No. of Cores	L1 Cache	L2 Cache	L3 Cache
General PC	Laptop	SAMSUNG NT900X3N-K59SS	2015. 03	14 nm	15W	Intel® Core™ i5-7200U	7th Gen. Kaby Lake	64	2.5 ~ 3.1 GHz	x86 -64	2	Per-core: I-32KB, D-32KB	Per-core: 256KB	3MB shared by 2 cores and GPU
		LG GRAM 17ZD90N-VX70K	2019. 12	10 nm	15W	Intel® Core™ i7-1065G7	10th Gen. Ice Lake	64	1.3 ~ 3.9 GHz	x86 -64	4	Per-core: I-32KB, D-48KB	Per-core: 512KB	8MB shared by 4 cores and GPU

4년

CPU product
→ intel이어서 비교 가능

여기서 혁신적인
변화가 일어난것.

Micro architecture

Group#2

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators										
				Fab. Tech	Power	Name	CPU							
							Micro-architecture							
							Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor				Pipeline depth
										No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	
General PC	Laptop	SAMSUNG NT900X3N-K59SS	2017. 07	14 nm	15W	Intel® Core™ i5-7200U	7th Gen. Kaby Lake	2016. 08	Super scalar	5	Yes	Yes	8	14-19
		LG GRAM 17ZD90N-VX70K	2019. 12	10 nm	15W	Intel® Core™ i7-1065G7	10th Gen. Ice Lake	2019. 05	Super scalar	5	Yes	Yes	10	14-19

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#1 (laptop)

큰변화있

Spec. of Superscalar processor			
No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports
5	Yes	Yes	8
5	Yes	Yes	10

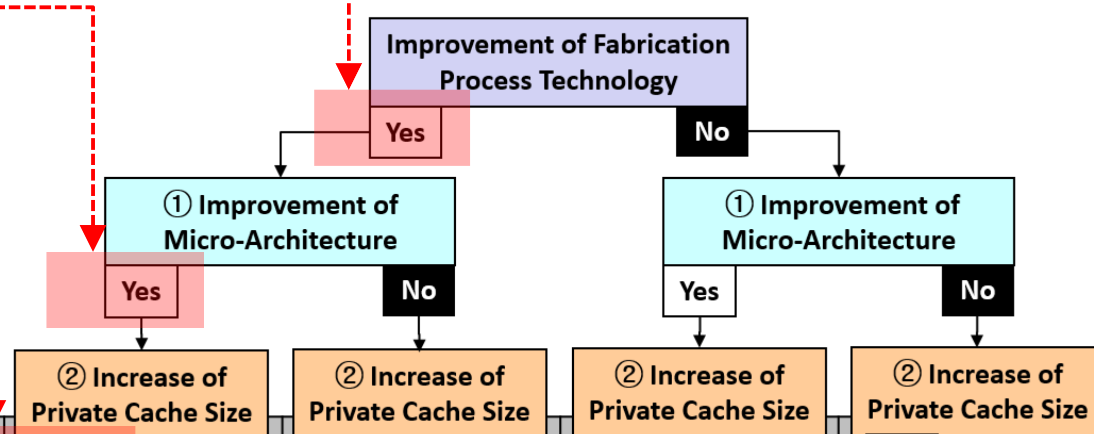
14 nm
10 nm

L1 Cache	L2 Cache
Per-core: I-32KB, D-32KB	Per-core: 256KB
Per-core: I-32KB, D-48KB	Per-core: 512KB

변화2배

Clock Freq.
2.5 ~ 3.1 GHz
1.3 ~ 3.9 GHz

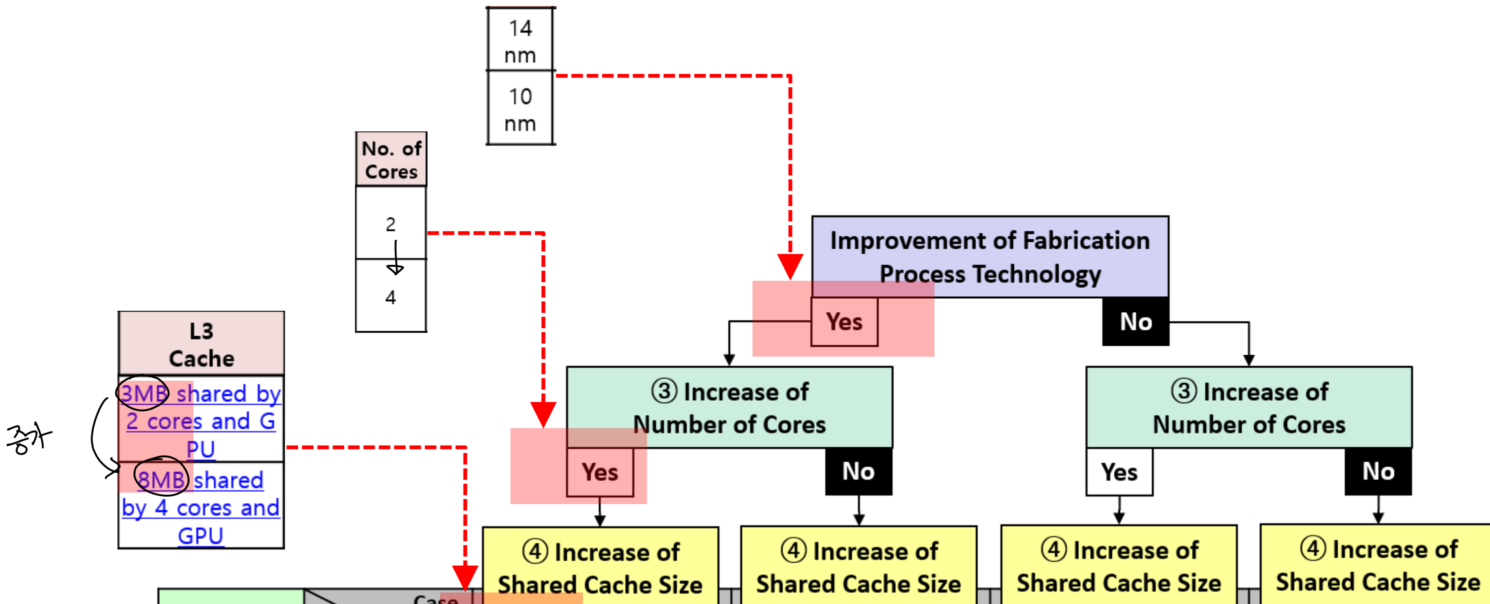
Max Clk 기준



⑤ Increase of Clock Freq.	Effect \ Case	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#1 (laptop)



Clock Freq.
2.5 ~ 3.1 GHz
1.3 ~ 3.9 GHz

⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#2-1 (smartphone-Galaxy)

High performance core만 비교하는것임.

Group#1 & 2

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators: Fab. Tech	Power	Name	CPU: Micro-architecture	Bit-Width	Clock Freq.	ISA	No. of Cores	L1 Cache	L2 Cache	L3 Cache
Embedded Computer Systems	Smart Phone	Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x **Mongoose2 (M2)** for high performance	64	2.3 GHz	ARM v8-A	8	Per-core: I-64KB, D-32KB	2MB shared	None
							4 x **Cortex-A53** for energy efficiency		1. 7 GHz			Per-core: I-32KB, D-32KB	256KB shared	
Embedded Computer Systems	Smart Phone	Galaxy S9	2018. 03	10 nm	?	Exynos 9810	4 x **Meerkat (M3)** for high performance	64	2.9 GHz	ARM v8-A	8	Per-core: I-64KB, D-64KB	Per-core: 512KB	4MB shared
							4 x **Cortex-A55** for energy efficiency		1. 9 GHz	ARM v8.2-A		Per-core: I-32KB, D-32KB	256KB Shared	

1년

증가

공정같음

공정이 그대로인데 micro-architecture 변화시킴

Group#1 & 2

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators: Fab. Tech	Power	Name	CPU / Micro-architecture: Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor: No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	Pipeline depth
Embedded Computer Systems	Smart Phone	Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x **Mongoose2 (M2)** for high performance	2017. 02	Super scalar	4	Yes	Yes	8	13
							4 x **Cortex-A53** for energy efficiency	2012. 10		2	No	Yes	2	8
Embedded Computer Systems	Smart Phone	Galaxy S9	2018. 03	10 nm	?	Exynos 9810	4 x **Meerkat (M3)** for high performance	2018. ?	Super scalar	6	Yes	Yes	12	15
							4 x **Cortex-A55** for energy efficiency	2017. 05		2	No	Yes	2	8

+2

+4

+2

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

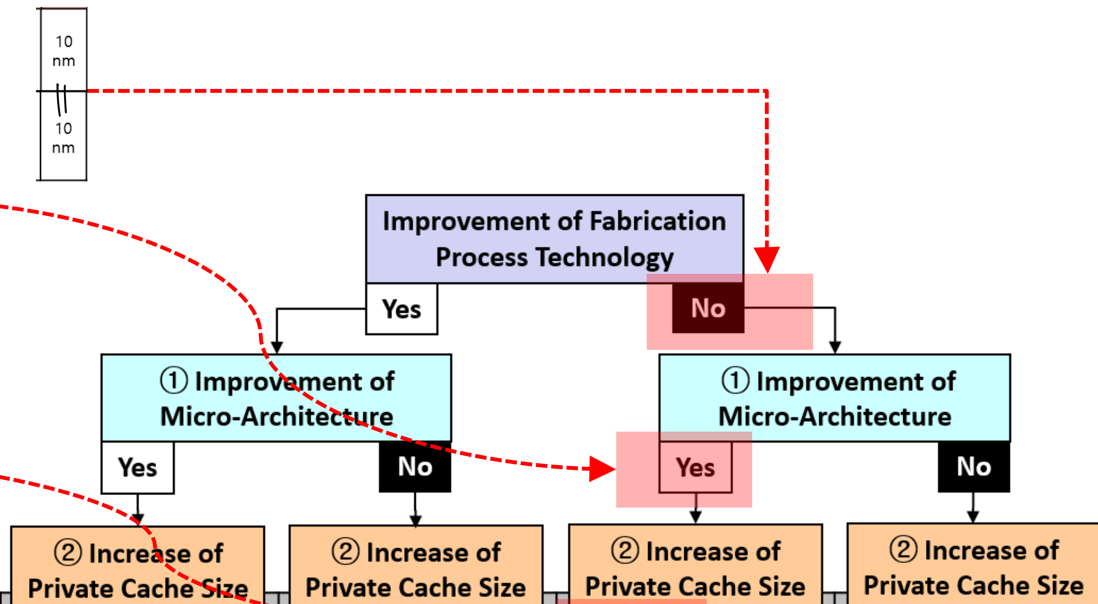
- **Commercial CPU evaluation :** Example#2-1 (smartphone-Galaxy)

Spec. of Superscalar processor				Pipeline depth
No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	
4	Yes	Yes	8	13
2	No	Yes	2	8
6	Yes	Yes	12	15

L1 Cache	L2 Cache
Per-core: I-64KB, D-32KB	2MB shared
Per-core: I-32KB, D-32KB	256KB shared
Per-core: I-64KB, D-64KB	Per-core: 512KB

Clock Freq.
2.3 GHz
1. 7 GHz
2.9 GHz

+0.6GHz

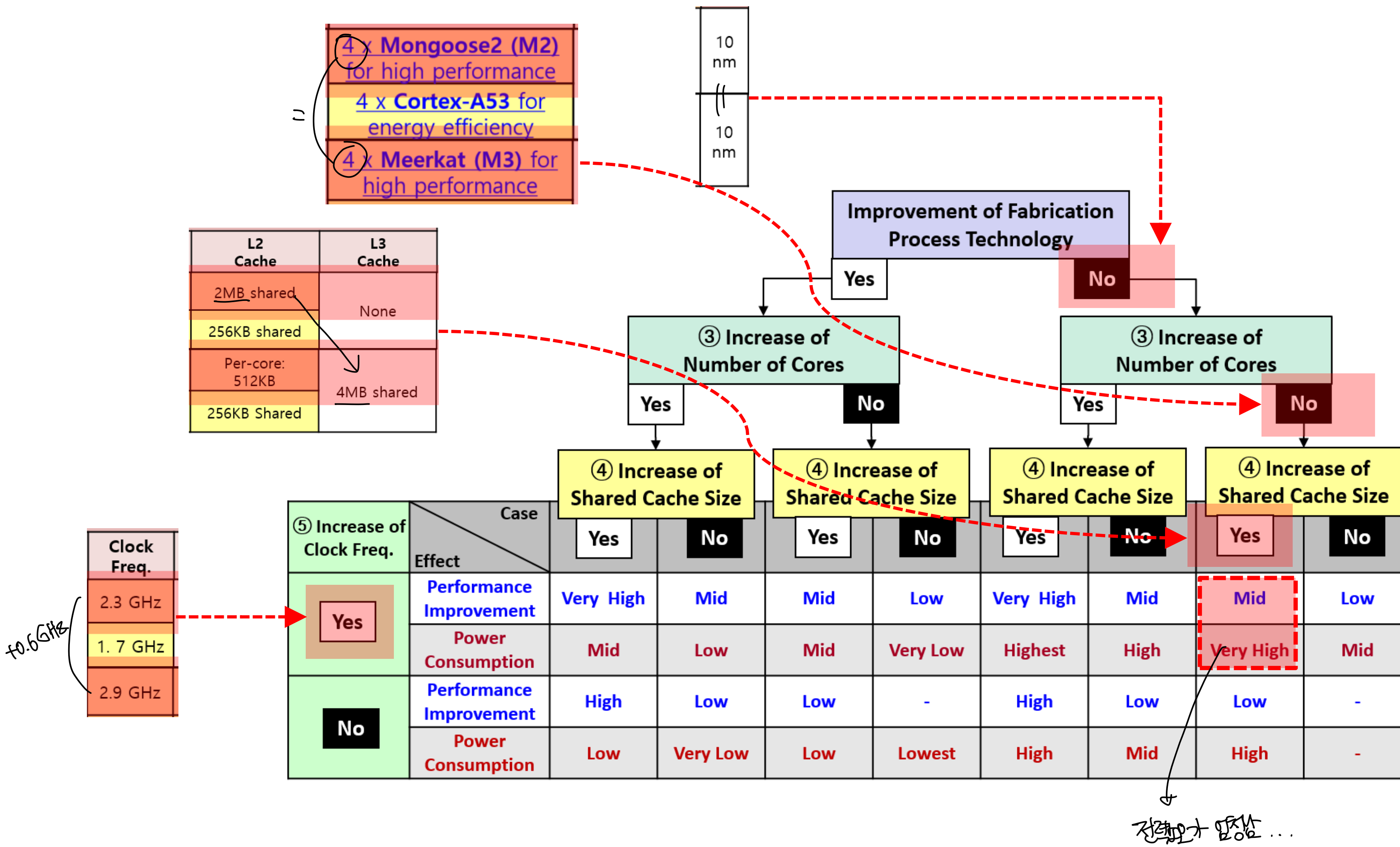


⑤ Increase of Clock Freq.	Effect \ Case	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

부담임 ▲ 전력소비가 엄청남. (CPU의 오험 ...)

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#2-1 (smartphone-Galaxy)



⑤ Increase of Clock Freq.	Effect \ Case	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#2-2 (smartphone-Galaxy)

Group#2

Type	Sub Type	Product Name	Release date (Year. Month)	Fab. Tech	Power	Name	Micro-architecture	Bit-Width	⑤ Clock Freq.	ISA	③ No. of Cores	② L1 Cache	② L2 Cache	④ L3 Cache
				SoC (System-on-Chip) = CPU + GPU + HW Accelerators			CPU							
Embedded Computer Systems	Smart Phone	Galaxy S9	2018. 03	10 nm	?	Exynos 9810	4 x **Meerkat (M3)** for high performance	64	2.9 GHz	ARM v8-A	8	Per-core: I-64KB, D-64KB	Per-core: 512KB	4MB shared
							4 x **Cortex-A55** for energy efficiency		1. 9 GHz	ARM v8.2-A		Per-core: I-32KB, D-32KB	256KB Shared	
		Galaxy Note10	2019. 08	7 nm	?	Exynos 9825	2 x **Cheetah (M4)** for high performance	64	2.73 GHz	ARM v8.2-A	8	Per-core: I-64KB, D-64KB	Per-core: 512KB	4MB shared
							2 x **Cortex-A75** for moderate performance		2.4 GHz			Per-core: I-64KB, D-64KB	Per-core: 256KB	
							4 x **Cortex-A55** for energy efficiency		1.95 GHz			Per-core: I-32KB, D-32KB	Per-core: 128KB	

1년

감소

power를 잡으려고
노력했것이
보임.

Group#2

Type	Sub Type	Product Name	Release date (Year. Month)	Fab. Tech	Power	Name	Micro-architecture Name	Intro' date (Year. Month)	Type	No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	Pipeline depth
				System-on-Chip			CPU — ① Micro-architecture			Spec. of Superscalar processor				
Embedded Computer Systems	Smart Phone	Galaxy S9	2018. 03	10 nm	?	Exynos 9810	4 x **Meerkat (M3)** for high performance	2018. ?	Super scalar	6	Yes	Yes	12	15
							4 x **Cortex-A55** for energy efficiency	2017. 05		2	No	Yes	2	8
		Galaxy Note10	2019. 08	7 nm	?	Exynos 9825	2 x **Cheetah (M4)** for high performance	2019. ?	Super scalar	6	Yes	Yes	12	15
							2 x **Cortex-A75** for moderate performance	2017. 05		3	Yes	Yes	8	11-13
							4 x **Cortex-A55** for energy efficiency	2017. 05		2	No	Yes	2	8

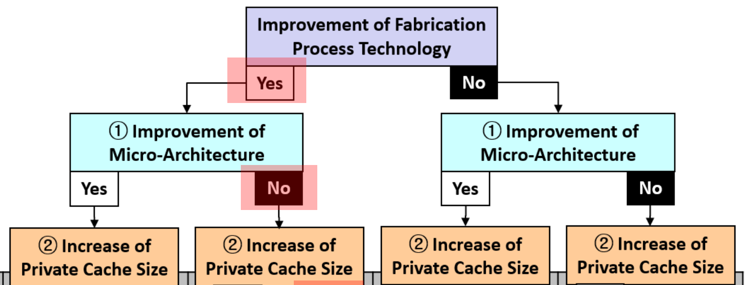
micro-architecture
동일

4개가 → 2개, → 2개 3 나눠짐

기존보다 저성능

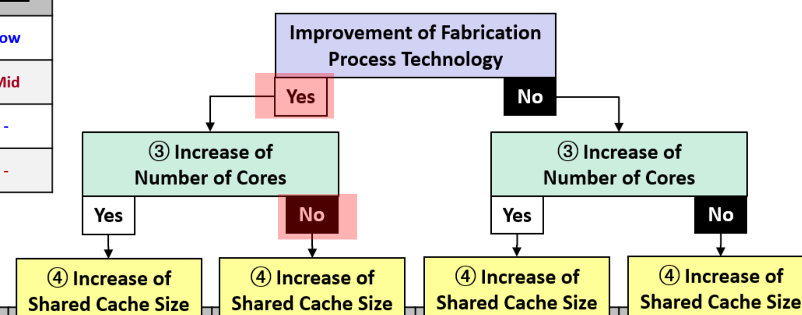
Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#2-2 (smartphone-Galaxy)



⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

성능향상X
power만 감소



⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#3-1 (smartphone-iPhone)

전력의 안정성은 가져가고 성능은 높여보자.

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators										
				Fab. Tech	Power	Name	CPU							
							Micro-architecture	Bit-Width	⑤ Clock Freq.	ISA	③ No. of Cores	② L1 Cache	④ L2 Cache	L3 Cache
Embedded Computer Systems	Smart Phone	iPhone 7	2016. 09	16 nm	?	Apple A10 Fusion	2 x **Hurricanes** for high performance	64	2.34 GHz	ARM v8.1-A	4	Per-core: I-64KB, D-64KB	3MB shared	4MB shared by the entire SoC
							2 x **Zephyr** for energy efficiency					Per-core: I-32KB, D-32KB	1MB shared	
		Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x **Mongoose2 (M2)** for high performance	64 늘어남	2.3 GHz	ARM v8-A	8	Per-core: I-64KB, D-32KB	2MB shared	None 동일함.
							4 x **Cortex-A53** for energy efficiency		1. 7 GHz			Per-core: I-32KB, D-32KB	256KB shared	
		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x **Monsoon** for high performance	64 줄어듦.	2.39 GHz	ARM v8.2-A	6	Per-core: I-64KB, D-64KB	8MB shared	None
							4 x **Mistral** for energy efficiency		1.42 GHz			Per-core: I-32KB, D-32KB	1MB shared	

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	System-on-Chip										
				Fab. Tech	Power	Name	CPU							
							① Micro-architecture							
							Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor				Pipeline depth
										No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	
Embedded Computer Systems	Smart phone	iPhone 7	2016. 09	16 nm	?	Apple A10 Fusion	2 x **Hurricanes** for high performance	2016. ?	Super scalar	6	Yes	Yes	9	16
							2 x **Zephyr** for energy efficiency	2016. ?		3	Yes	Yes	5	12
		Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x **Mongoose2 (M2)** for high performance	2017. 02	Super scalar	4	Yes	Yes	8	13
							4 x **Cortex-A53** for energy efficiency	2012. 10		2	No	Yes	2	8
		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x **Monsoon** for high performance	2017. ?	Super scalar	7	Yes	Yes	13	16
							4 x **Mistral** for energy efficiency	2017. ?		3	Yes	Yes	5	12

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#3-1 (smartphone-iPhone)

apple이 옳은 선택.
↳ SoC 엔지니어의 추측.

Improvement of Fabrication Process Technology: Yes / No

- Yes → ① Improvement of Micro-Architecture: Yes / No
  - Yes → ② Increase of Private Cache Size: Yes / No
  - No → ② Increase of Private Cache Size: Yes / No
- No → ① Improvement of Micro-Architecture: Yes / No
  - Yes → ② Increase of Private Cache Size: Yes / No
  - No → ② Increase of Private Cache Size: Yes / No

⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

성능향상 MID
power 소모는 적게

Improvement of Fabrication Process Technology: Yes / No

- Yes → ③ Increase of Number of Cores: Yes / No
  - Yes → ④ Increase of Shared Cache Size: Yes / No
  - No → ④ Increase of Shared Cache Size: Yes / No
- No → ③ Increase of Number of Cores: Yes / No
  - Yes → ④ Increase of Shared Cache Size: Yes / No
  - No → ④ Increase of Shared Cache Size: Yes / No

⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

성능향상 MID
전력소모 MID.

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#3-2 (smartphone-iPhone)

Group#1

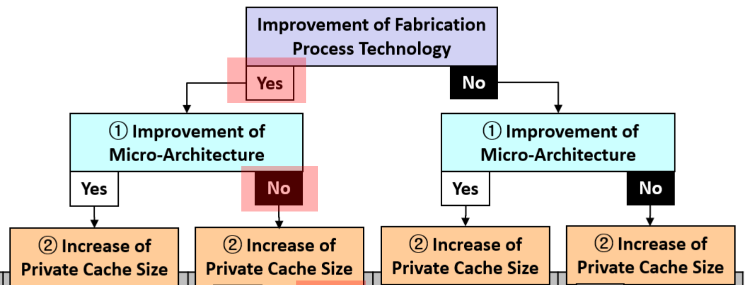
Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators										
				Fab. Tech	Power	Name	CPU							
							Micro-architecture	Bit-Width	⑤ Clock Freq.	ISA	③ No. of Cores	② L1 Cache	④ L2 Cache	L3 Cache
Embedded Computer Systems	Smart Phone	iPhone 7	2016. 09	16 nm	?	Apple A10 Fusion	2 x Hurricanes for high performance	64	2.34 GHz	ARM v8.1-A	4	Per-core: I-64KB, D-64KB	3MB shared	4MB shared by the entire SoC
							2 x Zephyr for energy efficiency					Per-core: I-32KB, D-32KB	1MB shared	
		Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x Mongoose2 (M2) for high performance	64	2.3 GHz	ARM v8-A	8	Per-core: I-64KB, D-32KB	2MB shared	None
							4 x Cortex-A53 for energy efficiency		1. 7 GHz			Per-core: I-32KB, D-32KB	256KB shared	
		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x Monsoon for high performance	64	2.39 GHz	ARM v8.2-A	6	Per-core: I-64KB, D-64KB	8MB shared	None
							4 x Mistral for energy efficiency		1.42 GHz			Per-core: I-32KB, D-32KB	1MB shared	

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	System-on-Chip										
				Fab. Tech	Power	Name	CPU							
							① Micro-architecture							
							Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor				Pipeline depth
										No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	
Embedded Computer Systems	Smart phone	iPhone 7	2016. 09	16 nm	?	Apple A10 Fusion	2 x Hurricanes for high performance	2016. ?	Super scalar	6	Yes	Yes	9	16
							2 x Zephyr for energy efficiency	2016. ?		3	Yes	Yes	5	12
		Galaxy S8	2017. 04	10 nm	?	Exynos 8895	4 x Mongoose2 (M2) for high performance	2017. 02	Super scalar	4	Yes	Yes	8	13
							4 x Cortex-A53 for energy efficiency	2012. 10		2	No	Yes	2	8
		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x Monsoon for high performance	2017. ?	Super scalar	7	Yes	Yes	13	16
							4 x Mistral for energy efficiency	2017. ?		3	Yes	Yes	5	12

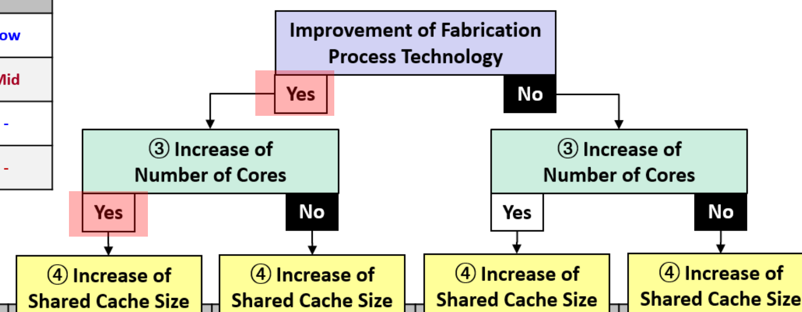
Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#3-2 (smartphone-iPhone)



⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

성능향상 X
power 낮게



⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

성능향상은 약간
power는 낮게

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#3-3 (smartphone-iPhone)

core개수 그대로에서 L2는 안늘림.

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators: Fab. Tech	Power	Name	CPU: Micro-architecture	Bit-Width	⑤ Clock Freq.	ISA	③ No. of Cores	② L1 Cache	④ L2 Cache	L3 Cache
Embedded Computer Systems		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x **Monsoon** for high performance	64	2.39 GHz	ARM v8.2-A	6	Per-core: I-64KB, D-64KB	8MB shared	None
							4 x **Mistral** for energy efficiency		1.42 GHz			Per-core: I-32KB, D-32KB	1MB shared	
		iPhone XS	2018. 09	7 nm	?	Apple A12	2 x **Vortex** for high performance	64	2.49 GHz	ARM v8.3-A	6	Per-core: I-128KB, D-128KB	8MB shared	None
							4 x **Tempest** for energy efficiency		1.52 GHz			Per-core: I-32KB, D-32KB	2MB shared	
		iPhone 11 Pro	2019. 09	7 nm	?	Apple A13	2 x **Lightning** for high performance	64	2.66 GHz	ARM v8.4-A	6	Per-core: I-128KB, D-128KB	8MB shared	None
							4 x **Thunder** for energy efficiency		1.82 GHz			Per-core: I-32KB, D-48KB	4MB shared	

동일.

동일

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	System-on-Chip: Fab. Tech	Power	Name	CPU — ① Micro-architecture: Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor: No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	Pipeline depth
Embedded Computer Systems		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x **Monsoon** for high performance	2017. ?	Super scalar	7	Yes	Yes	13	16
							4 x **Mistral** for energy efficiency	2017. ?		3	Yes	Yes	5	12
		iPhone XS	2018. 09	7 nm	?	Apple A12	2 x **Vortex** for high performance	2018. ?	Super scalar	7	Yes	Yes	13	16
							4 x **Tempest** for energy efficiency	2018. ?		3	Yes	Yes	5	12
		iPhone 11 Pro	2019. 09	7 nm	?	Apple A13	2 x **Lightning** for high performance	2019. ?	Super scalar	7	Yes	Yes	13	16
							4 x **Thunder** for energy efficiency	2019. ?		3	Yes	Yes	5	12

micro-architecture 동일

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#3-3 (smartphone-iPhone)

apple 안정 추구 ..

		Improvement of Fabrication Process Technology: Yes				Improvement of Fabrication Process Technology: No			
		① Improvement of Micro-Architecture: Yes		① Improvement of Micro-Architecture: No		① Improvement of Micro-Architecture: Yes		① Improvement of Micro-Architecture: No	
		② Increase of Private Cache Size		② Increase of Private Cache Size		② Increase of Private Cache Size		② Increase of Private Cache Size	
⑤ Increase of Clock Freq.	Effect \ Case	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

성능 Mid
power Mid

		Improvement of Fabrication Process Technology: Yes				Improvement of Fabrication Process Technology: No			
		③ Increase of Number of Cores: Yes		③ Increase of Number of Cores: No		③ Increase of Number of Cores: Yes		③ Increase of Number of Cores: No	
		④ Increase of Shared Cache Size		④ Increase of Shared Cache Size		④ Increase of Shared Cache Size		④ Increase of Shared Cache Size	
⑤ Increase of Clock Freq.	Effect \ Case	Yes	No	Yes	No	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

성능 Low
power Very Low

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#3-4 (smartphone-iPhone)

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators										
				Fab. Tech	Power	Name	CPU							
							Micro-architecture	Bit-Width	5 Clock Freq.	ISA	3 No. of Cores	2 L1 Cache	4 L2 Cache	L3 Cache
Embedded Computer Systems		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x **Monsoon** for high performance	64	2.39 GHz	ARM v8.2-A	6	Per-core: I-64KB, D-64KB	8MB shared	None
							4 x **Mistral** for energy efficiency		1.42 GHz			Per-core: I-32KB, D-32KB	1MB shared	
		iPhone XS	2018. 09	7 nm	?	Apple A12	2 x **Vortex** for high performance	64	2.49 GHz	ARM v8.3-A	6	Per-core: I-128KB, D-128KB	8MB shared	None
							4 x **Tempest** for energy efficiency		1.52 GHz			Per-core: I-32KB, D-32KB	2MB shared	
		iPhone 11 Pro	2019. 09	7 nm	?	Apple A13	2 x **Lightning** for high performance	64	2.66 GHz	ARM v8.4-A	6	Per-core: I-128KB, D-128KB	8MB shared	None
							4 x **Thunder** for energy efficiency		1.82 GHz			Per-core: I-32KB, D-48KB	4MB shared	

↳ S7에서 X로 늘었을때 4코 core 늘리고 이제서야 L2 캐시도 커짐

Group#1

Type	Sub Type	Product Name	Release date (Year. Month)	System-on-Chip											
				Fab. Tech	Power	Name	CPU								
							1 Micro-architecture								
							Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor					Pipeline depth
										No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports		
Embedded Computer Systems		iPhone X	2017. 11	10 nm	?	Apple A11 Bionic	2 x **Monsoon** for high performance	2017. ?	Super scalar	7	Yes	Yes	13	16	
							4 x **Mistral** for energy efficiency	2017. ?		3	Yes	Yes	5	12	
		iPhone XS	2018. 09	7 nm	?	Apple A12	2 x **Vortex** for high performance	2018. ?	Super scalar	7	Yes	Yes	13	16	
							4 x **Tempest** for energy efficiency	2018. ?		3	Yes	Yes	5	12	
		iPhone 11 Pro	2019. 09	7 nm	?	Apple A13	2 x **Lightning** for high performance	2019. ?	Super scalar	7	Yes	Yes	13	16	
							4 x **Thunder** for energy efficiency	2019. ?		3	Yes	Yes	5	12	

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#3-4 (smartphone-iPhone)

⑤ Increase of Clock Freq.	Case / Effect	Improvement of Fabrication Process Technology: Yes				No			
		① Improvement of Micro-Architecture: Yes		No		① Improvement of Micro-Architecture: Yes		No	
		② Increase of Private Cache Size: Yes	No	② Increase of Private Cache Size: Yes	No	② Increase of Private Cache Size: Yes	No	② Increase of Private Cache Size: Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

power는 mid로 유지
성능 mid

57 → X11
이제야 제대로 성능을 올려놓음.

⑤ Increase of Clock Freq.	Case / Effect	Improvement of Fabrication Process Technology: Yes				No			
		③ Increase of Number of Cores: Yes		No		③ Increase of Number of Cores: Yes		No	
		④ Increase of Shared Cache Size: Yes	No	④ Increase of Shared Cache Size: Yes	No	④ Increase of Shared Cache Size: Yes	No	④ Increase of Shared Cache Size: Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low	Very High	Mid	Mid	Low
	Power Consumption	Mid	Low	Mid	Very Low	Highest	High	Very High	Mid
No	Performance Improvement	High	Low	Low	-	High	Low	Low	-
	Power Consumption	Low	Very Low	Low	Lowest	High	Mid	High	-

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation** : Example#4 (desktop)

Group#2

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators										
				Fab. Tech	Power	Name	CPU							
							Micro-architecture	Bit-Width	⑤ Clock Freq.	ISA	③ No. of Cores	② L1 Cache	② L2 Cache	④ L3 Cache
General PC	Desktop	SAMSUNG DB400T6B	2015. 03	14 nm	65W	Intel® Core™ i7-6700	6th Gen. Skylake	64	3.4 ~ 4 GHz	x86 -64	4	Per-core: I-32KB, D-32KB	Per-core: 256KB	8MB shared by 4 cores and GPU
		Danawa 190721	2019. 07	14 nm	95W	Intel® Core™ i7-9700K	9th Gen. Coffee Lake	64	3.6 ~ 4.9 GHz	x86 -64	8	Per-core: I-32KB, D-32KB	Per-core: 256KB	12MB shared by 4 cores and GPU

↳ Intel 제품

Group#2

Type	Sub Type	Product Name	Release date (Year. Month)	System-on-Chip										
				Fab. Tech	Power	Name	CPU							
							① Micro-architecture							
							Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor				Pipeline depth
										No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	
General PC	Desktop	SAMSUNG DB400T6B	2015. 12	14 nm	65W	Intel® Core™ i7-6700	6th Gen. Skylake	2015. 08	Super scalar	5	Yes	Yes	8	14-19
		Danawa 190721	2019. 07	14 nm	95W	Intel® Core™ i7-9700K	9th Gen. Coffee Lake	2017. 10	Super scalar	5	Yes	Yes	8	14-19

↳ 4년차

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#4 (desktop)

		① Improvement of Micro-Architecture			
		Yes		No	
		② Increase of Private Cache Size		② Increase of Private Cache Size	
⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low
No	Performance Improvement	High	Low	Low	-

		③ Increase in the Number of Cores			
		Yes		No	
		④ Increase of Shared Cache Size		④ Increase of Shared Cache Size	
⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low
No	Performance Improvement	High	Low	Low	-

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#5 (workstation)

Group#2

Type	Sub Type	Product Name	Release date (Year. Month)	SoC (System-on-Chip) = CPU + GPU + HW Accelerators										
				Fab. Tech	Power	Name	CPU							
							Micro-architecture	Bit-Width	⑤ Clock Freq.	ISA	③ No. of Cores	② L1 Cache	② L2 Cache	④ L3 Cache
Server/ Workstation	High performance Workstation	Lenovo ThinkStation P500TW 850W	2015. 07	22 nm	140W	Intel® Xeon ® E5-1630 v3	Haswell	64	3.7 ~ 3.8 GHz	x86 -64	4	Per-core: I-32KB, D-32KB	Per-core: 256KB	10MB shared by 4 cores
		TYAN TAKO-KQT44	2020. 04	14 nm	150W	Intel® Xeon Gold 6226R	Cascade Lake	64	2.9 ~ 3.9 GHz	x86 -64	16	Per-core: I-32KB, D-32KB	Per-core: 1MB	22MB shared by 16 cores

하향

[illegible] Intel

Group#2

Type	Sub Type	Product Name	Release date (Year. Month)	System-on-Chip										
				Fab. Tech	Power	Name	CPU							
							① Micro-architecture							
							Name	Intro' date (Year. Month)	Type	Spec. of Superscalar processor				Pipeline depth
										No. of Issues (Decodes)	Out of order execution	Branch prediction (speculation)	No. of Execution ports	
Server/ Workstation	High performance Workstation	Lenovo ThinkStation P500TW 850W	2015. 07	22 nm	140W	Intel® Xeon ® E5-1630 v3	Haswell	2013. 06	Super scalar	4	Yes	Yes	8	14-19
		TYAN TAKO-KQT44	2020. 04	14 nm	150W	Intel® Xeon Gold 6226R	Cascade Lake	2019. ?	Super scalar	5	Yes	Yes	8	14-19

Performance-Power Consumption Metrics for Evaluating Commercial CPUs

- **Commercial CPU evaluation :** Example#5 (workstation)

		① Improvement of Micro-Architecture: Yes		① Improvement of Micro-Architecture: No	
		② Increase of Private Cache Size		② Increase of Private Cache Size	
⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low
No	Performance Improvement	High	Low	Low	-

		③ Increase in the Number of Cores: Yes		③ Increase in the Number of Cores: No	
		④ Increase of Shared Cache Size		④ Increase of Shared Cache Size	
⑤ Increase of Clock Freq.	Case / Effect	Yes	No	Yes	No
Yes	Performance Improvement	Very High	Mid	Mid	Low
No	Performance Improvement	High	Low	Low	-