```
#Address    # RISC-V Assembly
0x70        beq  s0, t5, L1      ⟩1
0x74        add  s1, s2, s3      ⟩2
0x78        sub  s5, s6, s7      ⟩3
0x7C        lw   t0, 0(s1)       ⟩4
0x80   L1:  addi s1, s1, -15
```

`L1` is 4 instructions (i.e., **16 bytes**) past `beq`

$imm_{12:0}$ = 16	0		0	0	0	0		0	0	0	1		0	0	0	0
bit number	12		11	10	9	8		7	6	5	4		3	2	1	0

Assembly

Field Values

	$imm_{12,10:5}$	rs2	rs1	funct3	$imm_{4:1,11}$	op
beq s0, t5, L1 beq x8, x30, 16	**0**000 000	30	8	0	**1000** 0	99
	7 bits	5 bits	5 bits	3 bits	5 bits	7 bits

Machine Code

$imm_{12,10:5}$	rs2	rs1	funct3	$imm_{4:1,11}$	o
0000 000	11110	01000	000	**1000** 0	110
7 bits	5 bits	5 bits	3 bits	5 bits	7 b

0

O

$m_{4:1,11}$ op

000 0 110 0011 **(0x01E40863)**

bits   7 bits