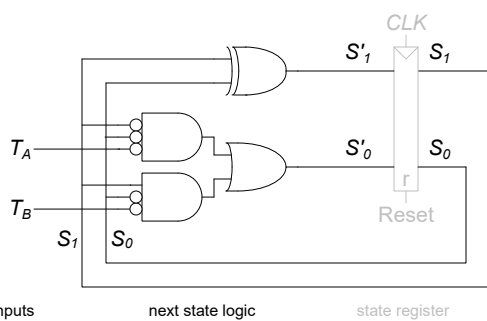


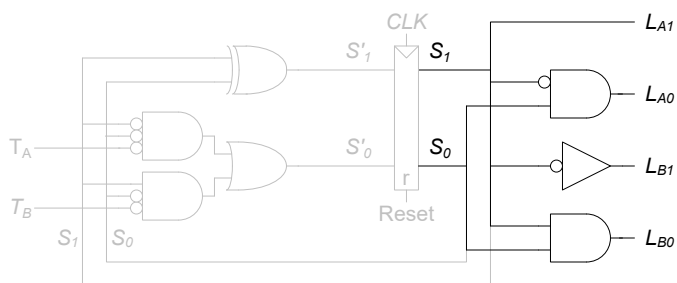
(a)



(b) inputs

next state logic

state register



(c) inputs

next state logic

state register

output logic

outputs