PROBE ’21 CPU DESIGN WORKSHOP

SOFTWARE PRE - REQUISITES

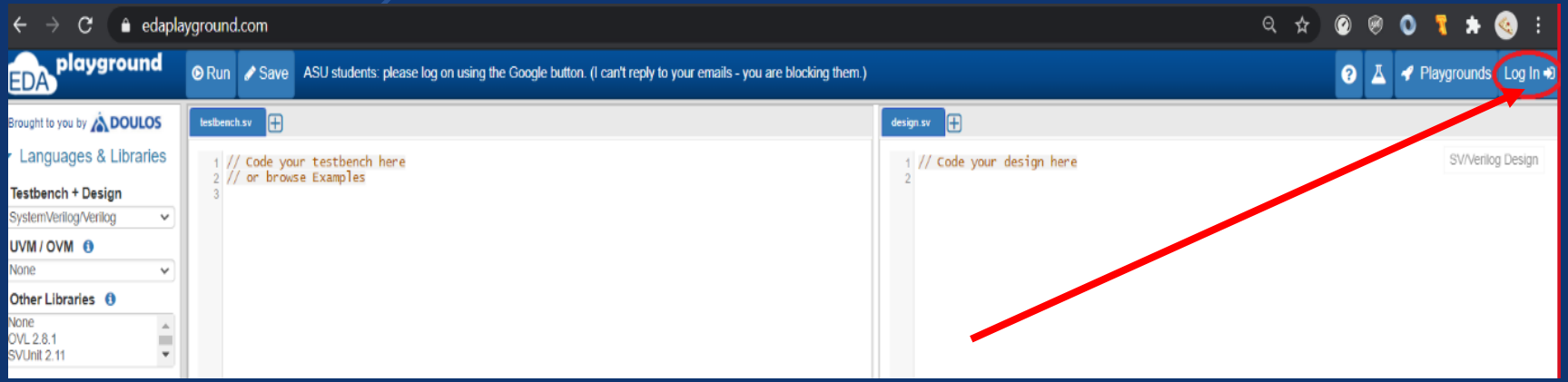
VERILOG COMPILER

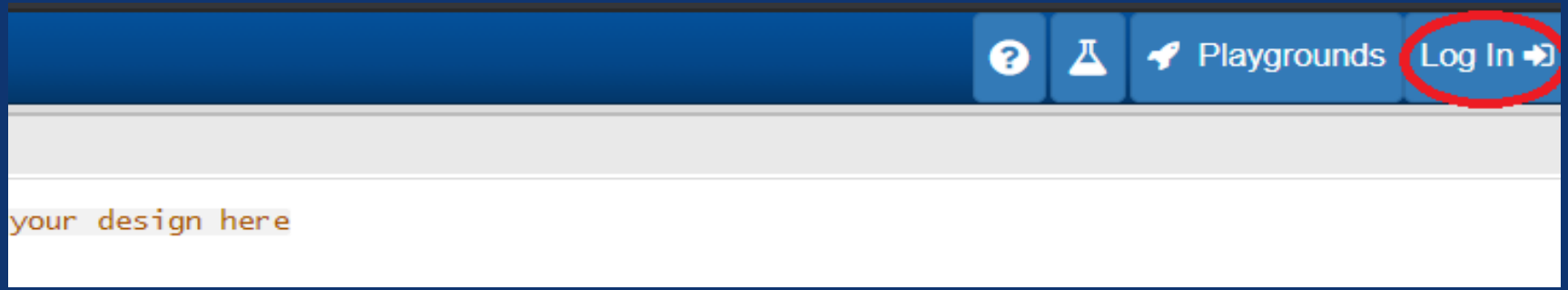
Step 1:

Go to https://www.edaplayground.com/home

Step 2:

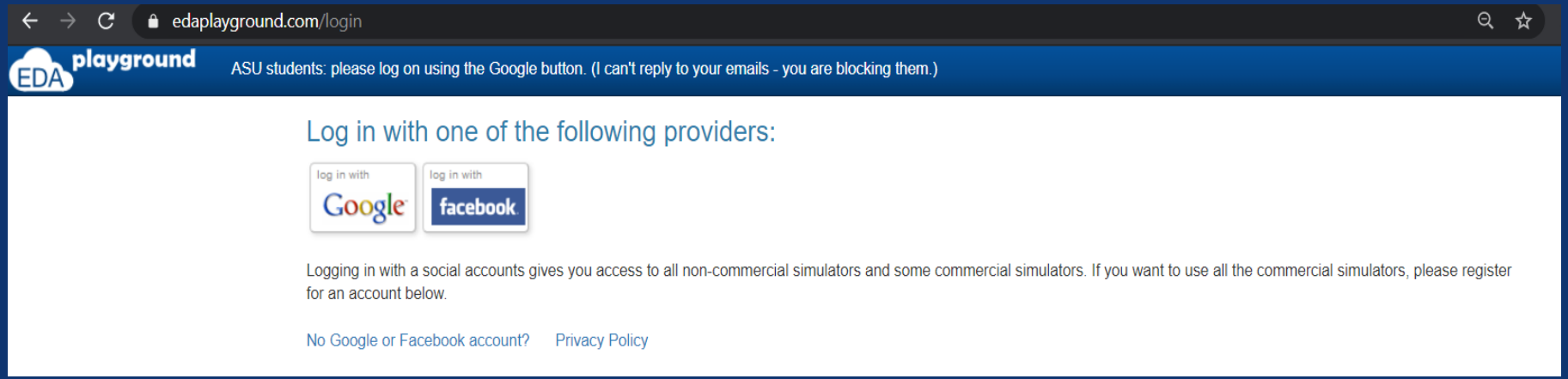
Click on the “**Login In**” button on the **top right corner** of the webpage.


edaplayground.com
playground
Run
Save
ASU students: please log on using the Google button. (I can't reply to your emails - you are blocking them.)
Playgrounds
Log In
Brought to you by DOULOS
Languages & Libraries
Testbench + Design
SystemVerilog/Verilog
UVM / OVM
None
Other Libraries
None
OVL 2.8.1
SVUnit 2.11
testbench.sv
// Code your testbench here
// or browse Examples
design.sv
// Code your design here
SV/Verilog Design


Playgrounds
Log In
your design here

Step 3:

Login in using your Google or Facebook account. (Full access registration not required).



To check the compiler

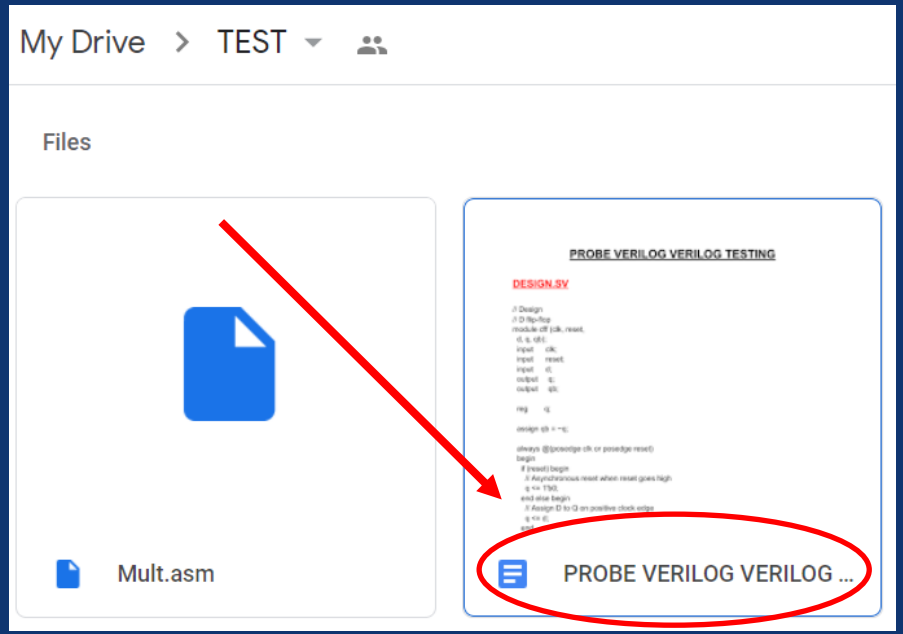
Step 1:

Go to https://drive.google.com/drive/folders/1yX0jJ3u-FbOTalZTzhT0BulFFCKKlGsk

Step 2:

Click the probe Verilog test file. And copy the text under DESIGN SV and paste it in EDA playground design.sv

Copy the text below TESTBENCH.SV and paste in it testbench.sv



DESIGN.SV

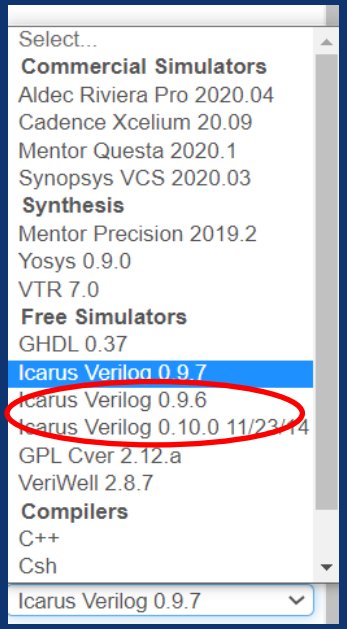
```
// Design
// D flip-flop
module dff (clk, reset,
  d, q, qb);
  input      clk;
  input      reset;
  input      d;
  output     q;
  output     qb;

  reg        q;

  assign qb = ~q;

  always @(posedge clk or posedge reset)
  begin
    if (reset) begin
      // Asynchronous reset when reset goes high
      q <= 1'b0;
    end else begin
      // Assign D to Q on positive clock edge
      q <= d;
    end
  end
endmodule
```

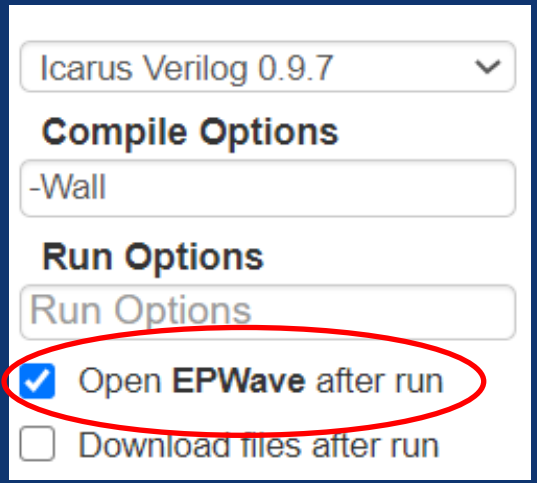
TESTBENCH.SV

```
module test;

  reg clk;
  reg reset;
  reg d;
  wire q;
  wire qb;

  // Instantiate design under test
  dff DFF(.clk(clk), .reset(reset),
          .d(d), .q(q), .qb(qb));

  initial begin
    // Dump waves
    $dumpfile("dump.vcd");
    $dumpvars(1);

    $display("Reset flop.");
    clk = 0;
    reset = 1;
    d = 1'bx;
    display;

    $display("Release reset.");
    d = 1;
    reset = 0;
    display;
```

Step 3:

Select the simulator Icarus Verilog 0.9.7 from the drop down and check out the “Open EPWave after run” box.



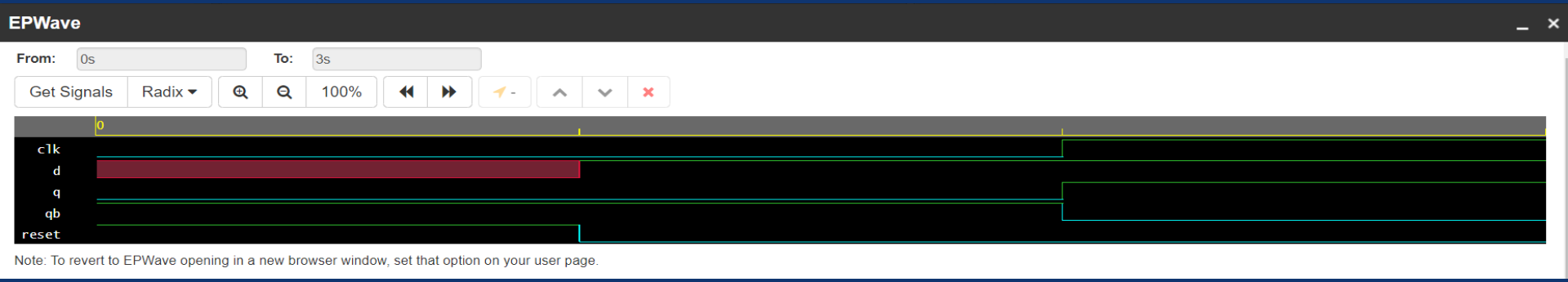


Step 4:

Check the output and waveform generated.

Log | Share

```
[2021-02-26 08:18:16 EST] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
Reset flop.
d:x, q:0, qb:1
Release reset.
d:1, q:0, qb:1
Toggle clk.
d:1, q:1, qb:0
Finding VCD file...
./dump.vcd
[2021-02-26 08:18:16 EST] Opening EPWave...
Done
```



ASSEMBLER AND EMULATOR

Step 1:

Go to the website https://java.com/en/download/

Step 2:

Click the Agree and Start Free Download button to download the installation file. Install the downloaded folder.

64-bit Java for Windows

Recommended Version 8 Update 281 (filesize: 79.68 MB)

Release date January 19, 2021

Important Oracle Java License Update

The Oracle Java License has changed for releases starting April 16, 2019.

The new Oracle Technology Network License Agreement for Oracle Java SE is substantially different from prior Oracle Java licenses. The new license permits certain uses, such as personal use and development use, at no cost -- but other uses authorized under prior Oracle Java licenses may no longer be available. Please review the terms carefully before downloading and using this product. An FAQ is available here.

Commercial license and support is available with a low cost Java SE Subscription.

Oracle also provides the latest OpenJDK release under the open source GPL License at jdk.java.net.

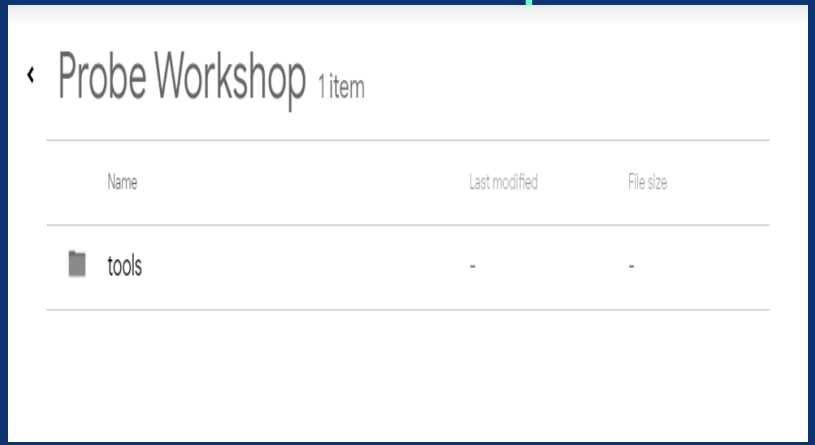
We have detected you are using Google Chrome and might be unable to use the Java plugin from this browser. Starting with Version 42 (released April 2015), Chrome has disabled the standard way in which browsers support plugins. More info

Agree and Start Free Download

Step 3:

https://drive.google.com/file/d/1tLjrK5b-oUZZI8myto9r4IEvBatEgmLR/view?usp=sharing

Download the zip folder and extract all the folders.



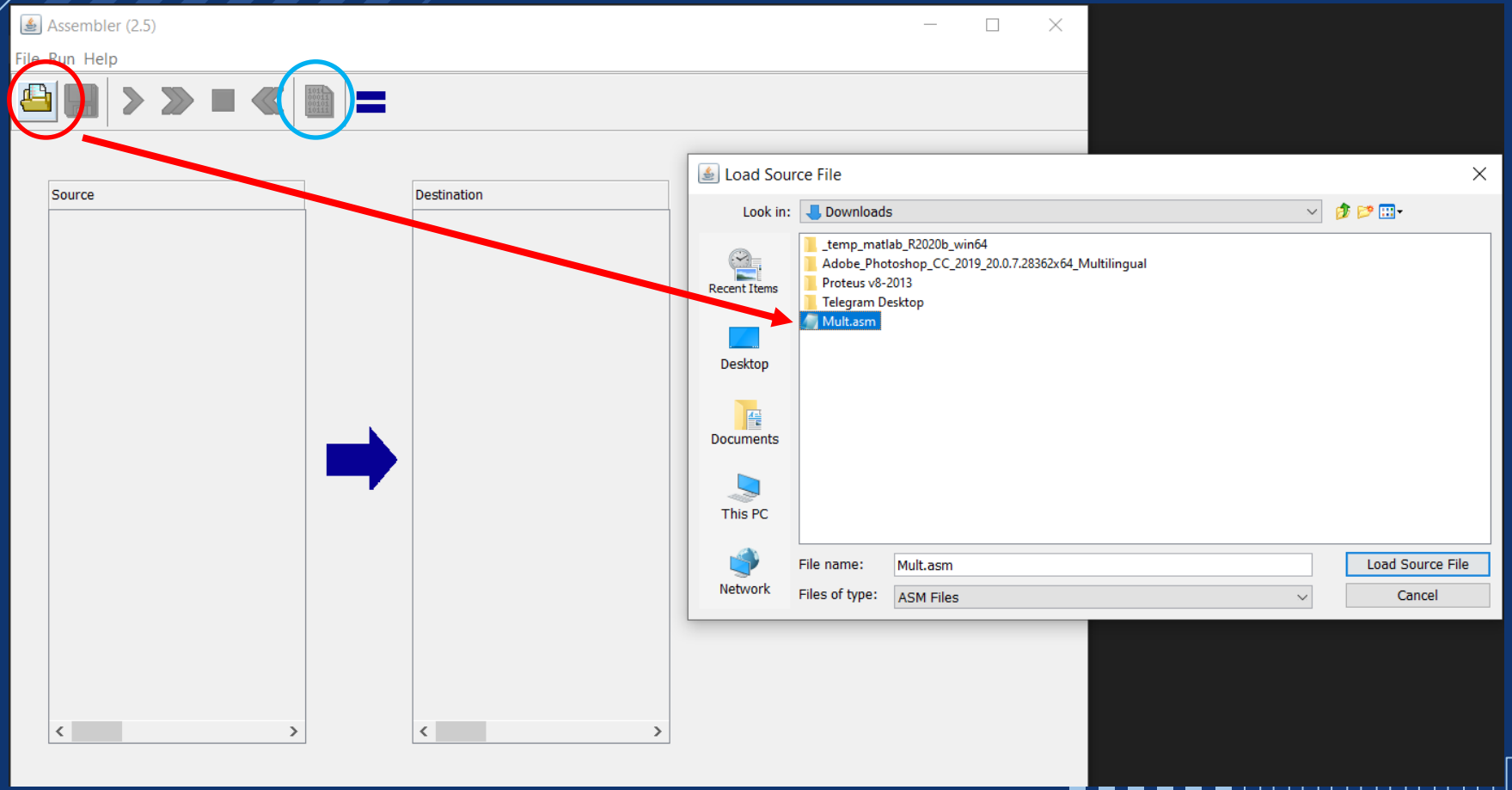
To check the Assembler

Step 1:

Navigate to Probe Workshop folder → to tools → Assembler.bat (A screen as shown in next page must pop).

Step 2:

Go to https://drive.google.com/drive/folders/1yX0jJ3u-FbOTalZTzhT0BulFFCKKlGsk and download Mult.asm.

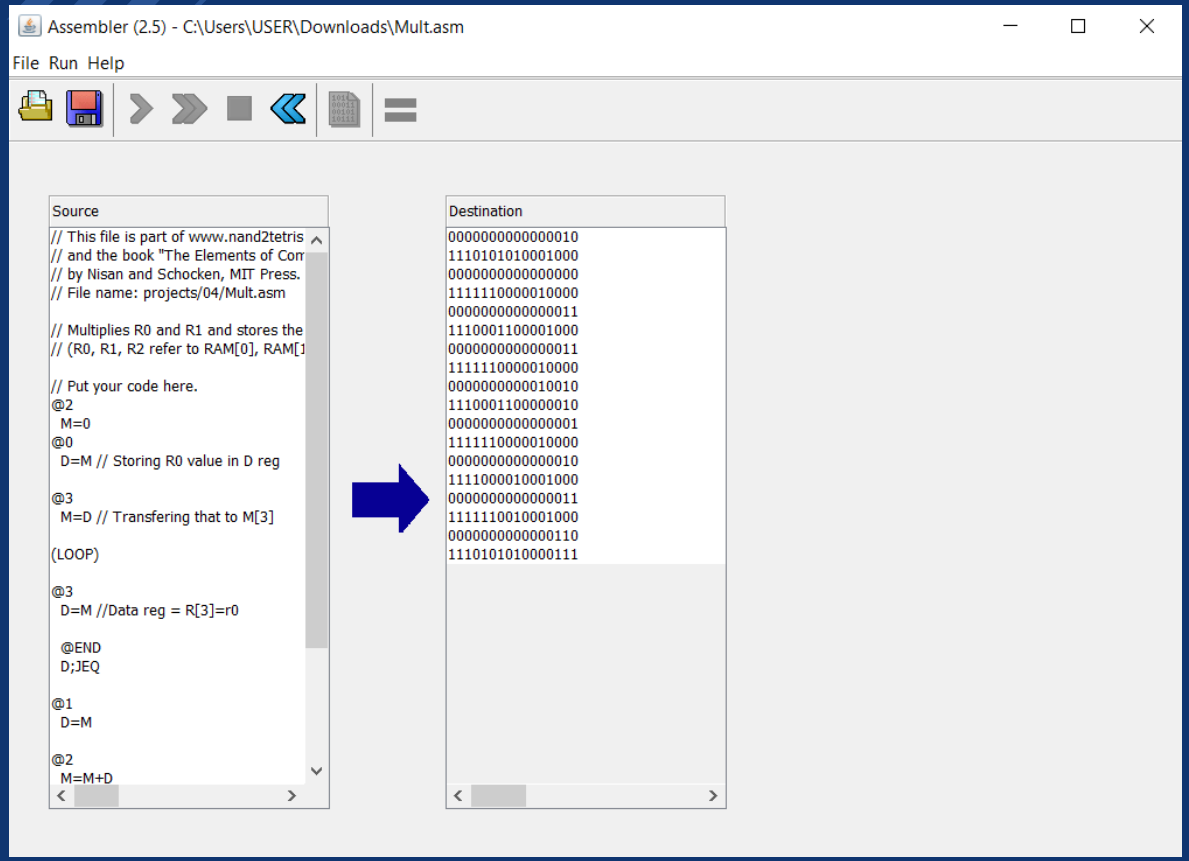

Assembler (2.5)
File Run Help
Source
Destination
Load Source File
Look in:
Downloads
_temp_matlab_R2020b_win64
Adobe_Photoshop_CC_2019_20.0.7.28362x64_Multilingual
Proteus v8-2013
Telegram Desktop
Mult.asm
Recent Items
Desktop
Documents
This PC
Network
File name:
Mult.asm
Files of type:
ASM Files
Load Source File
Cancel

Step 3:

Load the Mult.asm file by clicking top left corner button then select the file destination and click load source file. Then click the button indicated with Blue circle.

If done properly you shall get a output as shown in the next slide.

!! (Note: Don’t change any other files in tools file) !!


Assembler (2.5) - C:\Users\USER\Downloads\Mult.asm
File Run Help
Source
// This file is part of www.nand2tetris
// and the book "The Elements of Com
// by Nisan and Schocken, MIT Press.
// File name: projects/04/Mult.asm
// Multiplies R0 and R1 and stores the
// (R0, R1, R2 refer to RAM[0], RAM[1
// Put your code here.
@2
M=0
@0
D=M // Storing R0 value in D reg
@3
M=D // Transfering that to M[3]
(LOOP)
@3
D=M //Data reg = R[3]=r0
@END
D;JEQ
@1
D=M
@2
M=M+D
Destination
0000000000000010
1110101010001000
0000000000000000
1111110000010000
0000000000000011
1110001100001000
0000000000000011
1111110000010000
0000000000010010
1110001100000010
0000000000000001
1111110000010000
0000000000000010
1111000010001000
0000000000000011
1111110010001000
0000000000000110
1110101010000111

REGARDS,

PROBE WORKSHOP TEAM