SCHOOL OF COMPUTING
SRM UNIVERISTY
CYCLE TEST – 3

Subject Code &Title: 15CS202 – Digital System Design **Date: 21/10/2016**
Time: 2 hours 15 mins **Max Marks: 80**

Part – B (5 X 4 = 20 Marks)
Answer ANY FIVE Questions

21) (a)Find the hex sum of $(93)_{16}$ + $(DE)_{16}$.
(b)Perform the following operations using the 2's complement method: -48-23
22) Add 648 and 487 in BCD code.
23) Evaluate x = A'.B+C (A.D)' using the convention A = True and B = False.
24) The Karnaugh map for a SOP function is given below in Fig.1. Determine the simplified SOP Boolean expression.

AB/CD	00(C'D')	01	11	10
00(A'B')	1	1		1
01		1		
11				
10	1	1		1

Fig.1

25) Draw the circuit diagram for a full adder using half adder
26) With the help of a suitable diagram, explain how do you convert a JK flipflop to T type flipflop.
27) Write the HDL gate –level description of a 2-to-4- line decoder

Part – C (5 X 12 = 60 Marks)
Answer ALL the Questions

28) (a) Solve the following equations for X (6)
(i) $23.6_{10} = X_2$ (ii) $65.535_{10} = X_{16}$
(ii) Convert the decimal number 430 to Excess-3 code (3)
(iii) Convert the binary number 10110 to Gray code (3)

(OR)

28) (b) (i) Construct a logic circuit using NAND gates only for the expression x = A . (B + C). (6)
Perform following subtraction and verify
(ii) 11001-10110 using 1's complement (3)
(iii) 11011-11001 using 2's complement (3)

29) (a) (i)A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations
A is False, B is True
A is False, C is True
A, B, C are False
A, B, C are True

(a) Write the Truth table for F. Use the convention True=1 and False = 0.
(b) Write the simplified expression for F in SOP form.
(c) Write the simplified expression for F in POS form.
(d) Draw logic circuit using minimum number of 2-input NAND gates. (8)

(ii) For F = A.B.C+ B.C.D'+ A'.B.C, write the truth table and simplify using Karnaugh map . (4)

(OR)

29) (b) Use Tabulation method to simplify the given Boolean function, F(A,B,C,D) = $\sum$m (1,3,5,8,9,11,15) + d(2,13) (12)

30) (a) Design a 8 to 1 multiplexer by using the four variable function given by F(A,B,C,D) = $\sum$m(0,1,3,4,8,9,15) (12)

(OR)

30) (b) Write and explain the expression for the carry-output of a 4-bit carry lookahead adder with suitable diagram (12)

31) (a)Design a 4-bit shift counter that will count the sequence in the following order 0,8,12,14,15,7,3,1,0, (12)

(OR)

31) (b) Using D-Flip flops construct and explain the working of a 4-bit SISO shift register. (12)

32) (a) Write the behavioral VHDL code for a 32-bit adder (12)

(OR)

32) (b) Explain HDL models of combinational circuit in detail with example for each modelling. (12)