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1 module ControlUnit (
2     input trig,
3     input [3:0]value,
4     input clk,
5     input clear_e,
6     input clr,
7     output reg reset,
8     output reg loadA,
9     output reg loadB,
10    output reg AddSub,
11    output reg loadR,
12    output reg iuau
13);
14
15    reg[2:0]state, nextstate;
16    always@(posedge trig, negedge clr) begin
17        if(clr == 0)state <= 0;
18        else state <=nextstate;
19
20        case(state)
21        0: if(~trig) nextstate <= 1'b1; else nextstate <= 0;
22        1: if(~trig && (value[3:0] == 4'b1010 || value[3:0] == 4'b1011))
23            nextstate <= 2;
24            else nextstate <= 1;
25        2: if (~trig) nextstate <= 3;
26            else nextstate <= 2;
27        3: if (~trig && (value[3:0] == 4'b1111))
28            nextstate <= 4;
29            else nextstate <= 3;
30        4: if (~trig) nextstate <= 4; else nextstate <= 4;
31        default: nextstate <= 0;
32    endcase
33
34    if (clr == 0)
35        AddSub <= 0;
36    else if (state == 1 && value == 4'b1011)
37        AddSub <= 1;
38    else
39        AddSub <= AddSub;
40
41    end
42
43    always @(*) //combinational logic
44    case (state)
45    0: begin reset = 0; loadA = 1; loadB = 1; loadR =1; iuau = 0; end
46    1: begin reset = 1; loadA = 0; loadB = 1; loadR =1; iuau = 0; end
47
48    2: begin reset = 1; loadA = 1; loadB = 1; loadR =1; iuau = 0; end
49    3: begin reset = 1; loadA = 1; loadB = 0; loadR =1; iuau = 0; end
50    4: begin reset = 1; loadA = 1; loadB = 1; loadR =0; iuau = 1; end
51    default: begin reset = 0; loadA = 1; loadB = 1; loadR =1; iuau = 1;end
52    endcase
53 endmodule

```

```

ControlUnit ControlUnit_inst
(
    .trig(trig_sig) ,      // input  trig_sig
    .value(value_sig) ,    // input [3:0] value_sig
    .clk(clk_sig) , // input  clk_sig
    .clear_e(clear_e_sig) , // input  clear_e_sig
    .clr(clr_sig) , // input  clr_sig
    .reset(reset_sig) ,    // output  reset_sig
    .loadA(loadA_sig) ,    // output  loadA_sig
    .loadB(loadB_sig) ,    // output  loadB_sig
    .AddSub(AddSub_sig) ,  // output  AddSub_sig
    .loadR(loadR_sig) ,    // output  loadR_sig
    .iuau(iuau_sig)       // output  iuau_sig
);

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<<new>>		Filter on node names: *	Category: All					
tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✓	in clear_e	Location	PIN_A7	Yes			
2	✓	in clk	Location	PIN_P11	Yes			
3	✓	in clr	Location	PIN_B8	Yes			
4	✓	out iuau	Location	PIN_C13	Yes			
5	✓	out loadA	Location	PIN_A9	Yes			
6	✓	out loadB	Location	PIN_A10	Yes			
7	✓	out loadR	Location	PIN_D13	Yes			
8	✓	out reset	Location	PIN_A8	Yes			
9	✓	in trig	Location	PIN_AB5	Yes			
10	✓	in value[0]	Location	PIN_C10	Yes			
11	✓	in value[1]	Location	PIN_C11	Yes			
12	✓	in value[2]	Location	PIN_D12	Yes			
13	✓	in value[3]	Location	PIN_C12	Yes			
14	✓	out AddSub	Location	PIN_B10	Yes			
15		<<new>>	<<new>>					