

# Digital Electronics

## — Question solved —

\* Math  
\* Physics  
\* Science

Wish Book

CT-2

- \* Flip-flop
- \* Switching Device (TTL, DTL)
- \* Adder ADC, DAC

1

2020

51

between 0 and 9 will vanish to appear to 10

1.

Q. What are the advantages of BCD as compared to straight binary? What is its disadvantage?

\* The main advantage of binary coded decimal is that it allows easy conversion between decimal (base-10) and binary (base-2) form.

\* disadvantage:

- ① The addition and subtraction of BCD have different rules.
- ② The BCD arithmetic is little more complicated.
- ③ BCD needs more number of bits than binary to represent the decimal number. So, BCD is less efficient than binary.

(d) Perform the subtractions  $(01001_2 - 11010)_2$  and  $(10010_2 - 10011)_2$  using 2's complement system.

Step 1:  $(01001_2 - 11010)_2$

~~1001010010~~ 1's complement

~~01101~~

~~+1~~ 2's complement

~~01110~~

~~00011010~~ 1's complement

~~11100101~~ 1's complement

~~+1~~

~~11100110~~ 2's complement

Step 1:  $00010011$  1's complement

~~11101100~~ 2's complement

Step 2:  $00010010$  1's complement

~~11111111~~ 2's complement

Ans is: ~~1111~~

~~01001\_2 - 11010\_2~~

~~00011010~~ 1's complement

~~11100101~~ 1's complement

~~+1~~

~~11100110~~ 2's complement

~~-14~~

~~0111~~

~~0111~~

~~0111~~

~~00011010~~

(Ans:)

~~256 - 19~~

~~247~~

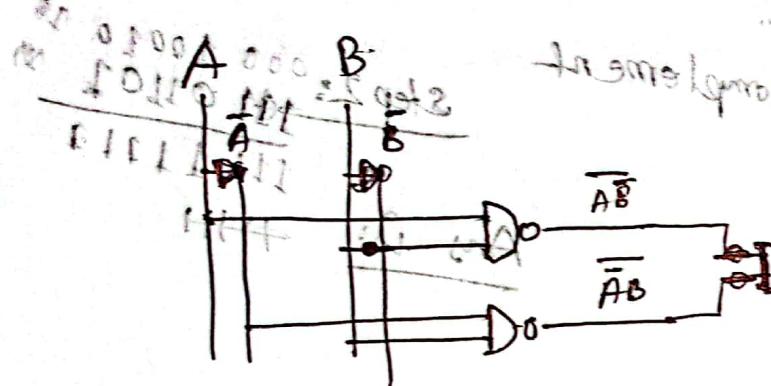
$-2 - (2^8 - 1) =$

b<sub>100</sub> s(000110) ~~2~~ ~~3~~ ~~4~~ ~~5~~ ~~6~~ ~~7~~ ~~8~~ ~~9~~ ~~10~~

② Draw the logic diagram and truth table of OR.

NOR and XOR gate using NAND gate only.

③ The logic diagram of EX-OR gate using NAND gate.

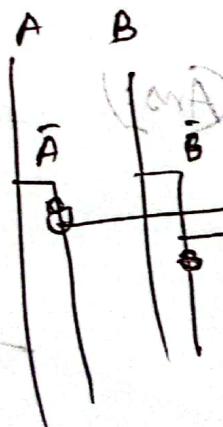


$$\begin{aligned} & A\bar{B} + \bar{A}B \\ & = \overline{\overline{A}\bar{B} + \bar{A}B} \\ & = \overline{\overline{A}\bar{B}} \cdot \overline{\overline{\bar{A}B}} \end{aligned}$$

NOR gate using NAND Gate:

$$\begin{aligned} \text{NOR gate: } & A + B \xrightarrow{\text{NOR}} \overline{A \cdot B} \\ & \overline{A \cdot B} \xrightarrow{\text{NAND}} \overline{\overline{A} \cdot \overline{B}} \end{aligned}$$

$$\begin{aligned} \text{NAND gate: } & \overline{A \cdot B} \xrightarrow{\text{NAND}} \overline{\overline{A} \cdot \overline{B}} \\ & = \overline{\overline{A} \cdot \overline{B}} \\ & = \overline{\overline{A} \cdot \overline{B}} \end{aligned}$$



$$\begin{aligned} & \overline{A} \cdot \overline{B} \\ & \overline{A} + \overline{B} \\ & \overline{\overline{A} \cdot \overline{B}} \end{aligned}$$

Truth Table		
A	B	
0	0	$\overline{A + B}$
0	1	0
1	0	1
1	1	0

$$\begin{aligned} & \overline{A} \cdot \overline{B} \\ & \overline{A} + \overline{B} \\ & \overline{\overline{A} \cdot \overline{B}} \end{aligned}$$

A	B	$\overline{A}$	$\overline{B}$	X
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

OR gate using NAND gate:

$$\overline{R \text{ gate using } \text{ storms not possible}} \quad \overline{A} \quad \overline{B} \quad \text{suppose} \quad \overline{A} \cdot \overline{B} = \overline{B}^{A+B}$$

$$\overline{A+B} = \overline{A} \cdot \overline{B} \quad \text{is (01101) true?} \quad \text{false} \quad \text{suppose} \quad \text{true}$$

A	B	$\bar{A}$	$\bar{B}$	X
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

$$g_{\text{one}}(10111) = \underline{s}(01101)$$

⑥ Simplify the following Boolean expressions:

using  $x = AB \cos \theta A' B' C + A C \cos \theta A' C' B$  and  $\sin \theta = BC (\sin A) + AC (\sin C)$  we get  $x = BC \sin A + AC \sin C$

$$\begin{aligned}
 & \text{⑪. } A'B(D'+CD) + AB + A'BCD \\
 & = A'BD' + \underline{A'BCD} + AB + \underline{A'BCD} \\
 & = A'BD' + \underline{A'BCD} + AB \\
 & = A'B(D'+CD) + AB \\
 & = A'B(D'+C) + AB \\
 & = A'BD' + \underline{A'BC} + AB \\
 & = A'BD' + B(A'C + A) \\
 & = A'BD' + B(A + C) \\
 & = A'BD' + AB + BC \\
 & = B(A'D + A) + AC \\
 & = B(A + D) + AC \\
 & = AB + BD + AC
 \end{aligned}$$

$$\begin{aligned}
 & \text{B.C.} \quad f(MB+BD) \\
 & \text{If } 1+0 = 0+0 \neq 0 \\
 & \text{= (10)} \quad \neq 0 \\
 & \text{= odd } 0+0 = 0
 \end{aligned}$$

$$\begin{aligned}
 & \textcircled{4} \quad A' B' (B' + CD + CD) + AB \\
 &= A' B' (B' + CD) + AB \\
 &= A' B' B' + A' B' CD + AB \\
 &= \cancel{B' (A' CD + A)} \\
 &= \cancel{B' (A + A)} + \cancel{(A + CD)} \\
 &= \cancel{B' (A + CD)} \\
 &= \cancel{AB + CD}
 \end{aligned}$$

stop bit, parity bit, stop bit

c) Which coding technique is good for error detection? Give example?  $\rightarrow$  Convert  $(10110)_2 = (2)_\text{gray}$

$$(10110)_2 = (11101)_\text{gray}$$

\* Hamming Code. Hamming Code is useful for both detection and correction of error present in the received data. This code uses multiple parity bits and we have to place these parity bits in the positions of power of 2.

3(a) Minimize the following function:

$$f(a, b, c, d) = \sum m(1, 3, 4, 7, 11) + \sum d(5, 12, 13, 14, 15)$$

Input:

$$\begin{matrix} 1, 0001 \\ 4, 0100 \end{matrix}$$

$$\begin{matrix} 3, 0011 \\ 5, 0101 \\ 12, 1100 \end{matrix}$$

$$\begin{matrix} 7, 0111 \\ 11, 1011 \end{matrix}$$

$$\begin{matrix} 13, 1101 \\ 14, 1110 \end{matrix}$$

$$15, 1111$$

Prime implicants:

$$(7, 5, 3, 1) 0-1$$

$$(3, 12, 5, 4) 1-10-$$

$$(15, 11, 7, 3) -11$$

$$(15, 13, 7, 5) -1-1$$

$$(15, 19, 13, 12) 11-$$

First Comparison:

$$1. (3, 1) 00-1$$

$$(5, 1) 0-01$$

$$\begin{matrix} (5, 4) 010- \\ (12, 4) -100 \end{matrix}$$

$$2. (7, 3) 0-11$$

$$(11, 3) -011$$

$$(7, 5) 011$$

$$(13, 5) -1011$$

$$(13, 12) 110-$$

$$(19, 12) 11-0$$

$$3. (15, 7) -111$$

$$(15, 11) 1-11$$

$$(15, 13) 11-1$$

$$(15, 19) -111-$$

Table:

	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	0	1
2	0	1	0	1	0	1	0	1
3	0	1	0	1	0	1	0	1
4	0	1	0	1	0	1	0	1
7	0	1	0	1	0	1	0	1
11	0	1	0	1	0	1	0	1

Table:

	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	0	1
2	0	1	0	1	0	1	0	1
3	0	1	0	1	0	1	0	1
4	0	1	0	1	0	1	0	1
7	0	1	0	1	0	1	0	1
11	0	1	0	1	0	1	0	1

Table:

	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	0	1
2	0	1	0	1	0	1	0	1
3	0	1	0	1	0	1	0	1
4	0	1	0	1	0	1	0	1
7	0	1	0	1	0	1	0	1
11	0	1	0	1	0	1	0	1

Table:

	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	0	1
2	0	1	0	1	0	1	0	1
3	0	1	0	1	0	1	0	1
4	0	1	0	1	0	1	0	1
7	0	1	0	1	0	1	0	1
11	0	1	0	1	0	1	0	1

Table:

	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	0	1
2	0	1	0	1	0	1	0	1
3	0	1	0	1	0	1	0	1
4	0	1	0	1	0	1	0	1
7	0	1	0	1	0	1	0	1
11	0	1	0	1	0	1	0	1

Using K-map

$$\Sigma m(1, 3, 4, 7, 11) \\ \Sigma d(5, 12, 13, 14, 15)$$

AB	00	01	11	10
CD	00	1	1	0
01	1	X	X	X
11	0	X	X	X

CD + BC + D

$$\begin{array}{c} 1000, F \\ 0010, P \\ 0011, S \end{array}$$

$$\begin{array}{c} 1100, L \\ 1010, R \\ 0011, S \end{array}$$

$$AB\bar{C} + CD + \bar{A}D$$

11- - S, F, L  
1- 1- S, F, P, R  
- 11 S, F, L, R

$$\begin{array}{c} 1100 (L, R) \\ 1110 (R, F) \\ 1010 (S, P) \\ 0110 (S, P) \end{array}$$

$$\begin{array}{c} 1110, F \\ 1101, L \\ 1011, S \\ 0111, P \end{array}$$

⑥ Define prime implicants with examples

A group of squares or rectangles made up of a bunch of adjacent minterms that is allowed by <sup>definition</sup> of a Karnaugh Map are known as prime implicants or PI.

AB	00	01	11	10
CD	00	1	1	0
01	1	1	1	1

Prime implicants 2

AB	00	01	11	10
CD	00	1	1	0
01	1	1	1	1

$$D'A + B'C + CD$$

(2)

Minimization - the following function using Quine Me  
cluskey method

8.4.21

$$f(a, b, c, d) = \{0, 1, 2, 4, 6, 8, 12, 14\}$$

Input:

0 0, 0000 ✓  
1 1, 0001 ✓  
2 2, 0010 ✓  
4 4, 0100 ✓  
8 8, 1000 ✓  
9 6, 0110 ✓  
10 1100 ✓  
3 14, 1110 ✓

		First comparison		Second comparison	
0	(0,1)	000 - 0		(0,2,4,6)	00 - 0
	(0,2)	00 - 0 ✓		(0,4,8,12)	- - 00
	(0,4)	- 000 ✓			
	(0,8)	0 - 00 ✓			
	(2,4)	0 - 10 ✓		(4,6,12,14)	- 1 - 0
	(8,14)	- 1 - 00 ✓			
	(4,6)	0 1 - 0 ✓			
	2 (12,14)	11 - 0 ✓			
	(6,14)	- 110 ✓			

Prime implicants:

(0,2,4,6) 0 - - 0  
(0,4,8,12) - - 00  
(4,6,12,14) - 1 - 0  
(0,1) 000 -

$$\bar{A}\bar{D} + \bar{C}\bar{D} + B\bar{D}$$

$$+ \bar{A}\bar{B}\bar{C}$$

	0 - 0	- - 00	- 1 - 0	000 +
0	✗	✗		✗
1				
2	✗			
3				
4	✗		✗	✗
5	✗		✗	✗
6	✗			
7				
8		✗		✗
9				
10			✗	
11				
12			✗	✗
13				
14				✗

ABC coverage Table

ABED + P

1 (a) Perform subtraction using 2's complement method

$$(85 - 47)_{10}$$

$$85 - \text{binary} = 01010101$$

$$47 \text{ binary} = 00101111$$

$$10010000 - 1.5 \text{ complement}$$

$$+1$$

$$\overline{1101001} - 2^1 \text{ complement}$$

$$(85 + (-47))_{10}$$

$$01010101$$

$$\text{④ } 101010001$$

$$(+87)_{10} = 11100110$$

$$(88)_{10} = 0.0100110$$

(b) convert  $(541.203)_6$  to base 5, base 8 and

base 10.

$$(541.203)_6 = \frac{5 \times 6 + 4 \times 6^0 + 1 \times 6^{-1} + 2 \times 6^{-2} + 3 \times 6^{-3}}{6}$$

$$= (205.3472)_{10}$$

$$(205.3472)_{10} = 5 \lfloor \frac{205}{5} \rfloor$$

$$\begin{array}{r} 5 \lfloor \frac{205}{5} \rfloor \\ 5 \lfloor \frac{41}{5} \rfloor \\ 5 \lfloor \frac{8}{5} \rfloor \\ 5 \lfloor \frac{1}{5} \rfloor \\ 0 \end{array}$$

$$\therefore (1310.2332)_5$$

$$\begin{array}{r} 3472 \\ \times 5 \\ \hline 17360 \\ \times 5 \\ \hline 86800 \\ \times 5 \\ \hline 43000 \\ \times 5 \\ \hline 20000 \end{array}$$

$$(\cdot 1332)_5$$

$$(205,3972)_{10} = \underline{\hspace{2cm}}$$

Bankomat

$$(205)_5 = (315)_8$$

$$(-3472)_{10} = 261637\ldots$$

$$(205.3472) \approx (315.1261637)$$

Thermiges 21

1000  
3972  
x 8  
-----  
27776  
x 8  
-----  
9504

6.2208

~~20 8~~

— 1.7669.

$$= \frac{B \times 8}{6-1312}$$

11 = 458818

1. 049

$$\frac{x}{3.9}$$

20

7.7

52

X

7

1. (a) Write the binary code for

the gray code -10110111

$$\text{binary} = 11011010$$

11011010  
11011010

01101  
10110111  
10110110  
(351, 10)

10110110  
10110110  
10110110

101101  
10101010

1.5 (SP) 1.2

10.2

1. 120

12

120  
119  
118  
E-1

1-7  
1-8  
E-1  
E-2

1-8  
E-4  
L-0

1-8  
E-4  
L-3

E-1  
L-0

① Represent the decimal number 28 to

excess 3 and BCD code

$$(28)_{10} = (2)_{\text{Ex-3}} + 8' A + 8A = 2$$

28 in binary is 10,000,000. After rounding

$$\begin{array}{r} +3 \\ +3 \\ \hline 5 \end{array}$$

$$\begin{array}{r} 11 \\ \downarrow \\ 0101 \\ 1011 \\ \hline 01011011 \end{array}$$

$$(28)_{10} = (2)_{\text{Ex-3}}$$

$$\begin{array}{r} 345/10 = 34 \\ \hline 6 \end{array}$$

$$\begin{array}{r} 3 \\ +3 \\ \hline 6 \end{array}$$

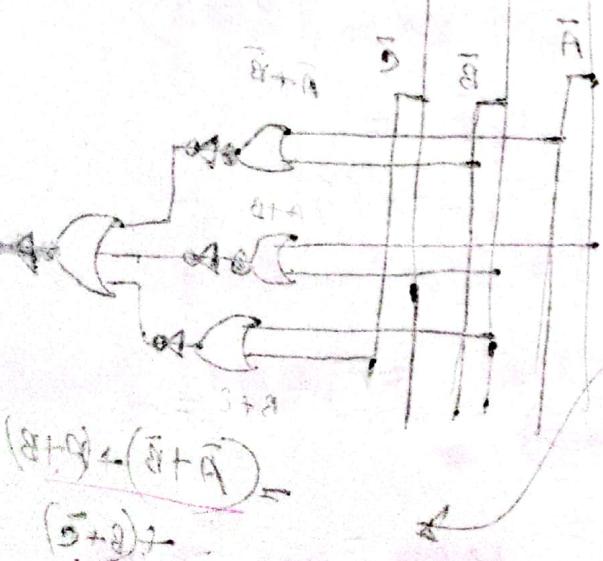
$$\begin{array}{r} 7 \\ 8 \\ \hline 1 \end{array}$$

$$\begin{array}{r} 0110 \\ 0111 \\ \hline 1000 \end{array}$$

$$(28)_{10} = (2)_{\text{BCD}}$$

$$\begin{array}{r} 2 \\ \downarrow \\ 0010 \\ 8 \\ \downarrow \\ 1000 \end{array}$$

$$(28)_{10} = (00101000)_{\text{BCD}}$$



28

$$\begin{array}{r} 2 \\ \downarrow \\ 3 \\ 3 \\ 5 \\ 8 \\ 8 \\ \hline 01011011 \end{array}$$

$$\begin{array}{r} 2 \\ \downarrow \\ 3 \\ 3 \\ 5 \\ 8 \\ 8 \\ \hline 01011011 \end{array}$$

$$5'8 + 8' A + 8A$$

$$\overline{5}8 + \overline{8}A + 8A$$

$$(\overline{5} + 8) \cdot (\overline{8} + A) \cdot (8 + \overline{A})$$

$$(\overline{5} + 8) + (\overline{8} + A) + (8 + \overline{A})$$

$$(\overline{5} + 8) + (\overline{8} + \overline{A}) + (\overline{8} + A)$$

$$(\overline{5} + 8) + 8 \cdot A + 8A$$

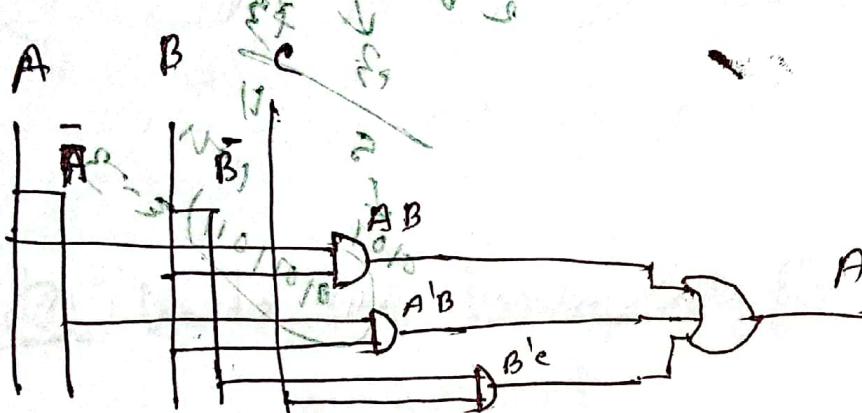
at 82 medium period off the circuit

2.

Given the boolean function:

$$k = AB + A'B + B'C \quad \text{E-43 (82)} = 01(82)$$

- ① Then implement with AND, OR and NOT gates.
- ② Implement it with OR and NOT gates.



$$\text{E-600x3 (11011010)}$$

$$AB + A'B + B'C \quad \text{E-43 (82)} = 01(82)$$

$$AB + \bar{A}\bar{B} + B'C$$

$$\bar{A}\bar{B} \cdot \bar{A}\bar{B} + \bar{B}C$$

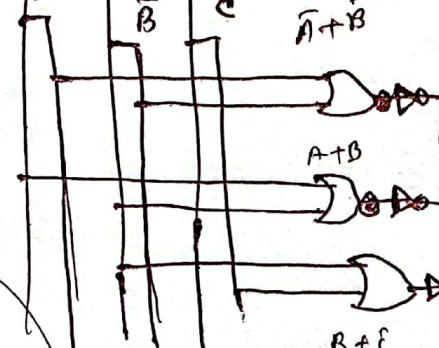
$$= (\bar{A} + \bar{B}) \cdot (\bar{A} + \bar{B}) \cdot (\bar{B} + \bar{C})$$

$$= (\bar{A} + \bar{B}) + (\bar{A} + \bar{B}) + (\bar{B} + \bar{C})$$

$$= (\bar{A} + \bar{B}) + (\bar{A} + \bar{B}) + (\bar{B} + \bar{C})$$

$$= AB + \bar{A}\bar{B} + \bar{B}C$$

$$AB + \bar{A}\bar{B} + B'C \quad \text{E-43 (82)} = 01(82)$$



$$= (\bar{A} + \bar{B}) + (\bar{A} + \bar{B}) + (\bar{B} + \bar{C})$$

Q) What are don't care terms? Explain with example?

In digital logic, a don't care term for a function is an input-sequence for which the function output does not matter.

AB	00	01	11	10
00	X	1	X	1
01	X	1	1	
11	X	1	1	1
10	1			

$$(A' + B) (A + B')$$

$$(A'B + AB') \times (A'B' + AB)$$

2(b)

$$A'B + AB'$$

Soln

$$(x \oplus y)' = (xy' + xy)'$$

$$= \overline{xy'} \cdot \overline{xy}$$

$$(x \oplus y)' = (x'y) \cdot (x+y')$$

$$\text{Duel of } (x \oplus y)' = \text{Duel of } (x'y + xy')$$

$$= (x+y') (x'y) \quad \text{--- (1)}$$

① ① are equal

	1	0	0	0	0	0	0	0
	0	1	0	0	0	0	0	0
	0	0	1	1	1	1	1	1
	0	1	1	0	0	0	0	0
	1	0	1	0	0	0	0	0
	1	1	0	1	0	0	0	0
	1	0	0	0	1	0	0	0
	0	1	0	0	0	1	0	0

3. How many parity bits are required to detect 3-bit odd errors?

parity generator and checker

24. The parity bit ensures that the total number of 1-bits in the string is even or odd.

According, there are two variants of parity bits. even parity bit and odd parity bit.

Parity bits are a simple form of error detecting code.

3bit message / odd parity bit generator

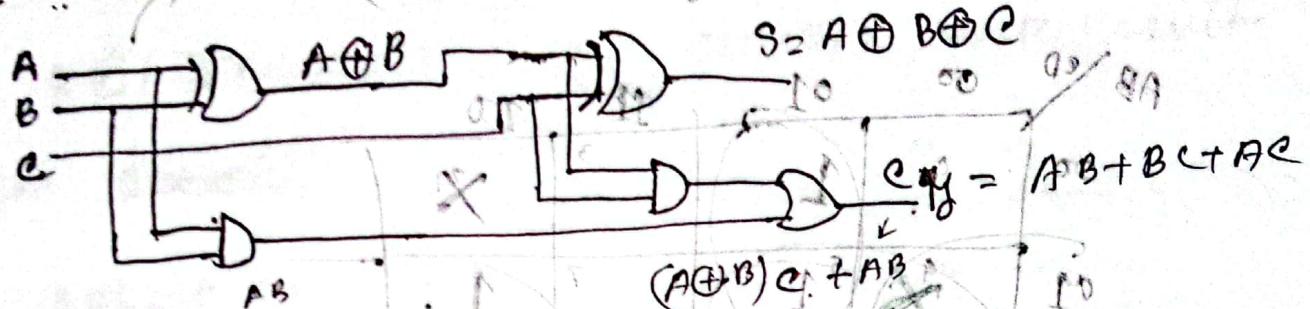
A	B	C	Y	Check
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	1	0
1	1	1	0	0

$p = A \oplus (B \oplus C)$

roitsmit - nö/008 gewählt auf 0000000000000000

3(b) Implement a full adder using two half

adder 9  $\rightarrow$  half adder  $(x_0, x_1, s_1, c_1)$  m3 = (0,1,0,1) 7



$$S = A \oplus B \oplus C$$

$$\text{Carry} = AB + BC + AC$$

full adder

$$S = A \oplus B \oplus C$$

$$C = AB + BC + AC$$

$$(A \oplus B)C + AB$$

$$(AB + A\bar{B})C + AB$$

$$\Rightarrow \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C}$$

$$= \bar{A}B\bar{C} + A(\bar{B}\bar{C} + B)$$

$$= \bar{A}B\bar{C} + \bar{A}B + AC$$

$$= B(\bar{A}C + A) + AB\bar{C}$$

$$= B(\bar{A} + C) + AC$$

$$= AB + BC + AC$$

A B C			Σ	P-erm
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

2018

1. a)  $(45)_{10} - (83)_{10}$ . Using two's complement form with 8-bit numbers. Then convert your result back to decimal.

$$(45)_{10} = 00101101$$

$$(83)_{10} = 01010011$$

10101100 - is complement

+1 - 2's complement

$$83$$

$$- 45$$

$$38$$

$$(45)_{10} = 00101101$$

$$(83)_{10} = 10101100$$

$$- 38 \quad (10) \quad (218)_{10} = 11011010$$

b)  $(65)_{10} + (72)_{10}$

$$\begin{array}{r} 01000001 \\ + 01001000 \\ \hline \end{array}$$

$$(137) \quad \underline{10001001}$$

$$83$$

$$45$$

$$38$$

1 c) Write the gray code for  $\underline{\underline{(1011)_2}}$

$\underline{(1011)_2}$

$\underline{= (1110)}$  gray

↓ first transform to oct ↓ first  
↓ second transform to oct ↓ second

2 a) convert  $\underline{(10000110)_BCD}$  to decimal, binary

Octal

$\underline{(10000110)_BCD} = (2)_2$

$\underline{100.00 \ 11 \ 0}$

8 6

decimal =  $(86)_{10}$

binary

$\underline{= (10000110)_2}$

$\begin{array}{r} 186 \\ 2 \ \cancel{43-0} \\ 2 \ \cancel{21-1} \\ 2 \ \cancel{10-1} \\ 2 \ \cancel{5-0} \\ 2 \ \cancel{2-1} \\ 2 \ \cancel{1-0} \\ 0-1 \end{array}$

$\underline{1010110}$

$\underline{(12 \ 6)_8}$

8 6

8 6

8 6

①

$10^{47} \text{ L}$

$$② f(A, B, C, D) = \sum m(0, 1, 3, 7, 8, 9, 11, 15) \quad (A'B'C'D')' (A'B'C'D) = 0$$

$$00A + 038A + 05A \bar{D} \bar{A} =$$

$$00A + 058A + (\bar{A} \bar{B} \bar{C} \bar{D})' \bar{D} \bar{A} =$$

Input:

0 0,0000.

First Complementation

Second Complementation

1 1,0001

$$(0,1) 000 - \cancel{0} \quad (0,1,8,9) - \cancel{0} - \cancel{0}A =$$

8, 1000

$$(0,8) - \cancel{0} \quad (0,8,6,9) - \cancel{0} -$$

9,

$$1 \cdot (1,3) 00-1 \quad 1 (1,3,9,11) - 0-1$$

2 3, 0011

(1,9)

-001

1

$$(1,9,3,11) - 0+1$$

9, 1001

(8,9)

100 -

1

$$(5,11,7,3) = -11$$

3 07, 0111

$$2 \begin{matrix} (1,3) & 0-11 \\ (3,11) & 0-011 \\ (9,11) & 10-1 \end{matrix} \quad \checkmark \quad \checkmark$$

9 15, 1111

$$3 (11,15) 1-11 \quad \checkmark$$

prime implement

-00-
-00-
-0-1
-0-1

-
-11

	-00-	-0-1	-11
0	X	.	
1	X	X	
3		X	X
7			X
8	X		
9	X	X	
11		X	
15			X
	$\bar{B} \bar{C} + \bar{B} \bar{C} +$	$\bar{C} \bar{D} + \bar{C} \bar{D}$	$\bar{B} \bar{C} + \bar{C} \bar{D}$

⑥ Compare between BCD and Binary Code'

11 (S) BCD Code

## Binary Code

- \* Represent the number using the base -2.

\* Represent the number using the base -2.

10. 10

- \* 10 is a decimal number.

Where as in the BCD system

0000 0001 3(473.6)

## Binary Coded Decimal

\* BCD is not a number system. It is a (110000101110)

\* Expressing decimal numbers in BCD code easy.

\* Represent BCD code

each decimal digit  
4 bit binary convert.

$$* (125)_{10} \rightarrow 000000100101_{BCD}$$

\* Binary is a number system

\* Decimal numbers are relatively difficult to express in binary numbers.

\* To express decimal numbers in binary divided by 2 for integers and 2 raised for fractions

$$\rightarrow \text{Ex } (125)_{10} \rightarrow \text{Binary } (1111101)_2$$

Q) What is Gray code? Explain with examples, how do you convert binary to Gray and Gray to binary.

Gray code also known as reflected binary code, because the first  $(n/2)$  values are complement of those of the last  $(n/2)$  values, but in reverse order. Gray code are used in Karnaugh maps, and error detection.

Binary code:

101011

000

111

$b_2 \ b_1 \ b_0$

gray code  
111110

000

100

$g_2 \ g_1 \ g_0$

111010 = RS  
110110 = OR (FS)

Q)

Q) ~~Explain that a two-input NAND gate~~ can be constructed from two-input NOR gate.

$$\begin{aligned}
 & \text{The following} \\
 & \overline{(A+B)} \cdot \overline{(\bar{A}+\bar{B})} = x \\
 & \overline{(A+B)} + \overline{(\bar{A}+\bar{B})} \\
 & = \overline{(\bar{A}+\bar{B})} \cdot \overline{(\bar{A}+\bar{B})}
 \end{aligned}$$

3@) What is DeMorgan's theorem? Explain with truth table?

36 Simplify the expression  $X = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC + A\bar{B}C$

$$\begin{aligned}
 X &= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C \\
 &= \bar{A}\bar{B}C + BC(\bar{A} + A) + A\bar{B}(C + \bar{C}) \\
 &= \bar{A}\bar{B}C + BC + A\bar{B} \\
 &= B\bar{B}(\bar{A}\bar{C} + \bar{A}) + BC \\
 &= B(\bar{A} + \bar{A}) + BC \\
 &= \bar{B} + BC
 \end{aligned}$$

	BC	00	01	11	10
00	1				
10					
01					
11					

$$\bar{B}\bar{C} + BC + A\bar{B}\bar{C}$$

$$\begin{aligned}
 &= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC + A\bar{B}\bar{C} + A\bar{B}C \\
 &= \bar{B}\bar{C}(\bar{A} + \bar{A}) + BC(A + \bar{A}) + A\bar{B}C \\
 &\Rightarrow \bar{B}\bar{C} + BC + A\bar{B}C \\
 &= \bar{B}\bar{C} + C(B + A\bar{B}) \\
 &= \bar{B}\bar{C} + C(B + A) \\
 &= \bar{B}\bar{C} + AB + AC
 \end{aligned}$$

	11	10	00	01	10
00	1				
10					
01					
11					

(Mitsubishi Diesel & F) MB = 0.913

$$0.8A + 0.9A + 0.8A + 0.5A =$$

$$0.8A + 0.9A + 0.8A + 0.2A =$$

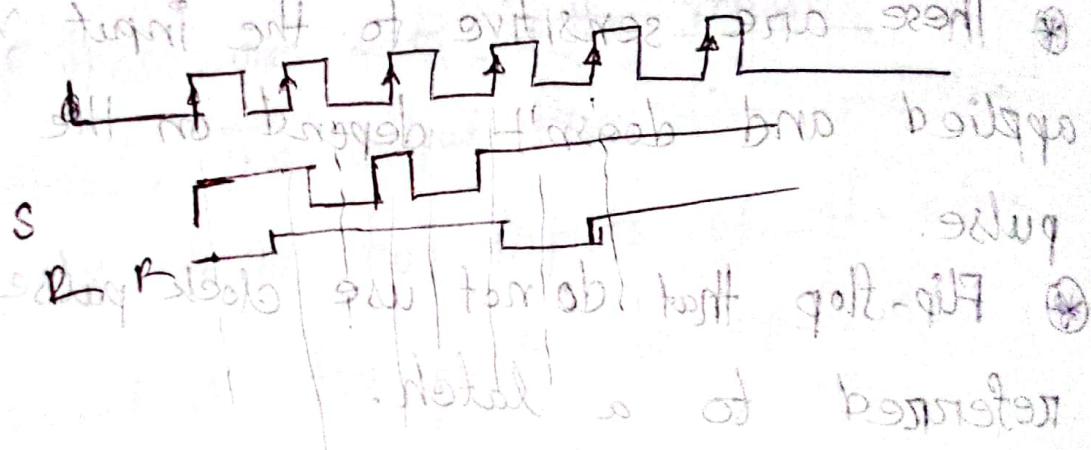
2020 - Section B

5 @ Write down some benefits of clocked flip-flop.  
Discuss the circuit diagram of the edge-triggered SR flip-flop with timing diagram.

Some benefits:

①

SR	Q	Q'
0 0	0	1
0 1	0	1
1 0	1	0
1 1	toggle	



Q. 6. B) Mention some applications of latch?

- ① Latches are useful for the design of the ~~asynchronous~~ <sup>asynchronous</sup> sequential circuit ~~theory~~ <sup>theory</sup> of it.
- ② Latches are ~~memory~~ <sup>memory</sup> sequential circuit ~~theory~~ <sup>theory</sup> of it.
- ③ These are sensitive to the input voltage applied and doesn't depend on the clock pulse.
- ④ Flip-flop that do not use clock pulse are referred to a latch.

C) Briefly explain the operation of master-slave flip-flop using logic and timing diagram

⑥ Briefly explain the operation of master-slave flip-flop using logic and timing diagram.

The master-slave flip-flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the "master" and the other as "slave". The output from the master flip-flop is connected to the two inputs of the slave flip-flop whose output is fed back to inputs of the master flip-flop.

\* In addition to these two flip-flop, the circuit also includes an inverter. The inverter is connected to the clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if  $CP=0$  for a master flip-flop, then  $CP=1$  for a slave flip-flop. and  $CP=1$  for master flip-flop then it becomes 0 for slave flip-flop.

- 7
- Q) Define resolution or step size of a D/A converter
- \* Resolution or step size defines the smallest voltage or current that is possible for the DAC output signal.
- For example: an 8 bit DAC that generates a maximum output voltage of 5 volts has a step size or resolution of  $\frac{5}{2^8-1} = 19.6 \text{ mV}$
- Sometimes, the resolution is stated in the percentage value.
- Q) For a DAC, if step size is 0.1V, then what will be the output voltage for a digital input 0001.1
- \* Full scale output = step size  $\times$  number of steps

$$\text{output} = 1 \times \frac{0.1}{2^4-1}$$

$$=$$

7

b) What is the advantage of R/2R ladder

DAC over weighted registers DAC?

- ① If contains only two values of resistors  $R$  and  $2R$ . So, it is easy to select and design more accurate resistor.
- ② Doesn't require high precision resistor.
- ③ Number of bits can be expanded by adding more sections of same R/2R values.
- ④ In inverted R/2R ladder DAC, node voltages remain constant with changing input binary words.

2019

5

Q. What are the advantage of a master slave JK FF? Mention some limitations of SR FF.

- ① The most sophisticated flip flop is the J-k flip-flop.
- ② It has two inputs J and K which can be in any one of four states 00, 01, 10, and 11. Each of these states will have a unique effect on the device.
- ③ Making it easier to use in larger circuit.
- ④ In master slave Jk flip-flop, the output of master change many times but slave output change only one time so master flip-flop act as level triggered and slave flip-flop act as edge triggered by which race around condition does not take place in the output of slave flip-flop.

Q@ What is the basic difference between latch and flip-flop?

Latch:

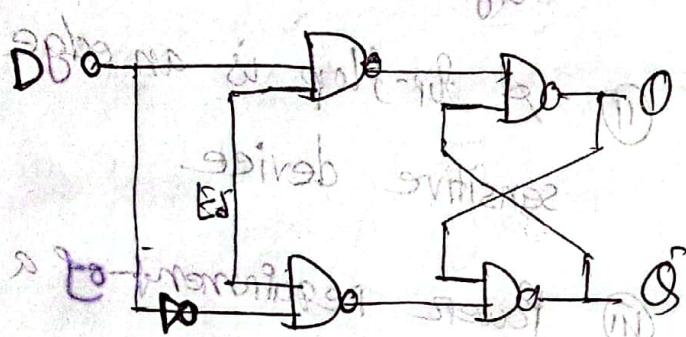
- ① Latches does not required clock signal
- ② A latches is a level sensitive devices
- ③ The power requirement of a latch is less
- ④ A latch works based on the enable signal
- ⑤ Asynchronous bistable devices
- ⑥ NOR gate latch

Flip-flop

- ① Flip-flop have clock signal
- ② A flip-flop is an edge sensitive device.
- ③ Power requirement of a flip-flop is more
- ④ A flip-flop works based on the clock signal
- ⑤ Synchronous bistable devices
- ⑥ SR, JK, D, T, FF

① Draw the circuit diagram and discuss the working operation of D flip-flop and I flip-flop.

D flip-flops



## Operation of D-Flip-flop:

④ D-Flip-flop is a bi-stable memory element

which can store one bit at a time, either '1' or '0' along

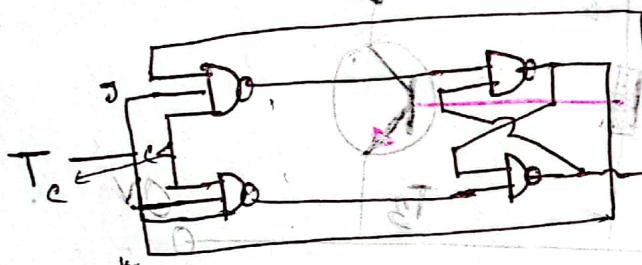
④ For edge triggered flip-flop, the circuit ~~receives~~ ~~obtains~~ ~~from~~ ~~input~~ ~~data~~ ~~at~~ ~~the~~ ~~time~~ ~~of~~ ~~clock~~ ~~transition~~ ~~according~~ ~~to~~ ~~which~~ ~~the~~ ~~flip-flop~~ ~~propagates~~ ~~the~~ ~~input~~ ~~to~~ ~~the~~ ~~output~~.

\* edge triggered can be positive edge triggered or negative triggered.

\* Positive edge triggered D flip-flop changes its output according to input with every transition of the clock pulse from 0 to 1.

\* As for the negative edge triggered D flip-flop changes its output according to input with every transition of the clock pulse from 1 to 0.

### T-Flip-flops



The toggle or T-flip-flop is a two-input flip-flop.

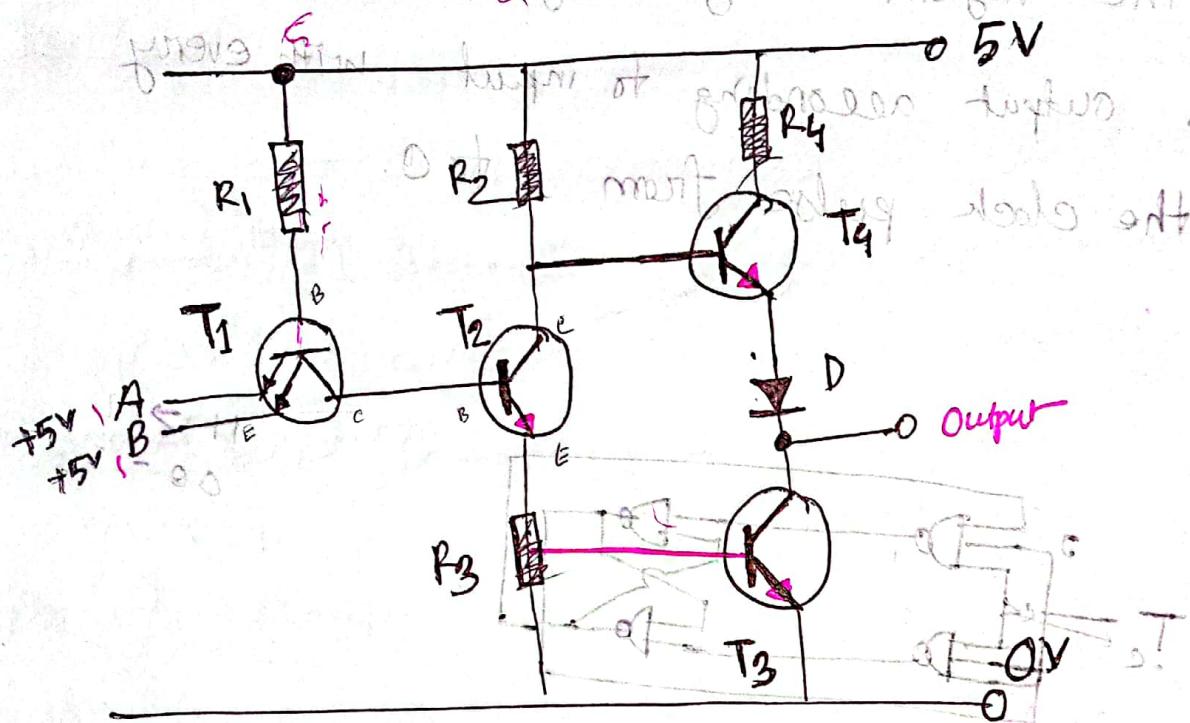
The inputs are the toggle (T) input and a clock (clock) input. If the toggle input is high, the T-Flip-flop changes state (toggle) when the clock signal is applied.

If the toggle input is low, T flip-flop holds the previous state.

Wrote ati regarding off-on behaviour of

① Draw the TTL NAND gate circuit and

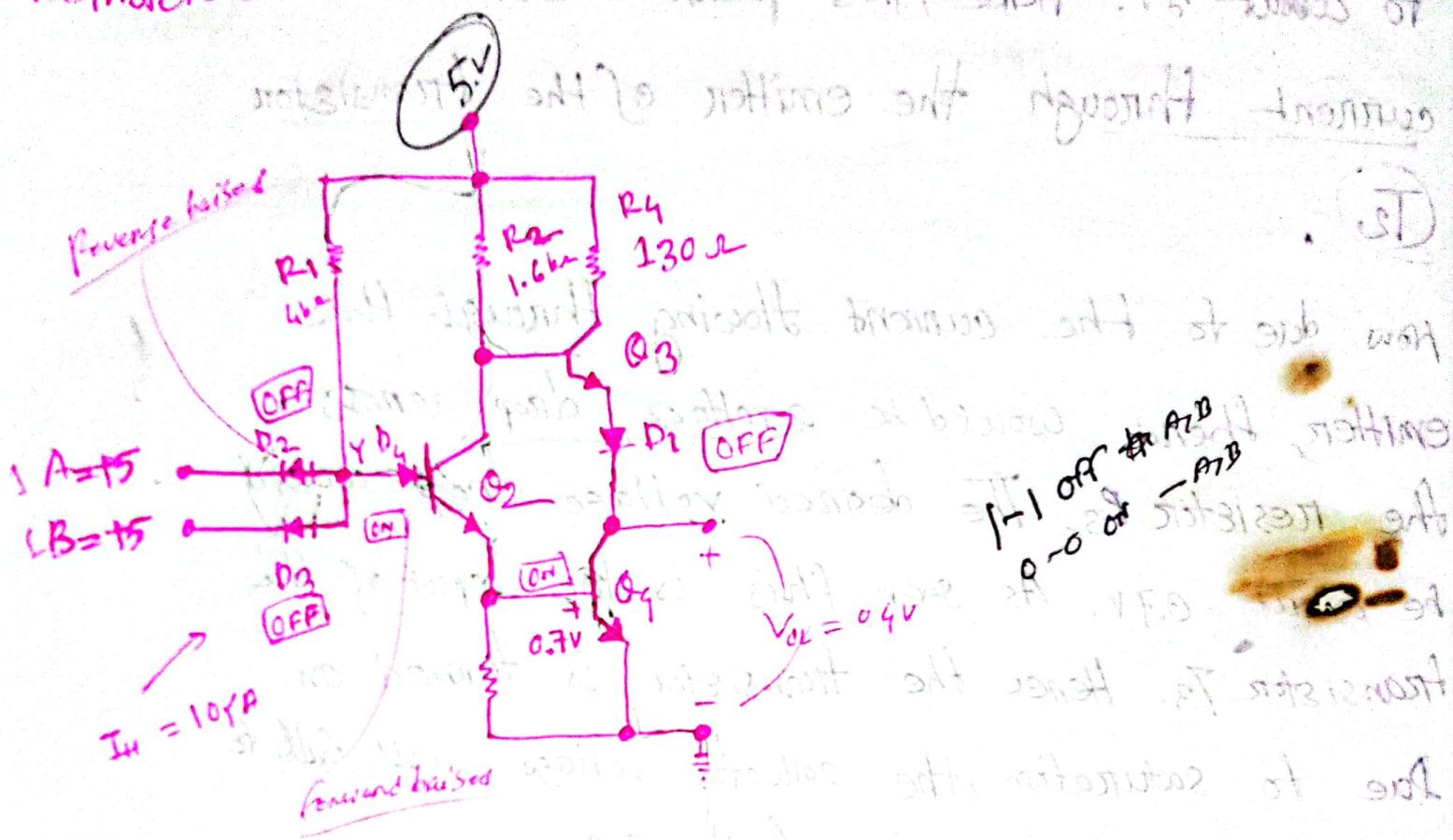
② explain its operation?



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

A TTL NAND gate logic circuit has at least four bipolar junction transistors in which the input (transistor which receives input) has

two emitters and collector of two different transistors with two inputs and two outputs of inverter.



From the diagram, we shall explain the working.

Now, as seen, the transistor  $T_1$  has two emitters to allow input into the transistor. Now, as connected the base voltage will be at 5V. If both inputs are logic 1, the potential difference across base and emitter would be zero. Hence, no current will flow and transistor is turned off.

So, the ~~collector~~ voltage would also be equal to about 5V. Hence, this potential can drive current through the emitter of the transistor  $T_2$ .

Now due to the current flowing through the emitter, there would be a voltage drop across the resistor  $R_3$ . The desired voltage drop would be about 0.7V. As seen, this is the input of the transistor  $T_3$ . Hence the transistor is turned on.

Due to saturation, the collector voltage will fall to about 0.2V. which is a logic 0.

For the transistor  $T_3$ , observe that the emitter voltage is made up of the entire voltage of the diode transistor  $T_3$  plus the voltage drop across the diode transistor  $T_3$ .

about 0.7V. Hence the emitter potential would be  $0.7 + 0.2 = 0.9V$ .

Hence the emitter voltage and collector voltage are equal; So the transistor  $T_3$  will be

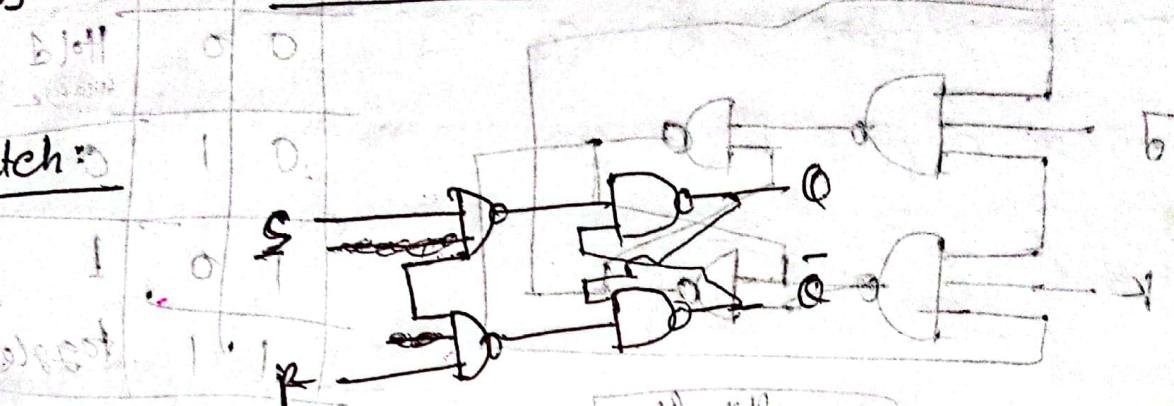
turned off. for

Explain the classification of a 9th Fibroblast

5. 2014

5. 2014 ④ Discuss - how an SR latch is converted into D latch?

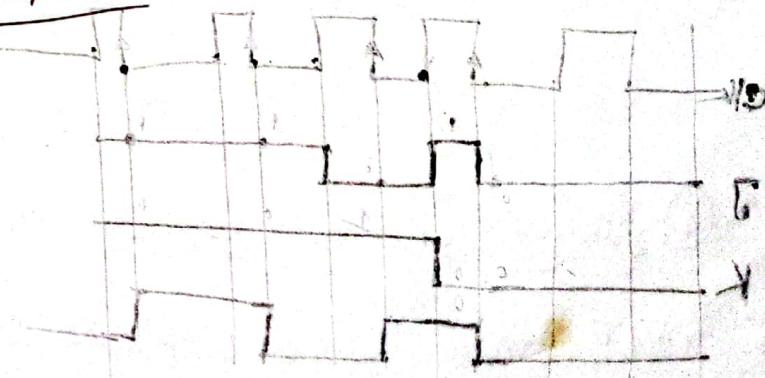
## SR Latch:



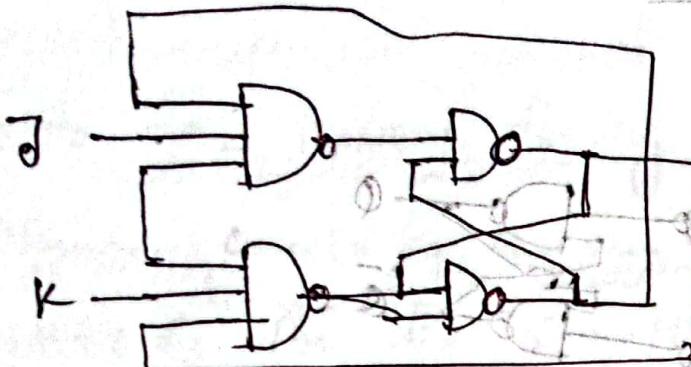
Q1. Diff. b/w SR and D flip-flops

D type flip-flops are easily converted from an SR flip-flop by simply connecting an inverter between the S and R inputs so that the input to the inverter is now the output of the inverter. A state printer is used to show the state of the flip-flop.

## table of D Latch



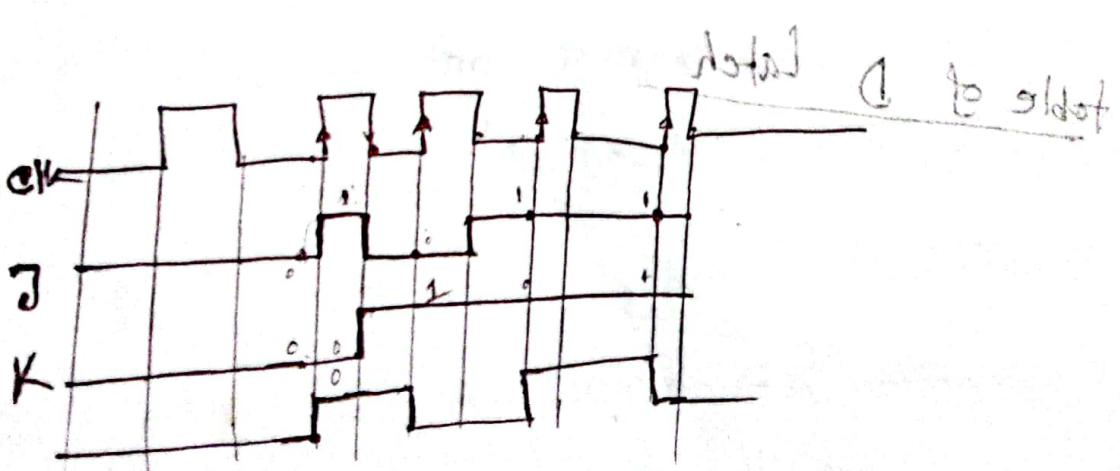
6 @ Explain the operation of a JK Flip-flop using timing diagram.



Q1		Q2		Hold
J	K	J	K	case
0	0	0	0	uncase
0	1	0	1	on next J
1	0	1	0	1
1	1	1	1	toggle

JK flip flop

working A JK flip-flop is nothing more than an S-R flip-flop with an adder layer of feedback.



if  $J=1$ ,  $K=1$ ,  $S=1$  and  $\bar{S}=0$ . This indicates that flip-flop outputs toggle meaning it which changes from 0 to 1 or from 1 to 0. and these changes are reflected at the output pins accordingly. Date: 20/01/2020

the output can be made equal to 0 using CLR pin. However pin while it can set to 1 using Date: 20/01/2020  $\bar{S}$  pin. However these pins can be either active high or active low. Date: 20/01/2020

law operated. Date: 20/01/2020

Standby timer alarm Date: 20/01/2020

transistor Date: 20/01/2020

alarm, Date: 20/01/2020

alarm standby timer alarm Date: 20/01/2020

alarm Date: 20/01/2020

## 555 Timers

2020

6@ Draw the internal functional diagram of a 555 timer and explain its basic operation. What are the applications of 555 timer?

⑥ Draw the pin configuration of a 555 timer and explain the function of each pin?

2021

8@ Discuss the operation of a 555 timer based monostable multi-vibrator?

2015

8@ What is timer? What are the different applications of timer?

⑥ Design an monostable multi-vibrator using 555 timer and explain its operation?

Q1. Draw the block diagram of a 555 timer and explain about its each pin?

Q2. Design an astable multi-vibrator using 555 timer and explain its operation?

blacksmith 2

## Each pin functions:

from 222 to max possible hold soft work

1. ground → 0v supply

2. trigger → When the pin voltage falls below 0.33Vc

the timer is triggered and output goes high.

In the monostable configuration, a high to low voltage transition on the trigger pin starts the timer.

3. output: → The output pulses during astable

operation and goes high for set time in monostable operation.

4. Reset → If reset is not used, connect it to Vcc.

If reset falls, a high output will be forced low.

5. Control voltage → For reliable operation add a 10nF capacitor rises above 0.66 Vcc and resets the output when this happens.

6. threshold:

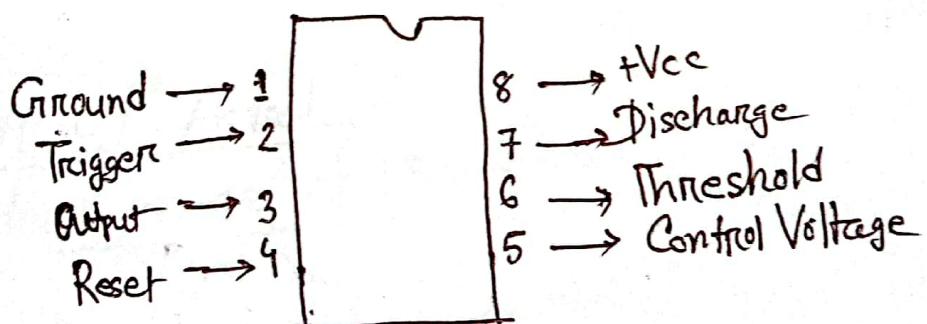
5. Control voltage: For reliable operation add a  $10\text{nF}$  capacitor to ground on this pin.

6. threshold: Detects when the voltage on the timing capacitor rises above  $0.66\text{ V}_{\text{cc}}$  and outputs when it happens.

7. discharge: Provides a discharge path from the timing capacitor to ground when the output is low.

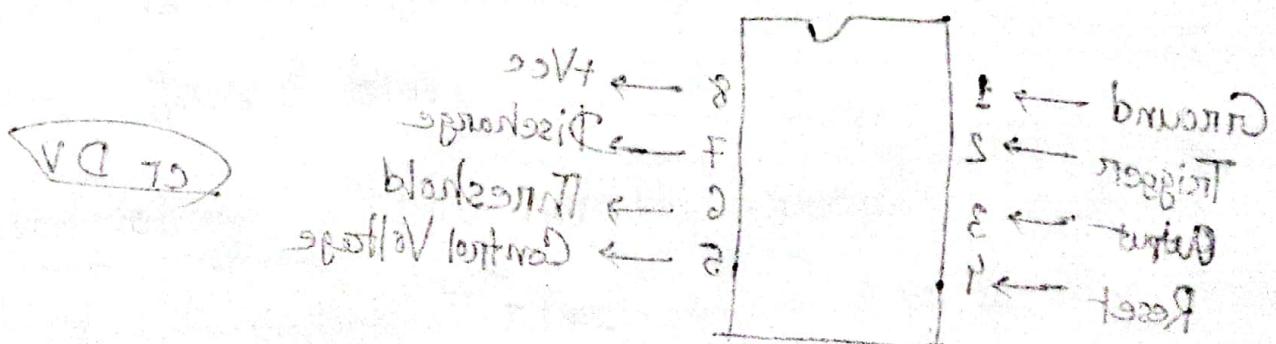
8.  $\text{V}_{\text{cc}}$ : Positive power supply voltage.

Pin diagram:

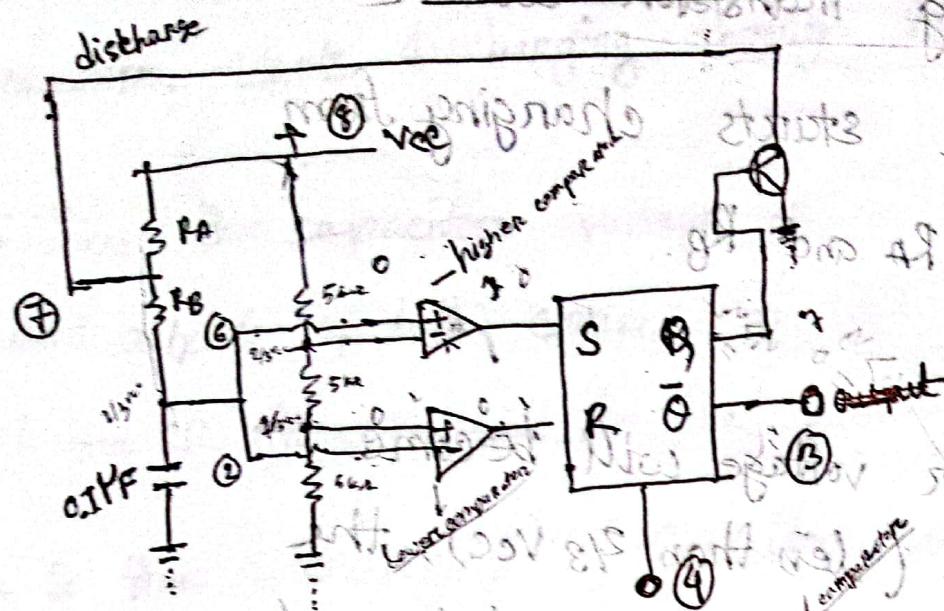


## Applications of 555 timers

- ① Beeping and tone generation.
- ② PWM signal generation.
- ③ Timing or delay circuit.
- ④ Frequency divider.
- ⑤ Missing pulse detector.
- ⑥ astable Multivibrator.
- ⑦ Monostable Multivibrator.
- ⑧ Pulse position modulator.



# Astable Multivibrator Using 555 timer

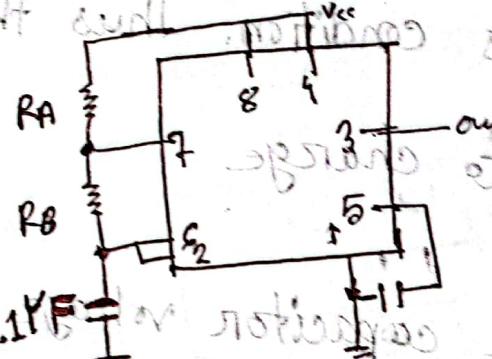
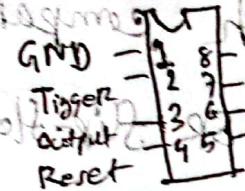


$$V_{th} = V_{cc} \times \frac{R}{3R} = V_{cc} \times \frac{1}{3}$$

$$V_{th} = V_{cc} \times \frac{R}{3R} = V_{cc} \times \frac{1}{3}$$

$$\begin{aligned} 0-0 &= \text{no charge} \\ 0-1 &= 0 \\ 1-0 &= 1 \end{aligned}$$

$$\begin{aligned} V_1 > V_2 &= \text{high} \\ V_1 < V_2 &= \text{low} \end{aligned}$$



## Operation of Astable Multivibrator mode of 555 timer IC

- \* When the circuit is switched on, the capacitor voltage will be less than  $1/3 V_{cc}$ . So the output of the lower comparator will be **HIGH** and of the **higher** comparator will be **LOW**. This sets (1) the output of the SR flip-flop.

Thus the discharging transistor will be

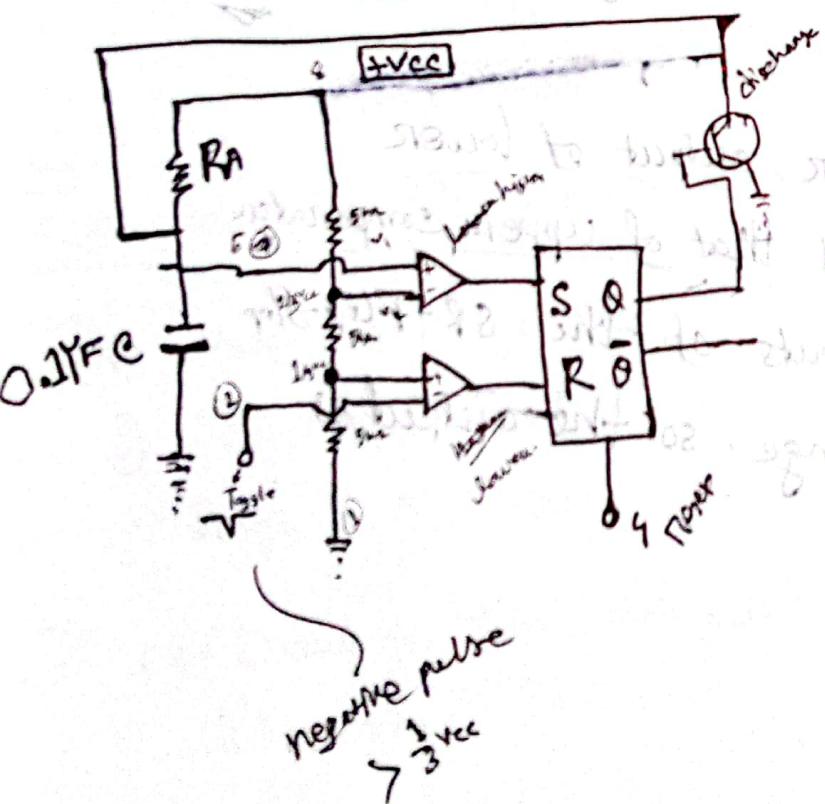
OFF and capacitor C starts changing from  $9.50V$  through resistor  $R_A$  and  $R_B$ .

④ When the capacitor voltage will become greater than  $\frac{1}{3} V_{cc}$  (less than  $\frac{2}{3} V_{cc}$ ), the output of both comparators will be low and output of SR flip-flop will be same as the previous condition. Thus the capacitor continues to charge.

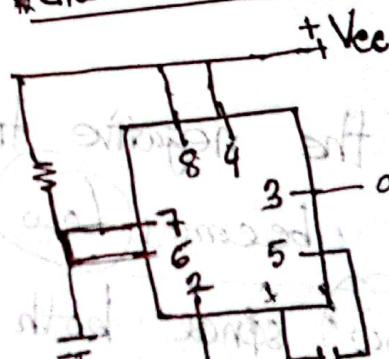
- \* When the capacitor voltage will becomes slightly greater than  $2/3 V_{cc}$  the output of the higher comparator will be HIGH and of lower comparator will be LOW. This resets the SR Flip-flop.

- Thus the discharging transistor turns ON and the capacitor starts discharging through resistor  $R_b$ .
- Soon the capacitor voltage will be less than  $\frac{2}{3}V_{cc}$  and output of both comparators will be low. So the output of the SR flip-flop will be the previous state.
- So the discharging of capacitor continues.
- This process continues and a rectangular wave will be obtained at the output.

### Monostable Multivibrator using 555 Timer (T-shun)



\* circuit Diagram



## Operation:

- \* The Monostable Multivibrator will be in its stable state (output Low) until it is triggered.
- \* When a negative trigger is applied to the trigger pin of 555 timer, output of lower comparator will become HIGH and output of upper comparator will be Low, since the capacitor voltage is zero. This make the output HIGH.
- \* The discharge transistor turns off and the capacitor starts charges through resistor  $R$  to  $V_{cc}$ .
- \* After the negative trigger, output of lower comparator becomes Low and that of upper comparator remains Low, since both inputs of the SR-Flip-Flop are Low. Output will not change, so the output is HIGH.

- \* When the capacitor voltage will become greater than  $\frac{1}{3} V_{cc}$  output of trigger comparator becomes High and that of lower comparator remains Low so the output becomes Low.
- \* This turns On the discharge transistor and the capacitor discharges.
- \* The circuit remains in its stable state - (output low) until next trigger occurs.

Ques

2019  
7. (a) Draw the TTL NAND gate circuit and explain its operation

2018  
7. (a) State advantage and disadvantage of TTL?

(b) Draw the circuit diagram of DTL-NAND gate?

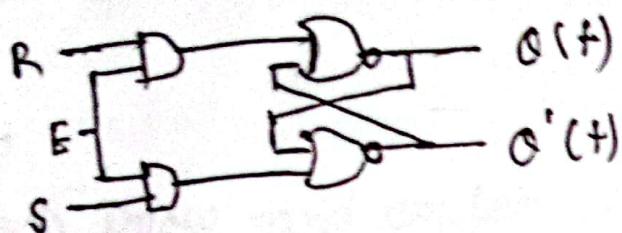
(c) Design a NOT gate using MOSFET

2015  
c. (a) Draw the basic DTL gates to implement NAND gate - Explain its operation.

2014

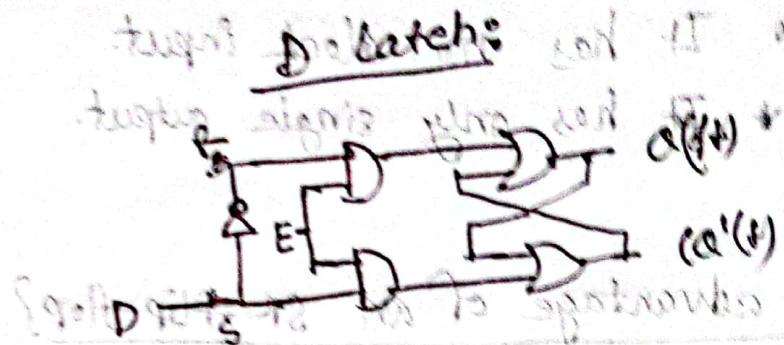
Q5(c) Discuss how an SR latch is converted into D latch?

SR Latch:



State table of SR Latch:

S	R	$Q(t+1)$
0	0	Q(t)
0	1	0
1	0	1
1	1	—



State table of D Latch

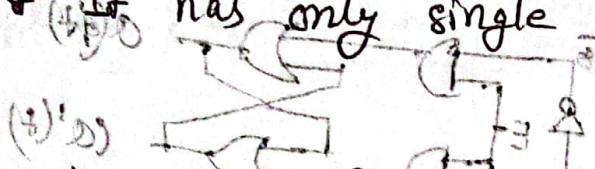
D	$Q(t+1)$
0	0
1	1

D latch is obtained from SR latch by placing an inverter between S and R inputs and connect D input to S. That means we eliminated the combinations of S and R are of same value. If  $D = 0 \rightarrow S = 0 \& R = 1$ , then next state  $Q(t+1)$  will be equal to 0 irrespective of present state Q(t) values.

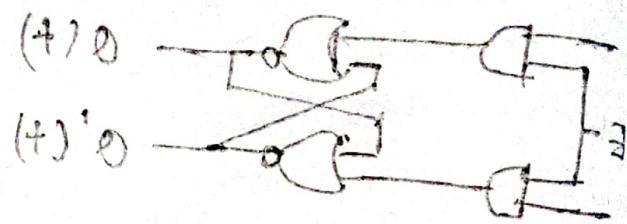
2019 50

\* Disadvantage of an SR Flip-flop? ~~except~~ **limitation**

- \* It has ~~not~~ **Enable** input. & ~~noted~~ #2 no work ~~and~~ **use** ~~id~~
- \* It has a **RACE** condition.
- \* It has ~~no~~ **clock** input.
- \* It has ~~only~~ **single** output.



\* advantage of an SR flip-flop?



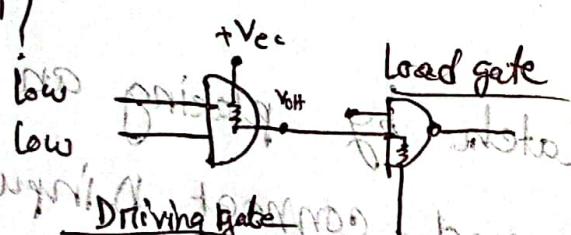
~~noted~~ (to add ~~start~~ state)

~~noted~~ #2 ~~to~~ ~~not~~ ~~start~~

2019

7

⑥ What is current sourcing and current sinking action?



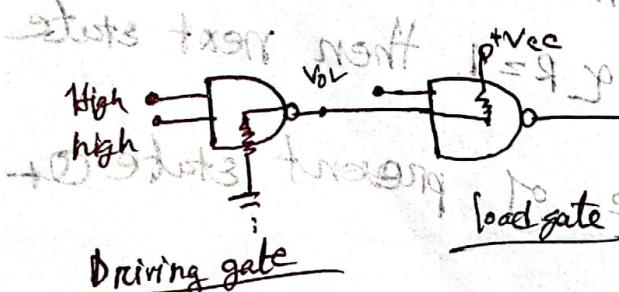
current sourcing

(H)	0	1
(H)	0	0
1	0	0
1	0	1
1	1	1

driving gate supplies

current to load gate in High state

→ step 3) ~~arrest~~ ~~switch~~ ~~on~~ ~~off~~ ~~state~~ ~~trans~~



current sinking

driving gate receives

(sinks) current ~~from~~ load gate in Low state

Source current: is the ability of the digital output/input port to supply current

Sink current: is the ability of the port to receive current.

Q1 7(c) Draw and explain a CMOS NOR gate circuit

Boolean equation:

$$Y = \overline{A + B}$$

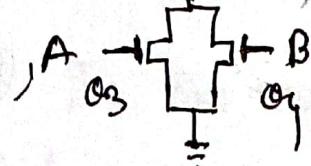
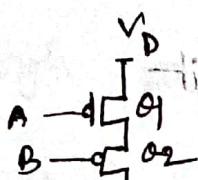
$$\Rightarrow Y = \overline{A} \cdot \overline{B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Operation:

Nmos = parallel connection

Pmos = series connection



Input		pmos	Output
A	B	Q1 or Q3 or Q4	0
0	0	on on off off	1
0	1	on off off on	0
1	0	off on on off	0
1	1	off off on on	0

2 Input CMOS NOR gate Circuit, Here, P-channel MOSFETs  $Q_1$  and  $Q_2$  are connected in series and N-channel MOSFETs  $Q_3$  and  $Q_4$  are connected in parallel.

2018

5@ What is Latch and flip-flop?

Latch :

A Latch is a special type of logical circuit. It has two stable states. The Latches have low and high two stable states. A latches is a storage device that holds the data using the feedback lane.

A latch is the most basic type of flip-flop circuit. It can be constructed using NOR gates. According to the latch are of two types. ① NAND gate latch ② NOR gate latch

A flip-flop is a device which stores a single bit (binary digit) of data. Two states represents a "one" and "zero".

	Q	Q'	Q	Q'	Q	Q'	Q	Q'
1	0	1	0	1	0	1	0	1
0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0



2018

Q1. What is meant by logic? What are the advantages and disadvantages of TTL?

Ans: Logic is a system of logic gates.

Advantages:

- ① It has strong drive capability.
- ② It is faster in some versions.
- ③ TTL requires only one supply voltage.
- ④ It has noise immunity better than ECL but less than BiCMOS.

CMOS

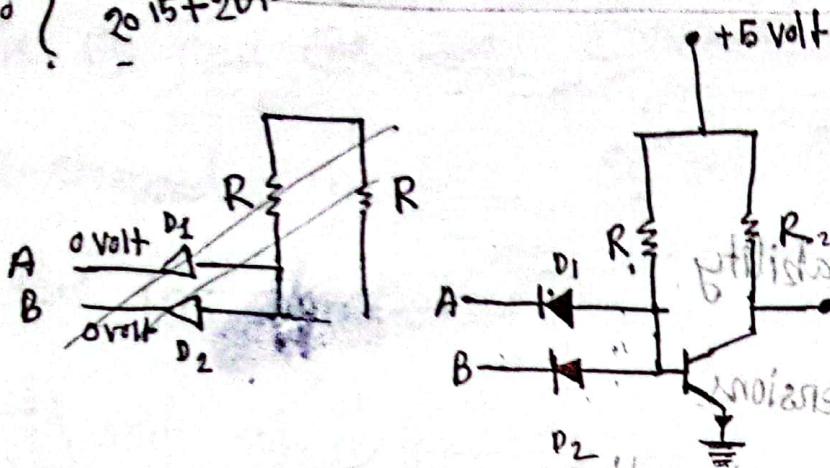
- ⑤ TTL provides very high speed.
- ⑥ TTL is more reliable.
- ⑦ TTL needs low power for any operation.
- ⑧ TTL circuit is not complicated.

Disadvantages of TTL

- ① High power consumption.
- ② It functions just on 5V.
- ③ The fan out capacity for this device is low.
- ④ Low input resistance.

⑥ Draw the circuit diagram of DTL-NAND

gate ? } 2015 + 2018



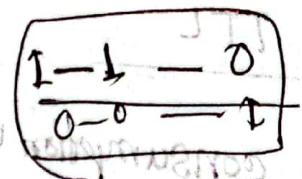
Diode transistor Nand gate:

प्रैट्ट:  $A, B = 0$  इस तेज़ forward biased and transistor ORP

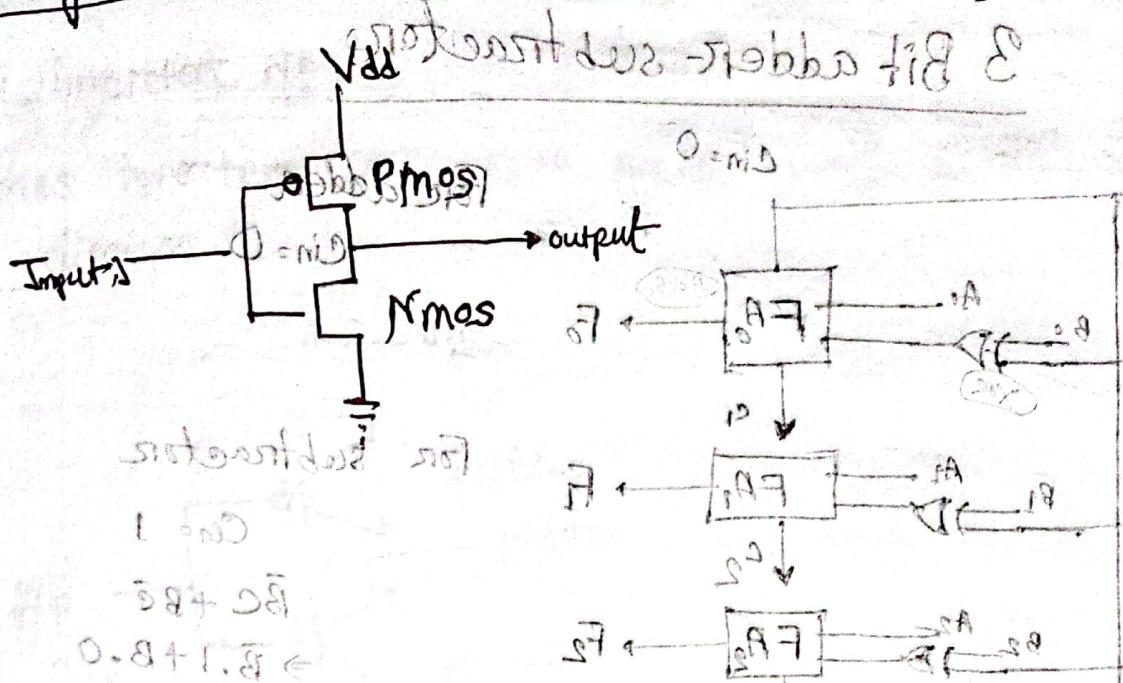
એકાલ R<sub>2</sub> એટિ 5 V કાર્યવાહી એકાલ, x=1

\*  $A, B = 1 \rightarrow$  diode off  $\rightarrow$  transistor ON  $\rightarrow$  ground

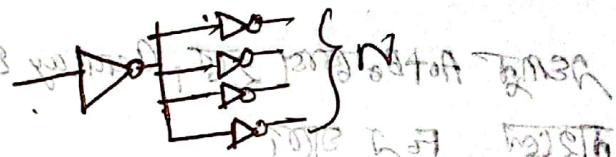
\*  $A, B = 0 \rightarrow$  diode on  $\rightarrow$



Design a NOT gate using MOSFET



Fan-Out: Number of gate inputs driven by the output of another single logic gate.



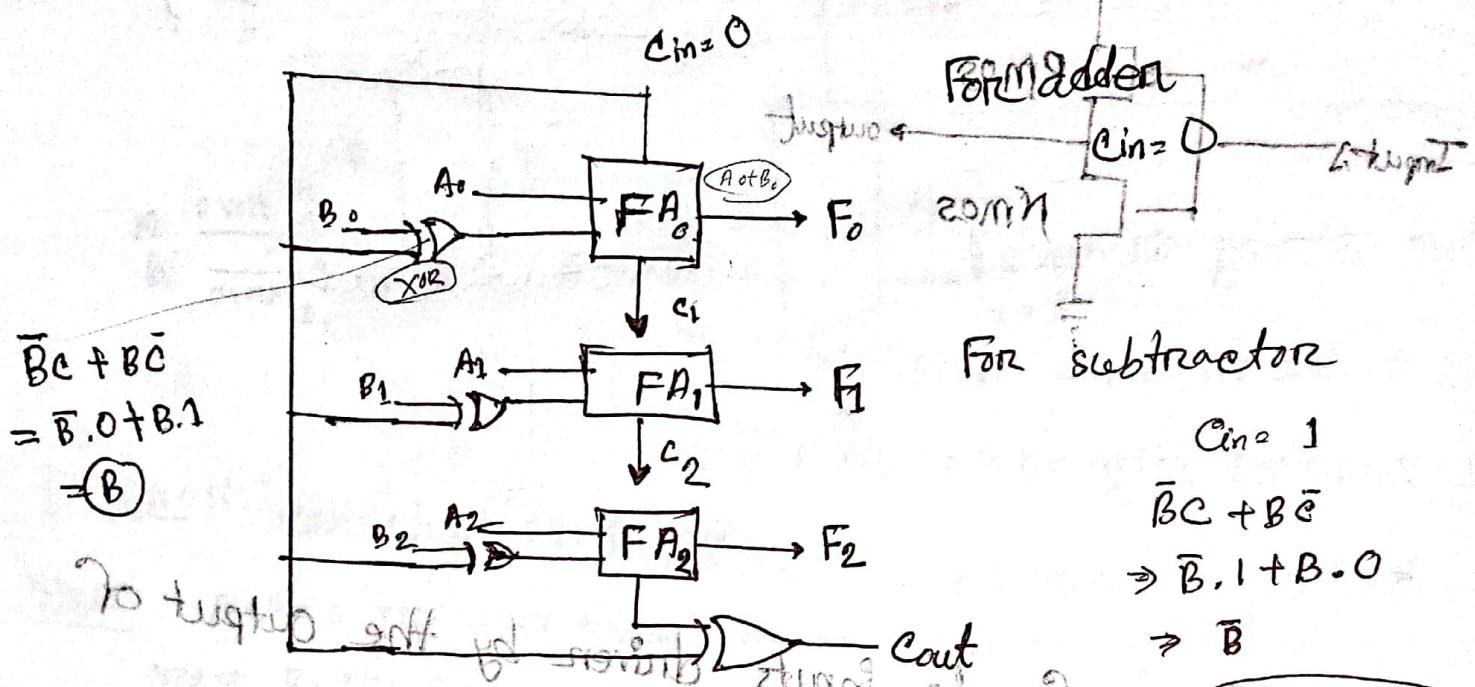
Fan-In: the number of inputs to the gate



Right input is a valid signal  
Left input is a valid signal  
Left input is a valid signal

73780M prior step TN  $\Rightarrow$  npisal

## 3 Bit adder-subtractor



যদি  $A + B_0$  কেবল ২'র, Carry এর পরামর্শ এবং

নতুনে  $F_0$  হাতে

\*  $A_1 + B_1$  কেবল ২'র, Carry এর পরামর্শ এবং  $F_1$  হাতে  
 Carry এর পরামর্শ এবং  $F_2$  হাতে

\* Subtractor (এখন  $B_0, B_1, B_2$  এর Input হাতে)

OPD Complement Result  $F_{ac}$

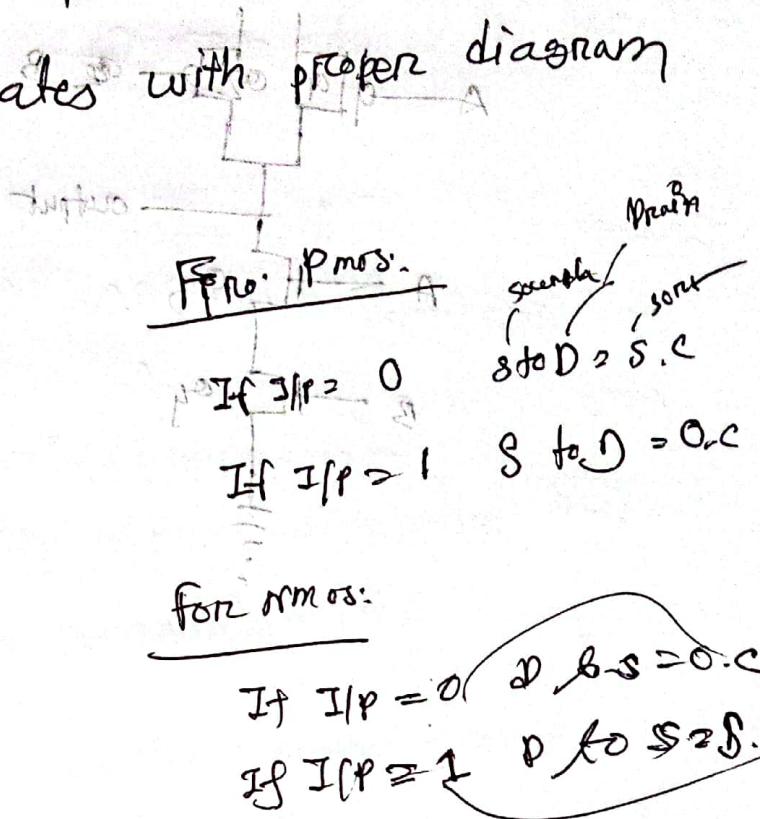
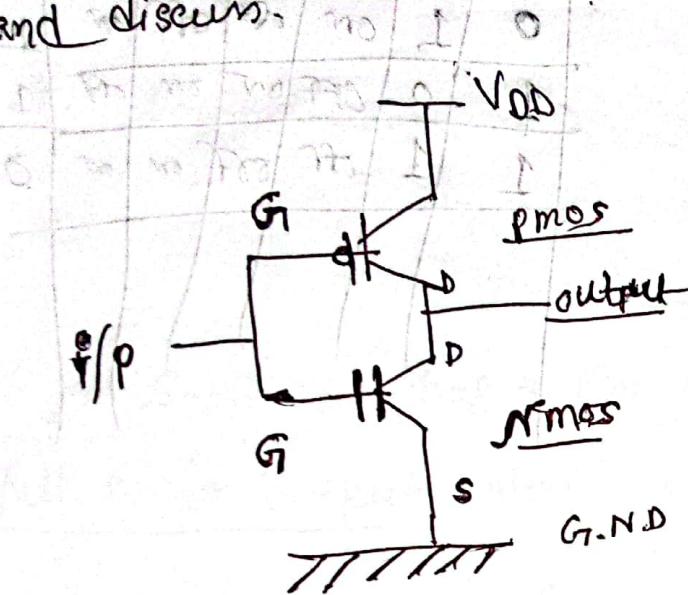
Assignments

\* TTL NAND gate circuit and its operations?

\* TTL, inverter, NAND, NOR gates?

\* 11. Inverters, NOR, NOR

\* CMOS inverters, NAND, NOR gates with proper diagram and discuss.



When Vin is loco

pmos with  $W_{ON}$

names "L" of

→ when  $m$  is high  
pmos — switch is off  
nmos — " " on

S.P.X

DAC Maths

1. Determined the resolution of (a) 6 bit DAC, (b) 12 bit DAC in terms of percentage.

$$(*) \text{ resolution} = \frac{1}{2^n-1} \times 100\% = \frac{1}{2^6-1} \times 100\% = 1.58\%$$

$$(*) \text{ resolution} = \frac{1}{2^{12}-1} \times 100\% = 0.0249\%$$

2. A 6-bit DAC has a step size of  $50\text{mV}$ . Determine the full scale output voltage and percentage

~~full scale output (F.S.O) = step size  $\times$  number of steps~~

~~full scale output =  $50\text{mV} \times (2^6-1)$~~

~~resolution =  $\frac{\text{step size}}{\text{full scale output}} = \frac{50\text{mV}}{3.15\text{V}} = 0.0158 \times 100\% = 1.58\%$~~

Ex-3 An 8-bit DAC produces  $V_{out} = 0.05\text{V}$  for a digital input of  $00000001$ . Find the full scale output. What is the resolution? What is  $V_{out}$  for an input of  $00101010$ ?

~~full scale output = step size  $\times$  number of steps~~

$$= 0.05 \times (2^8-1) = 12.75$$

~~Resolution =  $\frac{1}{2^n-1} = \frac{1}{2^8-1} \times 100\% = 0.391\%$~~ 

$$\text{Resolution} = \frac{\text{step size}}{\text{full scale}} = \frac{0.05}{12.75} = 3.91 \times 10^{-3}$$

V<sub>out</sub> for an ip of 00101010 =  $34.6842$   $32.842$   $\times 42$

V<sub>out</sub> = k<sub>v</sub> Digital input

DAC fid-2  $0.025 \times 42$   $\frac{1}{2}$  is multibit off by 2 bits so it is 2 times of previous

Ex-4  $\frac{V_{out}}{V_{ref}} = \frac{2^{n-1}}{2^n} = \frac{1}{2^n}$  a full scale output of  
A certain 6-bit DAC has a full scale output of  $\pm 0.5V$ . What is the  
amp and a full scale error off  $\pm 0.5V$ . What is the  
range of possible outputs for an input of 100000  
symmetric. V<sub>ref</sub> is 256 to 258 with a 6-bit DAC fid-2. If  
step size =  
step size =

last 6 bits  $\times 0.5V$  =  $0.2V$  with two steps left  
What is the Resolution in Volts of a 10-bit DAC

whose full scale output is 5V?

$$\frac{V_{out}}{V_{ref}} = \frac{1}{2^n}$$

Resolution =  $\frac{\text{Step size}}{\text{full scale output}}$

Two bits are not used = two steps left  
so resolution off by two bits =  $\frac{5V}{2^{10-2}} = 4.89mV$   
so resolution off by two bits =  $5mV$

01010100 to twos no. off two

$$\Delta F.SI = (1/2^n) \times 80.0 =$$

$$\Delta F.SI = \frac{1}{2^{10}} = \frac{1}{1024} = \text{micros}$$

$$\frac{2^n}{2^{n-1}} = \text{step size}$$

$$E_{F.SI} =$$

Q) An 8-bit DAC produces an output voltage of 2.0V for an input code of 01100100. What will the value of V<sub>out</sub> be for an input code of 10110011?

$$\Rightarrow V_1 = 2V \quad (01100100)_2 = (106)_{10} \text{ is the first 8 bits}$$

$$V_2 = ? \quad (10110011)_2 = (179)_{10}$$

$$\frac{2}{100} = \frac{V_2 - 4V_0}{179}$$

$$\frac{2.0}{1.0} = 2V_2 - 8V_0$$

$$\Rightarrow V_2 = \frac{179 \times 2}{100} = \frac{0.179}{0.001} = 3.58V_0$$

∴ 3.58 V<sub>0</sub> is the output voltage of the first 8 bits

Q) How many bits are required for a DAC so that its full scale output is 10mA and its resolution is less than 40 μA?

$$= \frac{f. 805}{\text{resolution}} = \text{bits}$$

$$\Rightarrow \text{bits} = \frac{10mA}{40 \mu A} = \frac{10 \times 10^{-3}}{40 \times 10^{-6}} = 250$$

6. An 8-bit DAC has a full-scale error of 0.2% F.S. If the DAC has a full-scale output of 10mA, what is the most that it can be in error for any digital input? If the DAC output reads 50mA for a digital input of 00000001 this within the specified range of accuracy?



$$\text{or } (\text{F.S.D}) = (11001101) \text{ V} = 8.5 \text{ V}$$

Full Scale error =  $0.2\% \times 10 \text{ mA}$

$$= 20 \text{ mA}$$

$$\text{Step-size} = \frac{\text{f.s.d}}{2^{n-1}}$$

$$= \frac{10}{255} \approx 39.2 \text{ mA}$$

Ideal output for  $00000001$  is  $39.2 \text{ mA}$

The possible range is  $(39.2 \text{ mA} \pm 20 \text{ mA})$  given with

$$[19.2 \text{ mA} \text{ to } 59.2 \text{ mA}]$$

Thus,  $50 \text{ mA}$  is within this range

④ Digital output  $\Rightarrow$  analog output  $\propto$  Resolution

$$\Rightarrow \text{Resolution} = \frac{\text{analog output}}{\text{Digital output}}$$

$$\star \text{ digital output} = \frac{6.005}{2.5 \times 10^6 \cdot 40 \times 10^{-3}} = 150.125 \approx 151.$$

8C      31

$$= \boxed{10010111}_2$$

$$\star \text{ digit} = \frac{6.035 \text{ V}}{40 \text{ mA}}$$

$$6.035 \rightarrow 10010111_2$$

time  $\rightarrow$  255

0      -255  
255      0

$$\text{Maximum conversion times} = (2^n - 1) \times t$$

$$= (2^8 - 1) \times \frac{1}{2.5 \times 10^6}$$

$$= 255 \times 4 \times 10^{-6} \text{ s} = 0.4 \text{ s}$$

$$\text{Average } a = \frac{102}{2} = 51 \text{ us} = \boxed{102 \text{ us}}$$