

Name: Mahfuza Khatun

ID : 2112376111

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Department : Computer Science and  
Engineering

Name of the experiment: DESIGN AND IMPLEMENTATION OF THE 4-BIT ADDER-SUBTRACTOR CIRCUIT USING DIGITAL IC-TRAINER,

Objectives:

- 1) To design and implement 4-bit Adder using IC 74LS283.
- 2) To Design and implement 4-bit Subtractor using IC 74LS283.

Theory:

The addition and subtraction operation can be combined into one circuit with one common binary adder. This is done by including an exclusive-OR gate with each full-adder. The mode input  $m$  controls the operation of the circuit, when  $m=0$ , the circuit is an adder and when  $m=1$ , the circuit becomes a subtractor.

Apparatus:

1. IC 74LS283, full adder
2. X-OR gate - 74LS86
3. Breadboard
4. Wires
5. Trainer board

## Truth Table:

Input Data A				Input Data B				Addition					Subtraction				
A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	C	S <sub>4</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	C	S <sub>4</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>
1	0	0	0	0	0	1	0	0	1	0	1	0	1	0	1	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	0	1	1	1	1
1	0	1	0	1	1	0	1	1	0	1	1	1	0	1	1	0	1

## Pin diagram:

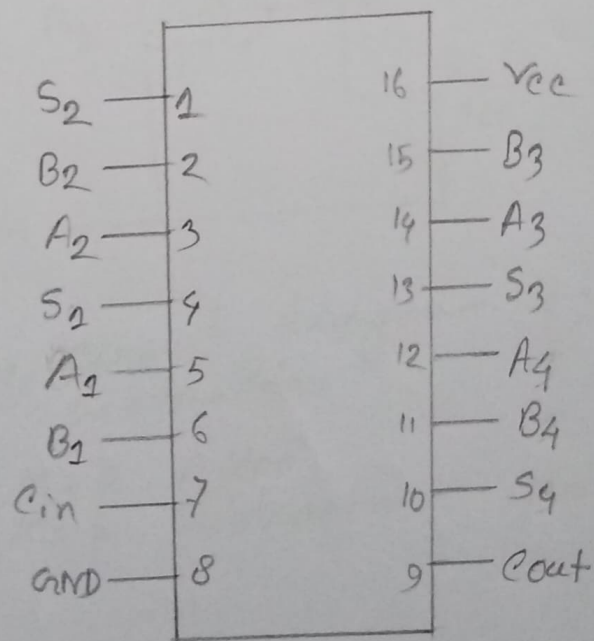


Fig: Pin Configuration of IC 74LS283



## Circuit Diagram:

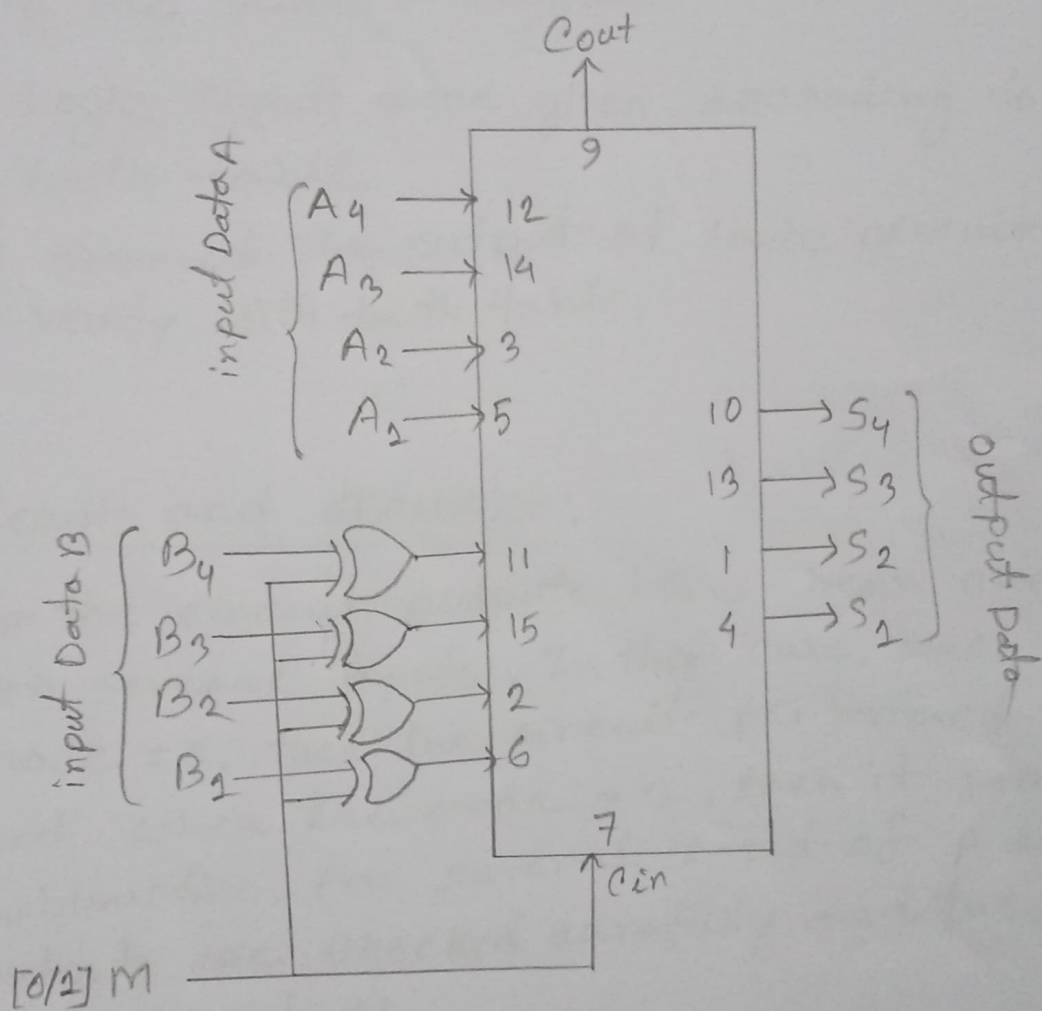


Fig: Circuit diagram of 4-bit Adder and Subtractor

when,  $M = 0$ , Adder  
 $M = 1$ , Subtractor

### Working procedure:

- ① implemented the circuit diagram according to the circuit diagram.
- ② Logic inputs were given according to the truth table.
- ③ observed the output of logic circuit and verify with truth table.

### Result and discussion:

For the circuit outputs have been checked for several inputs. In this case, when the mode = 0, then the circuit performed addition and when the mode = 1, then it performed subtraction. For several input of A and B outputs are checked carefully and the circuit worked perfectly.

### precautions:

- i) Check the power supply.
- ii) Check the vcc of all IC's
- iii) Check the ground of all IC's
- iv) The wires were connected carefully
- v) The circuit was powered on before it was completed.
- vi) The implementation was according to the circuit diagram.



Name of the experiment: DESIGN AND IMPLEMENTATION OF THE 4 bit - BCD ADDER USING DIGITAL IC-TRAINER.

Objectives:

1) To design and implement 4 bit BCD Adder using IC 74LS283.

Theory:

BCD adder is a circuit that performs the addition of two BCD numbers in parallel. BCD. BCD additions are performed in 4-bit binary form so there is a possibility of increasing binary number greater than 9 that results wrong output.

Initially in the BCD adders, four bit binary numbers are added using parallel binary adder and then, the binary output is checked to correct as BCD number. The correction logic generates the correction code based on the binary output values.

## Apparatus:

- i) Full adder IC 74LS283
- ii) AND gate IC (74LS08)
- iii) OR gate IC 74LS32
- iv) Bread board
- v) wires
- vi) Trainer Board

## Truth Table:

Binary Sum					BCD Sum					Decimal
K	Z <sub>4</sub>	Z <sub>3</sub>	Z <sub>2</sub>	Z <sub>1</sub>	C	S <sub>4</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	2
0	0	0	1	1	0	0	0	1	1	3
0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	1	0	0	1	0	1	5
0	0	1	1	0	0	0	1	1	0	6
0	0	1	1	1	0	0	1	1	1	7
0	1	0	0	0	0	1	0	0	0	8
0	1	0	0	1	0	1	0	0	1	9
0	1	0	1	0	1	0	0	0	0	10
0	1	0	1	1	1	0	0	0	1	11
0	1	1	0	0	1	0	0	1	0	12
0	1	1	0	1	1	0	0	1	1	13
0	1	1	1	0	1	0	1	0	0	14
0	1	1	1	1	1	0	1	0	1	15
1	0	0	0	0	1	0	1	1	0	16
1	0	0	0	1	1	0	1	1	1	17
1	0	0	1	0	1	1	0	0	0	18
1	0	0	1	1	1	1	0	0	1	19



## Pin Configuration:

$S_2$	1	16	$V_{CC}$
$B_2$	2	15	$B_3$
$A_2$	3	14	$A_3$
$S_1$	4	13	$S_3$
$A_1$	5	12	$A_4$
$B_1$	6	11	$B_4$
$C_{in}$	7	10	$S_4$
$C_{MD}$	8	9	$C_{out}$

Fig: Pin Configuration of IC 74LS283

## Circuit diagram:

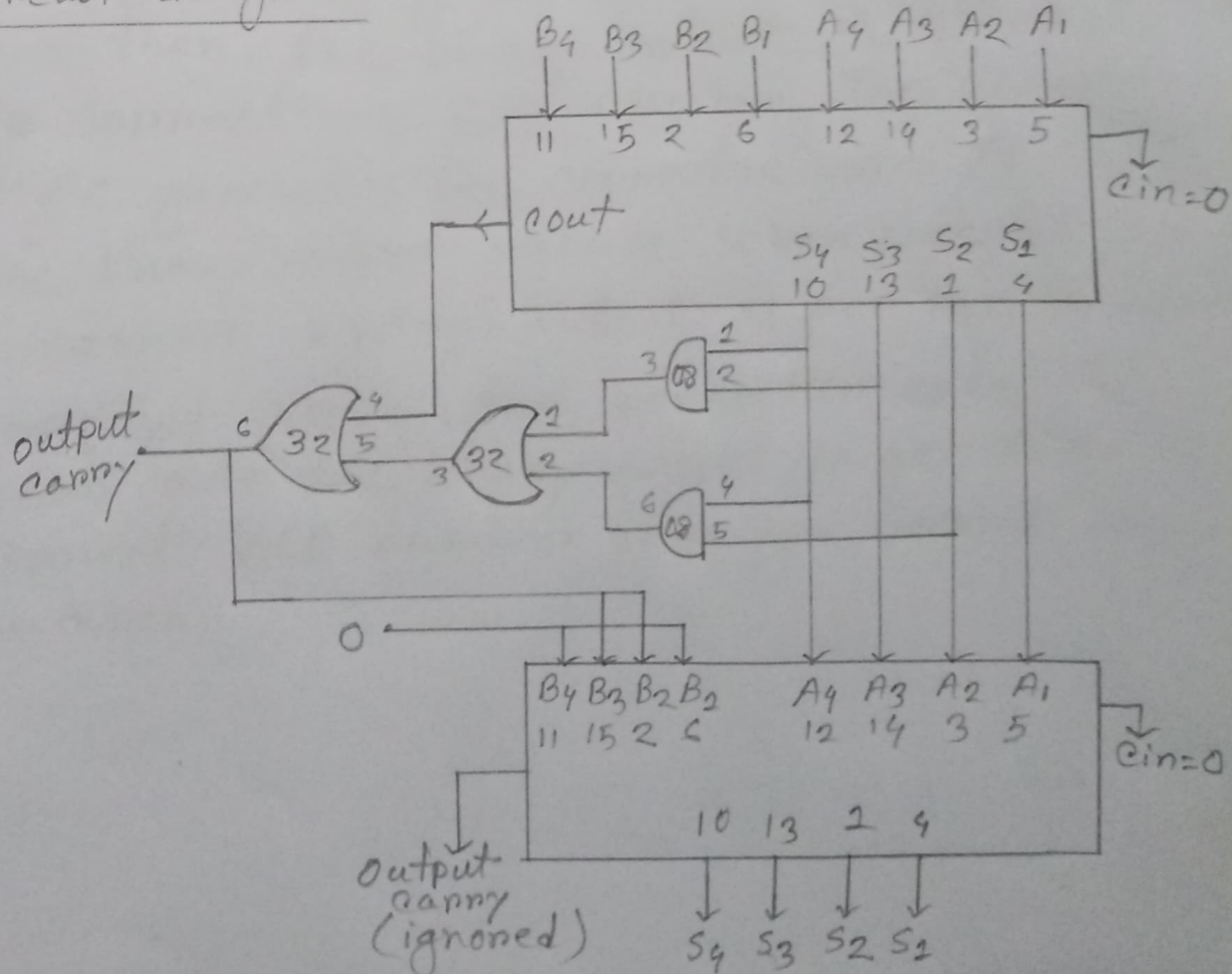


Fig: 4-bit BCD Adder using (74LS283 IC)

### Working procedure:

1. implemented the circuit diagram according to the circuit diagram.
2. Logic inputs were given according to the truth table.
3. observed the output of logic circuit and verify with truth table.

### Result and discussion:

BED adders, the four bit binary numbers are added using parallel binary adder and then, the binary output is checked to correct as BED number. The correction logic generates the correction code based on the binary output values. When we get the incorrect binary output as per the condition described above, the correction code is added with the binary output to get the correct BED number through second binary number.

### Precautions:

- i) Check the power supply.
- ii) Check the GND and VCC of all IC's
- iii) The wires were connected carefully
- iv) The circuit was powered on before it was completed.
- v) The implementation was according to the circuit diagram.