

Section A

1. (a) What are the advantages of encoding a decimal number in BCD as compared to straight binary? What is its disadvantage? 2
- (b) What range of decimal values can be represented by a four-digit octal number? 1.75
- (c) A typical PC uses a 20-bit address code for its memory locations- 3
- i) How many Hex digits are needed to represent a memory address?
  - ii) What is the range of addresses?
  - iii) What is the total number of memory locations?
- (d) Perform the subtractions  $(01001 - 11010)_2$  and  $(10010 - 10011)_2$  using 2's complement system. 2
2. (a) Draw the logic diagram and truth table of OR, NOR and XOR gate using NAND gate only. 3
- (b) Simplify the following Boolean expression 3
- i)  $X = ABC + A'BC + AC + AC'$
  - ii)  $A'B(D' + CD) + AB + A'BCD$
- (c) Which coding technique is good for error detection? Give example. Convert  $(10110)_2 = (?)_{\text{gray}}$ . 2.75
3. (a) Minimize the following function:  $f(a, b, c, d) = \sum a(1, 3, 4, 7, 11) + d(5, 12, 13, 14, 15)$  3
- (b) Define prime implicant with example. 1.75
- (c) Minimize the following function using Quine-McCluskey method. 4
- $$f(a, b, c, d) = \sum_m (0, 1, 2, 4, 6, 8, 12, 14)$$
4. (a) Define the following terms: i) Fan out ii) Noise margin 2.75
- (b) Draw and explain the circuit operation of 2 digit TTL NAND gate. 3
- (c) Design a two input CMOS NAND gate with necessary diagram and truth table. 3

Section B

5. (a) Write down some benefits of clocked flip-flop. Discuss the circuit diagram of the edge triggered SR flip-flop with timing diagram. 4
- (b) Mention some applications of Latch. 1.75
- (c) Briefly explain the operation of master-slave flip-flop using logic and timing diagram. 3
6. (a) Draw the internal functional diagram of a 555 timer and explain its basic operation. What are the applications of 555 timer? 4.75
- (b) Draw the pin configuration of a 555 timer IC and explain the function of each pin. 4
7. (a) Define resolution or step size of a D/A converter. For a DAC, if step size is 0.1 V, then what will be the output voltage for a digital input 0001. 2.75
- (b) What is the advantage of R/2R ladder DAC over weighted registers DAC? Draw and explain the basic operation of R/2R ladder DAC. 3
- (c) What is the main advantage of a SAC over digital ramp ADC? An 8-bit SAC has resolution of 20 mV. What will its digital output be for an analog input of 2.17 V? Illustrate with diagram. 3
8. Write short notes on the following (any three): 8.75
- (a) ECL NOR/OR gate
  - (b) Shift register
  - (c) Digital Ramp ADC
  - (d) 3 bit counter

University of Rajshahi  
 Department of Computer Science and Engineering  
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 Course: CSE1211 (Introduction to Digital Electronics)  
 Time: 3 Hrs. Full Marks: 52.5

[N.B. Answer SIX questions taking at least THREE from each Section.]

Section A

- |  |      |
|--|------|
| 1. (a) Perform subtraction using 2's complement method $(85-47)_{10}$ .  | 3    |
| (b) convert $(541.203)_6$ to base 5, base 8 and base 10.   | 3    |
| (c) Write the binary code for the gray code 10110111.  | 0.75 |
| (d) Represent the decimal number 28 to excess-3 and BCD code.  | 2    |
|  |      |
| 2. (a) Given the boolean function $K = AB + A'B' + B'C$<br>Then i) implement it with AND, OR and NOT gates<br>ii) implement it with only OR and NOT gates.         | 3    |
| (b) Show that the dual of the exclusive-OR is equal to its complement.<br>Simplify the following expression<br>$z = \bar{A}B\bar{C} + A\bar{B}\bar{C} + B\bar{C}D$ | 3.75 |
| (c) What are don't care terms? Explain with example.   | 2    |
|  |      |
| 3. (a) What is parity bit? Design 3-bit odd parity generator and checker.  | 6    |
| (b) Implement a full adder using two half adder.   | 2.75 |
|  |      |
| 4. (a) Design a logic circuit whose output is HIGH only when a majority of inputs A, B and C are LOW.  | 2.75 |
| (b) Simplify the following Boolean function using K-map and realize with basic gates:<br>$F(A, B, C, D) = \sum m(1, 5, 6, 12, 13, 14) + \sum d(2, 4)$ .            | 6    |

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Section B

- |   |      |
|---|------|
| 5(a) Show the logic diagram of a clocked RS flipflop with four NAND gates.  | 3    |
| (b) With the help of timing diagram, explain the operation of positive edge triggered JK FF.                                | 3    |
| c) What are the advantages of a master-slave JK FF? Mention some limitations of SR FF.                                      | 2.75 |
|   |      |
| 6(a) What is the basic difference between latch and flip-flop?  | 1    |
| (b) Define setup time, propagation delay and hold time for flip-flop using proper timing diagram.                           | 2.75 |
| (c) Draw the circuit diagrams and discuss the operation of D flip-flop and T flip-flop.                                     | 5    |
|   |      |
| 7.(a) Draw the TTL NAND gate circuit and explain its operation.   | 3    |
| (b) What is current sourcing and current sinking action?  | 1.75 |
| (c) Draw and explain a CMOS NOR gate circuit.   | 4    |
|   |      |
| 8.(a) Discuss the operation of a 555 timer IC based monostable multi-vibrator.  | 3    |
| (b) A certain binary-weighted-input DAC has a binary input of 1101. If a HIGH = +3.0 V and a LOW = 0 V, what is $V_{out}$ ? | 1.75 |
| (c) Draw the block diagram of a successive-approximation ADC and discuss its basic operation with a flow-chart.             | 4    |

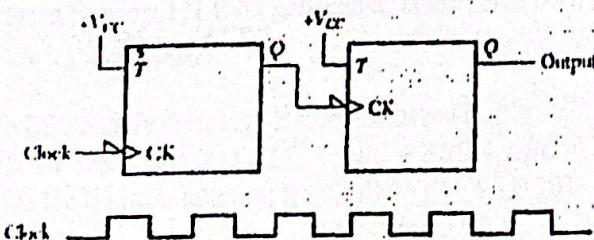
[N.B. Answer SIX questions taking at least THREE from each Section.]

### Section A

1. (a) Find  $(45)_{10} - (83)_{10}$  using two's complement format with 8-bit numbers. Then convert your result back to decimal. 3
1. (b) Add  $(65)_{10} + (72)_{10}$  using 8-bit sign-magnitude format for the numbers. Convert your result to decimal. Is your answer correct? Why or why not? 5
1. (c) Write the gray code for  $(1011)_2$ . 0.75
  
2. (a) Convert  $(1000\ 0110)_{BCD}$  to decimal, binary & octal. 3
2. (b) Simplify  $Z = A' C (A' B D)' + A' B C' D' + A B' C$  using Boolean algebra. 2.75
2. (c) State & prove De Morgan's theorems with the help of truth tables. 3
  
3. (a) Design and explain a full adder in detail with circuit diagram and truth table. 4
3. (b) Design a combinational logic circuit to compare two 2-bit binary numbers A and B and to generate the outputs  $A < B$ ,  $A = B$  and  $A > B$ . Is there a way to derive the third output from the first two outputs? 4.75
  
4. (a) Simplify the following Boolean expression using Quine-McCluskey technique  
 $f(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$ . 6
4. (b) List out the advantages and disadvantages of Quine-Mc Cluskey Method. 2.75

### Section B

- 5.(a) What is latch and flip-flop? 2
- 5.(b) Explain the master slave S-R flip-flop with timing diagram in detail. 6.75
  
- 6.(a) Draw a circuit diagram of a J-K latch and explain its operation. 4
- 6.(b) Plot the output waveforms referenced to the clock signal assuming the initial contents of all FFs is Q = 0. Assume all FFs are edge triggered. 4.75



- 7.(a) State advantages and disadvantages of TTL. 2
- 7.(b) Draw the circuit diagram of DTL-NAND gate. 3
- 7.(c) Design a NOT gate using MOSFET. 3.75
  
- 8.(a) Draw the block diagram of a system to interface a computer to the analog world so that the computer can monitor and control a physical variable and explain the functions of each block. 4
- 8.(b) What do you mean by resolution and accuracy for a DAC? 1.75
- 8.(c) Draw the block diagram of an ADC and discuss its basic operation. 3

Part A

1. (a) Do the following conversions: 4  
 i)  $(378)_{10}$  to 16 bit binary number;  
 ii)  $(1010110.1100)_2 = (?)_{10}$ ;  
 iii)  $(10101100)_2 = (?)_8$ ;  
 iv)  $(743)_{16} = (?)_2$ .
- (b) Compare between BCD and Binary code. 2  
 (c) What is Gray code? Explain with examples, how do you convert binary to Gray and Gray to binary? 2.75
2. (a) Subtract  $(100111)_2$  from  $(001100)_2$  using 2's complement method. Why do you need 2's complement method? 2  
 (b) Apply the input waveforms of fig-1 to a NOR gate, and draw the output waveform. Then repeat the output waveform with C hold permanently LOW. 2

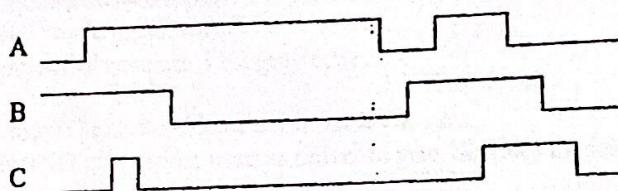


Fig-1

- (c) Determine the truth table for the circuit of fig-2. 2

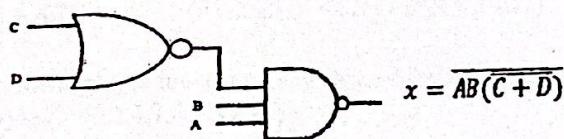


Fig-2

- (d) Show that a two-input NAND gate can be constructed from two-input NOR gate. Simplify the following:  $(A + B)(\bar{A} + \bar{B})$  2.75
3. (a) What is DeMorgan's theorem? Explain with truth table. 2.75  
 (b) Simplify the expression  $x = \bar{A}\bar{B}\bar{C} + \bar{A}BC + ABC + A\bar{B}\bar{C} + A\bar{B}C$  using Boolean algebra. 2  
 (c) Minimize the Boolean function  $f(a,b,c,d) = \sum_M(1,4,6,8,10)$  4
4. (a) Simplify the following expression using K-map method  
 $f(A,B,C,D) = \sum_M(7,9,10,11,12,13,14,15)$  5
- (b) Design the circuit corresponding to the truth table shown in Table-1. 3.75

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table-1

Part B

- |  |      |
|--|------|
| 5. (a) Explain the clocked S-R flip-flop in detail.  | 6    |
| (b) Explain D type flip-flop.  | 2.75 |
| 6. (a) Draw the basic DTL gates to implement NAND gate. Explain its operation.   | 2    |
| (b) Discuss the characteristic of TTL gates. Explain the operation of open collector TTL gates.                          | 2.75 |
| (c) Where ECL is more suitable? Draw and explain ECL to implement OR and NOR gates.                                      | 4    |
| 7. (a) Define transducer, analog-to-digital converter (ADC) and digital-to-analog converter (DAC).                       | 3    |
| (b) Draw the basic R/2R ladder DAC of 4-bit and write the $V_{out}$ expression.  | 2    |
| (c) Assume the $V_{REF} = 5V$ for the 4-bit DAC. What are the resolution and full-scale output of this converter?        | 1.75 |
| (d) An 8-bit DAC has an output of 3.92 mA for an input of 01100010. What are the DAC's resolution and full-scale output? | 2    |
| 8. (a) What is timer? What are the different applications of timer?  | 3    |
| (b) Design an monostable multi-vibrator using 555 timer and explain its operation.                                       | 5.75 |

[N.B. Answer SIX questions taking THREE from each part]

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### Part-A

1. (a) Do the following conversions: 4
  - (i)  $(10101011.1101)_2 = (?)_{10}$
  - (ii)  $(20345.125)_{10} = (?)_2$
  - (iii)  $(80914.25)_{10} = (?)_8$
  - (iv)  $(3AE8F.2D)_{16} = (?)_8$
  - (v)  $(1011001110)_2 = (?)_4$
- (b) Add  $(110111)_2$  with  $(100111)_2$ . Subtract  $(100110)_2$  from  $(110011)_2$  using 2's complement method. 3
- (c) Represent  $(-17)_{10}$  in sign magnitude, 1's complement and 2's complement representation. 1.75
  
2. (a) Write the procedure to convert a binary code to gray code with example. 4
- (b) With the help of example explain excess-3 code. 3
- (c) Write the BCD code for  $(9248)_{10}$ . 0.75
- (d) How can you easily generate 3 bit gray code . 1
  
3. (a) Define and draw the truth table of a 3-input X-OR gate. 2.75
- (b) Show that NAND gate can be used as universal gate. Simplify the following using De-Morgan's theorem
 
$$\overline{(A + \overline{B})} \overline{(\overline{A} + B)}$$
- (c) Simplify the following Boolean expressions to a minimum number of literals: 3
  - (i)  $ABC + A'B + ABC' + AC$
  - (ii)  $A'B(D' + CD) + B(A + A'CD)$
  
4. Simplify the following logic function using Quine-McCluskey technique 8.75
 
$$f(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$$

### Part-B

5. (a) Write the difference between asynchronous and synchronous system. 1.75
- (b) Explain the operation of a positive-edge triggered SR flip-flop by timing diagram. 4
- (c) Discuss how an SR latch is converted into D-latch. 3
  
6. (a) Explain the operation of a JK flip-flop using timing diagram. 3.75
- (b) Mention the limitations of a JK flip-flop. 2
- (c) Describe how a D-latch operates differently from an edge-triggered D flip-flop. 3
  
7. (a) Discuss the operation of an 8-bit DAC using op-amp summing amplifier with binary weighted registers. 3
- (b) Define R/2R ladder DAC with basic circuit diagram. Write the benefits of R/2R circuit. 3
- (c) Briefly discuss the operation of the digital ramp ADC. 2.75
  
8. (a) Draw the block diagram of a 555 timer and explain about its each pin. 3
- (b) Design an astable multi-vibrator using 555 timer and explain its operation. 5.75