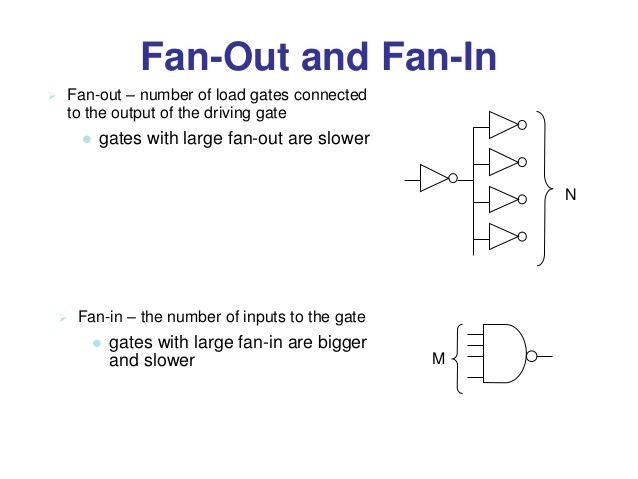
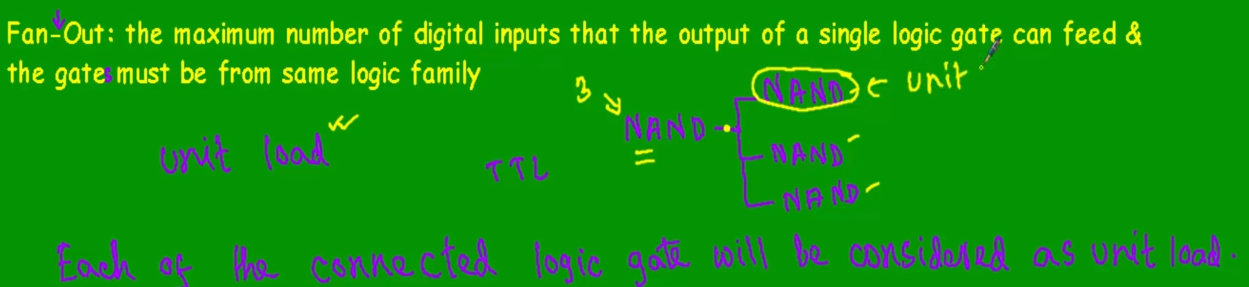
**Fan In and Fan Out**

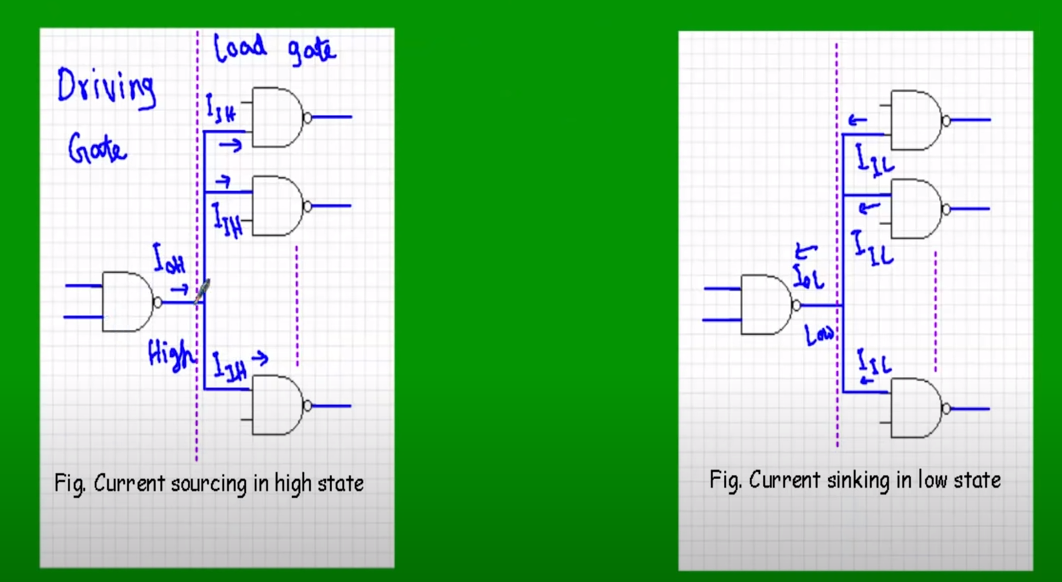
are characteristics of Digital ICs. Digital ICs are complete functioning logic networks. Typically, a Digital IC requires only a power supply, I/P (input) and O/P (output). Here are the definitions of Fan In and Fan Out.



**Fan In**: The fan-in defined as the maximum number of inputs that a logic gate can accept. If number of input exceeds, the output will be undefined or incorrect. It is specified by manufacturer and is provided in the data sheet.

**Fan Out**: The fan-out is defined as the maximum number of inputs (load) that can be connected to the output of a gate without degrading the normal operation. Fan Out is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of the connecting gate. It is specified by manufacturer and is provided in the data sheet. Exceeding the specified maximum load may cause a malfunction because the circuit will not be able supply the demanded power.

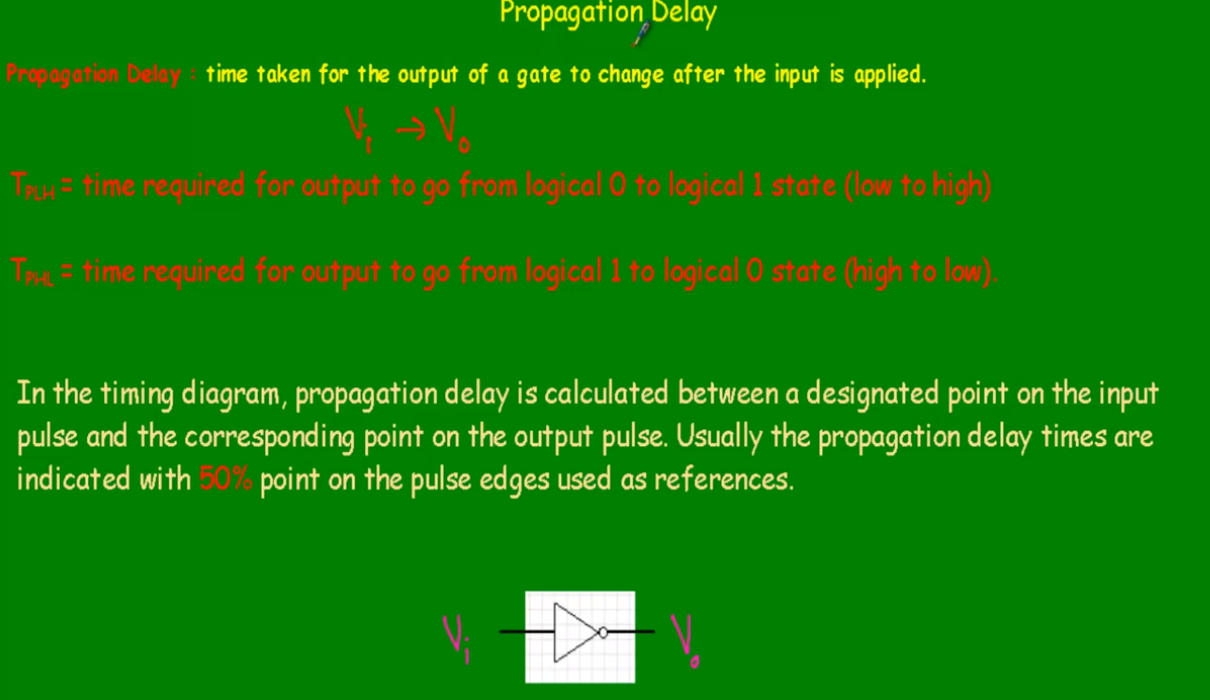


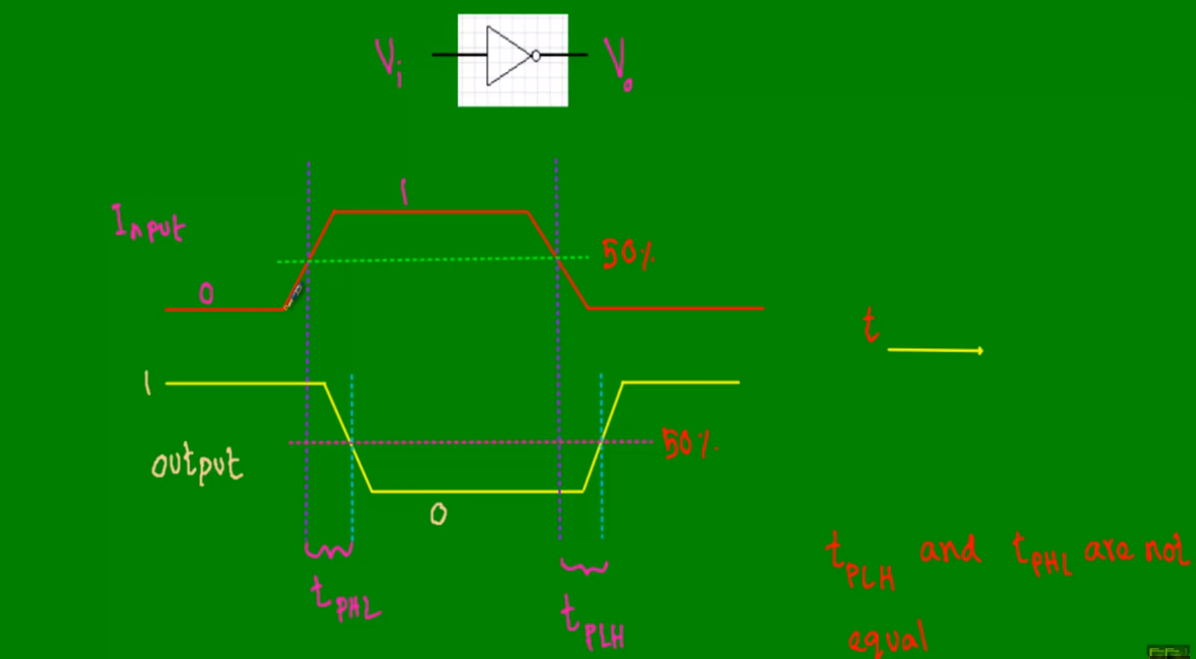


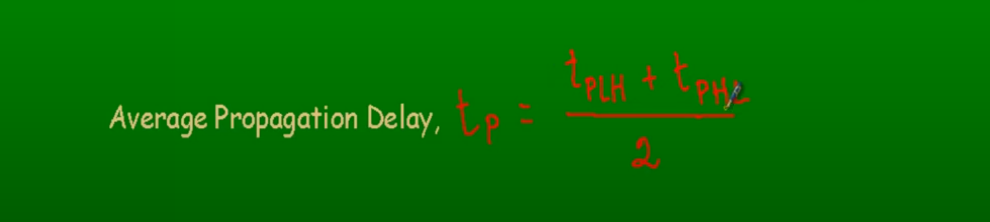


**Propagation Delays.** –

the delay before a change in the input is reflected in the output

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**Power Dissipation**

Power dissipation is the amount of heat (in mill watts) that the IC dissipates in the form of heat.

Each gate is connected to a power supply VCC (VDD in the case of CMOS). It draws a certain amount of current during its operation. Since each gate can be in a High, Transition or Low state, there are three different currents drawn from power supply.

· ICCH: Current drawn during HIGH state.

· ICCT: Current drawn during HIGH to LOW, LOW to HIGH transition.

· ICCL: Current drawn during LOW state.

For TTL, ICCT the transition current is negligible, in comparison to ICCH and ICCL. If we assume that ICCH and ICCL are equal then,

Average Power Dissipation = Vcc \* (ICCH + ICCL)/2

For CMOS, ICCH and ICCL current is negligible, in comparison to ICCT. So the Average power dissipation is calculated as below.

Average Power Dissipation = Vcc \* ICCT.

So for TTL like logics family, power dissipation does not depend on frequency of operation, and for CMOS the power dissipation depends on the operation frequency.

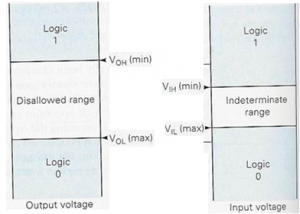
Power Dissipation is an important metric for two reasons. The amount of current and power available in a battery is nearly constant. Power dissipation of a circuit or system defines battery life: the greater the power dissipation, the shorter the battery life. Power dissipation is proportional to the heat generated by the chip or system; excessive heat dissipation may increase operating temperature and cause gate circuitry to drift out of its normal operating range; will cause gates to generate improper output values. Thus power dissipation of any gate implementation must be kept as low as possible.

Noise Margin

Definition: Ability of the gate to tolerate fluctuations of the voltage levels.The input and output voltage levels defined above point. Stray electric and magnetic fields may induce unwanted voltages, known as noise, on the connecting wires between logic circuits. This may cause the voltage at the input to a logic circuit to drop below VIH or rise above VIL and may produce undesired operation. The circuit's ability to tolerate noise signals is referred to as the noise immunity, a quantitative measure of which is called noise margin.  
The noise margins defined above are referred to as dc noise margins. Strictly speaking, the noise is generally thought of as an a.c. signal with amplitude and pulse width. For high speed ICs, a pulse width of a few microseconds is extremely long in comparison to the propagation delay time of the circuit and therefore, treated as d.c. as far as the response of the logic circuit is concerned. As the noise pulse width decreases and approaches the propagation delay time of the circuit, the pulse duration is too short for the circuit to respond. Under this condition, a large pulse amplitude would be required to produce a change in the circuit output. This means that a logic circuit can effectively tolerate a large noise amplitude if the noise is of a very short duration. This is referred to as ac noise margin and is substantially greater than the dc noise margin. It is generally supplied by the manufacturers in the form of a curve between noise margin and noise pulse width.

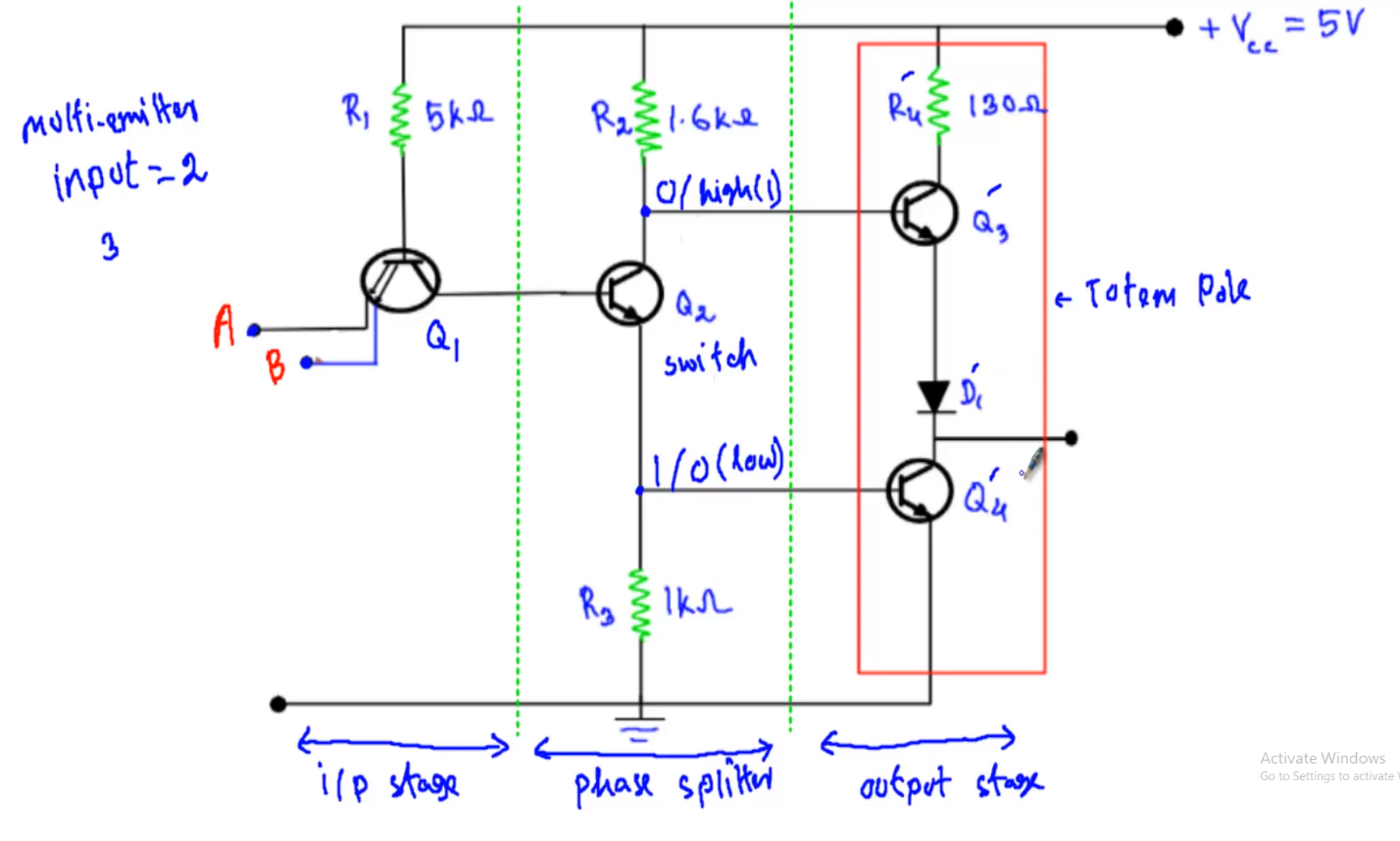
VNH = HIGH-state noise margin  
VNL = LOW-state noise margin  
VIL = LOW-state input voltage  
VIH = HIGH-state input voltage  
VOL = LOW-state output voltage  
VOH = HIGh-state output voltage  
Where,  
VNH = VOH -VIH  
VNL = VIL – VOL

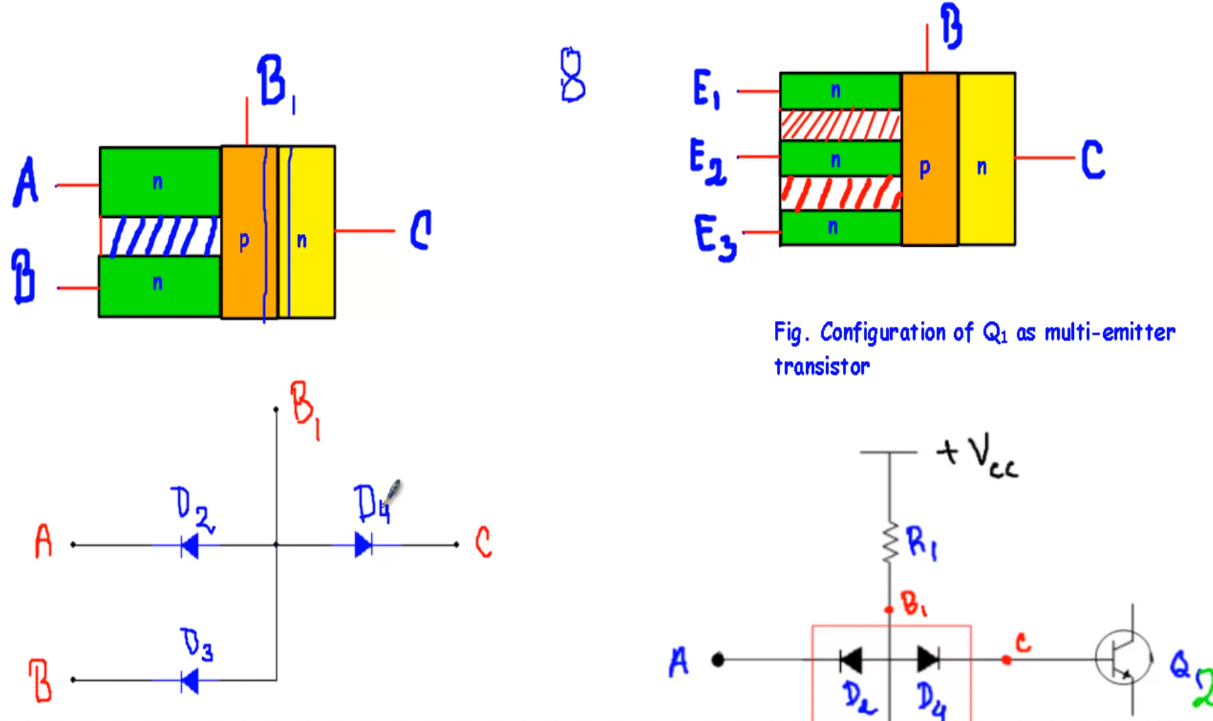
See below Figure to calculate noise margin

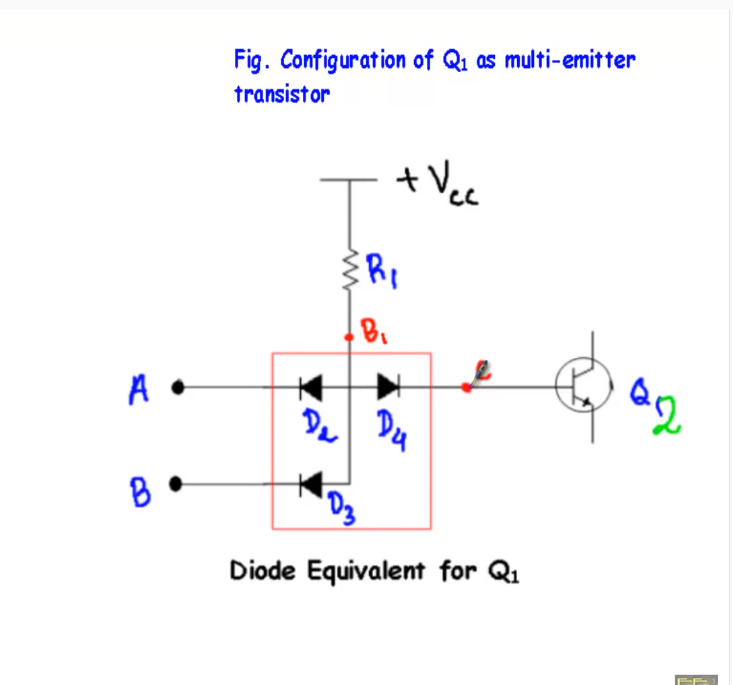
[](https://www.electronics-tutorial.net/wp-content/uploads/2015/09/logic4.png)

Manufacturers specify voltage limits to represent the logical 0 or 1. These limits are not the same at the input and output sides. For example, a particular gate A may output a voltage of 4.8V when it is supposed to output a HIGH but, at its input side, it can take a voltage of 3V as HIGH. In this way, if any noise should corrupt the signal, there is some margin for error.

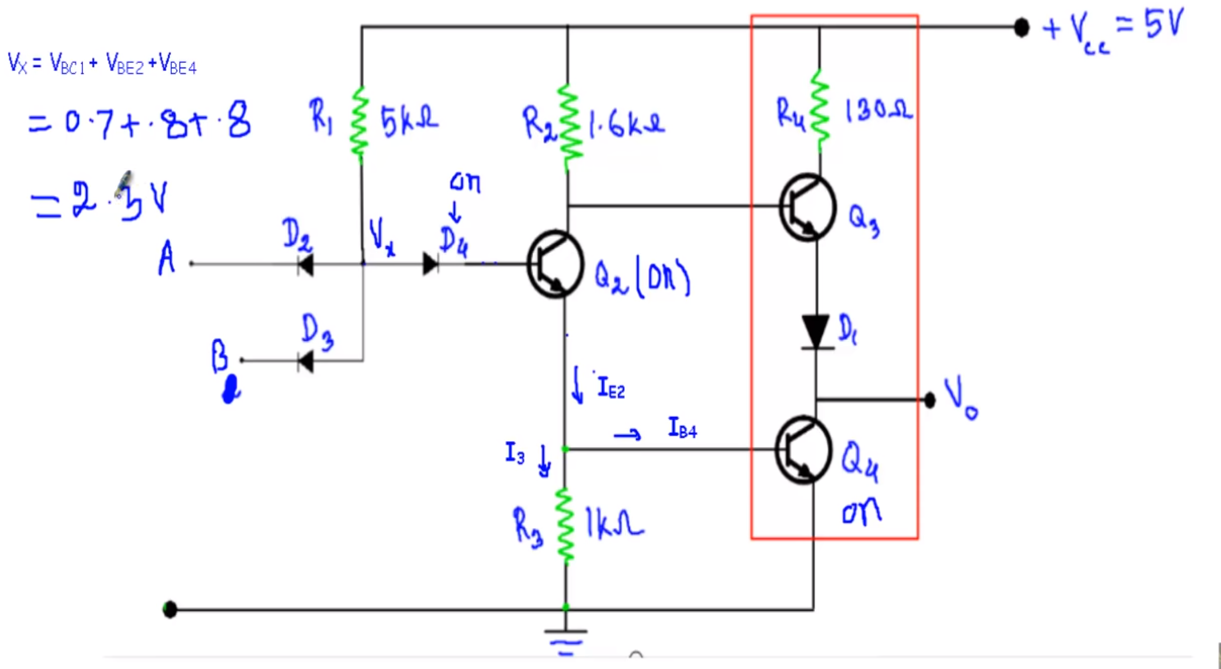
TTL NAND



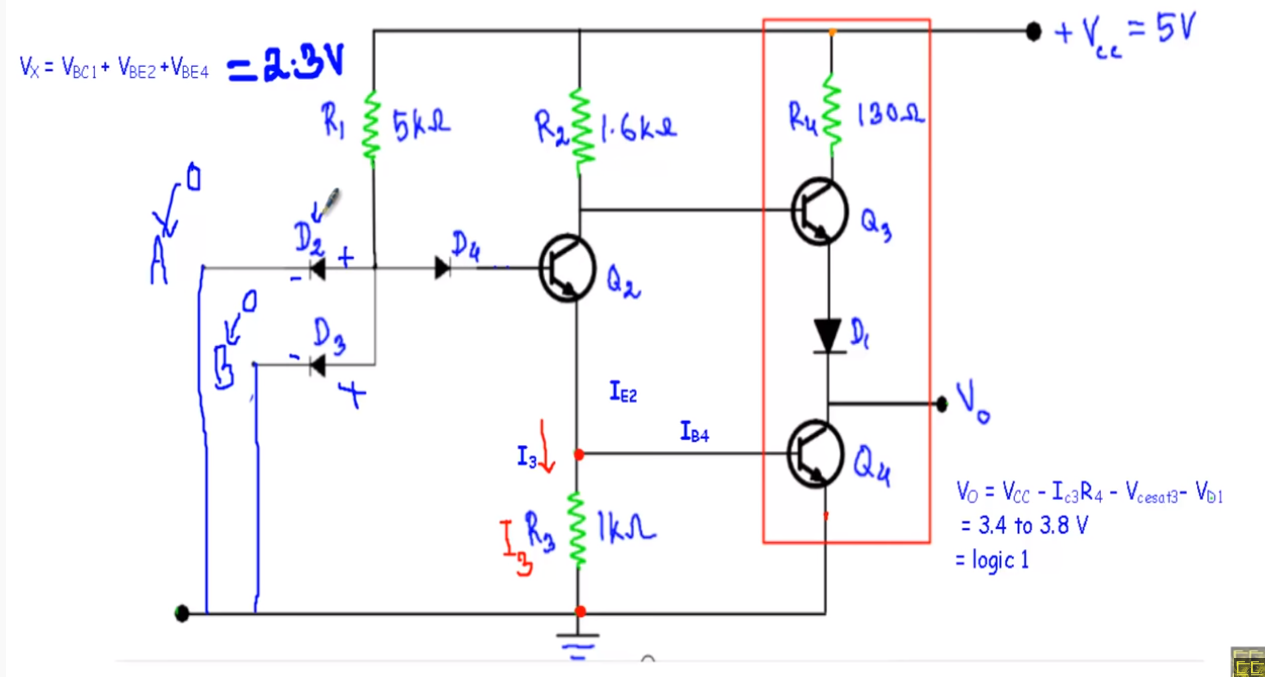


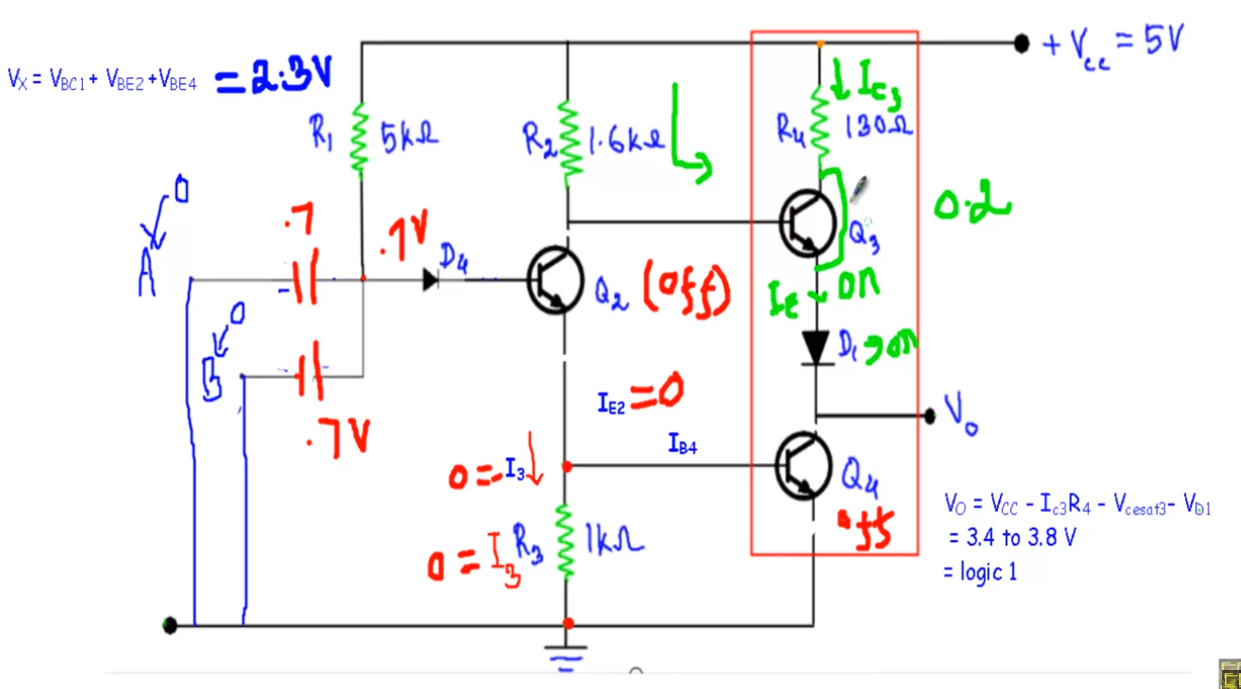


For Q2 ON

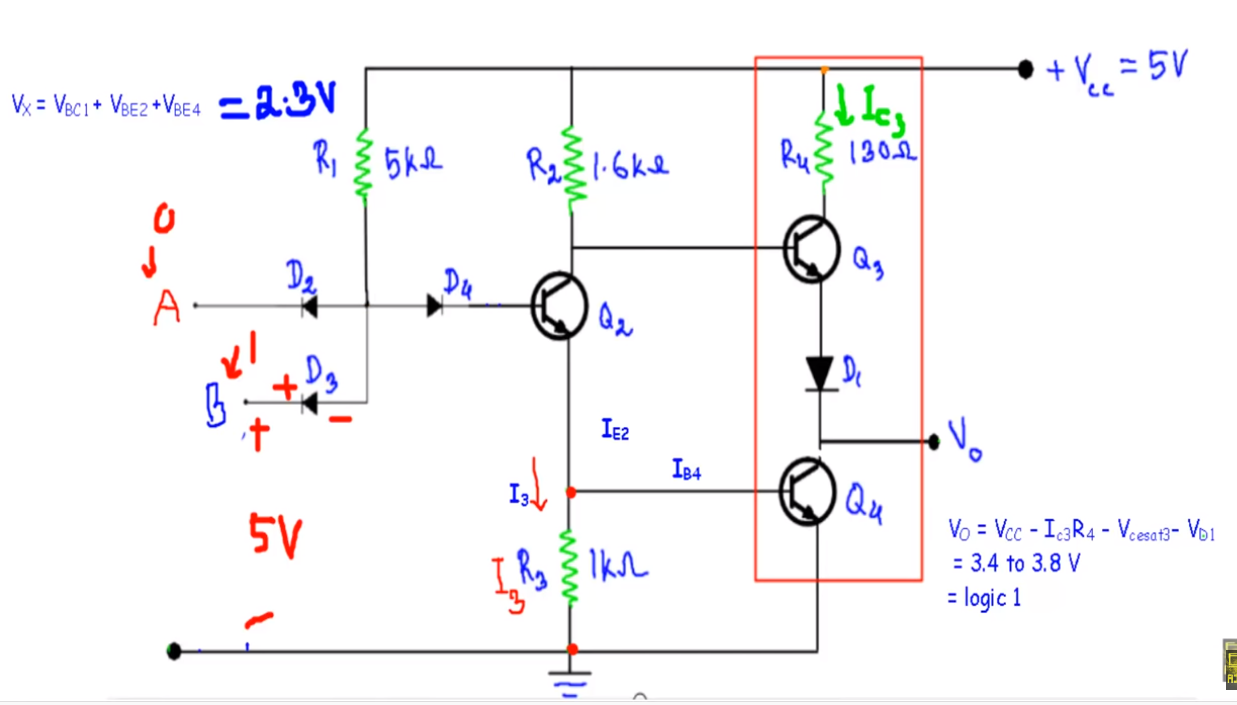


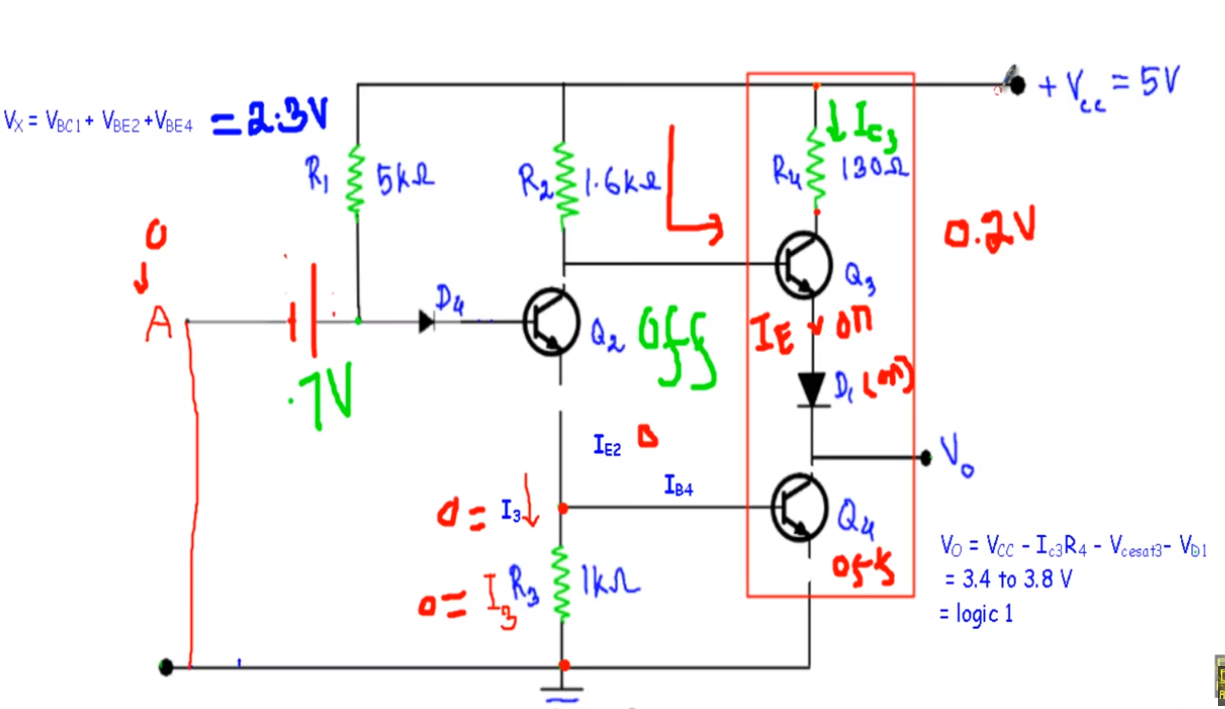
Input A=0, B=0



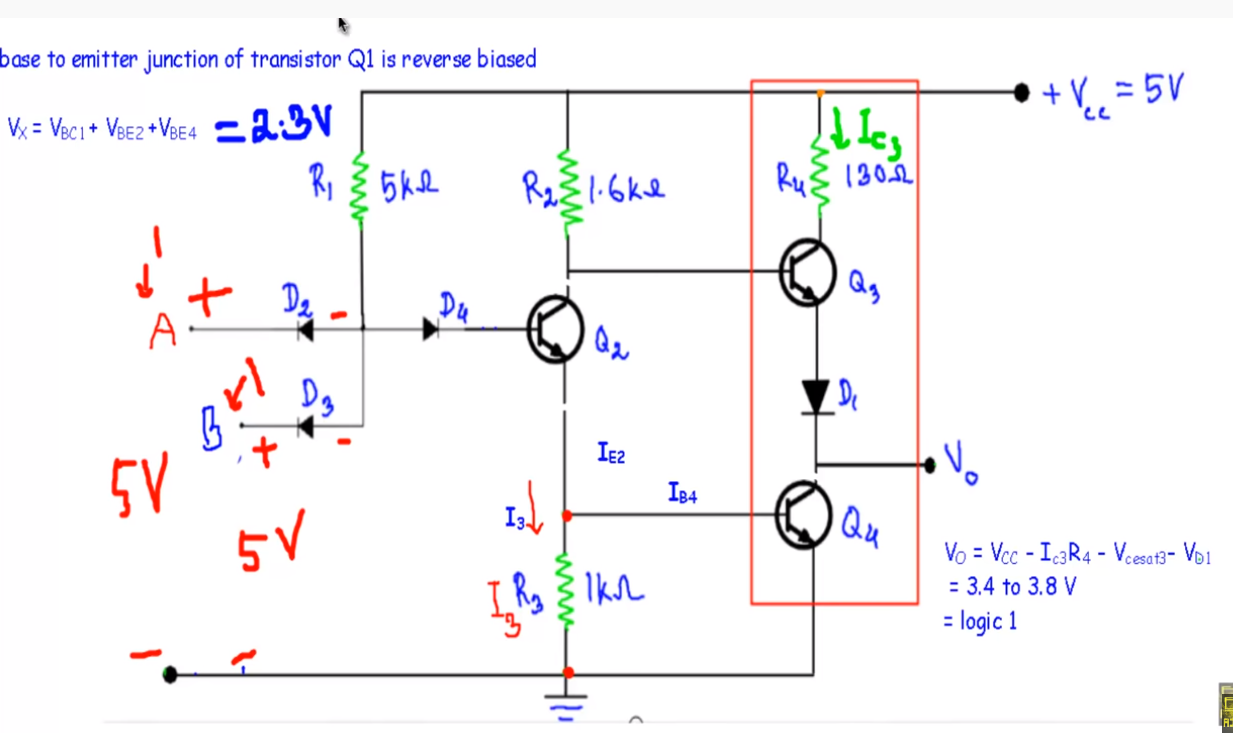


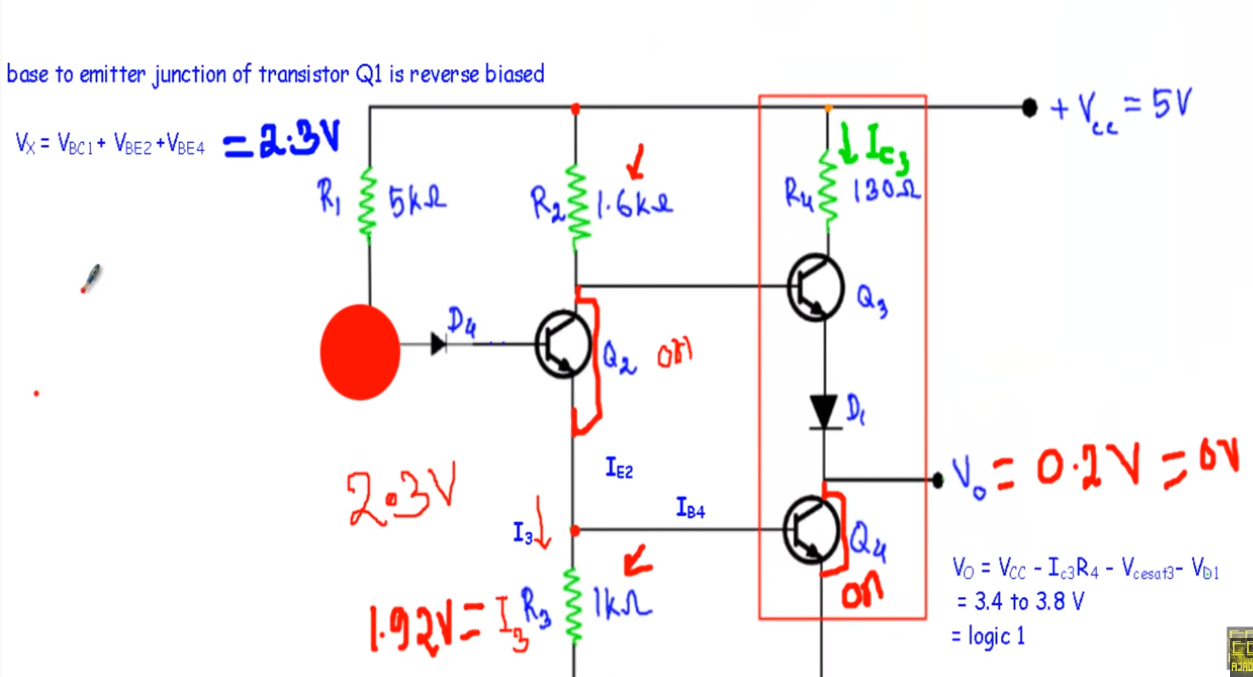
Input A=0, B=1

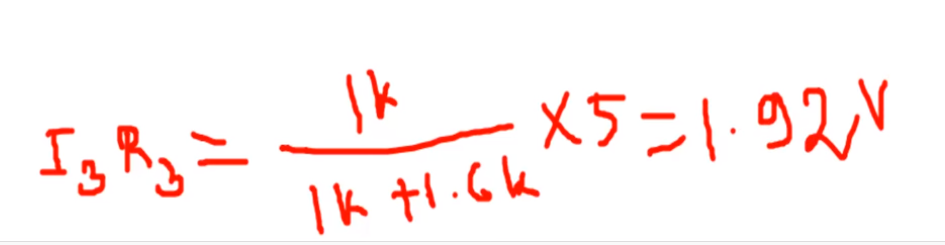




Input A=1, B=1







TTL NOR --- Study Home

DTL



