Assignment No: 7

- ***Title:*** **Synchronous counter**
- ***Objective:*** 3 Bit up/down synchronous Counter
- ***Problem Statement:*** To design and implement 3 bit UP and Down, Controlled UP/Down Synchronous Counter using MS-JK Flip-flop.
- **Hardware Requirement's :**

  Digital Trainer Kit, IC 7476, IC 7408, IC 7432 & IC 7404.patch cords, +5V power supply.

Theory:

Counters: counters are logical device or registers capable of counting the no of states or no of clock pulse arriving at its clock input where clock is a timing parameter arriving at regular intervals of time, so counters can be also used to measure time & frequencies. They are made up of flip flops. Where the pulse are counted to be made of it goes up step by step & the o/p of counter in the flip flop is decoded to read the count to its starting step after counting n pulse incase of module & counters.

- **Synchronous Counter:**

  In this counter, all the flip flops receive the external clock pulse simultaneously.

  Ex:- Ring counter & Johnson counter

  The gates propagation delay at reset time will not be present or we may say will not occur.

- **Classification of synchronous counter:**

  Depending on the way in which counting processes, the synchronous counter is classified is :-

  1) Up counter.
  2) Down counter.
  3) Up down counter.

  - **Up Counter:**

The up counter counts binary form 0 to7 i.e.(000 to 111).It counts from small to large number. It's O/P goes on increasing as they receive clock pulse

- **Down Counter:**

This down counter counts binary from 7-0 i.e.(111-000).It counts from large to small number. It's O/P goes on increasing as they receive clock pulse

- **Excitation Table**:- The tabular representation of the operation of flip flop (i.e: Operational Characteristic)

Present State	Next State	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

For M = 0, it acts as an Up counter and for M =1 as an Down counter.

State Table for 3 bit Up-Down Synchronous Counter:

Control input M	Present State			Next State			Input for Flip-flop					
	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	1
0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	1
0	1	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	1	1	0	X	0	1	X	X	1
0	1	1	0	1	1	1	X	0	X	0	1	X
0	1	1	1	0	0	0	X	1	X	1	X	1
1	0	0	0	1	1	1	1	X	1	X	X	1
1	0	0	1	0	0	0	0	X	0	X	1	X
1	0	1	0	0	0	1	0	X	X	1	X	1
1	0	1	1	0	1	0	0	X	X	0	1	X
1	1	0	0	0	1	1	X	1	1	X	X	1
1	1	0	1	1	0	0	X	0	0	X	1	X
1	1	1	0	1	0	1	X	0	X	1	X	1
1	1	1	1	1	1	0	X	0	X	0	1	X

K- map Simplification:

MQC \ QBQA	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

JA = 1

MQC \ QBQA	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

KA = 1

MQC \ QBQA	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	1	0	X	X
10	1	0	X	X

JB = M $\overline{QA}$ + $\overline{M}$ QA

MQC \ QBQA	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	0	1
10	X	X	0	1

KB = M $\overline{QA}$ + $\overline{M}$ QA

MQC \ QBQA	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	1	X	0	0

JC = M QA' QB ' + M' QA QB

MQC \ QBQA	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	1	0	0	0
10	X	X	X	X

KC = M QA' QB ' + M' QA QB

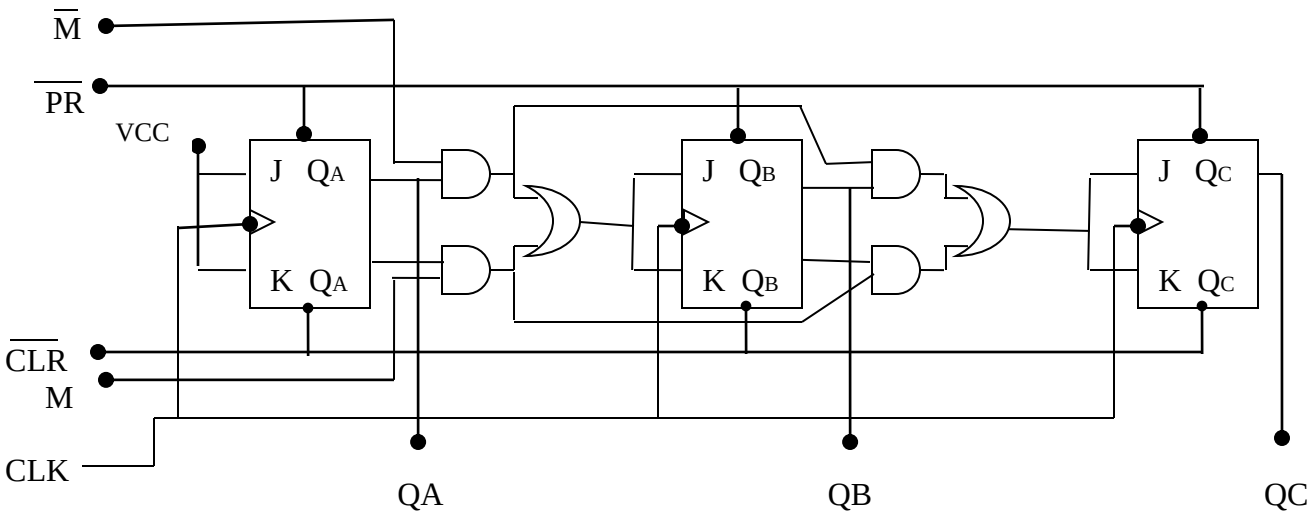

Fig : Logical Diagram of Up/ down counter using JK Flip Flop

Uses:

2) The synchronous counter is specially used as the counting devices.
3) They are also used as counter to count the no of clock pulses applied.
4) It also works for counting frequency & is used in frequency divider circuit.
5) It is used in digital voltmeter.
6) It is also used in counter type A to D converter.
7) It is also used for time measurement.
8) It is also used in digital triangular wave generator.
9) It helps in counting the no of product coming out from machinery where product is coming out at equal interval of time.

Outcome:

Up and down counters are successfully implemented, the counters are studied & o/p are checked. The truth table is verified.