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## Chapter 10

# Digital Integrated Circuits

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### 10.1 INTRODUCTION

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The integrated circuit (IC) and the digital logic families were introduced in Section 2.9. This chapter presents the electronic circuits in each IC digital logic family and analyzes their electrical operation. A basic knowledge of electrical circuits is assumed.

The IC digital logic families to be considered here are

RTL	Resistor–transistor logic
DTL	Diode–transistor logic
TTL	Transistor–transistor logic
ECL	Emitter-coupled logic
MOS	Metal-oxide semiconductor
CMOS	Complementary metal-oxide semiconductor

The first two, RTL and DTL, have only historical significance, since they are no longer used in the design of digital systems. RTL was the first commercial family to have been used extensively. It is included here because it represents a useful starting point for explaining the basic operation of digital gates. DTL circuits have been replaced by TTL. In fact, TTL is a modification of the DTL gate. The operation of the TTL gate will be easier to understand after the DTL gate is analyzed. TTL, ECL, and CMOS have a large number of SSI circuits, as well as MSI, LSI, and VLSI components.

The basic circuit in each IC digital logic family is a **NAND or NOR gate**. This basic circuit is the primary building block from which all other, more complex digital components are obtained. Each IC logic family has a data book that lists all the integrated circuits in that family. The differences in the logic functions available from each family are not so much in the functions that

they achieve as in the specific electrical characteristics of the basic gate from which the circuit is constructed.

NAND and NOR gates are usually defined by the Boolean functions that they implement in terms of binary variables. In analyzing them as electronic circuits, it is necessary to investigate their input–output relationships in terms of two voltage levels: a *high* level, designated by *H*, and a *low* level, designated by *L*. As mentioned in Section 2.8, the assignment of binary 1 to *H* results in a positive logic system and the assignment of binary 1 to *L* results in a negative logic system. The truth table, in terms of *H* and *L*, of a positive-logic NAND gate is shown in Fig. 10.1. We notice that the output of the gate is high as long as one or more inputs are low. The output is low only when both inputs are high. The behavior of a positive-logic NAND gate in terms of high and low signals can be stated as follows:

If *any* input of a NAND gate is low, the output is high.

If *all* inputs of a NAND gate are high, the output is low.

The corresponding truth table for a positive-logic NOR gate is shown in Fig. 10.2. The output of the NOR gate is low when one or more inputs are high. The output is high when both inputs are low. The behavior of a positive-logic NOR gate, in terms of high and low signals, can be stated as follows:

If *any* input of a NOR gate is high, the output is low.

If *all* inputs of a NOR gate are low, the output is high.

These statements for NAND and NOR gates must be remembered, because they will be used during the analysis of the electronic gates in this chapter.

Inputs		Output
<i>x</i>	<i>y</i>	<i>z</i>
<i>L</i>	<i>L</i>	<i>H</i>
<i>L</i>	<i>H</i>	<i>H</i>
<i>H</i>	<i>L</i>	<i>H</i>
<i>H</i>	<i>H</i>	<i>L</i>



**FIGURE 10.1**  
Positive-logic NAND gate

Inputs		Output
<i>x</i>	<i>y</i>	<i>z</i>
<i>L</i>	<i>L</i>	<i>H</i>
<i>L</i>	<i>H</i>	<i>L</i>
<i>H</i>	<i>L</i>	<i>L</i>
<i>H</i>	<i>H</i>	<i>L</i>



**FIGURE 10.2**  
Positive-logic NOR gate

A *bipolar junction transistor* (BJT) can be either an *npn* or a *pnp* junction transistor. In contrast, the *field-effect transistor* (FET) is said to be unipolar. The operation of a bipolar transistor depends on the flow of two types of carriers: electrons and holes. The operation of a unipolar transistor depends on the flow of only one type of majority carrier, which may be electrons (in an *n*-channel transistor) or holes (in a *p*-channel transistor). The first four digital logic families listed at the beginning of the chapter—RTL, DTL, TTL, and ECL—use bipolar transistors. The last two families—MOS and CMOS—employ a type of unipolar transistor called a metal-oxide-semiconductor field-effect transistor, abbreviated MOSFET, or MOS for short.

In this chapter, we first introduce the most common characteristics by which the digital logic families are compared. We then describe the properties of the bipolar transistor and analyze the basic gates in the bipolar logic families. Finally, we explain the operation of the MOS transistor and introduce the basic gates of its two logic families.

## 10.2 SPECIAL CHARACTERISTICS

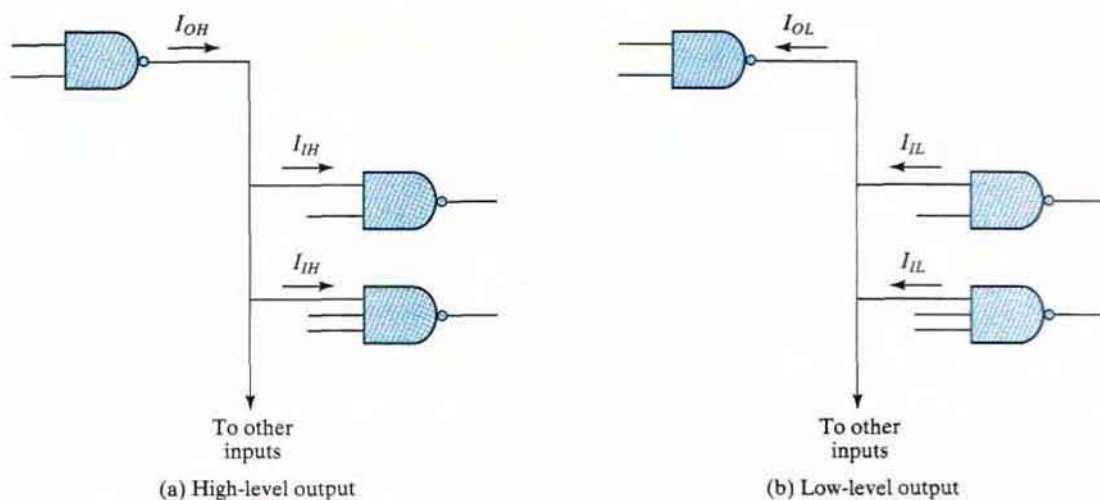
The characteristics of IC digital logic families are usually compared by analyzing the circuit of the basic gate in each family. The most important parameters that are evaluated and compared are fan-out, power dissipation, propagation delay, and noise margin. We first explain the properties of these parameters and then use them to compare the IC logic families.

### Fan-Out

The fan-out of a gate specifies the number of standard loads that can be connected to the output of the gate without degrading its normal operation. A standard load is usually defined as the amount of current needed by an input of another gate in the same logic family. Sometimes the term *loading* is used instead of fan-out. The term is derived from the fact that the output of a gate can supply a limited amount of current, above which it ceases to operate properly and is said to be *overloaded*. The output of a gate is usually connected to the inputs of other gates. Each input requires a certain amount of current from the gate output, so that each additional connection adds to the load of the gate. Loading rules are sometimes specified for a family of digital circuits. These rules give the maximum amount of loading allowed for each output of each circuit in the family. Exceeding the specified maximum load may cause a malfunction because the circuit cannot supply the power demanded of it by its loads. The fan-out is the maximum number of inputs that can be connected to the output of a gate and is expressed by a number.

The fan-out is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of a gate. Consider the connections shown in Fig. 10.3. The output of one gate is connected to one or more inputs of other gates. The output of the gate is in the high-voltage level in Fig. 10.3(a). It provides a current source  $I_{OH}$  to all the gate inputs connected to it. Each gate input requires a current  $I_{IH}$  for proper operation. Similarly, the output of the gate is in the low-voltage level in Fig. 10.3(b). It provides a current sink  $I_{OL}$  for all the gate inputs connected to it. Each gate input supplies a current  $I_{IL}$ . The fan-out of the gate





**FIGURE 10.3**  
Fan-out computation

is calculated from the ratio  $I_{OH}/I_{IH}$  or  $I_{OL}/I_{IL}$ , whichever is smaller. For example, the standard TTL gates have the following values for the currents:

$$I_{OH} = 400 \mu\text{A}$$

$$I_{IH} = 40 \mu\text{A}$$

$$I_{OL} = 16 \text{ mA}$$

$$I_{IL} = 1.6 \text{ mA}$$

The two ratios give the same number in this case:

$$\frac{400 \mu\text{A}}{40 \mu\text{A}} = \frac{16 \text{ mA}}{1.6 \text{ mA}} = 10$$

Therefore, the fan-out of standard TTL is 10. This means that the output of a TTL gate can be connected to no more than 10 inputs of other gates in the same logic family. Otherwise, the gate may not be able to drive or sink the amount of current needed from the inputs that are connected to it.

## Power Dissipation

Every electronic circuit requires a certain amount of power to operate. The power dissipation is a parameter expressed in milliwatts (mW) and represents the amount of power needed by the gate. The number that represents this parameter does not include the power delivered from another gate; rather, it represents the power delivered to the gate from the power supply. An IC with four gates will require, from its power supply, four times the power dissipated in each gate.

The amount of power that is dissipated in a gate is calculated from the supply voltage  $V_{CC}$  and the current  $I_{CC}$  that is drawn by the circuit. The power is the product  $V_{CC} \times I_{CC}$ . The current drain from the power supply depends on the logic state of the gate. The current drawn from the power supply when the output of the gate is in the high-voltage level is termed  $I_{CCH}$ . When the output is in the low-voltage level, the current is  $I_{CCL}$ . The average current is

$$I_{CC}(\text{avg}) = \frac{I_{CCH} + I_{CCL}}{2}$$

and is used to calculate the average power dissipation:

$$P_D(\text{avg}) = I_{CC}(\text{avg}) \times V_{CC}$$

For example, a standard TTL NAND gate uses a supply voltage  $V_{CC}$  of 5 V and has current drains  $I_{CCH} = 1$  mA and  $I_{CCL} = 3$  mA. The average current is  $(3 + 1)/2 = 2$  mA. The average power dissipation is  $5 \times 2 = 10$  mW. An IC that has four NAND gates dissipates a total of  $10 \times 4 = 40$  mW. In a typical digital system, there will be many ICs, and the power required by each one must be considered. The total power dissipation in the system is the sum total of the power dissipated in all the ICs.

## Propagation Delay

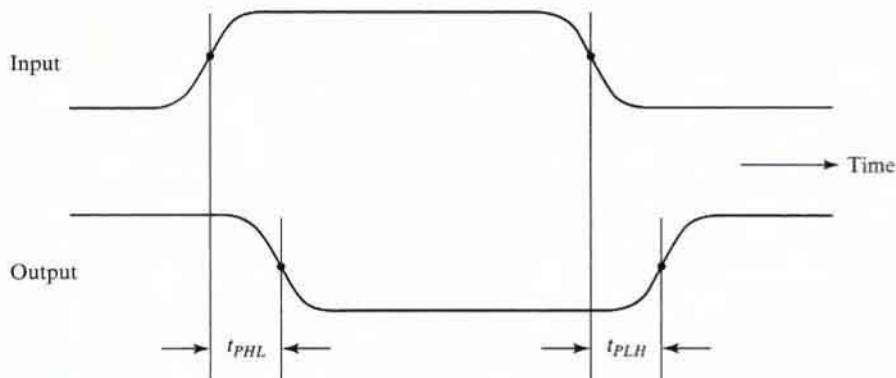
The *propagation delay* of a gate is the average transition-delay time for the signal to propagate from input to output when the binary input signal changes in value. The signals through a gate take a certain amount of time to propagate from the inputs to the output. This interval of time is defined as the propagation delay of the gate. Propagation delay is measured in nanoseconds (ns); 1 ns is equal to  $10^{-9}$  second.

The signals that travel from the inputs of a digital circuit to its outputs pass through a series of gates. The sum of the propagation delays through the gates is the total delay of the circuit. When speed of operation is important, each gate must have a short propagation delay and the digital circuit must have a minimum number of gates between inputs and outputs.

The average propagation delay time of a gate is calculated from the input and output waveforms, as shown in Fig. 10.4. The signal-delay time between the input and the output when the output changes from the high to the low level is referred to as  $t_{PHL}$ . Similarly, when the output goes from the low to the high level, the delay is  $t_{PLH}$ . It is customary to measure the time between the 50 percent point on the input and output transitions. In general, the two delays are not the same, and both will vary with loading conditions. The average propagation-delay time is calculated as the average of the two delays.

As an example, the delays for a standard TTL gate are  $t_{PHL} = 7$  ns and  $t_{PLH} = 11$  ns. These quantities are given in the TTL data book and are measured with a load resistance of 400 ohms and a load capacitance of 15 pF. The average propagation delay of the TTL gate is  $(11 + 7)/2 = 9$  ns.

Under certain conditions, it is more important to know the maximum delay time of a gate rather than the average value. The TTL data book lists the following maximum propagation delays for a standard NAND gate:  $t_{PHL} = 15$  ns and  $t_{PLH} = 22$  ns. When speed of operation is critical, it is necessary to take into account the maximum delay to ensure proper operation of the circuit.



**FIGURE 10.4**  
Measurement of propagation delay

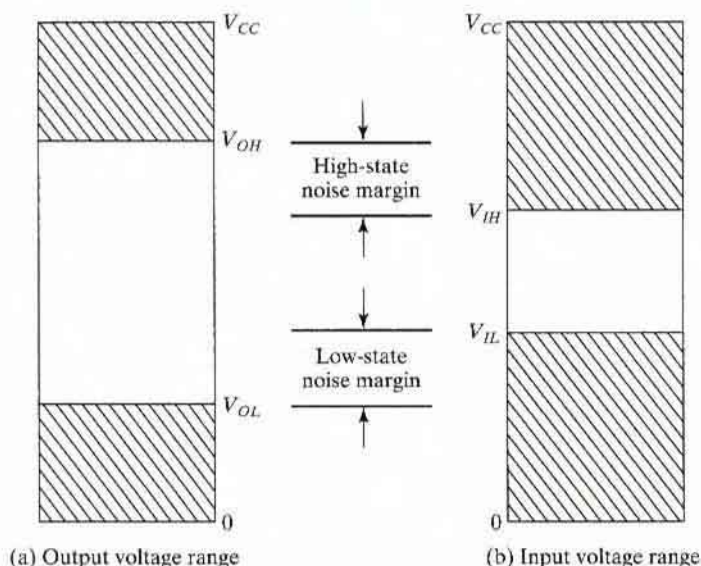
The input signals in most digital circuits are applied simultaneously to more than one gate. All the gates that are connected to external inputs constitute the first logic level of the circuit. Gates that receive at least one input from an output of a first-level gate are considered to be in the second logic level, and similarly for the third and higher logic levels. The total propagation delay of the circuit is equal to the propagation delay of a gate times the number of logic levels in the circuit. Thus, a reduction in the number of logic levels results in a reduction in signal delay and faster circuits. The reduction in the propagation delay in circuits may be more important than the reduction in the total number of gates if speed of operation is a major factor.

## Noise Margin

Spurious electrical signals from industrial and other sources can induce undesirable voltages on the connecting wires between logic circuits. These unwanted signals are referred to as *noise*. There are two types of noise. DC noise is caused by a drift in the voltage levels of a signal. AC noise is a random pulse that may be created by other switching signals. Thus, *noise* is a term used to denote an undesirable signal that is superimposed upon the normal operating signal. The *noise margin* is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit's output. The ability of circuits to operate reliably in an environment with noise is important in many applications. Noise margin is expressed in volts and represents the maximum noise signal that can be tolerated by the gate.

The noise margin is calculated from knowledge of the voltage signal available in the output of the gate and the voltage signal required in the input of the gate. Figure 10.5 illustrates the signals used in computing the noise margin. Part (a) shows the range of output voltages that can occur in a typical gate. Any voltage in the gate output between  $V_{CC}$  and  $V_{OH}$  is considered to be the high-level state, and any voltage between 0 and  $V_{OL}$  in the gate output is considered to be the low-level state. Voltages between  $V_{OL}$  and  $V_{OH}$  are indeterminate and do not appear





**FIGURE 10.5**  
Signals for evaluating noise margin

under normal operating conditions, except during transition between the two levels. The corresponding two voltage ranges that are recognized by the input of the gate are indicated in Fig. 10.5(b). In order to compensate for any noise signal, the circuit must be designed so that  $V_{IL}$  is greater than  $V_{OL}$  and  $V_{IH}$  is less than  $V_{OH}$ . The noise margin is the difference  $V_{OH} - V_{IH}$  or  $V_{IL} - V_{OL}$ , whichever is smaller.

As illustrated in Fig. 10.5,  $V_{OL}$  is the maximum voltage that the output can be in the low-level state. The circuit can tolerate any noise signal that is less than the noise margin ( $V_{IL} - V_{OL}$ ) because the input will recognize the signal as being in the low-level state. Any signal greater than  $V_{OL}$  plus the noise-margin figure will send the input voltage into the indeterminate range, which may cause an error in the output of the gate. In a similar fashion, a negative-voltage noise greater than  $V_{OH} - V_{IH}$  will send the input voltage into the indeterminate range.

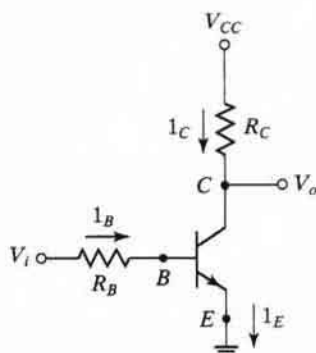
The parameters for the noise margin in a standard TTL NAND gate are  $V_{OH} = 2.4$  V,  $V_{OL} = 0.4$  V,  $V_{IH} = 2$  V, and  $V_{IL} = 0.8$  V. The high-state noise margin is  $2.4 - 2 = 0.4$  V, and the low-state noise margin is  $0.8 - 0.4 = 0.4$  V. In this case, both values are the same.

## 10.3 BIPOLAR-TRANSISTOR CHARACTERISTICS

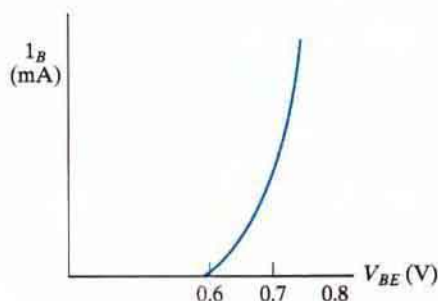
This section reviews the bipolar transistor as applied to digital circuits. The information presented will be used in the analysis of the basic circuit in the four bipolar logic families. As mentioned earlier, bipolar transistors may be of the *npn* or *pnp* type. Moreover, they are constructed either with germanium or silicon semiconductor material. Bipolar IC transistors, however, are made with silicon and are usually of the *npn* type.

The basic data needed in the analysis of digital circuits may be obtained by inspection of the typical characteristic curves of a common-emitter *npn* silicon transistor, shown in Fig. 10.6. The circuit in (a) is a simple inverter with two resistors and a transistor. The current marked  $I_C$  flows through resistor  $R_C$  and the collector of the transistor. Current  $I_B$  flows through resistor  $R_B$  and the base of the transistor. The emitter is connected to ground, and its current  $I_E = I_C + I_B$ . The supply voltage is between  $V_{CC}$  and ground. The input is between  $V_i$  and ground, and the output is between  $V_o$  and ground.

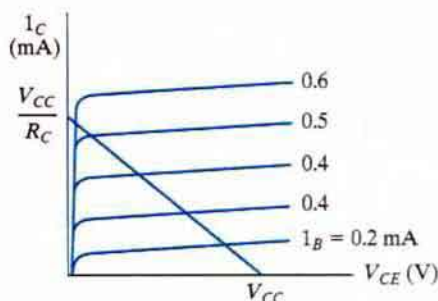
We have assumed positive directions for the currents as indicated. These are the directions in which the currents normally flow in an *npn* transistor. Collector and base currents ( $I_C$  and  $I_B$ , respectively) are positive when they flow into the transistor. Emitter current  $I_E$  is positive when it flows out of the transistor, as indicated by the arrow in the emitter terminal. The symbol  $V_{CE}$  stands for the voltage drop from collector to emitter and is always positive. Correspondingly,  $V_{BE}$  is the voltage drop across the base-to-emitter junction. This junction is forward biased when  $V_{BE}$  is positive and reverse biased when  $V_{BE}$  is negative.



(a) Common emitter inverter circuit



(b) Transistor-base characteristic



(c) Transistor-collector characteristic

**FIGURE 10.6**  
Silicon *npn* transistor characteristics



The base-emitter graphical characteristic is shown in Fig. 10.6(b), which is a plot of  $V_{BE}$  versus  $I_B$ . If the base-emitter voltage is less than 0.6 V, the transistor is said to be *cut off* and no base current flows. When the base-emitter junction is forward biased with a voltage greater than 0.6 V, the transistor conducts and  $I_B$  starts rising very fast whereas  $V_{BE}$  changes very little. The voltage  $V_{BE}$  across a conducting transistor seldom exceeds 0.8 V.

The graphical collector-emitter characteristics, together with the load line, are shown in Fig. 10.6(c). When  $V_{BE}$  is less than 0.6 V, the transistor is cut off with  $I_B = 0$ , and a negligible current flows in the collector. The collector-to-emitter circuit then behaves like an open circuit. With  $I_C = 0$  the drop across  $R_C$  is 0 and  $V_o = V_{CC}$ . The output is then said to be *pulled up*. In the *active* region, collector voltage  $V_{CE}$  may be anywhere from about 0.8 V up to  $V_{CC}$ . Collector current  $I_C$  in this region can be calculated to be approximately equal to  $I_B h_{FE}$ , where  $h_{FE}$  is a transistor parameter called the *dc current gain*. The maximum collector current depends not on  $I_B$ , but rather on the external circuit connected to the collector. This is because  $V_{CE}$  is always positive and its lowest possible value is 0 V. For example, in the inverter shown, the maximum  $I_C$  is obtained by making  $V_{CE} = 0$ , to obtain  $I_C = V_{CC}/R_C$ .

The parameter  $h_{FE}$  varies widely over the operating range of the transistor, but still, it is useful to employ an average value for the purpose of analysis. In a typical operating range,  $h_{FE}$  is about 50, but under certain conditions it could be as low as 20. It must be realized that the base current  $I_B$  may be increased to any desirable value, but the collector current  $I_C$  is limited by external circuit parameters. As a consequence, a situation can be reached in which  $h_{FE} I_B$  is greater than  $I_C$ . If this condition exists, then the transistor is said to be in the *saturation* region. Thus, the condition for saturation is determined from the relationship

$$I_B \geq \frac{I_{CS}}{h_{FE}}$$

where  $I_{CS}$  is the maximum collector current flowing during saturation.  $V_{CE}$  is not exactly zero in the saturation region, but is normally about 0.2 V. In this condition,  $V_o = V_{BE} = 0.2$  V and the output is said to be *pulled down*.

The basic data needed for analyzing bipolar-transistor digital circuits are listed in Table 10.1. In the cutoff region,  $V_{BE}$  is less than 0.6 V,  $V_{CE}$  is considered to be an open circuit, and both currents are negligible. In the active region,  $V_{BE}$  is about 0.7 V,  $V_{CE}$  may vary over a wide range, and  $I_C$  can be calculated as a function of  $I_B$ . In the saturation region,  $V_{BE}$  hardly changes, but  $V_{CE}$  drops to 0.2 V. The base current must be large enough to satisfy the inequality listed. To simplify the analysis, we will assume that  $V_{BE} = 0.7$  V if the transistor is conducting, whether in the active or saturation region.

**Table 10.1**  
*Typical npn Silicon Transistor Parameters*

Region	$V_{BE}$ (V)	$V_{CE}$ (V)	Current Relationship
Cutoff	<0.6	Open circuit	$I_B = I_C = 0$
Active	0.6–0.7	>0.8	$I_C = h_{FE} I_B$
Saturation	0.7–0.8	0.2	$I_B \geq I_{CS}/h_{FE}$

Digital circuits may be analyzed by means of the following prescribed procedure: For each transistor in the circuit, determine whether its  $V_{BE}$  is less than 0.6 V. If so, then the transistor is cut off and the collector-to-emitter circuit is considered an open circuit. If  $V_{BE}$  is greater than 0.6 V, the transistor may be in the active or saturation region. Calculate the base current, assuming that  $V_{BE} = 0.7$  V. Next, calculate the maximum possible value of collector current  $I_{CS}$ , assuming that  $V_{CE} = 0.2$  V. These calculations will be in terms of voltages applied and resistor values. Then, if the base current is large enough that  $I_B \geq I_{CS}/h_{FE}$ , we infer that the transistor is in the saturation region with  $V_{CE} = 0.2$  V. However, if the base current is smaller and the preceding relationship is not satisfied, the transistor is in the active region and we recalculate collector current  $I_C$ , using the equation  $I_C = h_{FE}I_B$ .

To demonstrate with an example, consider the inverter circuit of Fig. 10.6(a) with the following parameters:

$$\begin{aligned} R_C &= 1 \text{ k}\Omega & V_{CC} &= 5 \text{ V (voltage supply)} \\ R_B &= 22 \text{ k}\Omega & H &= 5 \text{ V (high-level voltage)} \\ h_{FE} &= 50 & L &= 0.2 \text{ V (low-level voltage)} \end{aligned}$$

With input voltage  $V_i = L = 0.2$  V, we have  $V_{BE} < 0.6$  V and the transistor is cut off. The collector-emitter circuit behaves like an open circuit, so output voltage  $V_o = 5 \text{ V} = H$ .

With input voltage  $V_i = H = 5$  V, we infer that  $V_{BE} > 0.6$  V. Assuming that  $V_{BE} = 0.7$ , we calculate the base current:

$$I_B = \frac{V_i - V_{BE}}{R_B} = \frac{5 - 0.7}{22 \text{ k}\Omega} = 0.195 \text{ mA}$$

The maximum collector current, assuming that  $V_{CE} = 0.2$  V, is

$$I_{CS} = \frac{V_{CC} - V_{CE}}{R_C} = \frac{5 - 0.2}{1 \text{ k}\Omega} = 4.8 \text{ mA}$$

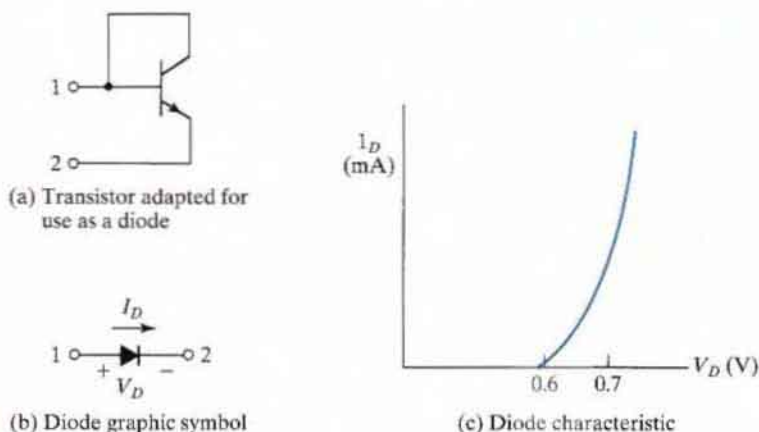
We then check for saturation, using the condition

$$0.195 = I_B \geq \frac{I_{CS}}{h_{FE}} = \frac{4.8}{50} = 0.096 \text{ mA}$$

whereupon we find that the inequality is satisfied, since  $0.195 > 0.096$ . We conclude that the transistor is saturated and output voltage  $V_o = V_{CE} = 0.2 \text{ V} = L$ . Thus, the circuit behaves as an inverter.

The procedure just described will be used extensively during the analysis of the circuits in the sections that follow. We will perform a *qualitative* analysis—that is, an analysis that does not involve the specific numerical equations. A *quantitative* analysis and specific calculations will be left as exercises in the “Problems” section at the end of the chapter.

There are occasions when not only transistors, but also diodes, are used in digital circuits. An IC diode is usually constructed from a transistor with its collector connected to the base, as shown in Fig. 10.7(a). The graphic symbol employed for a diode is shown in Fig. 10.7(b). The diode behaves essentially like the base-emitter junction of a transistor. Its graphical



**FIGURE 10.7**  
Silicon diode symbol and characteristic

characteristic, shown in Fig. 10.7(c), is similar to the base-emitter characteristic of a transistor. We can then conclude that a diode is off and nonconducting when its forward voltage  $V_D$  is less than 0.6 V. When the diode conducts, current  $I_D$  flows in the direction shown in Fig. 10.7(b) and  $V_D$  stays at about 0.7 V. One must always provide an external resistor to limit the current in a conducting diode, since its voltage remains fairly constant at a fraction of a volt.

## 10.4 RTL AND DTL CIRCUITS

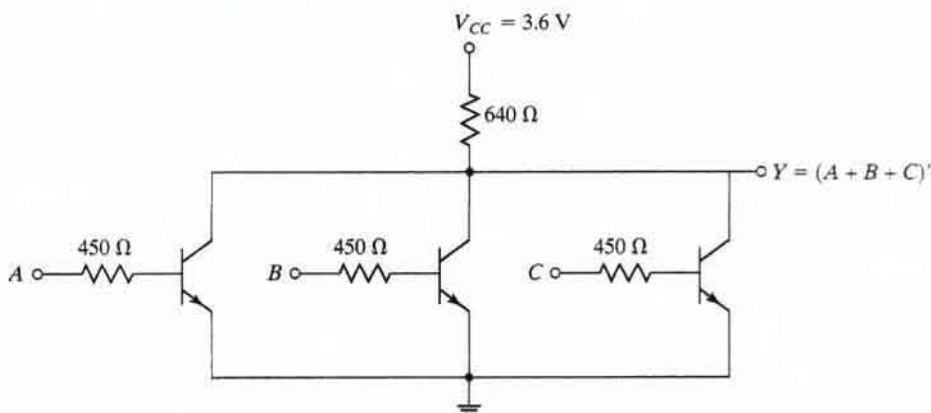
### RTL Basic Gate

The basic circuit of the RTL digital logic family is the NOR gate shown in Fig. 10.8. Each input is associated with one resistor and one transistor. The collectors of the transistors are tied together at the output. The voltage levels for the circuit are 0.2 V for the low level and from 1 to 3.6 V for the high level.

The analysis of the RTL gate is simple and follows the procedure outlined in the previous section. If any input of the RTL gate is high, the corresponding transistor is driven into saturation and the output goes low, regardless of the states of the other transistors. If all inputs are low at 0.2 V, all transistors are cut off because  $V_{BE} < 0.6$  V and the output of the circuit goes high, approaching the value of the supply voltage  $V_{CC}$ . This confirms the conditions stated in Fig. 10.2 for the NOR gate. Note that the noise margin for low signal input is  $0.6 - 0.2 = 0.4$  V.

The fan-out of the RTL gate is limited by a high output voltage. As the output is loaded with inputs of other gates, more current is consumed by the load. This current must flow through the 640- $\Omega$  resistor. A simple calculation (see Problem 10.2) shows that if  $h_{FE}$  drops to 20, the output voltage drops to about 1 V when the fan-out is 5. Any voltage below 1 V in the output





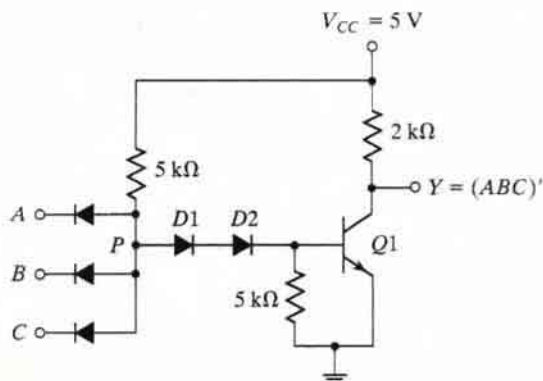
**FIGURE 10.8**  
Basic RTL NOR gate

may not drive the next transistor into saturation as required. The power dissipation of the RTL gate is about 12 mW and the propagation delay averages 25 ns.

### DTL Basic Gates

The basic circuit in the DTL digital logic family is the NAND gate shown in Fig. 10.9. Each input is associated with one diode. The diodes and the 5-k $\Omega$  resistor form an AND gate. The transistor serves as a current amplifier while inverting the digital signal. The two voltage levels are 0.2 V for the low level and between 4 and 5 V for the high level.

The analysis of the DTL gate should conform to the conditions listed in Fig. 10.1 for the NAND gate. If any input of the gate is low at 0.2 V, the corresponding input diode conducts



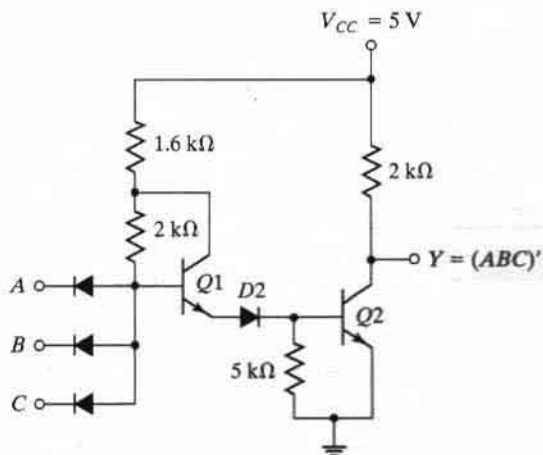
**FIGURE 10.9**  
Basic DTL NAND gate

current through  $V_{CC}$  and the  $5\text{-k}\Omega$  resistor into the input node. The voltage at point  $P$  is equal to the input voltage of  $0.2\text{ V}$  plus a diode drop of  $0.7\text{ V}$ , for a total of  $0.9\text{ V}$ . In order for the transistor to start conducting, the voltage at point  $P$  must overcome (i.e., be at least as high as) a  $1\text{-}V_{BE}$  drop in  $Q1$  plus two diode drops across  $D1$  and  $D2$ , or  $3 \times 0.6 = 1.8\text{ V}$ . Since the voltage at  $P$  is maintained at  $0.9\text{ V}$  by the input conducting diode, the transistor is cut off with no drop across the  $2\text{-k}\Omega$  resistor, and the output voltage is high at  $5\text{ V}$ .

If all inputs of the gate are high, the transistor is driven into the saturation region. The voltage at  $P$  now is equal to  $V_{BE}$  plus the two diode drops across  $D1$  and  $D2$ , or  $0.7 \times 3 = 2.1\text{ V}$ . Since all inputs are high at  $5\text{ V}$  and since  $V_P = 2.1\text{ V}$ , the input diodes are reverse biased and off. The base current is equal to the difference of the currents flowing in the two  $5\text{-k}\Omega$  resistors and is sufficient to drive the transistor into saturation. (See Problem 10.3.) With the transistor saturated, the output drops to  $V_{CE} = 0.2\text{ V}$ , which is the low level for the gate.

The power dissipation of a DTL gate is about  $12\text{ mW}$  and the propagation delay averages  $30\text{ ns}$ . The noise margin is about  $1\text{ V}$  and a fan-out as high as  $8$  is possible. The fan-out of the DTL gate is limited by the maximum current that can flow in the collector of the saturated transistor. (See Problem 10.4.)

The fan-out of a DTL gate may be increased by replacing one of the diodes in the base circuit with a transistor, as shown in Fig. 10.10. Transistor  $Q1$  is maintained in the active region when output transistor  $Q2$  is saturated. As a consequence, the modified circuit can supply a larger amount of base current to the output transistor, which can now draw a larger amount of collector current before it goes out of saturation. Part of the collector current comes from the conducting diodes in the loading gates when  $Q2$  is saturated. Thus, an increase in the allowable saturated current in the collector allows more loads to be connected to the output, increasing the fan-out capability of the gate.



**FIGURE 10.10**  
Modified DTL gate

## 10.5 TRANSISTOR-TRANSISTOR LOGIC

The original basic transistor-transistor logic (TTL) gate was a slight improvement over the DTL gate. As TTL technology progressed, improvements were added to the point where this logic family became widely used in the design of digital systems. Today, MOS and CMOS logic, which will be discussed in Sections 10.7 and 10.8, are the dominant technologies in VLSI circuits.

There are several subfamilies or series of the TTL technology. The names and characteristics of eight TTL series appear in Table 10.2. Commercial TTL ICs have a number designation that starts with 74 and follows with a suffix that identifies the series. Examples are 7404, 74S86, and 74ALS161. Fan-out, power dissipation, and propagation delay were defined in Section 10.2. The speed-power product is an important parameter used in comparing the various TTL series. The product of the propagation delay and power dissipation, the speed-power product is measured in picojoules (pJ). A low value for this parameter is desirable, because it indicates that a given propagation delay can be achieved without excessive power dissipation, and vice versa.

The standard TTL gate was the first version in the TTL family. This basic gate was then designed with different resistor values to produce gates with lower power dissipation or with higher speed. The propagation delay of a transistor circuit that goes into saturation depends mostly on two factors: storage time and  $RC$  time constants. Reducing the storage time decreases the propagation delay. Reducing resistor values in the circuit reduces the  $RC$  time constants and decreases the propagation delay. Of course, the trade-off is higher power dissipation, because lower resistances draw more current from the power supply. The speed of the gate is inversely proportional to the propagation delay.

In the low-power TTL gate, the resistor values are higher than in the standard gate in order to reduce the power dissipation, but the propagation delay is increased. In the high-speed TTL gate, resistor values are lowered to reduce the propagation delay, but the power dissipation is increased. The Schottky TTL gate was the next improvement in the technology. The effect of the Schottky transistor is to remove the storage time delay by preventing the transistor from

**Table 10.2**  
*TTL Series and Their Characteristics*

TTL Series Name	Prefix	Fan-out	Power Dissipation (mW)	Propagation Delay (ns)	Speed-Power Product (pJ)
Standard	74	10	10	9	90
Low power	74L	20	1	33	33
High speed	74H	10	22	6	132
Schottky	74S	10	19	3	57
Low-power Schottky	74LS	20	2	9.5	19
Advanced Schottky	74AS	40	10	1.5	15
Advanced low-power Schottky	74ALS	20	1	4	4
Fast	74F	20	4	3	12



going into saturation. This series increases the speed of operation of the circuit without an excessive increase in power dissipation. The low-power Schottky TTL sacrifices some speed for reduced power dissipation. It is equal to the standard TTL in propagation delay, but has only one-fifth the power dissipation. Further innovations led to the development of the advanced Schottky series, which provides an improvement in propagation delay over the Schottky series and also lowers the power dissipation. The advanced low-power Schottky has the lowest speed–power product and is the most efficient series. The fast TTL family is the best choice for high-speed designs.

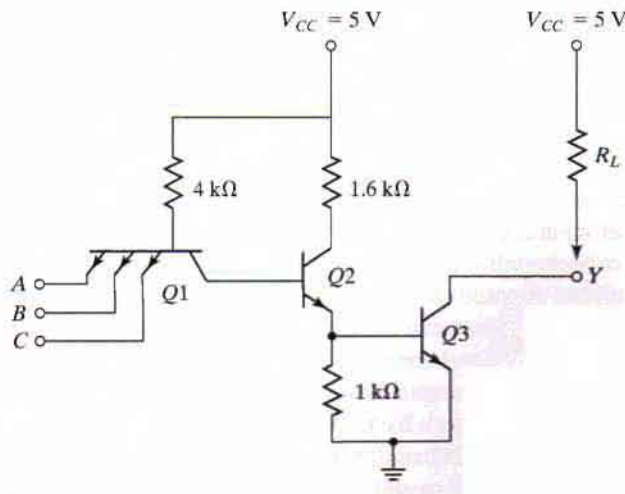
All TTL series are available in SSI components and in more complex forms, such as MSI and LSI components. The differences in the TTL series are not in the digital logic that they perform, but rather in the internal construction of the basic NAND gate. In any case, TTL gates in all the available series come in three different types of output configuration:

1. Open-collector output
2. Totem-pole output
3. Three-state output

These three types of outputs are considered next, in conjunction with the circuit description of the basic TTL gate.

### Open-Collector Output Gate

The basic TTL gate shown in Fig. 10.11 is a modified circuit of the DTL gate. The multiple emitters in transistor  $Q1$  are connected to the inputs. Most of the time, these emitters behave like the input diodes in the DTL gate, since they form a  $pn$  junction with their common base. The base–collector junction of  $Q1$  acts as another  $pn$  junction diode corresponding to  $D1$  in the



**FIGURE 10.11**  
Open-collector TTL NAND gate

DTL gate. (See Fig. 10.9.) Transistor  $Q_2$  replaces the second diode,  $D_2$ , in the DTL gate. The output of the TTL gate is taken from the open collector of  $Q_3$ . A resistor connected to  $V_{CC}$  must be inserted externally to the IC package for the output to “pull up” to the high voltage level when  $Q_3$  is off; otherwise, the output acts as an open circuit. The reason for not providing the resistor internally will be discussed later.

The two voltage levels of the TTL gate are 0.2 V for the low level and from 2.4 to 5 V for the high level. The basic circuit is a NAND gate. If any input is low, the corresponding base-emitter junction in  $Q_1$  is forward biased. The voltage at the base of  $Q_1$  is equal to the input voltage of 0.2 V plus a  $V_{BE}$  drop of 0.7, or 0.9 V. In order for  $Q_3$  to start conducting, the path from  $Q_1$  to  $Q_3$  must overcome a potential of one diode drop in the base-collector  $pn$  junction of  $Q_1$  and two  $V_{BE}$  drops in  $Q_2$  and  $Q_3$ , or  $3 \times 0.6 = 1.8$  V. Since the base of  $Q_1$  is maintained at 0.9 V by the input signal, the output transistor cannot conduct and is cut off. The output level will be high if an external resistor is connected between the output and  $V_{CC}$  (or an open circuit if a resistor is not used).

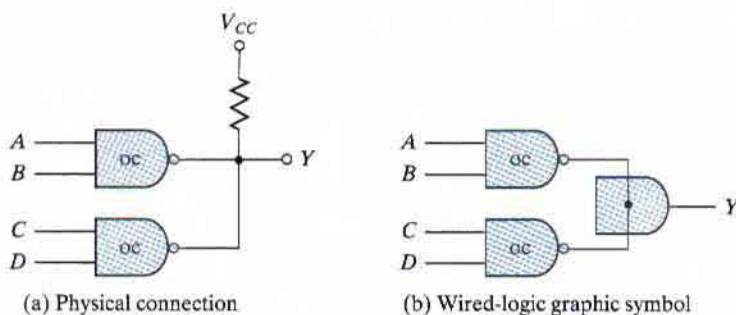
If all inputs are high, both  $Q_2$  and  $Q_3$  conduct and saturate. The base voltage of  $Q_1$  is equal to the voltage across its base-collector  $pn$  junction plus two  $V_{BE}$  drops in  $Q_2$  and  $Q_3$ , or about  $0.7 \times 3 = 2.1$  V. Since all inputs are high and greater than 2.4 V, the base-emitter junctions of  $Q_1$  are all reverse biased. When output transistor  $Q_3$  saturates (provided that it has a current path), the output voltage goes low to 0.2 V. This confirms the conditions of a NAND operation.

In the analysis presented thus far, we said that the base-collector junction of  $Q_1$  acts like a  $pn$  diode junction. This is true in the steady-state condition. However, during the turnoff transition,  $Q_1$  does exhibit transistor action, resulting in a reduction in propagation delay. When all inputs are high and then one of the inputs is brought to a low level, both  $Q_2$  and  $Q_3$  start turning off. At this time, the collector junction of  $Q_1$  is reverse biased and the emitter is forward biased, so transistor  $Q_1$  goes momentarily into the active region. The collector current of  $Q_1$  comes from the base of  $Q_2$  and quickly removes the excess charge stored in  $Q_2$  during its previous saturation state. This causes a reduction in the storage time of the circuit compared with that of the DTL type of input. The result is a reduction in the turnoff time of the gate.

The open-collector TTL gate will operate without the external resistor when connected to inputs of other TTL gates, although this kind of operation is not recommended because of the low noise immunity encountered. Without an external resistor, the output of the gate will be an open circuit when  $Q_3$  is off. An open circuit to an input of a TTL gate behaves as if it has a high-level input (but a small amount of noise can change this to a low level). When  $Q_3$  conducts, its collector will have a current path supplied by the input of the loading gate through  $V_{CC}$ , the 4-k $\Omega$  resistor, and the forward-biased base-emitter junction.

Open-collector gates are used in three major applications: driving a lamp or relay, performing wired logic, and constructing a common-bus system. An open-collector output can drive a lamp placed in its output through a limiting resistor. When the output is low, the saturated transistor  $Q_3$  forms a path for the current that turns the lamp on. When the output transistor is off, the lamp turns off because there is no path for the current.

If the outputs of several open-collector TTL gates are tied together with a single external resistor, a wired-AND logic is performed. Remember that a positive-logic AND function gives

**FIGURE 10.12****Wired-AND of two open-collector (oc) gates,  $Y = (AB + CD)'$** 

a high level only if all variables are high; otherwise, the function is low. With the outputs of open-collector gates connected together, the common output is high only when all output transistors are off (or high). If an output transistor conducts, it forces the output into the low state.

The wired logic performed with open-collector TTL gates is depicted in Fig. 10.12. The physical wiring in (a) shows how the outputs must be connected to a common resistor. The graphic symbol for such a connection is demonstrated in (b). The AND function formed by connecting the two outputs together is called a wired-AND function. The AND gate is drawn with the lines going through the center of the gate, to distinguish it from a conventional gate. The wired-AND gate is not a physical gate, but only a symbol to designate the function obtained from the indicated connection. The Boolean function obtained from the circuit of Fig. 10.12 is the AND operation between the outputs of the two NAND gates:

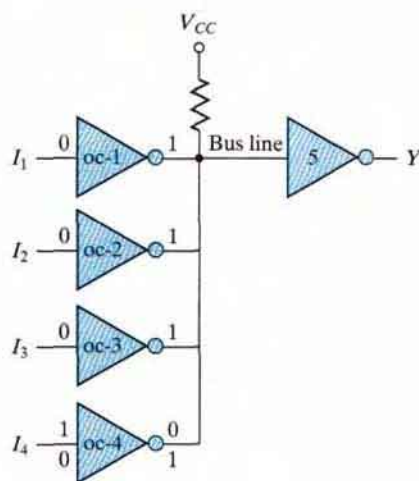
$$Y = (AB)' \cdot (CD)' = (AB + CD)'$$

The second expression is preferred, since it shows an operation commonly referred to as an AND–OR–INVERT function. (See Section 3.8.)

Open-collector gates can be tied together to form a common bus. At any time, all gate outputs tied to the bus, except one, must be maintained in their high state. The selected gate may be in either the high or low state, depending on whether we want to transmit a 1 or a 0 on the bus. Control circuits must be used to select the particular gate that drives the bus at any given time.

Figure 10.13 demonstrates the connection of four sources tied to a common bus line. Each of the four inputs drives an open-collector inverter, and the outputs of the inverters are tied together to form a single bus line. The figure shows that three of the inputs are 0, producing a 1, or high level, on the bus. The fourth input,  $I_4$ , can now transmit information through the common-bus line into inverter 5. Remember that an AND operation is performed in the wired logic. If  $I_4 = 1$ , the output of gate 4 is 0 and the wired-AND operation produces a 0. If  $I_4 = 0$ , the output of gate 4 is 1 and the wired-AND operation produces a 1. Thus, if all other outputs are maintained at 1, the selected gate can transmit its value through the bus. The value transmitted is the complement of  $I_4$ , but inverter 5 at the receiving end can easily invert this signal again to make  $Y = I_4$ .





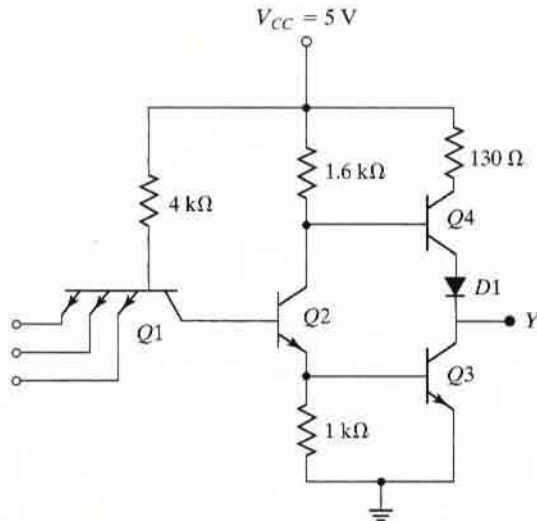
**FIGURE 10.13**  
Open-collector gates forming a common bus line

## Totem-Pole Output

The output impedance of a gate is normally a resistive plus a capacitive load. The capacitive load consists of the capacitance of the output transistor, the capacitance of the fan-out gates, and any stray wiring capacitance. When the output changes from the low to the high state, the output transistor of the gate goes from saturation to cutoff and the total load capacitance  $C$  charges exponentially from the low to the high voltage level with a time constant equal to  $RC$ . For the open-collector gate,  $R$  is the external resistor marked  $R_L$ . For a typical operating value of  $C = 15$  pF and  $R_L = 4$  k $\Omega$ , the propagation delay of a TTL open-collector gate during the turnoff time is 35 ns. With an *active pull-up* circuit replacing the passive pull-up resistor  $R_L$ , the propagation delay is reduced to 10 ns. This configuration, shown in Fig. 10.14, is called a *totem-pole* output because transistor  $Q_4$  “sits” upon  $Q_3$ .

The TTL gate with the totem-pole output is the same as the open-collector gate, except for the output transistor  $Q_4$  and the diode  $D_1$ . When the output  $Y$  is in the low state,  $Q_2$  and  $Q_3$  are driven into saturation as in the open-collector gate. The voltage in the collector of  $Q_2$  is  $V_{BE}(Q_3) + V_{CE}(Q_2)$ , or  $0.7 + 0.2 = 0.9$  V. The output  $Y = V_{CE}(Q_3) = 0.2$  V. Transistor  $Q_4$  is cut off because its base must be one  $V_{BE}$  drop plus one diode drop, or  $2 \times 0.6 = 1.2$  V, to start conducting. Since the collector of  $Q_2$  is connected to the base of  $Q_4$ , the latter’s voltage is only 0.9 V instead of the required 1.2 V, so  $Q_4$  is cut off. The reason for placing the diode in the circuit is to provide a diode drop in the output path and thus ensure that  $Q_4$  is cut off when  $Q_3$  is saturated.

When the output changes to the high state because one of the inputs drops to the low state, transistors  $Q_2$  and  $Q_3$  go into cutoff. However, the output remains momentarily low because the voltages across the load capacitance cannot change instantaneously. As soon as  $Q_2$  turns off,  $Q_4$  conducts, because its base is connected to  $V_{CC}$  through the 1.6-k $\Omega$  resistor. The current needed to charge the load capacitance causes  $Q_4$  to saturate momentarily, and the output



**FIGURE 10.14**  
TTL gate with totem-pole output

voltage rises with a time constant  $RC$ . But  $R$  in this case is equal to  $130\ \Omega$ , plus the saturation resistance of  $Q4$ , plus the resistance of the diode, for a total of approximately  $150\ \Omega$ . This value of  $R$  is much smaller than the passive pull-up resistance used in the open-collector circuit. As a consequence, the transition from the low to high level is much faster.

As the capacitive load charges, the output voltage rises and the current in  $Q4$  decreases, bringing the transistor into the active region. Thus, in contrast to the other transistors,  $Q4$  is in the *active* region when  $Q4$  is in a steady-state condition. The final value of the output voltage is then  $5\text{ V}$ , minus a  $V_{BE}$  drop in  $Q4$ , minus a diode drop in  $D1$  to about  $3.6\text{ V}$ . Transistor  $Q3$  goes into cutoff very fast, but during the initial transition time, both  $Q3$  and  $Q4$  are on and a peak current is drawn from the power supply. This current spike generates noise in the power-supply distribution system. When the change of state is frequent, the transient-current spikes increase the power-supply current requirement and the average power dissipation of the circuit increases.

The wired-logic connection is not allowed with totem-pole output circuits. When two totem poles are wired together, with the output of one gate high and the output of the second gate low, the excessive amount of current drawn can produce enough heat to damage the transistors in the circuit. (See Problem 10.7.) Some TTL gates are constructed to withstand the amount of current that flows under this condition. In any case, the collector current in the low gate may be high enough to move the transistor into the active region and produce an output voltage greater than  $0.8\text{ V}$  in the wired connection. This voltage is not a valid binary signal for TTL gates.

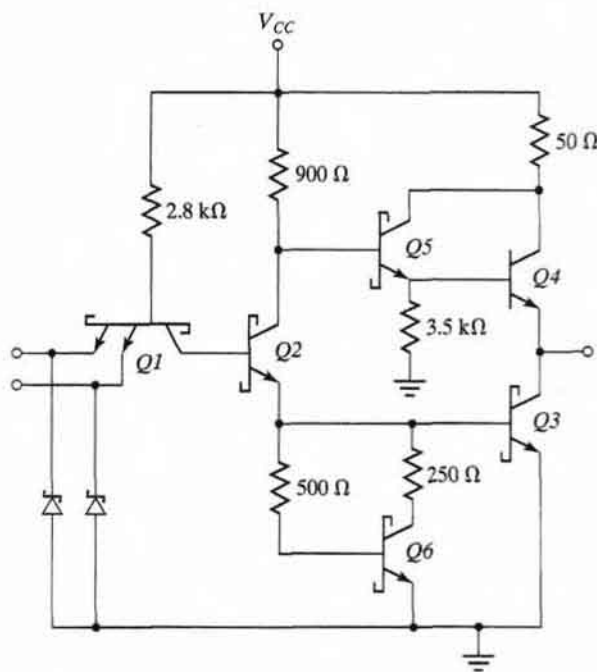
### Schottky TTL Gate

As mentioned before, a reduction in storage time results in a reduction in propagation delay. This is because the time needed for a transistor to come out of saturation delays the switching

of the transistor from the on condition to the off condition. Saturation can be eliminated by placing a Schottky diode between the base and collector of each saturated transistor in the circuit. The Schottky diode is formed by the junction of a metal and semiconductor, in contrast to a conventional diode, which is formed by the junction of  $p$ -type and  $n$ -type semiconductor material. The voltage across a conducting Schottky diode is only 0.4 V, compared with 0.7 V in a conventional diode. The presence of a Schottky diode between the base and collector prevents the transistor from going into saturation. The resulting transistor is called a *Schottky transistor*. The use of Schottky transistors in a TTL decreases the propagation delay without sacrificing power dissipation.

The Schottky TTL gate is shown in Fig. 10.15. Note the special symbol used for the Schottky transistors and diodes. The diagram shows all transistors except  $Q4$  to be of the Schottky type. An exception is made for  $Q4$ , since it does not saturate, but stays in the active region. Note also that resistor values have been reduced in order to decrease the propagation delay further.

In addition to using Schottky transistors and lower resistor values, the circuit of Fig. 10.15 includes other modifications not available in the standard gate of Fig. 10.14. Two new transistors,  $Q5$  and  $Q6$ , have been added, and Schottky diodes are inserted between each input terminal and ground. There is no diode in the totem-pole circuit. However, the new combination of  $Q5$  and  $Q4$  still gives the two  $V_{BE}$  drops necessary to prevent  $Q4$  from conducting when the output is low. This combination constitutes a double emitter–follower called a *Darlington pair*. The Darlington



**FIGURE 10.15**  
Schottky TTL gate



pair provides a very high current gain and extremely low resistance, exactly what is needed during the low-to-high swing of the output, resulting in a decrease in propagation delay.

The diodes in each input shown in the circuit help clamp any ringing that may occur in the input lines. Under transient switching conditions, signal lines appear inductive; this, along with stray capacitance, causes signals to oscillate, or “ring.” When the output of a gate switches from the high to the low state, the ringing waveform at the input may have excursions as great as 2–3 V below ground, depending on the line length. The diodes connected to ground help clamp this ringing, since they conduct as soon as the negative voltage exceeds 0.4 V. When the negative excursion is limited, the positive swing is also reduced. Clamp diodes have been so successful in limiting line effects that all versions of TTL gates use them.

The emitter resistor  $Q2$  in Fig. 10.14 has been replaced in Fig. 10.15 by a circuit consisting of transistor  $Q6$  and two resistors. The effect of this circuit is to reduce the turnoff current spikes discussed previously. The analysis of such a circuit, whose operation helps to reduce the propagation time of the gate, is too involved to present in this brief discussion.

## Three-State Gate

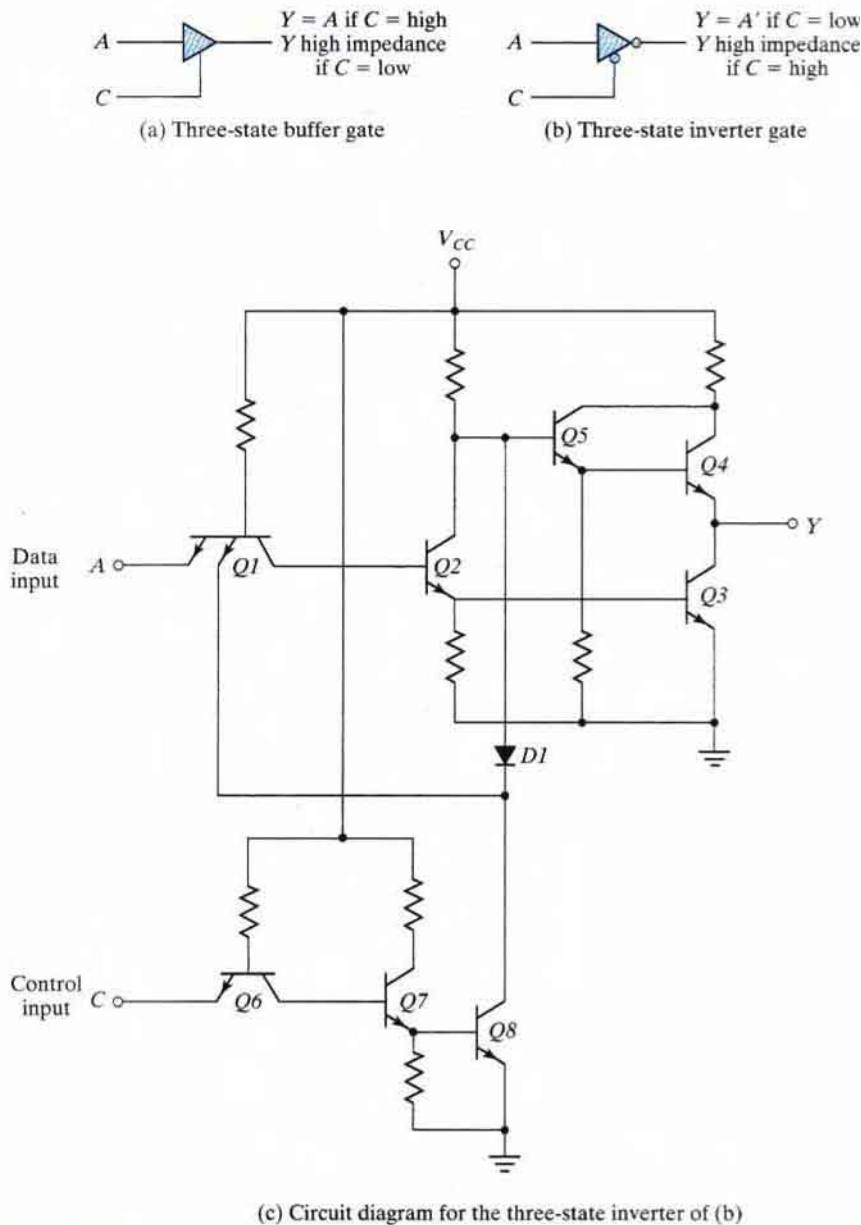
As mentioned earlier, the outputs of two TTL gates with totem-pole structures cannot be connected together as in open-collector outputs. There is, however, a special type of totem-pole gate that allows the wired connection of outputs for the purpose of forming a common-bus system. When a totem-pole output TTL gate has this property, it is called a *three-state* gate.

A three-state gate exhibits three output states: (1) a low-level state when the lower transistor in the totem pole is on and the upper transistor is off, (2) a high-level state when the upper transistor in the totem pole is on and the lower transistor is off, and (3) a third state when both transistors in the totem pole are off. The third state is an open-circuit, or high-impedance, state that allows a direct wire connection of many outputs to a common line. Three-state gates eliminate the need for open-collector gates in bus configurations.

Figure 10.16(a) shows the graphic symbol of a three-state buffer gate. When the control input  $C$  is high, the gate is enabled and behaves like a normal buffer, with the output equal to the input binary value. When the control input is low, the output is an open circuit, which gives a high impedance (the third state) regardless of the value of input  $A$ . Some three-state gates produce a high-impedance state when the control input is high. This is shown symbolically in Fig. 10.16(b), where we have two small circles, one for the inverter output and the other to indicate that the gate is enabled when  $C$  is low.

The circuit diagram of the three-state inverter is shown in Fig. 10.16(c). Transistors  $Q6$ ,  $Q7$ , and  $Q8$  associated with the control input form a circuit similar to the open-collector gate. Transistors  $Q1$ – $Q5$ , associated with the data input, form a totem-pole TTL circuit. The two circuits are connected together through diode  $D1$ . As in an open-collector circuit, transistor  $Q8$  turns off when the control input at  $C$  is in the low-level state. This prevents diode  $D1$  from conducting. In addition, the emitter in  $Q1$  connected to  $Q8$  has no conduction path. Under this condition, transistor  $Q8$  has no effect on the operation of the gate and the output in  $Y$  depends only on the data input at  $A$ .

When the control input is high, transistor  $Q8$  turns on and the current flowing from  $V_{CC}$  through diode  $D1$  causes transistor  $Q8$  to saturate. The voltage at the base of  $Q5$  is now equal



**FIGURE 10.16**  
Three-state TTL gate

to the voltage across the saturated transistor,  $Q8$ , plus one diode drop, or 0.9 V. This voltage turns off  $Q5$  and  $Q4$ , since it is less than two  $V_{BE}$  drops. At the same time, the low input to one of the emitters of  $Q1$  forces transistor  $Q3$  (and  $Q2$ ) to turn off. Thus, both  $Q3$  and  $Q4$  in the totem pole are turned off, and the output of the circuit behaves like an open circuit with a very high output impedance.

A three-state bus is created by wiring several three-state outputs together. At any given time, only one control input is enabled while all other outputs are in the high-impedance state. The single gate not in a high-impedance state can transmit binary information through the common bus. Extreme care must be taken that all except one of the outputs be in the third state; otherwise, we have the undesirable condition of having two active totem-pole outputs connected together.

An important feature of most three-state gates is that the output enable delay is longer than the output disable delay. If a control circuit enables one gate and disables another at the same time, the disabled gate enters the high-impedance state before the other gate is enabled. This eliminates the situation of both gates being active at the same time.

There is a very small leakage current associated with the high-impedance condition in a three-state gate. Nevertheless, this current is so small that as many as 100 three-state outputs can be connected together to form a common-bus line.

## 10.6 EMITTER-COUPLED LOGIC

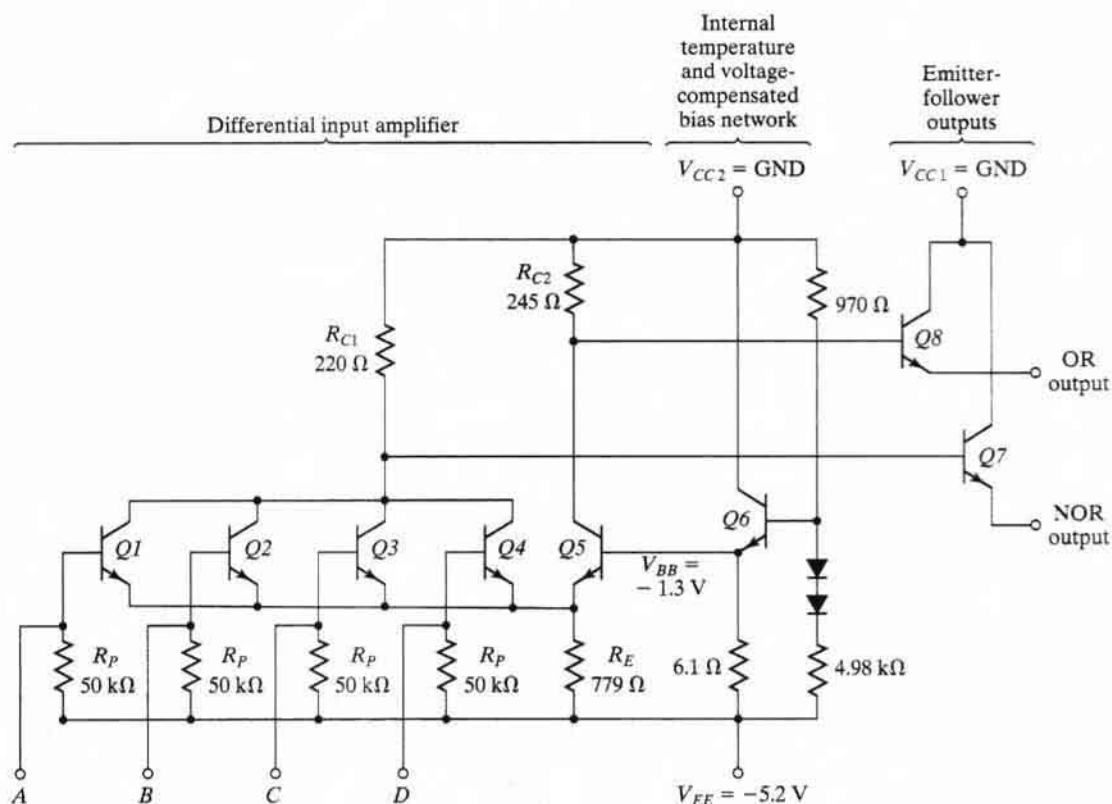
Emitter-coupled logic (ECL) is a nonsaturated digital logic family. Since transistors do not saturate, it is possible to achieve propagation delays as low as 1–2 ns. This logic family has the lowest propagation delay of any family and is used mostly in systems requiring very high speed operation. Its noise immunity and power dissipation, however, are the worst of all the logic families available.

A typical basic circuit of the ECL family is shown in Fig. 10.17. The outputs provide both the OR and NOR functions. Each input is connected to the base of a transistor. The two voltage levels are about  $-0.8$  V for the high state and about  $-1.8$  V for the low state. The circuit consists of a differential amplifier, a temperature- and voltage-compensated bias network, and an emitter-follower output. The emitter outputs require a pull-down resistor for current to flow. This is obtained from the input resistor  $R_P$  of another similar gate or from an external resistor connected to a negative voltage supply.

The internal temperature- and voltage-compensated bias circuit supplies a reference voltage to the differential amplifier. Bias voltage  $V_{BB}$  is set at  $-1.3$  V, which is the midpoint of the signal's logic swing. The diodes in the voltage divider, together with  $Q6$ , provide a circuit that maintains a constant  $V_{BB}$  value despite changes in temperature or supply voltage. Any one of the power supply inputs could be used as ground. However, the use of the  $V_{CC}$  node as ground and  $V_{EE}$  at  $-5.2$  V results in the best noise immunity.

If any input in the ECL gate is high, the corresponding transistor is turned on and  $Q5$  is turned off. An input of  $-0.8$  V causes the transistor to conduct and places  $-1.6$  V on the emitters of all of the transistors. (The  $V_{BE}$  drop in ECL transistors is 0.8 V.) Since  $V_{BB} = -1.3$  V, the base voltage of  $Q5$  is only 0.3 V more positive than its emitter.  $Q5$  is cut off because its  $V_{BE}$



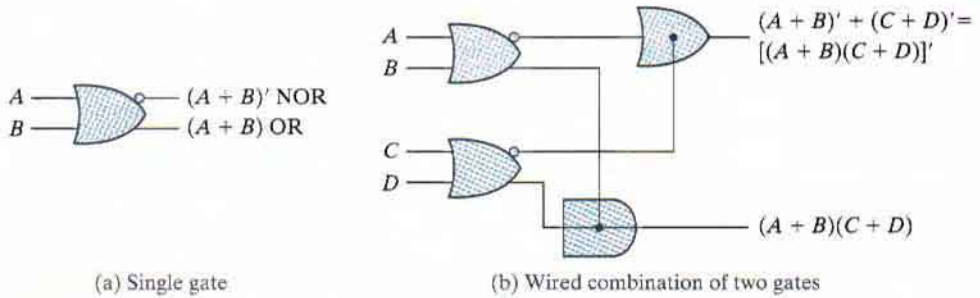


**FIGURE 10.17**  
Basic ECL gate

voltage needs at least 0.6 V to start conducting. The current in resistor  $R_{C2}$  flows into the base of  $Q8$  (provided that there is a load resistor). This current is so small that only a negligible voltage drop occurs across  $R_{C2}$ . The OR output of the gate is one  $V_{BE}$  drop below ground, or  $-0.8$  V, which is the high state. The current flowing through  $R_{C1}$  and the conducting transistor causes a drop of about 1 V below ground. (See Problem 10.9.) The NOR output is one  $V_{BE}$  drop below this level, or  $-1.8$  V, which is the low state.

If all inputs are at the low level, all input transistors turn off and  $Q5$  conducts. The voltage in the common-emitter node is one  $V_{BE}$  drop below  $V_{BB}$ , or  $-2.1$  V. Since the base of each input is at a low level of  $-1.8$  V, each base-emitter junction has only 0.3 V and all input transistors are cut off.  $R_{C2}$  draws current through  $Q5$  that results in a voltage drop of about 1 V, making the OR output one  $V_{BE}$  drop below this, at  $-1.8$  V, or the low level. The current in  $R_{C1}$  is negligible, and the NOR output is one  $V_{BE}$  drop below ground, at  $-0.8$  V, or the high level. This analysis verifies the OR and NOR operations of the circuit.

The propagation delay of the ECL gate is 2 ns and the power dissipation is 25 mW, giving a speed-power product of 50, which is about the same as that for the Schottky TTL. The noise



**FIGURE 10.18**  
Graphic symbol and wired combination of ECL gates

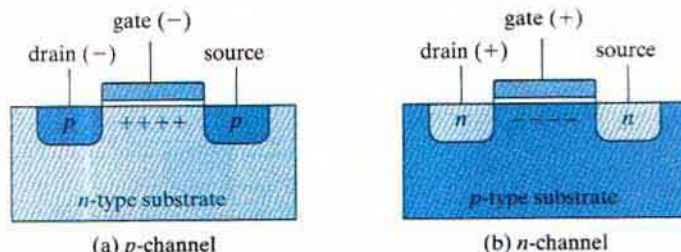
margin is about 0.3 V and is not as good as that in the TTL gate. High fan-out is possible in the ECL gate because of the high input impedance of the differential amplifier and the low output impedance of the emitter-follower. Because of the extreme high speed of the signals, external wires act like transmission lines. Except for very short wires of a few centimeters, ECL outputs must use coaxial cables with a resistor termination to reduce line reflections.

The graphic symbol for the ECL gate shown in Fig. 10.18(a). Two outputs are available: one for the NOR function and the other for the OR function. The outputs of two or more ECL gates can be connected together to form wired logic. As shown in Fig. 10.18(b), an *external* wired connection of two NOR outputs produces a wired-OR function. An *internal* wired connection of two OR outputs is employed in some ECL ICs to produce a wired-AND (sometimes called dot-AND) logic. This property may be utilized when ECL gates are used to form the OR-AND-INVERT and the OR-AND functions.

## 10.7 METAL-OXIDE SEMICONDUCTOR

The field-effect transistor (FET) is a unipolar transistor, since its operation depends on the flow of only one type of carrier. There are two types of FETs: the junction field-effect transistor (JFET) and the metal-oxide semiconductor (MOS). The former is used in linear circuits and the latter in digital circuits. MOS transistors can be fabricated in less area than bipolar transistors.

The basic structure of the MOS transistor is shown in Fig. 10.19. The *p*-channel MOS consists of a lightly doped substrate of *n*-type silicon material. Two regions are heavily doped by diffusion with *p*-type impurities to form the *source* and *drain*. The region between the two *p*-type sections serves as the *channel*. The *gate* is a metal plate separated from the channel by an insulated dielectric of silicon dioxide. A negative voltage (with respect to the substrate) at the gate terminal causes an induced electric field in the channel that attracts *p*-type carriers (holes) from the substrate. As the magnitude of the negative voltage on the gate increases, the region below the gate accumulates more positive carriers, the conductivity increases, and current can flow from source to drain, provided that a voltage difference is maintained between these two terminals.



**FIGURE 10.19**  
Basic structure of MOS transistor

There are four basic types of MOS structures. The channel can be *p* or *n* type, depending on whether the majority carriers are holes or electrons. The mode of operation can be enhancement or depletion, depending on the state of the channel region at zero gate voltage. If the channel is initially doped lightly with *p*-type impurity (in which case it is called a *diffused channel*), a conducting channel exists at zero gate voltage and the device is said to operate in the *depletion* mode. In this mode, current flows unless the channel is depleted by an applied gate field. If the region beneath the gate is left initially uncharged, a channel must be induced by the gate field before current can flow. Thus, the channel current is enhanced by the gate voltage, and such a device is said to operate in the *enhancement* mode.

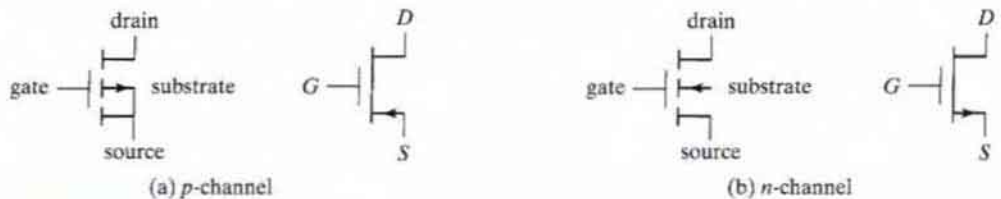
The source is the terminal through which the majority carriers enter the device. The drain is the terminal through which the majority carriers leave the device. In a *p*-channel MOS, the source terminal is connected to the substrate and a negative voltage is applied to the drain terminal. When the gate voltage is above a threshold voltage  $V_T$  (about  $-2$  V), no current flows in the channel and the drain-to-source path is like an open circuit. When the gate voltage is sufficiently negative below  $V_T$ , a channel is formed and *p*-type carriers flow from source to drain. *p*-type carriers are positive and correspond to a positive current flow from source to drain.

In the *n*-channel MOS, the source terminal is connected to the substrate and a positive voltage is applied to the drain terminal. When the gate voltage is below the threshold voltage  $V_T$  (about  $2$  V), no current flows in the channel. When the gate voltage is sufficiently positive above  $V_T$  to form the channel, *n*-type carriers flow from source to drain. *n*-type carriers are negative and correspond to a positive current flow from drain to source. The threshold voltage may vary from  $1$  to  $4$  V, depending on the particular process used.

The graphic symbols for the MOS transistors are shown in Fig. 10.20. The symbol for the enhancement type is the one with the broken-line connection between source and drain. In this symbol, the substrate can be identified and is shown connected to the source. An alternative symbol omits the substrate, and instead an arrow is placed in the source terminal to show the direction of *positive* current flow (from source to drain in the *p*-channel MOS and from drain to source in the *n*-channel MOS).

Because of the symmetrical construction of source and drain, the MOS transistor can be operated as a bilateral device. Although normally operated so that carriers flow from source to drain, there are circumstances when it is convenient to allow carriers to flow from drain to source. (See Problem 10.12.)

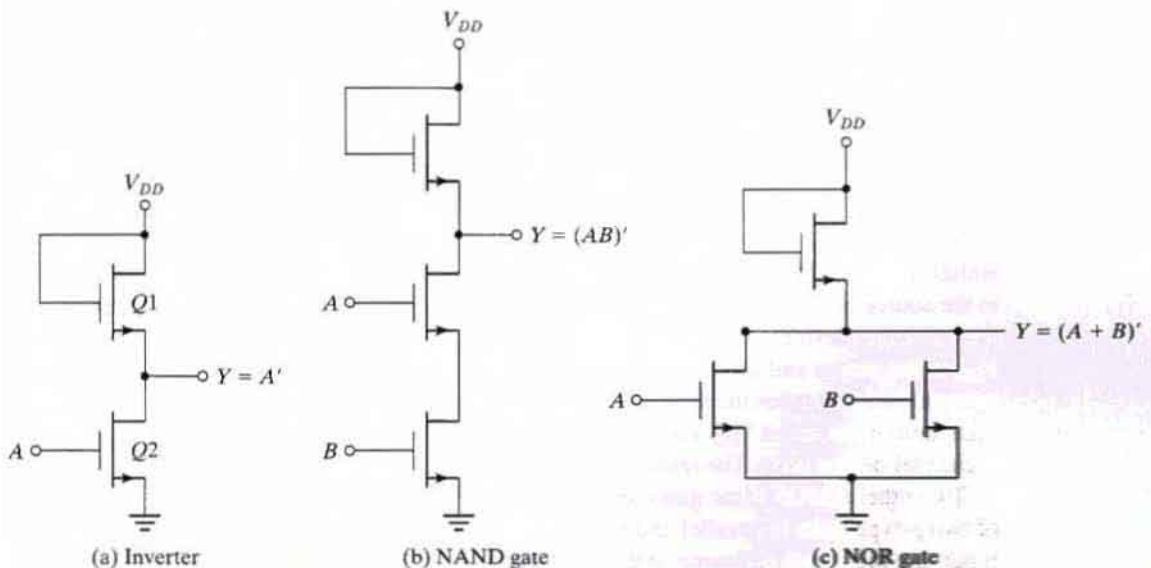




**FIGURE 10.20**  
Symbols for MOS transistors

One advantage of the MOS device is that it can be used not only as a transistor, but as a resistor as well. A resistor is obtained from the MOS by permanently biasing the gate terminal for conduction. The ratio of the source-drain voltage to the channel current then determines the value of the resistance. Different resistor values may be constructed during manufacturing by fixing the channel length and width of the MOS device.

Three logic circuits using MOS devices are shown in Fig. 10.21. For an  $n$ -channel MOS, the supply voltage  $V_{DD}$  is positive (about 5 V), to allow positive current flow from drain to source. The two voltage levels are a function of the threshold voltage  $V_T$ . The low level is anywhere from zero to  $V_T$ , and the high level ranges from  $V_T$  to  $V_{DD}$ . The  $n$ -channel gates usually employ positive logic. The  $p$ -channel MOS circuits use a negative voltage for  $V_{DD}$ , to allow positive current flow from source to drain. The two voltage levels are both negative above and below the negative threshold voltage  $V_T$ .  $p$ -channel gates usually employ negative logic.



**FIGURE 10.21**  
 $n$ -channel MOS logic circuits

The inverter circuit shown in Fig. 10.21(a) uses two MOS devices.  $Q1$  acts as the load resistor and  $Q2$  as the active device. The load-resistor MOS has its gate connected to  $V_{DD}$ , thus maintaining it in the conduction state. When the input voltage is low (below  $V_T$ ),  $Q2$  turns off. Since  $Q1$  is always on, the output voltage is about  $V_{DD}$ . When the input voltage is high (above  $V_T$ ),  $Q2$  turns on. Current flows from  $V_{DD}$  through the load resistor  $Q1$  and into  $Q2$ . The geometry of the two MOS devices must be such that the resistance of  $Q2$ , when conducting, is much less than the resistance of  $Q1$  to maintain the output  $Y$  at a voltage below  $V_T$ .

The NAND gate shown in Fig. 10.21(b) uses transistors in series. Inputs  $A$  and  $B$  must both be high for all transistors to conduct and cause the output to go low. If either input is low, the corresponding transistor is turned off and the output is high. Again, the series resistance formed by the two active MOS devices must be much less than the resistance of the load-resistor MOS. The NOR gate shown in Fig. 10.21(c) uses transistors in parallel. If either input is high, the corresponding transistor conducts and the output is low. If all inputs are low, all active transistors are off and the output is high.

## 10.8 COMPLEMENTARY MOS

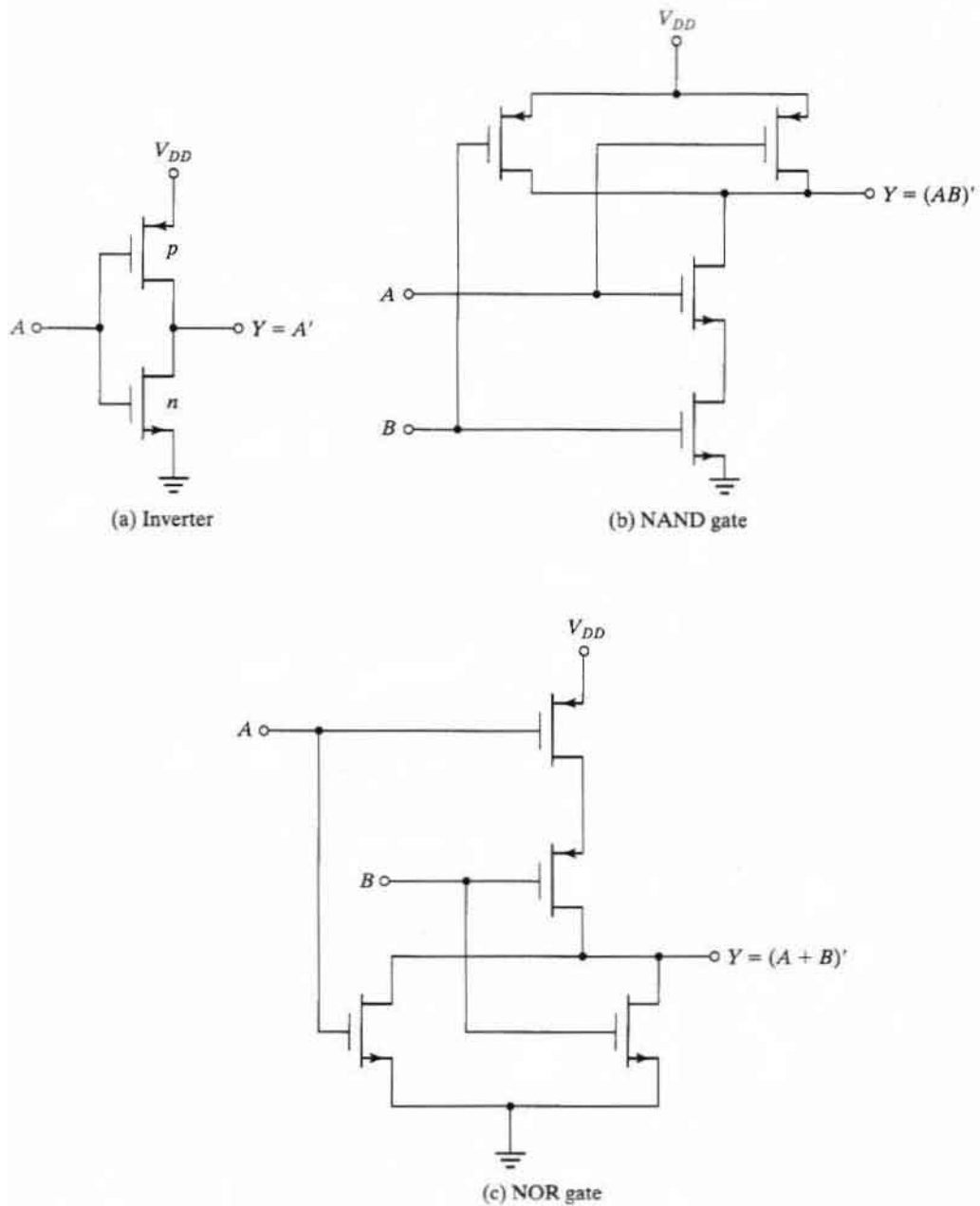
Complementary MOS (CMOS) circuits take advantage of the fact that both  $n$ -channel and  $p$ -channel devices can be fabricated on the same substrate. CMOS circuits consist of both types of MOS devices, interconnected to form logic functions. The basic circuit is the inverter, which consists of one  $p$ -channel transistor and one  $n$ -channel transistor, as shown in Fig. 10.22(a). The source terminal of the  $p$ -channel device is at  $V_{DD}$ , and the source terminal of the  $n$ -channel device is at ground. The value of  $V_{DD}$  may be anywhere from +3 to +18 V. The two voltage levels are 0 V for the low level and  $V_{DD}$  for the high level (typically, 5 V).

To understand the operation of the inverter, we must review the behavior of the MOS transistor from the previous section:

1. The  $n$ -channel MOS conducts when its gate-to-source voltage is positive.
2. The  $p$ -channel MOS conducts when its gate-to-source voltage is negative.
3. Either type of device is turned off if its gate-to-source voltage is zero.

Now consider the operation of the inverter. When the input is low, both gates are at zero potential. The input is at  $-V_{DD}$  relative to the source of the  $p$ -channel device and at 0 V relative to the source of the  $n$ -channel device. The result is that the  $p$ -channel device is turned on and the  $n$ -channel device is turned off. Under these conditions, there is a low-impedance path from  $V_{DD}$  to the output and a very high impedance path from output to ground. Therefore, the output voltage approaches the high level  $V_{DD}$  under normal loading conditions. When the input is high, both gates are at  $V_{DD}$  and the situation is reversed: The  $p$ -channel device is off and the  $n$ -channel device is on. The result is that the output approaches the low level of 0 V.

Two other CMOS basic gates are shown in Fig. 10.22. A two-input NAND gate consists of two  $p$ -type units in parallel and two  $n$ -type units in series, as shown in Fig. 10.22(b). If all inputs are high, both  $p$ -channel transistors turn off and both  $n$ -channel transistors turn on. The output has a low impedance to ground and produces a low state. If any input is low, the associated  $n$ -channel transistor is turned off and the associated  $p$ -channel transistor is turned



**FIGURE 10.22**  
CMOS logic circuits



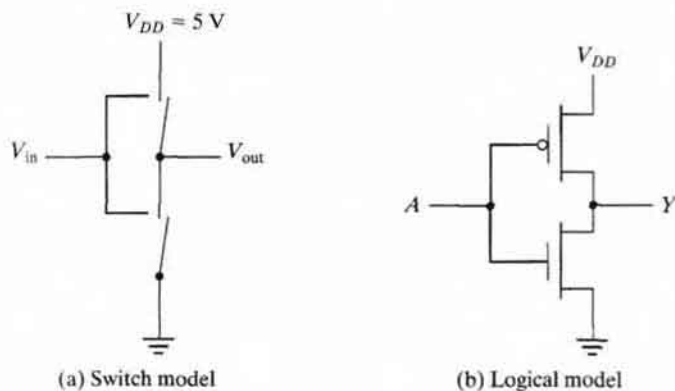
on. The output is coupled to  $V_{DD}$  and goes to the high state. Multiple-input NAND gates may be formed by placing equal numbers of  $p$ -type and  $n$ -type transistors in parallel and series, respectively, in an arrangement similar to that shown in Fig. 10.22(b).

A two-input NOR gate consists of two  $n$ -type units in parallel and two  $p$ -type units in series, as shown in Fig. 10.22(c). When all inputs are low, both  $p$ -channel units are on and both  $n$ -channel units are off. The output is coupled to  $V_{DD}$  and goes to the high state. If any input is high, the associated  $p$ -channel transistor is turned off and the associated  $n$ -channel transistor turns on, connecting the output to ground and causing a low-level output.

MOS transistors can be considered to be electronic switches that either conduct or are open. As an example, the CMOS inverter can be visualized as consisting of two switches as shown in Fig. 10.23(a). Applying a low voltage to the input causes the upper switch ( $p$ ) to close, supplying a high voltage to the output. Applying a high voltage to the input causes the lower switch ( $n$ ) to close, connecting the output to ground. Thus, the output  $V_{out}$  is the complement of the input  $V_{in}$ . Commercial applications often use other graphic symbols for MOS transistors to emphasize the logical behavior of the switches. The arrows showing the direction of current flow are omitted. Instead, the gate input of the  $p$ -channel transistor is drawn with an inversion bubble on the gate terminal to show that it is enabled with a low voltage. The inverter circuit is redrawn with these symbols in Fig. 10.23(b). A logic 0 in the input causes the upper transistor to conduct, making the output logic 1. A logic 1 in the input enables the lower transistor, making the output logic 0.

## CMOS Characteristics

When a CMOS logic circuit is in a static state, its power dissipation is very low. This is because at least one transistor is always off in the path between the power supply and ground when the state of the circuit is not changing. As a result, a typical CMOS gate has static power dissipation on the order of 0.01 mW. However, when the circuit is changing state at the rate of 1 MHz, the power dissipation increases to about 1 mW, and at 10 MHz it is about 5 mW.



**FIGURE 10.23**  
CMOS inverter

CMOS logic is usually specified for a single power-supply operation over a voltage range from 3 to 18 V with a typical  $V_{DD}$  value of 5 V. Operating CMOS at a larger power-supply voltage reduces the propagation delay time and improves the noise margin, but the power dissipation is increased. The propagation delay time with  $V_{DD} = 5$  V ranges from 5 to 20 ns, depending on the type of CMOS used. The noise margin is usually about 40 percent of the power supply voltage. The fan-out of CMOS gates is about 30 when they are operated at a frequency of 1 MHz. The fan-out decreases with an increase in the frequency of operation of the gates.

There are several series of the CMOS digital logic family. The 74C series are pin and function compatible with TTL devices having the same number. For example, CMOS IC type 74C04 has six inverters with the same pin configuration as TTL type 7404. The high-speed CMOS 74HC series is an improvement over the 74C series, with a tenfold increase in switching speed. The 74HCT series is electrically compatible with TTL ICs. This means that circuits in this series can be connected to inputs and outputs of TTL ICs without the need of additional interfacing circuits. Newer versions of CMOS are the high-speed series 74VHC and its TTL-compatible version 74VHCT.

The CMOS fabrication process is simpler than that of TTL and provides a greater packing density. Thus, more circuits can be placed on a given area of silicon at a reduced cost per function. This property, together with the low power dissipation of CMOS circuits, good noise immunity, and reasonable propagation delay, makes CMOS the most popular standard as a digital logic family.

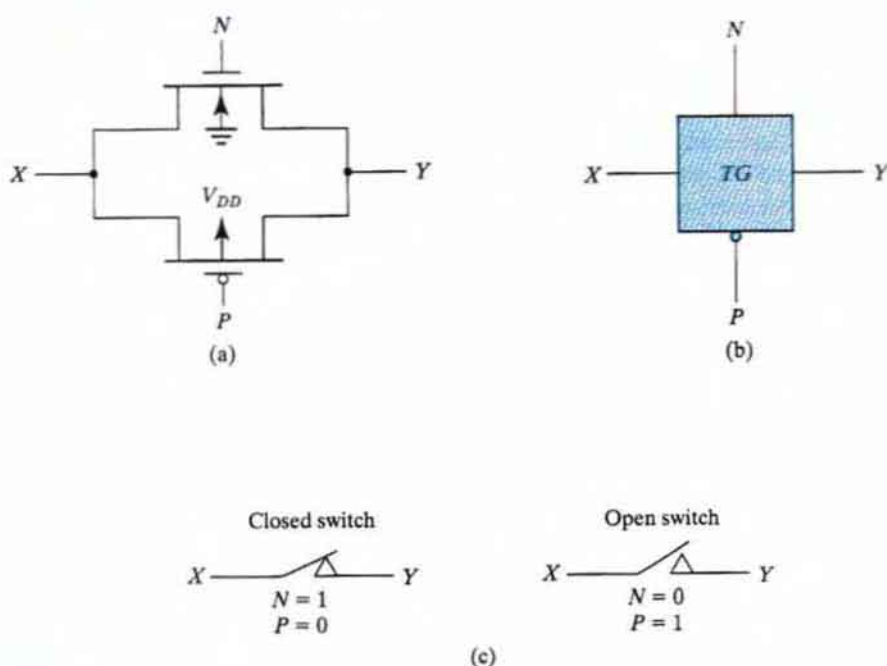
## 10.9 CMOS TRANSMISSION GATE CIRCUITS

A special CMOS circuit that is not available in the other digital logic families is the *transmission gate*. The transmission gate is essentially an electronic switch that is controlled by an input logic level. It is used to simplify the construction of various digital components when fabricated with CMOS technology.

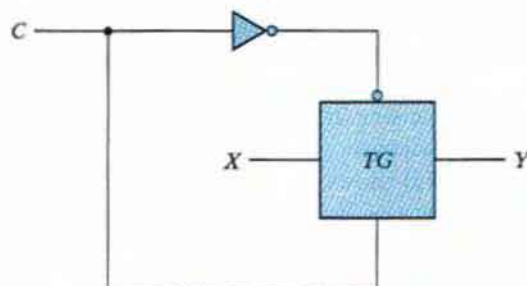
Figure 10.24(a) shows the basic circuit of the transmission gate. Whereas a CMOS inverter consists of a  $p$ -channel transistor connected in series with an  $n$ -channel transistor, a transmission gate is formed by one  $n$ -channel and one  $p$ -channel MOS transistor connected in parallel.

The  $n$ -channel substrate is connected to ground and the  $p$ -channel substrate is connected to  $V_{DD}$ . When the  $N$  gate is at  $V_{DD}$  and the  $P$  gate is at ground, both transistors conduct and there is a closed path between input  $X$  and output  $Y$ . When the  $N$  gate is at ground and the  $P$  gate is at  $V_{DD}$ , both transistors are off and there is an open circuit between  $X$  and  $Y$ . Figure 10.24(b) shows the block diagram of the transmission gate. Note that the terminal of the  $p$ -channel gate is marked with the negation symbol. Figure 10.24(c) demonstrates the behavior of the switch in terms of positive-logic assignment with  $V_{DD}$  equivalent to logic 1 and ground equivalent to logic 0.

The transmission gate is usually connected to an inverter, as shown in Fig. 10.25. This type of arrangement is referred to as a *bilateral switch*. The control input  $C$  is connected directly to the  $n$ -channel gate and its inverse to the  $p$ -channel gate. When  $C = 1$ , the switch is



**FIGURE 10.24**  
Transmission gate (TG)



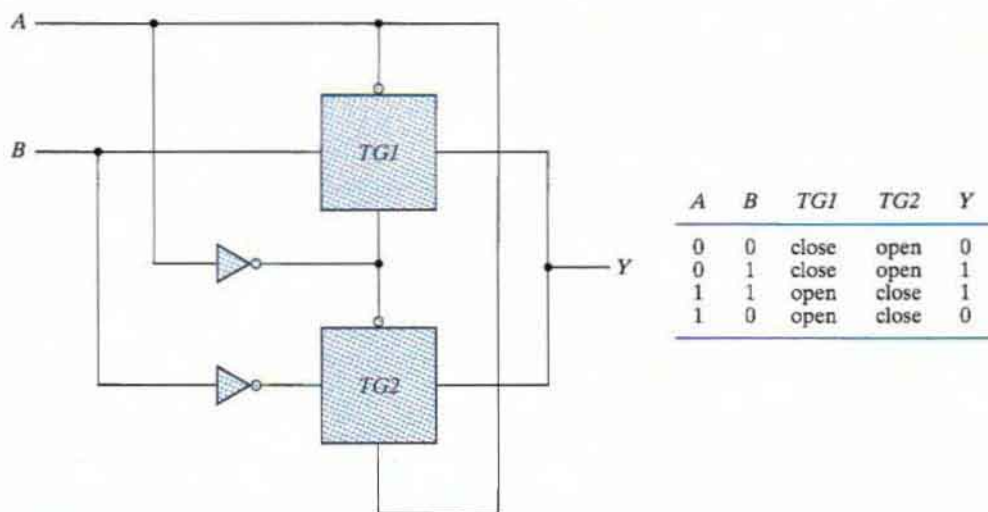
**FIGURE 10.25**  
Bilateral switch

closed, producing a path between  $X$  and  $Y$ . When  $C = 0$ , the switch is open, disconnecting the path between  $X$  and  $Y$ .

Various circuits can be constructed that use the transmission gate. To demonstrate its usefulness as a component in the CMOS family, we will show three examples.

The exclusive-OR gate can be constructed with two transmission gates and two inverters, as shown in Fig. 10.26. Input  $A$  controls the paths in the transmission gates and input  $B$  is



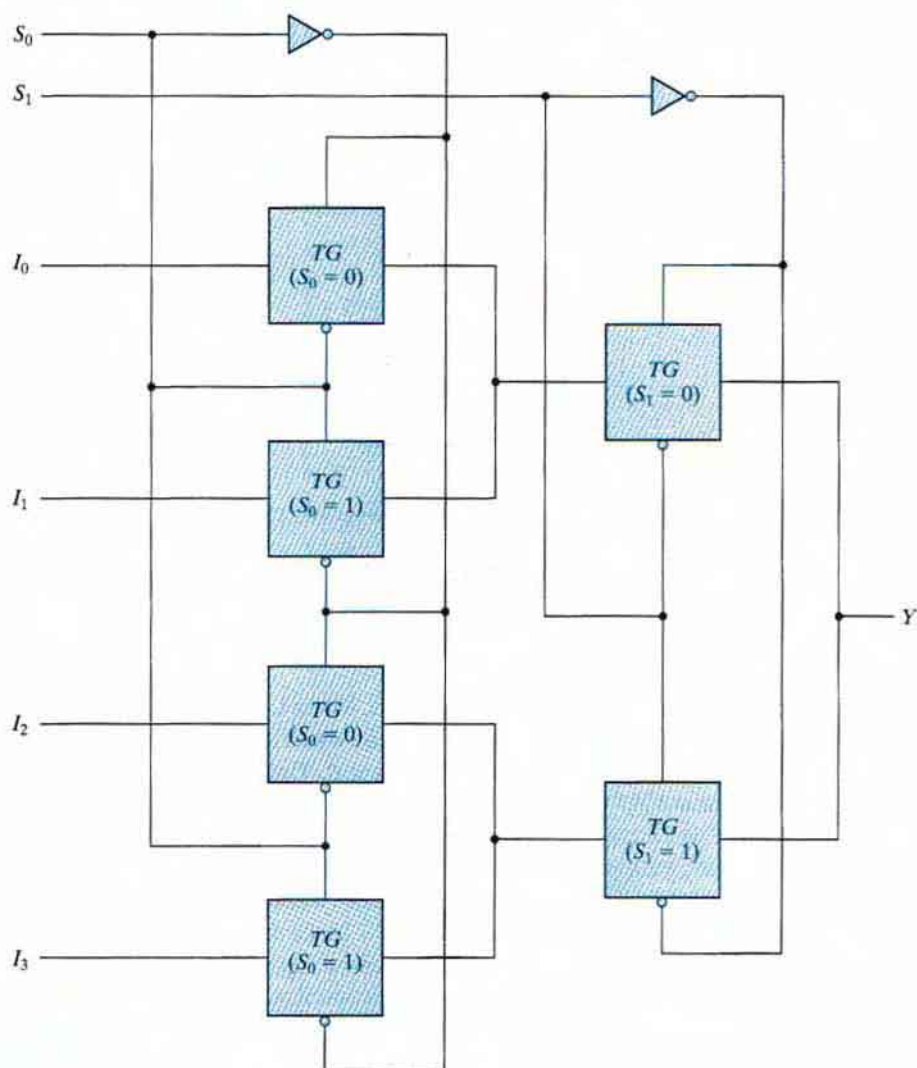
**FIGURE 10.26**

Exclusive-OR constructed with transmission gates

connected to output  $Y$  through the gates. When input  $A$  is equal to 0, transmission gate  $TG1$  is closed and output  $Y$  is equal to input  $B$ . When input  $A$  is equal to 1,  $TG2$  is closed and output  $Y$  is equal to the complement of input  $B$ . This results in the exclusive-OR truth table, as indicated in Fig. 10.26.

Another circuit that can be constructed with transmission gates is the multiplexer. A four-to-one-line multiplexer implemented with transmission gates is shown in Fig. 10.27. The  $TG$  circuit provides a transmission path between its horizontal input and output lines when the two vertical control inputs have the value of 1 in the uncircled terminal and 0 in the circled terminal. With an opposite polarity in the control inputs, the path disconnects and the circuit behaves like an open switch. The two selection inputs,  $S_1$  and  $S_0$ , control the transmission path in the  $TG$  circuits. Inside each box is marked the condition for the transmission gate switch to be closed. Thus, if  $S_0 = 0$  and  $S_1 = 0$ , there is a closed path from input  $I_0$  to output  $Y$  through the two  $TG$ s marked with  $S_0 = 0$  and  $S_1 = 0$ . The other three inputs are disconnected from the output by one of the other  $TG$  circuits.

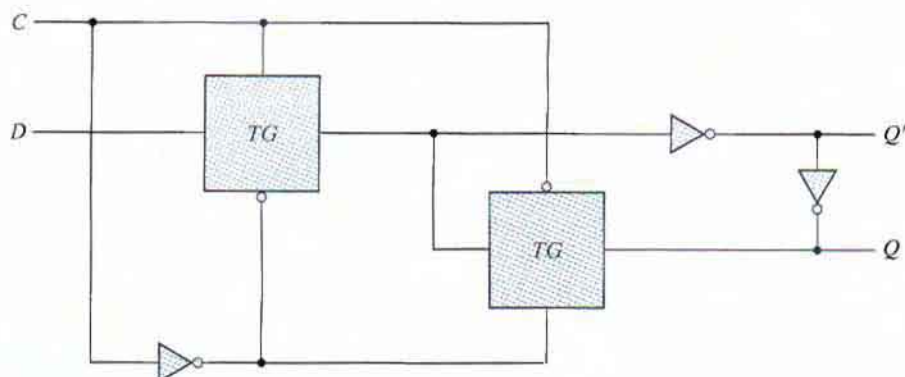
The level-sensitive  $D$  flip-flop commonly referred to as the gated  $D$  latch can be constructed with transmission gates, as shown in Fig. 10.28. The  $C$  input controls two transmission gates  $TG$ . When  $C = 1$ , the  $TG$  connected to input  $D$  has a closed path and the one connected to output  $Q$  has an open path. This configuration produces an equivalent circuit from input  $D$  through two inverters to output  $Q$ . Thus, the output follows the data input as long as  $C$  remains active. When  $C$  switches to 0, the first  $TG$  disconnects input  $D$  from the circuit and the second  $TG$  produces a closed path between the two inverters at the output.



**FIGURE 10.27**  
Multiplexer with transmission gates

Thus, the value that was present at input  $D$  at the time that  $C$  went from 1 to 0 is retained at the  $Q$  output.

A master-slave  $D$  flip-flop can be constructed with two circuits of the type shown in Fig. 10.28. The first circuit is the master and the second is the slave. Thus, a master-slave  $D$  flip-flop can be constructed with four transmission gates and six inverters.



**FIGURE 10.28**  
Gated *D* latch with transmission gates

## 10.10 SWITCH-LEVEL MODELING WITH HDL

CMOS is the dominant digital logic family used with integrated circuits. By definition, CMOS is a complementary connection of an NMOS and a PMOS transistor. MOS transistors can be considered to be electronic switches that either conduct or are open. By specifying the connections among MOS switches, the designer can describe a digital circuit constructed with CMOS. This type of description is called *switch-level modeling* in Verilog HDL.

The two types of MOS switches are specified in Verilog HDL with the keywords **nmos** and **pmos**. They are instantiated by specifying the three terminals of the transistor, as shown in Fig. 10.20:

```
nmos (drain, source, gate);
pmos (drain, source, gate);
```

Switches are considered to be primitives, so the use of an instance name is optional.

The connections to a power source ( $V_{DD}$ ) and to ground must be specified when MOS circuits are designed. Power and ground are defined with the keywords **supply1** and **supply0**. They are specified, for example, with the following statements:

```
supply1 PWR;
supply0 GRD;
```

Sources of type **supply1** are equivalent to  $V_{DD}$  and have a value of logic 1. Sources of type **supply0** are equivalent to ground connection and have a value of logic 0.

The description of the CMOS inverter of Fig. 10.22(a) is shown in HDL Example 10.1. The input, the output, and the two supply sources are declared first. The module instantiates a PMOS and an NMOS transistor. The output *Y* is common to both transistors at their drain terminals. The input is also common to both transistors at their gate terminals. The source terminal of the PMOS transistor is connected to PWR and the source terminal of the NMOS transistor is connected to GRD.



**HDL Example 10.1**


---

```
// CMOS inverter of Fig. 10.22(a)
module inverter (Y, A);
  input A;
  output Y;
  supply1 PWR;
  supply0 GRD;
  pmos (Y, PWR, A);           // (Drain, source, gate)
  nmos (Y, GRD, A);           // (Drain, source, gate)
endmodule
```

---

The second module, set forth in HDL Example 10.2, describes the two-input CMOS NAND circuit of Fig. 10.22(b). There are two PMOS transistors connected in parallel, with their source terminals connected to PWR. There are also two NMOS transistors connected in series and with a common terminal *W1*. The drain of the first NMOS is connected to the output, and the source of the second NMOS is connected to GRD.

**HDL Example 10.2**


---

```
// CMOS two-input NAND of Fig. 10.22(b)
module NAND2 (Y, A, B);
  input A, B;
  output Y;
  supply1 PWR;
  supply0 GRD;
  wire W1;           // terminal between two nmos
  pmos (Y, PWR, A);  // source connected to Vdd
  pmos (Y, PWR, B);  // parallel connection
  nmos (Y, W1, A);    // serial connection
  nmos (W1, GRD, B);  // source connected to ground
endmodule
```

---

**Transmission Gate**

The transmission gate is instantiated in Verilog HDL with the keyword **cmos**. It has an output, an input, and two control signals, as shown in Fig. 10.24. It is referred to as a **cmos** switch. The relevant code is as follows:

```
cmos (output, input, ncontrol, pcontrol); // general description
cmos (Y, X, N, P); // transmission gate of Fig. 10.24(b)
```

Normally, *ncontrol* and *pcontrol* are the complement of each other. The **cmos** switch does not need power sources, since  $V_{DD}$  and ground are connected to the substrates of the MOS transistors. Transmission gates are useful for building multiplexers and flip-flops with CMOS circuits.

HDL Example 10.3 describes a circuit with **cmos** switches. The exclusive-OR circuit of Fig. 10.26 has two transmission gates and two inverters. The two inverters are instantiated within the module describing a CMOS inverter. The two **cmos** switches are instantiated without an instance name, since they are primitives in the language. A test module is included to test the circuit's operation. Applying all possible combinations of the two inputs, the result of the simulator verifies the operation of the exclusive-OR circuit. The output of the simulation is as follows:

```
A = 0  B = 0  Y = 0
A = 0  B = 1  Y = 1
A = 1  B = 0  Y = 1
A = 1  B = 1  Y = 0
```

### HDL Example 10.3

---

//CMOS\_XOR with CMOS switches, Fig. 10.26

---

```
module CMOS_XOR (A, B, Y);
  input A, B;
  output Y;
  wire A_b, B_b;
  // instantiate inverter
  inverter v1 (A_b, A);
  inverter v2 (B_b, B);
  // instantiate cmos switch
  cmos (Y, B, A_b, A);           //(output, input, ncontrol, pcontrol)
  cmos (Y, B_b, A, A_b);
endmodule

// CMOS inverter Fig. 10-22(a)
module inverter (Y, A);
  input A;
  output Y;
  supply1 PWR;
  supply0 GND;
  pmos (Y, PWR, A);             //(Drain, source, gate)
  nmos (Y, GND, A);             //(Drain, source, gate)
endmodule

// Stimulus to test CMOS_XOR
module test_CMOS_XOR;
  reg A,B;
  wire Y;
  //Instantiate CMOS_XOR
  CMOS_XOR X1 (A, B, Y);
  // Apply truth table
  initial
    begin
```

```

A = 1'b0; B = 1'b0;
#5 A = 1'b0; B = 1'b1;
#5 A = 1'b1; B = 1'b0;
#5 A = 1'b1; B = 1'b1;
end
// Display results
initial
$monitor ("A =%b B= %b Y =%b", A, B, Y);
endmodule

```

## PROBLEMS

Answers to problems marked with \* appear at the end of the book.

**10.1\*** Following are the specifications for the Schottky TTL 74S00 quadruple two-input NAND gates:

Parameter	Name	Value
$V_{CC}$	Supply voltage	5 V
$I_{CCH}$	High-level supply current (four gates)	10 mA
$I_{CCL}$	Low-level supply current (four gates)	20 mA
$V_{OH}$	High-level output voltage (min)	2.7 V
$V_{OL}$	Low-level output voltage (max)	0.5 V
$V_{IH}$	High-level input voltage (min)	2 V
$V_{IL}$	Low-level input voltage (max)	0.8 V
$I_{OH}$	High-level output current (max)	1 mA
$I_{OL}$	Low-level output current (max)	20 mA
$I_{IH}$	High-level input current (max)	0.05 mA
$I_{IL}$	Low-level input current (max)	2 mA
$t_{PLH}$	Low-to-high delay	3 ns
$t_{PHL}$	High-to-low delay	3 ns

Calculate the fan-out, power dissipation, propagation delay, and noise margin of the Schottky NAND gate.

- 10.2\***
- Determine the high-level output voltage of the RTL gate for a fan-out of 5.
  - Determine the minimum input voltage required to drive an RTL transistor to saturation when  $h_{FE} = 20$ .
  - From the results in parts (a) and (b), determine the noise margin of the RTL gate when the input is high and the fan-out is 5.
- 10.3\*** Show that the output transistor of the DTL gate of Fig. 10.9 goes into saturation when all inputs are high. Assume that  $h_{FE} = 20$ .



- 10.4\*** Connect the output  $Y$  of the DTL gate shown in Fig. 10.9 to  $N$  inputs of other, similar gates. Assume that the output transistor is saturated and its base current is 0.44 mA. Let  $h_{FE} = 20$ .
- Calculate the current in the 2-k $\Omega$  resistor.
  - Calculate the current coming from each input connected to the gate.
  - Calculate the total collector current in the output transistor as a function of  $N$ .
  - Find the value of  $N$  that will keep the transistor in saturation.
  - What is the fan-out of the gate?
- 10.5\*** Let all inputs in the open-collector TTL gate of Fig. 10.11 be in the high state of 3 V.
- Determine the voltages in the base, collector, and emitter of all transistors in the circuit.
  - Determine the minimum  $h_{FE}$  of  $Q2$  which ensures that this transistor saturates.
  - Calculate the base current of  $Q3$ .
  - Assume that the minimum  $h_{FE}$  of  $Q3$  is 6.18. What is the maximum current that can be tolerated in the collector to ensure saturation of  $Q3$ ?
  - What is the minimum value of  $R_L$  that can be tolerated to ensure saturation of  $Q3$ ?
- 10.6** (a) Using the actual output transistors of two open-collector TTL gates, show (by means of a truth table) that, when connected together to an external resistor and  $V_{CC}$ , the wired connection produces an AND function.
- (b) Prove that two open-collector TTL inverters, when connected together, produce the NOR function.
- 10.7** It was stated in Section 10.5 that totem-pole outputs should not be tied together to form wired logic. To see why this is prohibitive, connect two such circuits together and let the output of one gate be in the high state and the output of the other gate be in the low state. Show that the load current (which is the sum of the base and collector currents of the saturated transistor  $Q4$  in Fig. 10.14) is about 32 mA. Compare this value with the recommended load current in the high state of 0.4 mA.
- 10.8** For the following conditions, list the transistors that are off and the transistors that are conducting in the three-state TTL gate of Fig. 10.16(c) (for  $Q1$  and  $Q6$ , it is necessary to list the states in the base-emitter and base-collector junctions separately):
- when  $C$  is low and  $A$  is low.
  - when  $C$  is low and  $A$  is high.
  - when  $C$  is high.
- What is the state of the output in each case?
- 10.9\*** (a) Calculate the emitter current  $I_E$  across  $R_E$  in the ECL gate of Fig. 10.17 when at least one input is high at  $-0.8$  V.
- (b) Calculate the same current when all inputs are low at  $-1.8$  V.
- (c) Now assume that  $I_C = I_E$ . Calculate the voltage drop across the collector resistor in each case and show that it is about 1 V, as required.
- 10.10\*** Calculate the noise margin of the ECL gate.
- 10.11** Using the NOR outputs of two ECL gates, show that, when connected together to an external resistor and a negative supply voltage, the wired connection produces an OR function.
- 10.12** The MOS transistor is bilateral (i.e., current may flow from source to drain or from drain to source). On the basis of this property, derive a circuit that implements the Boolean function

$$Y = (AB + CD + AED + CEB)'$$

using six MOS transistors.

- 10.13** (a) Show the circuit of a four-input NAND gate using CMOS transistors.  
(b) Repeat for a four-input NOR gate.
- 10.14** Construct an exclusive-NOR circuit with two inverters and two transmission gates.
- 10.15** Construct an eight-to-one-line multiplexer using transmission gates and inverters.
- 10.16** Draw the logic diagram of a master–slave  $D$  flip-flop using transmission gates and inverters.
- 10.17** Write a test bench that will test the NAND circuit of HDL Example 10.2. The simulation should verify the truth table of the gate.

## REFERENCES

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