IC Logic Families and Characteristics

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Introduction

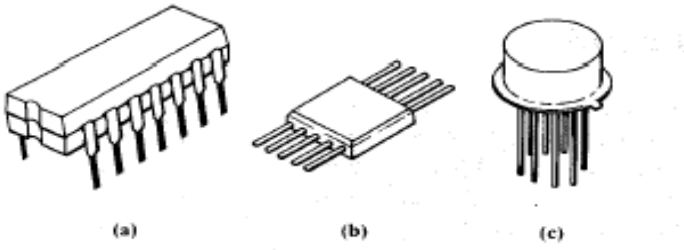
- miniature, low-cost electronics circuits whose components are fabricated on a single, continuous piece of semiconductor material to perform a high-level function.
- usually referred to as a monolithic IC.
- first introduced in 1958
- categorized as digital or linear ICs or according to the level of complexity of the IC

Category		Number of Gates
Small scale integration	SSI	<12
Medium scale integration	MSI	12 to 99
Large scale integration	LSI	100 to 9999
Very large scale integration	VLSI	10,000 or more

Packaging

1. protect the chip from mechanical damage and chemical contamination.
2. provides a completed unit large enough to handle.
3. so that it is large enough for electrical connections to be made.
4. material is molded plastic, epoxy, resin, or silicone. Ceramic used if higher thermal dissipation capabilities required. Metal/glass used in special cases.

Three most common packages for ICs are



- dual-in-line (DIPS) (most common)
- flat pack
- axial lead (TO5)

Digital IC terminology

Although there are many manufacturers of digital ICs and several logic families, a fair amount of terminology associated with digital ICs is somewhat standardized between the various manufacturers and logic families.

Common digital IC terminology

Voltage and Current Levels

Symbol	Definition
VIH	HIGH-state input voltage, corresponding to logic 1 at input
VIL	LOW-state input voltage, corresponding to logic 0 at input
VOH	HIGH-state output voltage, corresponding to logic 1 at output
VOL	LOW-state output voltage, corresponding to logic 0 at output
IIH	HIGH-state input current; current flowing from input when the input voltage corresponds to logic 1.
IIL	LOW-state input current; current flowing from an input when the input voltage corresponds to logic 0.
IOH	HIGH-state output current; current flowing from output when the output voltage corresponds to logic 1.
IOL	LOW-state output current; current flowing from an output when the output voltage corresponds to logic 0.

Properties of Digital ICs

Fan-in

Fan-in (input load factor)
is the number of input signals that can be connected to a gate without causing it to operate outside its intended operating range. expressed in terms of standard inputs or units loads (ULs)

Example: for standard TTL one unit load is defined as

1 UL = 40μA in the HIGH state
1.6mA in the LOW state

to determine the fan-in (or fan-out) for a gate, take the lower of

$$\frac{\text{HIGH – state current}}{\text{HIGH – state unit load}} \quad \text{and} \quad \frac{\text{LOW – state current}}{\text{LOW – state unit load}}$$

A fan-in of 8 means that 8 unit loads can be safely connected to the gate inputs.

Fan-out

Fan-out (output load factor)
is the maximum number of inputs that can be driven by a logic gate. A fan out of 10 means that 10 unit loads can be driven by the gate while still maintaining the output voltage within specifications for logic levels 0 and 1.

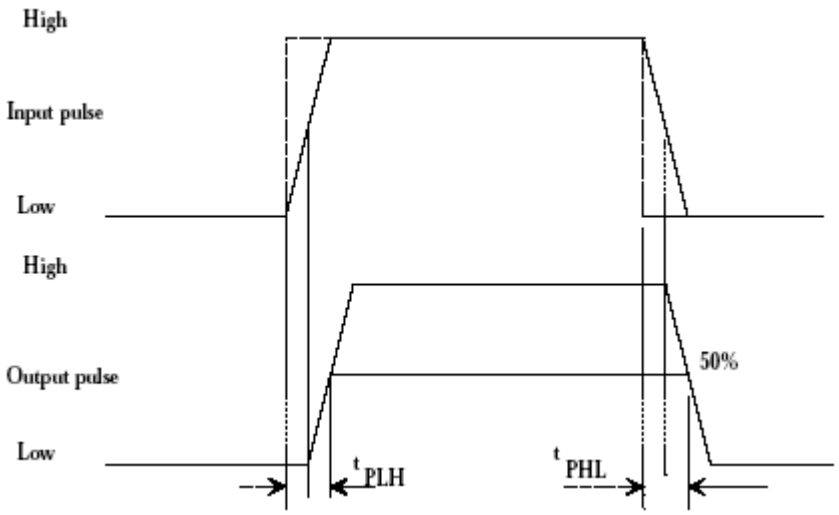
Example:
A unit load for some particular logic family is as follows:

$$1\,\text{UL} = \begin{matrix} 50\mu\text{A} & \text{HIGH state} \\ 1\text{mA} & \text{LOW state} \end{matrix}$$

Determine the fan-in and fan-out for a gate in this family that has the following parameters:
IOH = 400μA
IOL = 10mA
IIH = 150μA
IIL = 4 mA

Solution:
fan-in = 150/50 = 3 UL or 4/1 = 4 UL
therefore fan-in = 3.
fan-out = 400/50 = 8 UL or 10/1 = 10 UL
therefore fan-out = 8 UL.

Propagation Delays.
- the delay before a change in the input is reflected in the output.

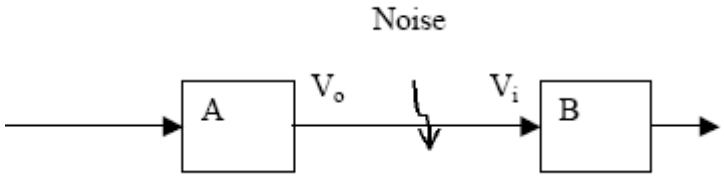


- tPHL : delay time in going from logic 1 to logic 0 (*turn-off delay*).
- tPLH : delay time in going from logic 0 to logic 1(*turn-on delay*).

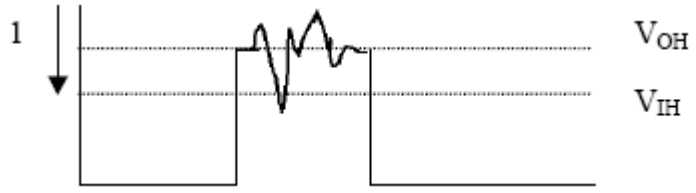
Noise Margin/Immunity
- ability of the gate to tolerate fluctuations of the voltage levels.
VNH = HIGH-state noise margin
VNL = LOW-state noise margin
VIL = LOW-state input voltage
VIH = HIGH-state input voltage
VOL = LOW-state output voltage
VOH = HIGh-state output voltage
where

VNH = VOH –VIH
VNL = VIL – VOL

Manufacturers specify voltage limits to represent the logical 0 or 1. These limits are not the same at the input and output sides. For example, a particular gate A may output a voltage of 4.8V when it is supposed to output a HIGH but, at its input side, it can take a voltage of 3V as HIGH. In this way, if any noise should corrupt the signal, there is some margin for error.
Consider the following case where the output of logic circuit A is connected to the input of logic circuit B.



When the output of A is low, V_O, the input to B, V_i, should also be low. But because of noise V_i is not exactly V_O but could higher. As long as V_i is not more than V_{IL}, B will still take the signal as a LOW. If V_i is more than V_{IL} though, then the signal may not appear as a LOW.
The effect of noise is shown in the following figure.



Example:

Find the HIGH state and LOW state noise margins for the IC with the characteristics given in the table.

	Minimum	Typical	Maximum
V_{OH}	2.8 V	3.6V	
V_{OL}		0.2V	0.4V
V_{IH}	2.0V		
V_{IL}			0.8V

From table,

HIGH-state noise margin $V_{NH} = 2.8 - 2 = 0.8$

LOW-state noise margin $V_{NL} = 0.8 - 0.4 = 0.4$

Power Dissipation

Power dissipation is the amount of heat (in mill watts) that the IC dissipates in the form of heat.

IC Logic Families

Thus far, we have specified the logic level as either 0 or 1, or HIGH or LOW. In circuit implementation, we will have to specify the actual voltage/current levels that constitute a HIGH or a LOW. These standardized voltage/current levels are grouped in families of digital ICs so that ICs belonging to the same family will have the same characteristics.
Common families are

- TTL: transistor-transistor logic
- ECL: emitter-coupled logic.
- IIL integrated injection logic.
- MOS ICs: metal-oxide-semiconductor ICs.

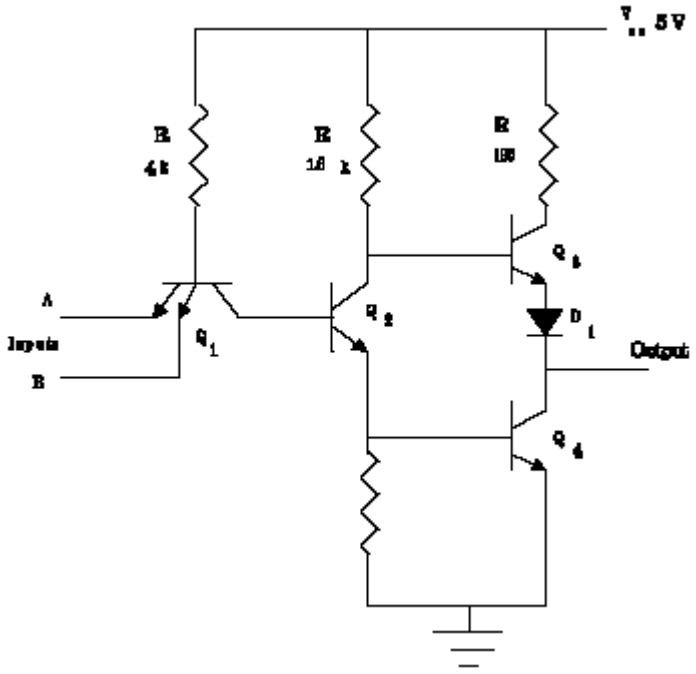
TTL

- most popular and widely used IC logic family.
- introduced by Texas Instruments in 1964.
- operate from a +5V supply.
- Standardized labeling system starting with 54 or 74. For example 7400, 7401, 74121
- A HIGH is nominally +5V while a LOW is nominally 0V or GROUND.
- to provide greater flexibility with regard to speed and power dissipation considerations, the following sub-families have been developed:

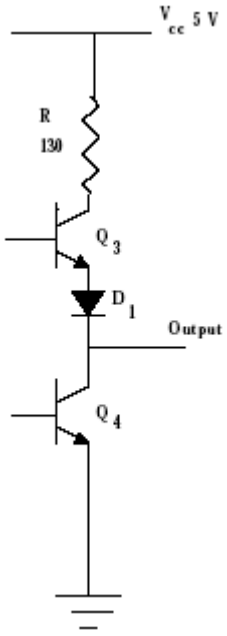
- 7400 standard series.
- 74L00 low-power series
- 74H00 high-speed series
- 74S00 Schottky series
- 74LS00 low-power Schottky series.

Totem Pole TTL

The basic TTL NAND gate circuit is shown below:



Transistors Q_3 and Q_4 form what is known as a totem pole arrangement.



The features of this arrangement are
- low power consumption
- fast switching
- low output impedance

Noise Margins

maximum logic 0 output, VOL = 0.4 V
maximum logic 0 input, VIL = 0.8 V

therefore, the LOW state noise margin is

VNL= 0.8V - 0.4V = 400 mV.

Similarly,

minimum logic 1 output, VOH = 2.4 V
minimum logic 1 input, VIH = 2.0 V

therefore, the HIGH state noise margin is
VNH = 2.4 - 2.0 = 400 mV.
These are the guaranteed worse case. The actual values typically are VNL= 1 V and VNH = 1.6 V.

Low-power TTL

designated as 74L00.
essentially same as standard TTL except that the resistor values are increased. This will decrease power consumption (typical 1 mW) but there is a corresponding decrease in speed (propagation delay of 33 ns).
low-power TTL gates have a fan-out of 10 other low-power TTL gates but will only drive two standard series TTL gate.

High-speed TTL

designated as 74H00
resistor values have been decreased. Speed is increased (delay = 6 ns) but power dissipation will increase (22 mW).

Summary of fan-out capabilities for the TTL series

TTL Driving Device	TTL load device				
	7400	74L00	74H00	74S00	74LS00
7400	10	50	8	8	20
74L00	2	10	1	1	10
74H00	12	50	10	10	25
74S00	12	100	10	10	50
74LS00	5	40	4	4	10

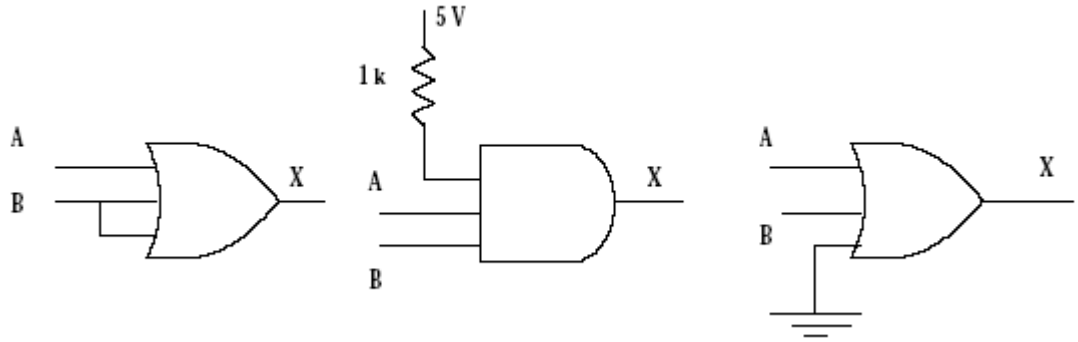
Speed-Power relationship for TTL

Series	Propagation Delay (ns)	Power Dissipation (mW)
7400	9	10
74L00	33	1
74H00	6	22
74S00	3	19
74LS00	9	2

Unused Inputs on TTL devices

Unused inputs on TTL gates behave as though a logic 1 is connected to them. This present a problem with OR or NOR gates. With AND or NAND gates, the logic would not pose a problem but for better noise immunity, the inputs should not be allowed to "float". It is advisable to connect unused HIGH inputs to +5V through resistors ("pull-up" resistors) of 1kΩ.

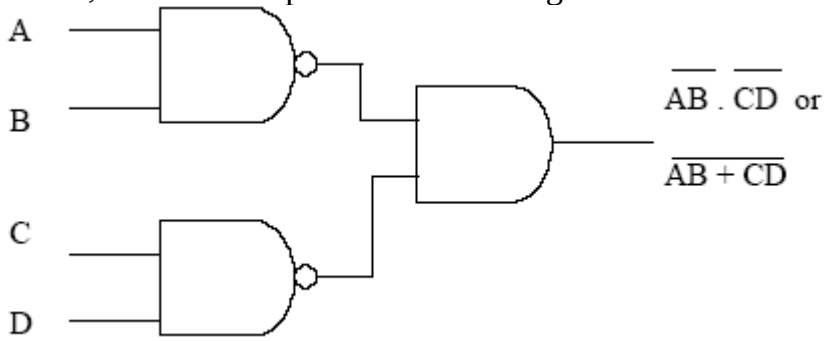
Unused inputs should be connected as follows:



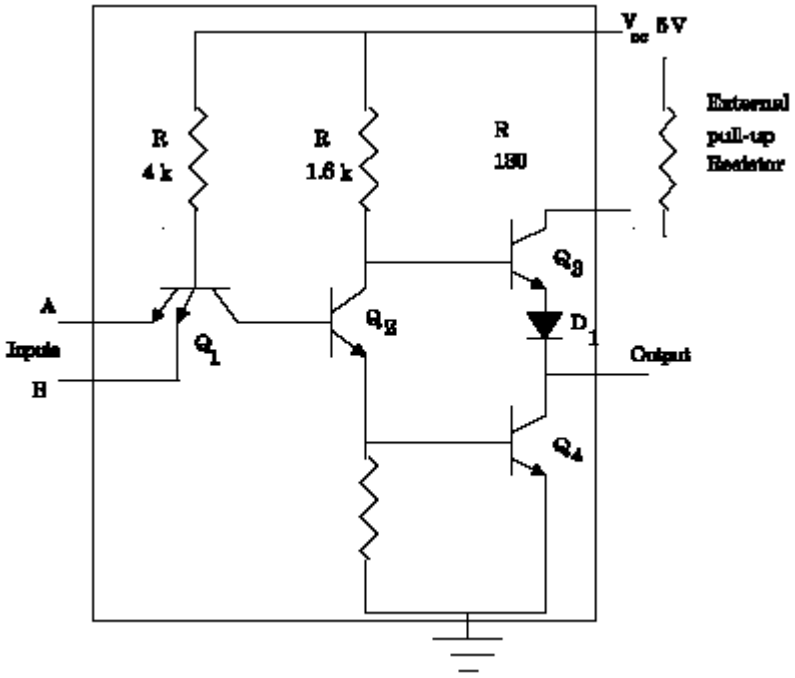
TTL open-collector devices

In some applications, it is necessary to connect the output of the gates together. In such cases, *TTL open-collector* devices are used as the output of standard totempole TTL gates cannot be connected together.

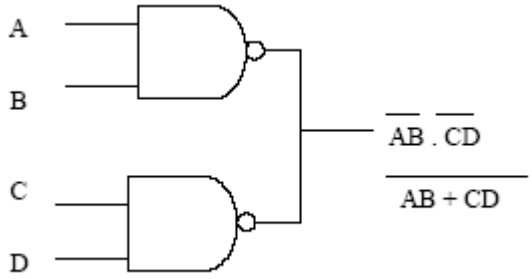
To connect the output of standard totem-pole TTL gates together, we can use an AND gate as below, but this is impractical if more signals need to be ANDed.



To overcome this problem, TTL manufacturers have developed a series of open collector logic devices. As can be seen from the diagram, an external resistor, called a “pull-up” resistor must be connected from the power supply to the output of the device.



Wiring the open-collector NAND gate output directly will accomplish the same result as the circuit earlier. We call such circuit wired AND or wired OR.



IC Data Sheets

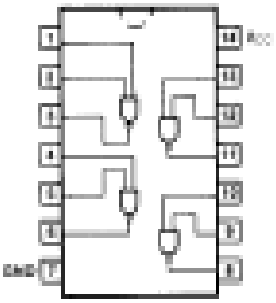
All manufacturers of ICs print data sheets for each type of IC they manufacture. The purpose of the data sheet is to provide the user with information about the IC such as the pin assignments, electrical and mechanical specifications, logic function and ratings.

The following is a sample data sheet of the 7400 IC.

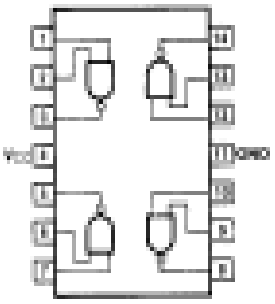
54/7400
54H/74H00
54S/74S00
54LS/74LS00

QUAD 2-INPUT NAND GATE

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5% T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10% T_A = −55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7400PC, 74H00PC 74LS00PC, 74S00PC		9A
Ceramic DIP (D)	A	7400DC, 74H00DC 74LS00DC, 74S00DC	5400DM, 54H00DM 54LS00DM, 54S00DM	6A
Flatpak (F)	A	74LS00FC, 74S00FC	54LS00FM, 54S00FM	3I
	B	7400FC, 74H00FC	5400FM, 54H00FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		8.0		16.8		16		1.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		22		40		36		4.4		V_{IN} = Open	
t_{PLH}	Propagation Delay		22		10	2.0	4.5		10	ns	Figs. 3-1, 3-4	
t_{PHL}			15		10	2.0	5.0		10			

* [c] Limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.