ECEN4618: Experiment #1
Timing circuits with the 555 timer

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The purpose of this lab assignment is to examine operating principles and several practical applications of the 555 integrated-circuit timer. The 555 is capable of producing accurate time delays or oscillations. These functions are needed in many analog, digital or mixed-signal applications. The circuits you design and test in this lab assignment will be applied as building blocks in the lab assignments that follow.

1 The 555 Timer

A functional block diagram of the 555 timer is shown in Fig. 1. Various timing functions can be obtained by connecting resistors and capacitors around the 555.

The 555 consists of two voltage comparators ($C1$ and $C2$), an R-S flip-flop FF, a discharge transistor Q_{14}, a resistive voltage divider (R_3, R_4, R_5), and an output buffer.

The $(-)$ input of the voltage comparator $C1$ is internally connected to the resistive voltage divider. The voltage at the $(-)$ input is equal to $V_H = 2V_{CC}/3$, which is called the *threshold level*. The $(+)$ input of the comparator $C1$ is connected to the external *THRESHOLD* pin (pin 6). The $(+)$ input of the voltage comparator $C2$ is connected to $V_L = V_{CC}/3$, which is called the *trigger level*, while the $(-)$ input is the external *TRIGGER* pin (pin 2). The $(-)$ input of the voltage comparator $C1$ is also available as the *CONTROL* pin (pin 5), which can be used for external adjustment of the threshold and trigger levels.

The comparator $C1$ and $C2$ outputs are the reset R and the set S inputs, respectively, for the flip-flop. When the *TRIGGER* input falls bellow the trigger level V_L, the output of the voltage comparator $C2$ goes high and sets the flip-flop. If the *TRIGGER* input is above the trigger level, and the *THRESHOLD* input is above the threshold level, the output of the voltage comparator $C1$ is high and the flip-flop is reset. The flip-flop output $\overline{Q}$ drives the discharge transistor Q_{14}, and an inverting output buffer: when the flip-flop output $\overline{Q}$ is high, Q_{14} is on and the voltage at the *OUTPUT* pin (pin 3) is low (close to zero); when the flip-flop output $\overline{Q}$ is low, Q_{14} is off and the *OUTPUT* is high (close to V_{CC}). The output driver is capable of sinking or sourcing current up to about 200mA. The collector of the discharge transistor Q_{14} is available at the *DISCHARGE* pin (pin 7).

The active-low *RESET* input (pin 4) to the flip-flop can be used to disable the timer operation and ensure that the *OUTPUT* stays at zero, regardless of the comparator outputs.

The dc supply voltage can be between $V_{CC} = 5$V and $V_{CC} = 15$V. It should be connected between the *VCC* (pin 8) and the *GROUND* (pin 1). With a 5V supply, the output, and the *RESET* input levels are compatible with standard TTL or CMOS digital logic circuits.

2 Basic Applications

With the addition of an external capacitor and one or two external resistors, the 555 can provide two basic functions: *monostable operation*, where an output pulse of fixed duration is initiated by a short negative pulse on the *TRIGGER* input, and *astable operation*, where the timer produces periodic output pulses.

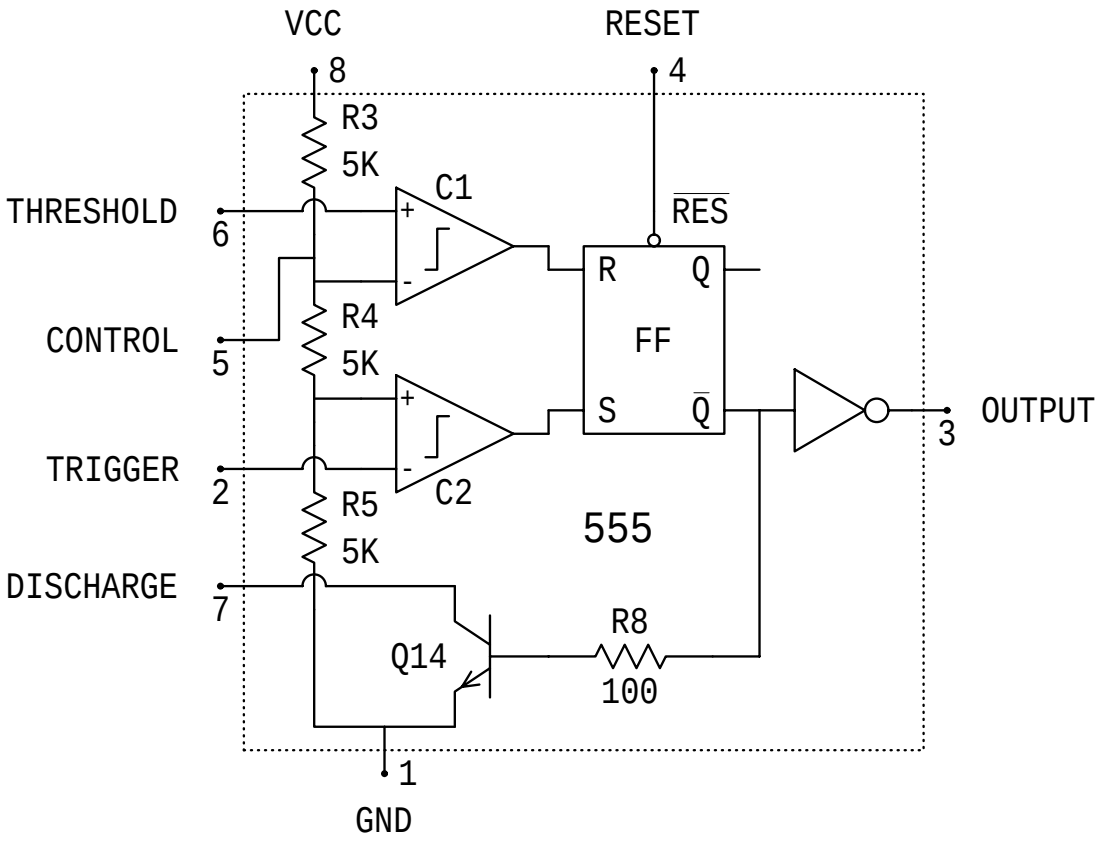


Figure 1: Functional block diagram of the 555 integrated-circuit timer.

2.1 Monostable operation

The circuit connection for the monostable operation is shown in Fig. 2. The corresponding waveforms are shown in Fig. 3.

Initially, the *TRIGGER* input voltage is above the trigger level. Therefore, the flip-flop is reset, $\overline{Q}$ is high, *OUTPUT* is low, and the discharge transistor Q_{14} is on. Since Q_{14} is on, and the *DISCHARGE* pin is connected to the *THRESHOLD* input, the capacitor C is discharged. The *THRESHOLD* voltage is equal to the saturation V_{CES} voltage of the discharge transistor Q_{14}, which is close to zero. Note that the *CONTROL* input is left open so that the trigger and the threshold levels are $V_L = V_{CC}/3$ and $V_H = 2V_{CC}/3$. In applications where the *CONTROL* input is not used, it is a good practice to connect a noise-decoupling capacitor $C_d = 10 - 100$nF from the *CONTROL* pin to ground. This provides a low-impedance path for ac noise to ground and ensures that the trigger and the threshold levels stay at the expected dc levels. Note also that the *RESET* input is high (tied to V_{CC}) so that the timer operation is enabled.

At $t = t_0$, a short pulse takes the *TRIGGER* input below the trigger level. This sets the flip-flop, the *OUTPUT* goes high, and the discharge transistor Q_{14} is turned off. Since Q_{14} is off, the capacitor C starts to charge up through the resistor R toward V_{CC}. After the interval T_w, the capacitor voltage reaches the threshold level $V_H = 2V_{CC}/3$, the flip-flop is reset, the output returns to low, and the discharge transistor Q_{14} is turned on again. When Q_{14} is turned on, its collector current quickly discharges the capacitor toward zero, and the circuit is again in the initially assumed steady state. Another short pulse on the *TRIGGER*

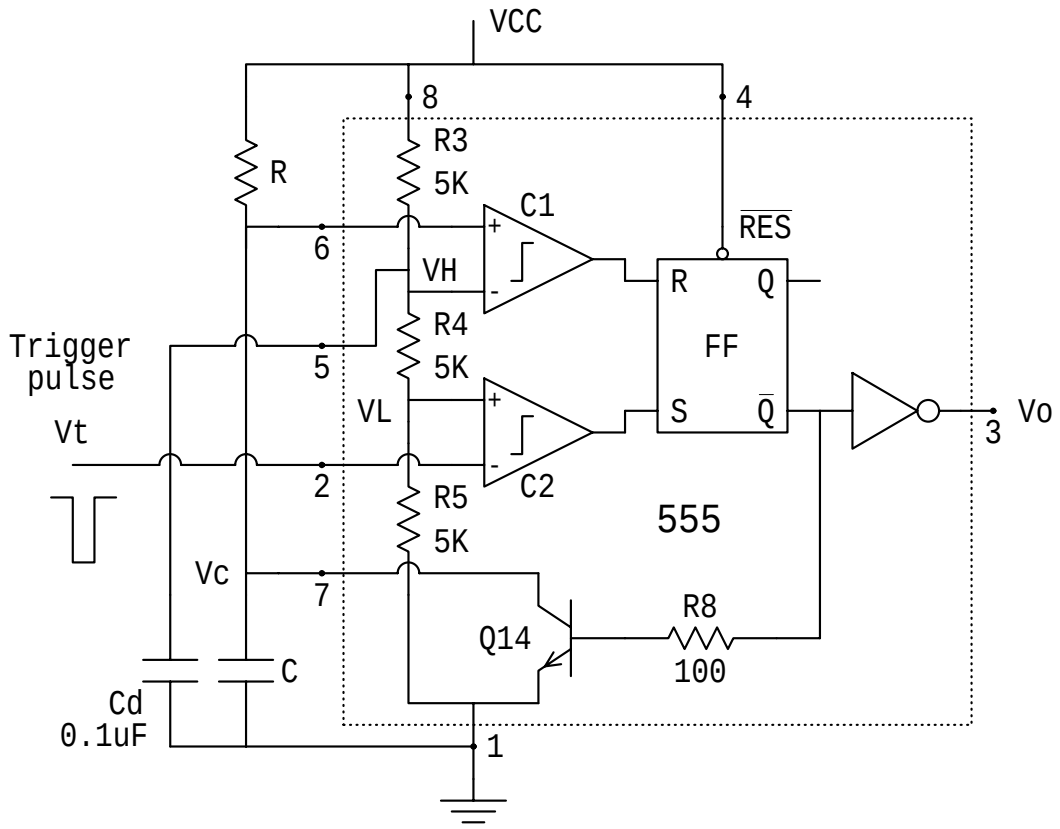


Figure 2: Monostable circuit built around the 555 timer.

input would be needed to produce another output pulse of duration T_w. Without the external trigger input, the output always stays low, which is why the circuit is called monostable, or one-shot.

The basic design specification for a monostable circuit is the output pulse duration T_w. The pulse duration depends on the selection of the external R and C components. Therefore, we would like to determine how T_w depends on R and C. The solution will be found here in more general terms, so that the results can be applied to other similar problems.

Consider the $R-C$ circuit in Fig. 4, where at $t=0$, the initial capacitor voltage is $v_c(0)=V_o$. For $t \geq 0$, the circuit is described by the first-order differential equation:

$$\frac{dv_c}{dt} + \frac{v_c}{RC} = \frac{V_1}{RC}\,, \;\; v_c(0) = V_o\,. \tag{1}$$

where V_1 is a dc voltage. If we let the capacitor charge (or discharge) completely (for $t \to \infty$), the final capacitor voltage is $v_c(1) = V_1$). The solution to Eq. 1 is given by[1]:

$$v_c(t) = V_1 + (V_o - V_1)e^{-t/\tau}\,, \;\; \tau = RC\,. \tag{2}$$

Now, if we want to know *when* the capacitor voltage reaches a certain threshold V_{TH}, we can use the solution given by Eq. 2 as follows:

$$v_c(t) = V_{TH} = V_1 + (V_o - V_1)e^{-t/\tau}\,, \tag{3}$$

[1]This should be well known ...

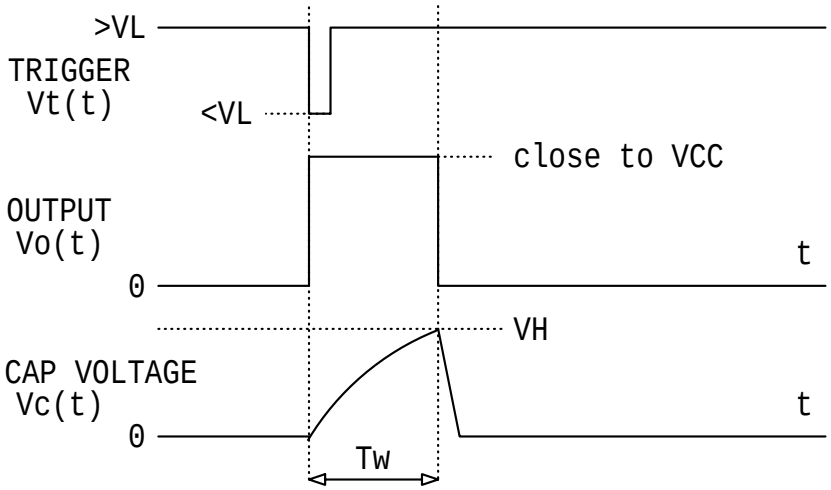


Figure 3: Typical waveforms in the monostable circuit with the 555 timer.

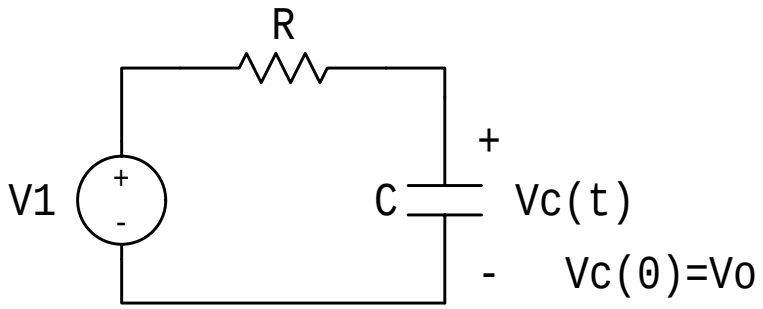


Figure 4: Capacitor charging (or discharging) circuit.

$$e^{t/\tau} = \frac{V_o - V_1}{V_{TH} - V_1}\,, \tag{4}$$

Therefore,

$$t = \tau \ln\left(\frac{V_o - V_1}{V_{TH} - V_1}\right)\,. \tag{5}$$

Let us apply the above solution to the problem of finding the output pulse width T_w as a function of the time constant $\tau = RC$. From Figs. 2 and 3, we have that $V_o \approx 0$, $V_1 = V_{CC}$, and $V_{TH} = V_H = 2V_{CC}/3$, so that

$$T_w = \tau \ln\left(\frac{-V_{CC}}{2V_{CC}/3 - V_{CC}}\right) = \tau \ln 3 \approx 1.1RC\,. \tag{6}$$

For a specified T_w, Eq. 6 gives only one constraint for R and C. Further constraints, which are less obvious, can nevertheless make a difference between a good and a bad design. Here is a summary of considerations that should be taken into account when selecting the values for R and C:

1. When the output is in the low steady-state, the discharge transistor Q_{14} is on, and we assume that the transistor is saturated so that the voltage at the *DISCHARGE* and the *THRESHOLD* pins is $V_{CES} \approx 0$. The current through the resistor R is then given by:

$$I_R = \frac{V_{CC} - V_{CES}}{R} \approx \frac{V_{CC}}{R} \,. \tag{7}$$

   If R is smaller, I_R is higher, and the timer takes more power from the dc supply V_{CC}. Also, if R is too small, the discharge transistor Q_{14} will come out of saturation, and the voltage at the *DISCHARGE/THRESHOLD* pins can be significantly higher than zero. As a result, in addition to the wasteful power loss, we may have a significant error in the output pulse width T_w.

2. The input currents to the comparators $C1$ and $C2$ are small, but not equal to zero. From the data sheets, we read that the threshold input current can be as high as 250nA, and that the trigger input current can be as high as 0.9μA. Even worse, the threshold/trigger input current is not a very reliable parameter, because it can vary in a wide range from one device to another. For example, as given in the data sheets, the typical value for the threshold current is only 30nA, although it can be as high as 250nA. In addition, the threshold input current (which is the base current of the internal BJT Q_1 (see data sheets), certainly has a very strong temperature dependence, which would further invalidate any design based on the precise knowledge of this current.

   In the analysis for T_w, we assumed that the threshold input current is zero. In a good design, we should attempt to make the contribution of the threshold current negligible. Therefore, R should be selected so that I_R is always much greater than the threshold input current, which gives a maximum R that can be used in the circuit. The condition:

$$I_R >> 250\text{nA} \tag{8}$$

   results in

$$R << \frac{V_{CC}}{250\text{nA}} \,. \tag{9}$$

   For $V_{CC} = 10$V, we need $R << 40M\Omega$. A practical limit would include a factor of 10, so: $R < 4M\Omega$.

3. At the end of the output pulse, the discharge transistor Q_{14} is turned on to discharge the capacitor C toward zero. The discharge is not instantaneous. During the discharge transient, Q_{14} operates in the active region with approximately constant collector current I_C. Assuming that $I_C >> I_R$, which is the case if R was selected properly (see comment 1. above), the discharge takes

$$t_{\text{discharge}} \approx \frac{C}{I_C} \frac{2V_{CC}}{3} \tag{10}$$

   If the discharge time is too long, the timer may not be ready in time to respond to another trigger pulse at the *TRIGGER* input.

4. Parasitic capacitances on the circuit board and on the inputs to the integrated circuit are usually around $5 - 10$pF. These values are not known in advance, may vary from one set-up to another, and from one component to another. Therefore, to avoid errors, the capacitance C should be much greater than the parasitic capacitances.

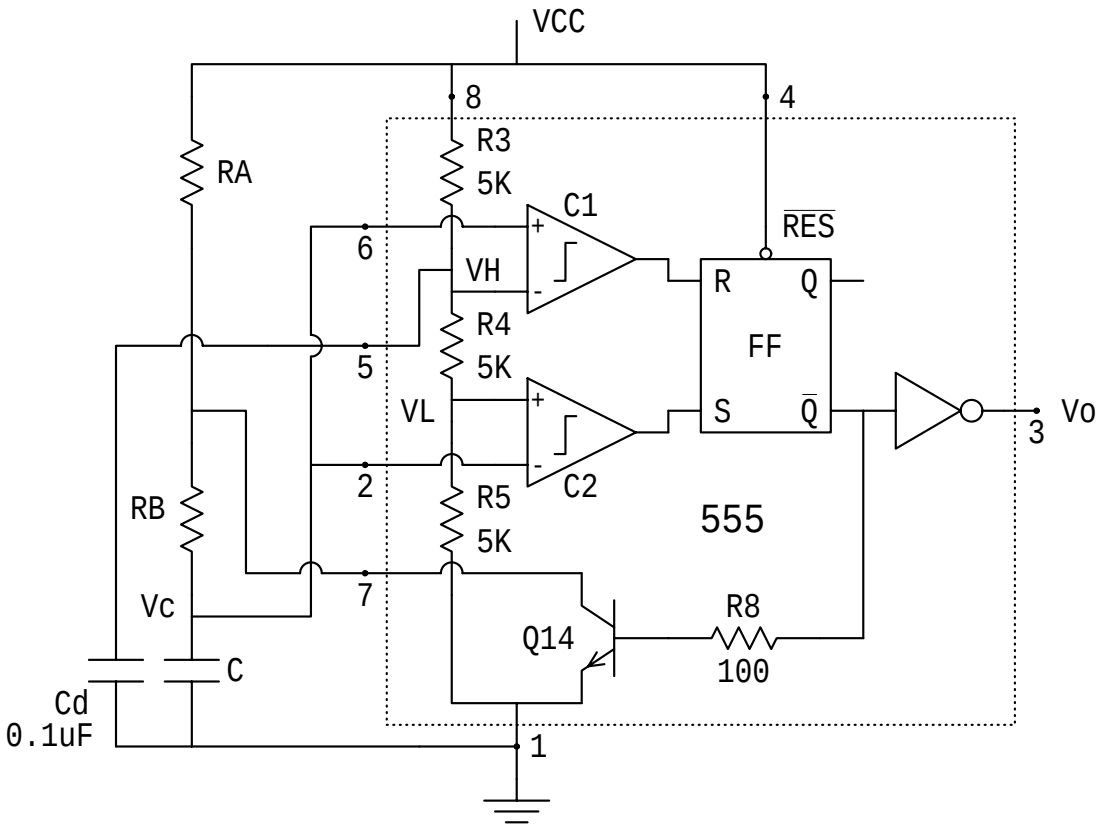


Figure 5: Astable circuit (pulse generator) built around the 555 timer.

2.2 Astable operation

With the addition of an external capacitor and two external resistors, the 555 can be configured to produce a periodic pulsating waveform at the output, without any external trigger pulses. The basic configuration for the astable operation is shown in Fig. 5, together with typical steady-state waveforms in Fig. 6.

The key difference between the monostable and the astable operation is that the *TRIGGER* input is connected together with the *THRESHOLD* input so that the timer triggers itself during operation. The capacitor C is periodically charged and discharged between the trigger level $V_L = V_{CC}/3$ and the threshold level $V_H = 2V_{CC}/3$. Suppose that at $t = 0$ the output is high, and the discharge transistor Q_{14} is off. The capacitor is charged through R_A and R_B until the capacitor voltage reaches $V_H = 2V_{CC}/3$ at $t = t_H$. At this point, the flip-flop is reset, the output goes low, and the discharge transistor Q_{14} is turned on. As a result, C is discharged through R_B and the saturated discharge transistor Q_{14}. At $t = t_H + t_L = T_p$, the capacitor voltage drops to $V_L = V_{CC}/3$, the flip-flop is set again, the output voltage goes high and the discharge transistor is turned off, starting another period.

The times t_H and t_L can be determined using the same approach used to determine T_w in the monostable circuit. The results are:

$$t_L = R_B C \ln 2 \approx 0.693 R_B C \tag{11}$$

$$t_H = (R_A + R_B) C \ln 2 \approx 0.693 (R_A + R_B) C \tag{12}$$

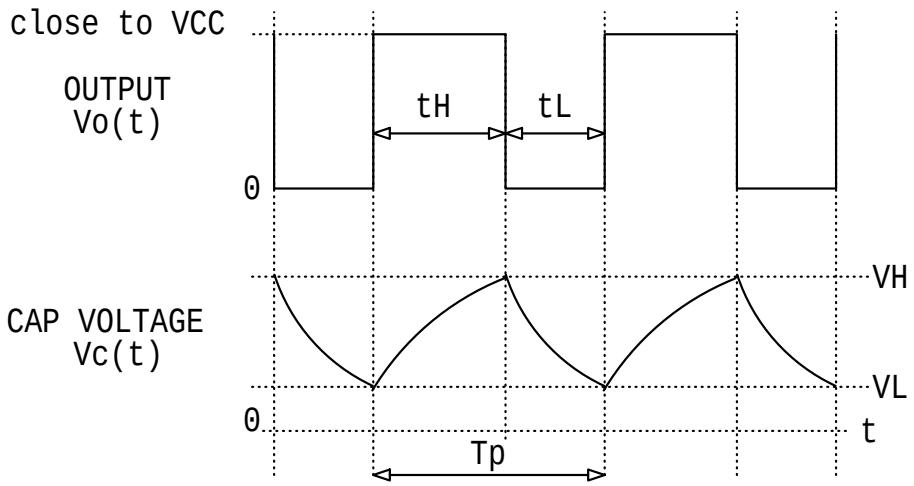


Figure 6: Typical waveforms in the astable circuit with the 555 timer.

The period of the waveforms is

$$T_p = (R_A + 2R_B)C \ln 2\,. \tag{13}$$

and the frequency is $f_p = 1/T_p$. The output waveform duty cycle D is:

$$D = \frac{t_H}{T_p} = \frac{t_H}{t_H + t_L} = \frac{R_A + R_B}{R_A + 2R_B}\,. \tag{14}$$

Since $t_H > t_L$, the duty cycle must be greater than 50% in this configuration.

3 Experiment

The experiment has three parts. Unless otherwise noted, use $V_{CC} = 15$V supply voltage in all experiments.

Before you start constructing any circuit on the protoboard, make sure that the DC supply voltage is properly decoupled with an electrolytic capacitor of at least 10μF. Also, your first step in putting the circuit together on the protoboard should be to connect the DC supply pins (V_{CC} and ground) and to place a ceramic decoupling capacitor of at least $0.1\mu F$ between the supply pins. Errors in connecting the supply voltages can easily lead to permanent damages to the ICs. Also, without proper DC voltage decoupling, many seemingly well designed and correctly connected circuits fail to operate properly.

3.1 Monostable circuit design and experimental verification

Design the monostable circuit of Fig. 2 to produce the output pulse of duration $T_w = 30\mu$s, $\pm 2\%$, for each short trigger pulse. To verify operation of the monostable, generate the trigger pulses from a laboratory pulse generator. If necessary, i.e., if the lab signal generator cannot produce the required trigger pulses, use the circuit you designed in the prelab problem #2. Verify the amplitude, the frequency and the pulse width of the trigger signal **before** connecting the trigger pulses to the *TRIGGER* input of the monostable. You must not apply a voltage outside the supply-voltage range (zero to V_{CC}) to any pin of the 555 !

In the report, show the circuit diagram with labeled component names and values, together with a labeled oscilloscope plot that verifies operation of the monostable. Show waveforms of the *TRIGGER* input, the capacitor voltage, and the *OUTPUT*. Label the waveforms with signal names, and significant voltage levels, and time intervals. Measure and record the output pulse duration, and the frequency of the trigger pulses used in the test. Correct the design if the error in the length of the output pulse is more than $\pm 2\%$.

Explain what happens if another trigger pulse comes before the end of the output pulse. Show the same scope waveforms as above, and explain the results, if the frequency of the trigger pulses is 50kHz.

3.2 Astable circuit design and experimental verification

Design the astable circuit of Fig. 5 to produce periodic output pulses with frequency $f_p = 40$kHz ($\pm 2\%$), and with the width of the LOW output that satisfies $0.5\mu s < t_L < 1\mu s$.

In this part, you should observe that the actual f_p is significantly lower that the theoretical value from your paper design. Your task is to investigate and explain the source of the error. Hint: look at the voltage waveform across the capacitor. Why doesn't it oscillate between $V_L = V_{CC}/3$ and $V_H = 2V_{CC}/3$?

Correct the component values to meet the specifications.

Show a complete circuit diagram with labeled component names and values. Attach labeled scope waveforms of the capacitor voltage and the output. Measure and record the actual frequency f_p and the width t_L.

Measure and record the actual frequency f_p and the width t_L for $V_{CC} = 10$V and $V_{CC} = 5$V. Can the design meet the specs for the range of supply voltages between 5V and 15V ?

3.3 Design of a "touch-tone" circuit

It is required to design a circuit where pressing a push-button switch (or touching a jumper wire on the proto-board) produces a 50kHz ($\pm 5\%$) tone (square-wave waveform with $50 \pm 1\%$ duty ratio, ($t_H = t_L$, $1/(t_H + t_L) = 20$kHz) that lasts 0.1 ($\pm 5\%$) seconds.

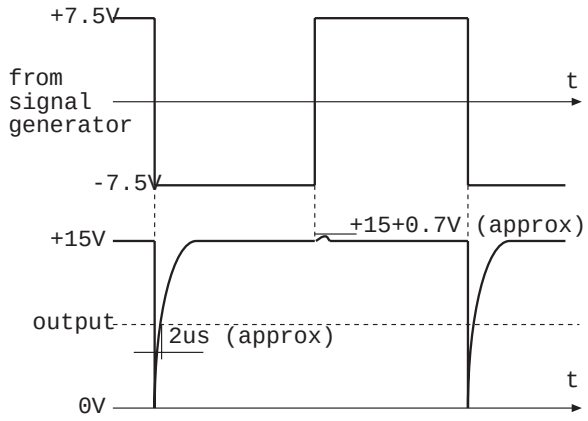
Show the complete circuit diagram with labeled component names and values. Report the results of experimental verification of your design. Measure the actual tone frequency, the actual duty ratio, and the actual duration of the tone.

4 Prelab Assignment

The prelab assignment is due in the lab on the day when you start working on the experiment.

1. Derive expressions (11) and (12).

2. Suppose a signal generator produces a square-wave signal of ± 7.5V amplitude, and $f = 10$kHz frequency, as shown below. Using a resistor, a diode, and a capacitor, and a $V_{CC} = 15$V DC power supply, design a circuit that would produce output pulses as shown in the figure below. Find the capacitance and the resistance values. This circuit can be used to generate the short trigger pulses required in Section 3.1 of the experiment.



3. Design the monostable circuit of Fig. 2 to produce an output pulse of duration T_w for each short trigger pulse, as specified in Section 3.1. Show the circuit diagram with labeled component names and values. Do a PSpice transient simulation to verify the design and attach the simulation results (one page of waveforms). A 555 Spice model is available with the evaluation version of PSpice. This is a paper design for the experimental task described in Section 3.1.

4. Design the astable circuit of Fig. 5 to produce periodic output pulses with frequency f_p, and with the width of the LOW output $t_L = 0.75\mu$s, as specified in Section 3.2. Show a complete circuit diagram with labeled component names and values. Do a PSpice transient simulation to verify the design and attach the simulation results (one page of waveforms). This is a paper design for the experimental task described in Section 3.2.

5. Design the "touch-tone" circuit as specified in Section 3.3. Show a complete circuit diagram with labeled component names and values.

Make a copy of your prelab work so that you can use it during the Lab session.