INTERFACE WITH ANALOG WORLD

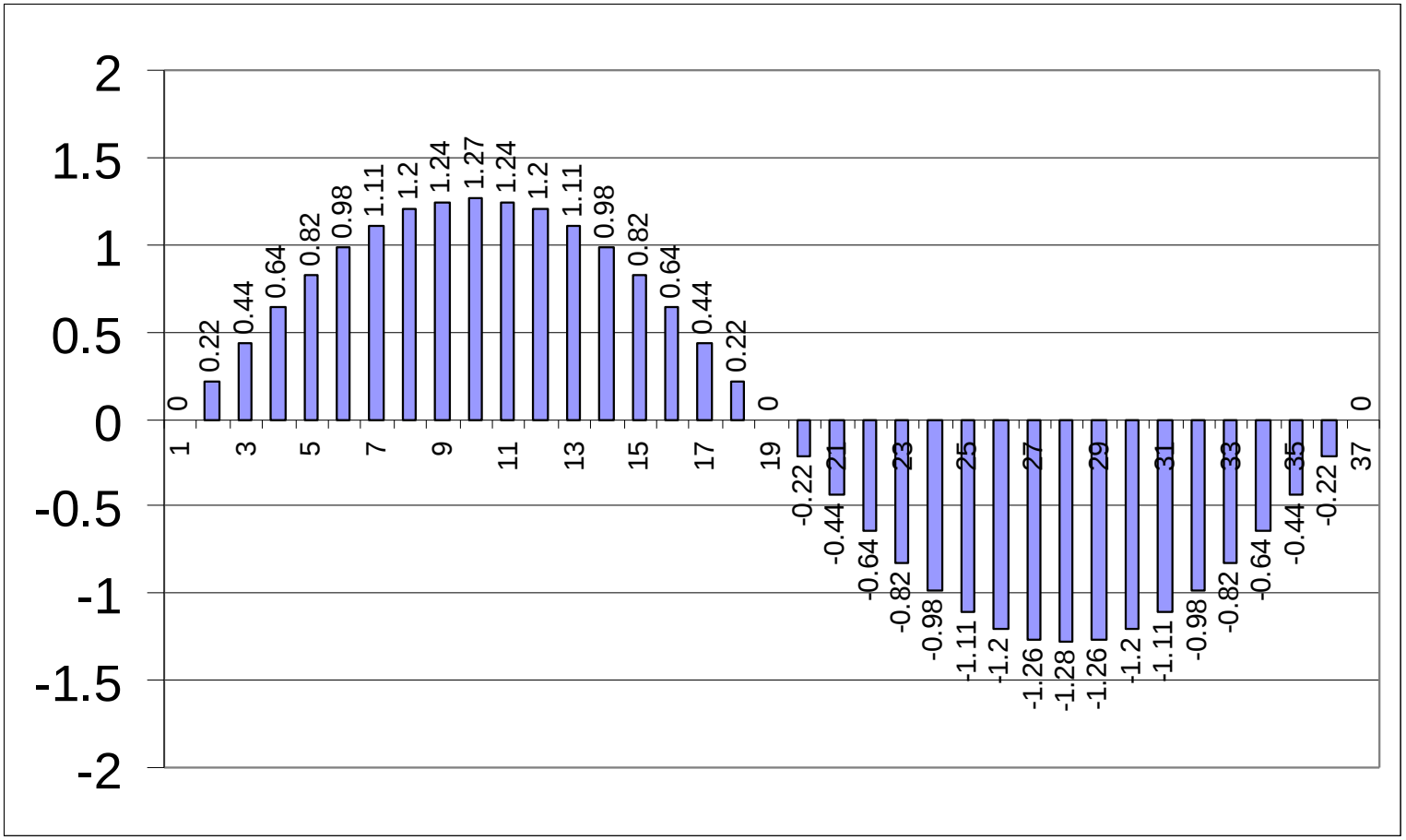
- Conversion between analog and digital signals is common. The following aspects will be examined:
  - DAC and ADC
  - Troubleshooting
- Different conversion methods
  - Analog multiplexing
  - DSP

What is DSP?

The analog waveform is sliced into equal segments and the waveform amplitude is measured in the middle of each segment

The collection of measurements make up the digital representation of the waveform

What is DSP?


2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
0
0.22
0.44
0.64
0.82
0.98
1.11
1.2
1.24
1.27
1.24
1.2
1.11
0.98
0.82
0.64
0.44
0.22
0
-0.22
-0.44
-0.64
-0.82
-0.98
-1.11
-1.2
-1.26
-1.28
-1.26
-1.2
-1.11
-0.98
-0.82
-0.64
-0.44
-0.22
0
1
3
5
7
9
11
13
15
17
19
21
23
25
27
29
31
33
35
37

Converting Analog into Digital
Electronically

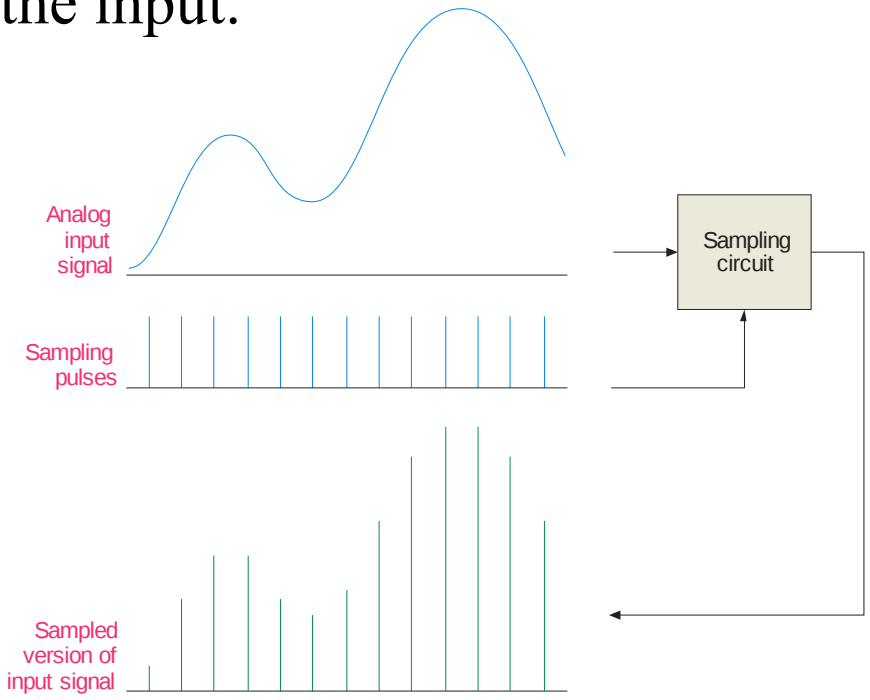
The device that does the conversion is called an Analog to Digital Converter (ADC)

There is a device that converts digital to analog that is called a Digital to Analog Converter (DAC)

Sampling

Most input signals to an electronic system start out as analog signals. For processing, the signal is normally converted to a digital signal by sampling the input.

Before sampling, the analog input must be filtered with a low-pass anti-aliasing filter. The filter eliminates frequencies that exceed a certain limit that is determined by the sampling rate.



Anti-aliasing Filter

To understand the need for an anti-aliasing filter, you need to understand the sampling theorem which essentially states:

In order to recover a signal, the sampling rate must be greater than twice the highest frequency in the signal.

Stated as an equation, $f_{sample} > 2f_{a(max)}$

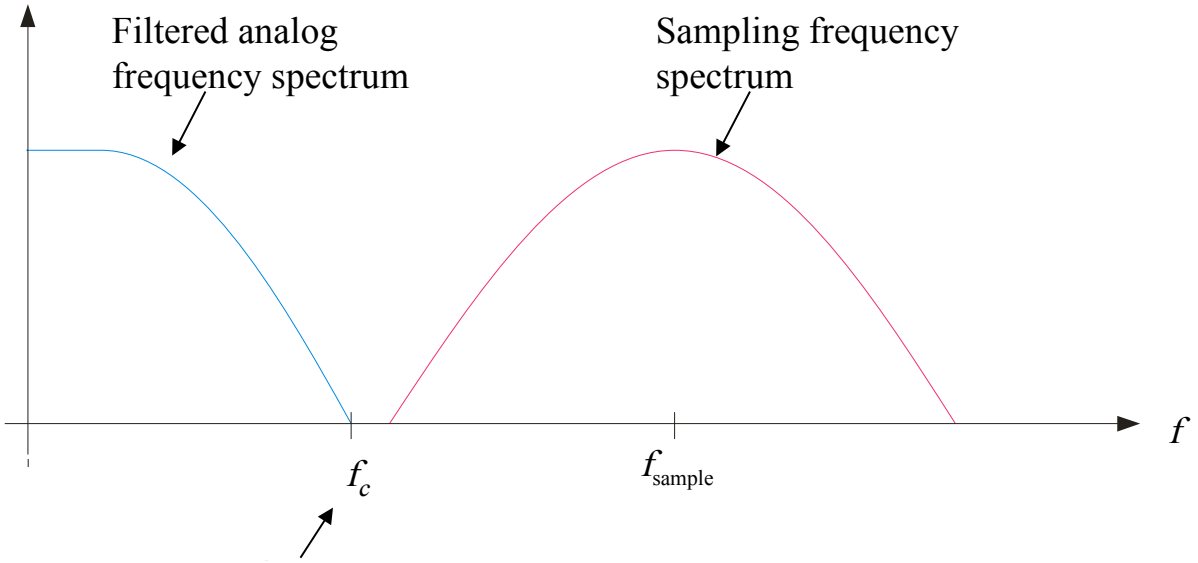
where f_{sample} = sampling frequency

$f_{a(max)}$ = highest harmonic in the analog signal

If the signal is sampled less than this, the recovery process will produce frequencies that are entirely different than in the original signal. These "masquerading" signals are called aliases.

Anti-aliasing Filter

The anti-aliasing filter is a low-pass filter that limits high frequencies in the input signal to only those that meet the requirements of the sampling theorem.



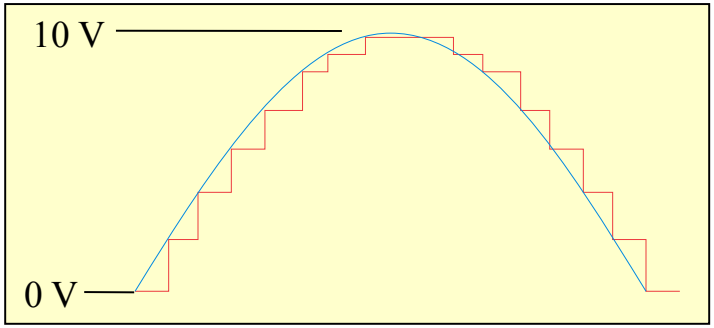
The filter's cutoff frequency, f_c, should be less than ½ f_{sample}.

Analog-to-Digital Conversion

To process naturally occurring analog quantities with a digital system, the analog signal is converted to digital form after the anti-aliasing filter.

The first step in converting a signal to digital form is to use a sample-and-hold circuit. This circuit samples the input signal at a rate determined by a clock signal and holds the level on a capacitor until the next clock pulse.

A positive half-wave from 0-10 V is shown in blue. The sample-and-hold circuit produces the staircase representation shown in red.

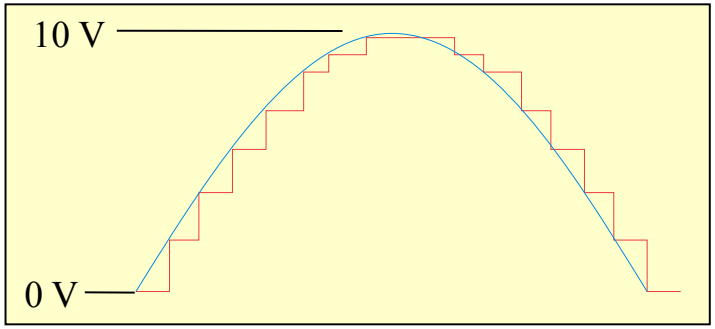


Analog-to-Digital Conversion

The second step is to **quantize** these staircase levels to binary coded form using an analog-to-digital converter (ADC). The digital values can then be processed by a digital signal processor or computer.

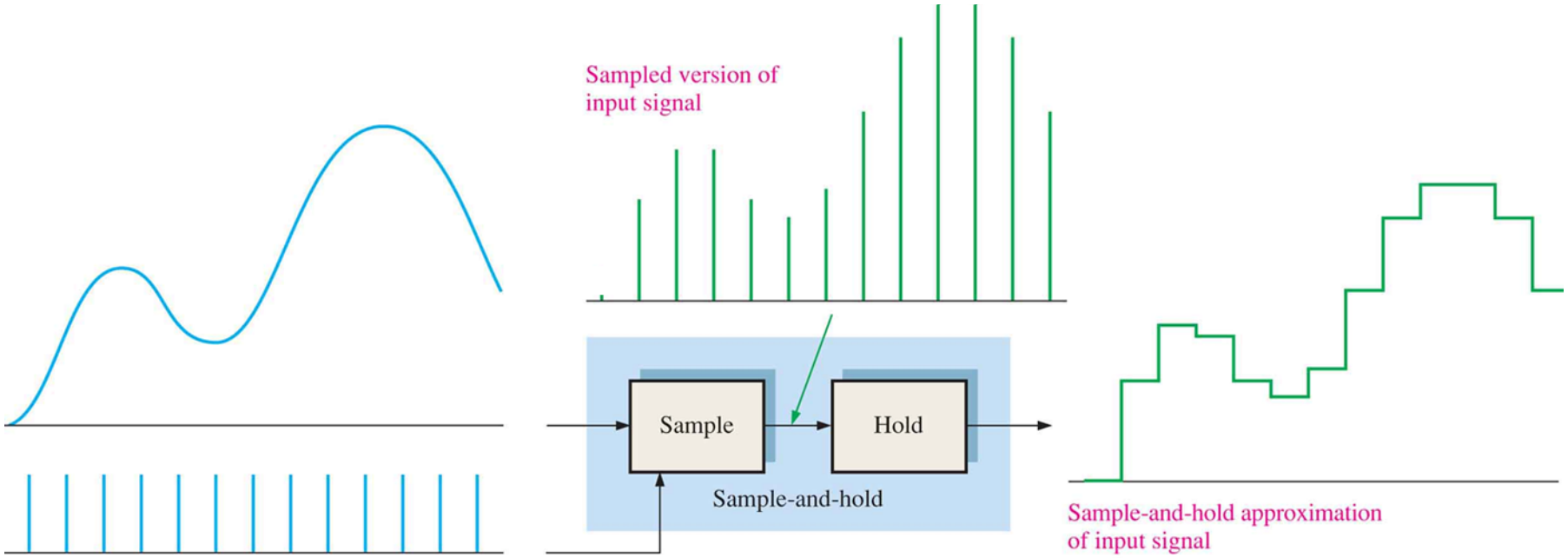
Example What is the maximum unsigned binary value for the waveform?

Solution 10 V = 1010_2 V. The table lists the quantized binary values for all of the steps.



0.0000
10.0001
100.0001
101.1110
111.0111
1000.1011
1001.1001
Peak = 10 V → 1010.0000
1010.0000
1001.1001
1000.1011
111.0111
101.1110
100.0001
10.0001
0.0000

Figure 12.5 Illustration of a sample-and-hold operation.



Note: I've modified this figure by making the first sample much closer to 0 than is shown in the original figure.

Analog-to-Digital Conversion (Quantization)

The final step is to **quantize** these staircase levels to binary coded form using an analog-to-digital converter (ADC). The digital values can then be processed by a computer.

Number of Bits and Accuracy

- During the quantization process, the ADC converts each sampled value of the analog signal into a binary code.
- The more bits that are used in this code, the more accurate is the representation of the original signal.
- The following slides show an example of how using 2 bits (Figures 12.7 and 12.8) results in much less accuracy than using 4 bits (Figures 12.9 and 12.10).

Figure 12.7 Light gray = original waveform. Blue = Sample-and-hold output waveform. Pink = Four quantization levels if we use 2 bits to quantize. **Next figure shows the result of this 2-bit quantization.**

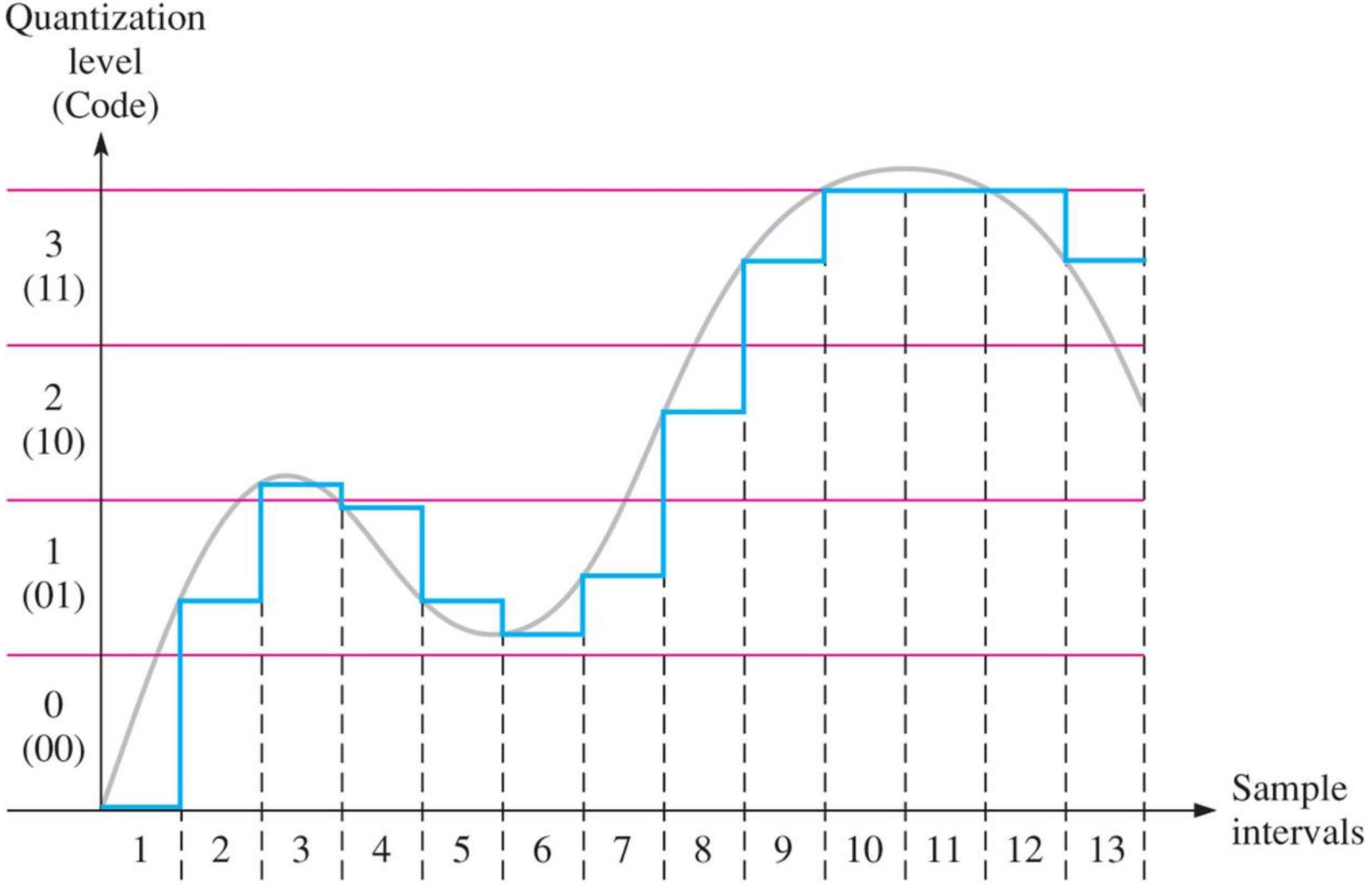


Figure 12.8 Light gray = original waveform. Blue = Reconstructed waveform using four quantization levels (2 bits).

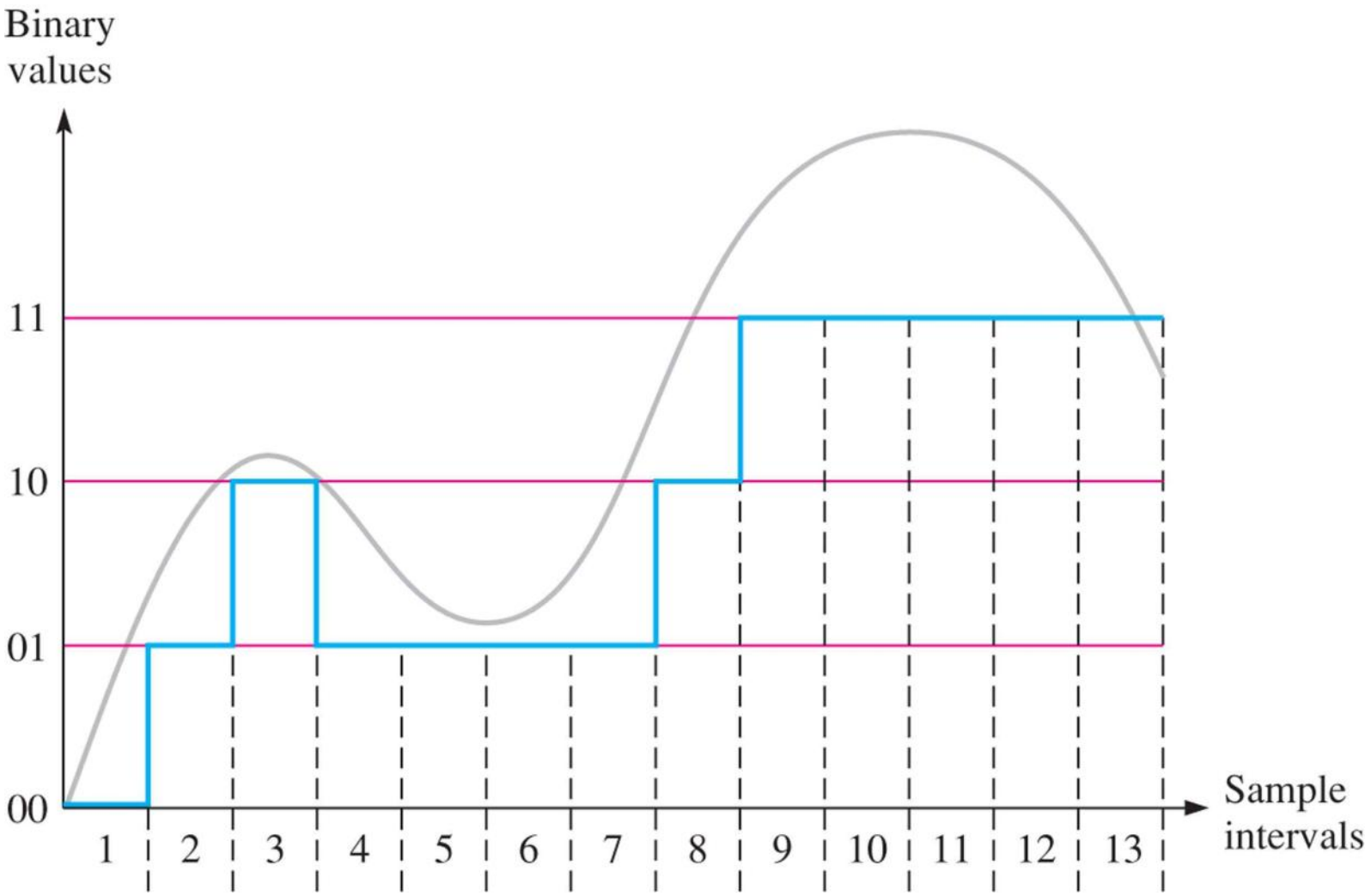


Figure 12.9 Light gray = original waveform. Blue = Sample-and-hold output waveform. Pink = Sixteen quantization levels if we use 4 bits to quantize. **Next figure shows the result of this 4-bit quantization.**

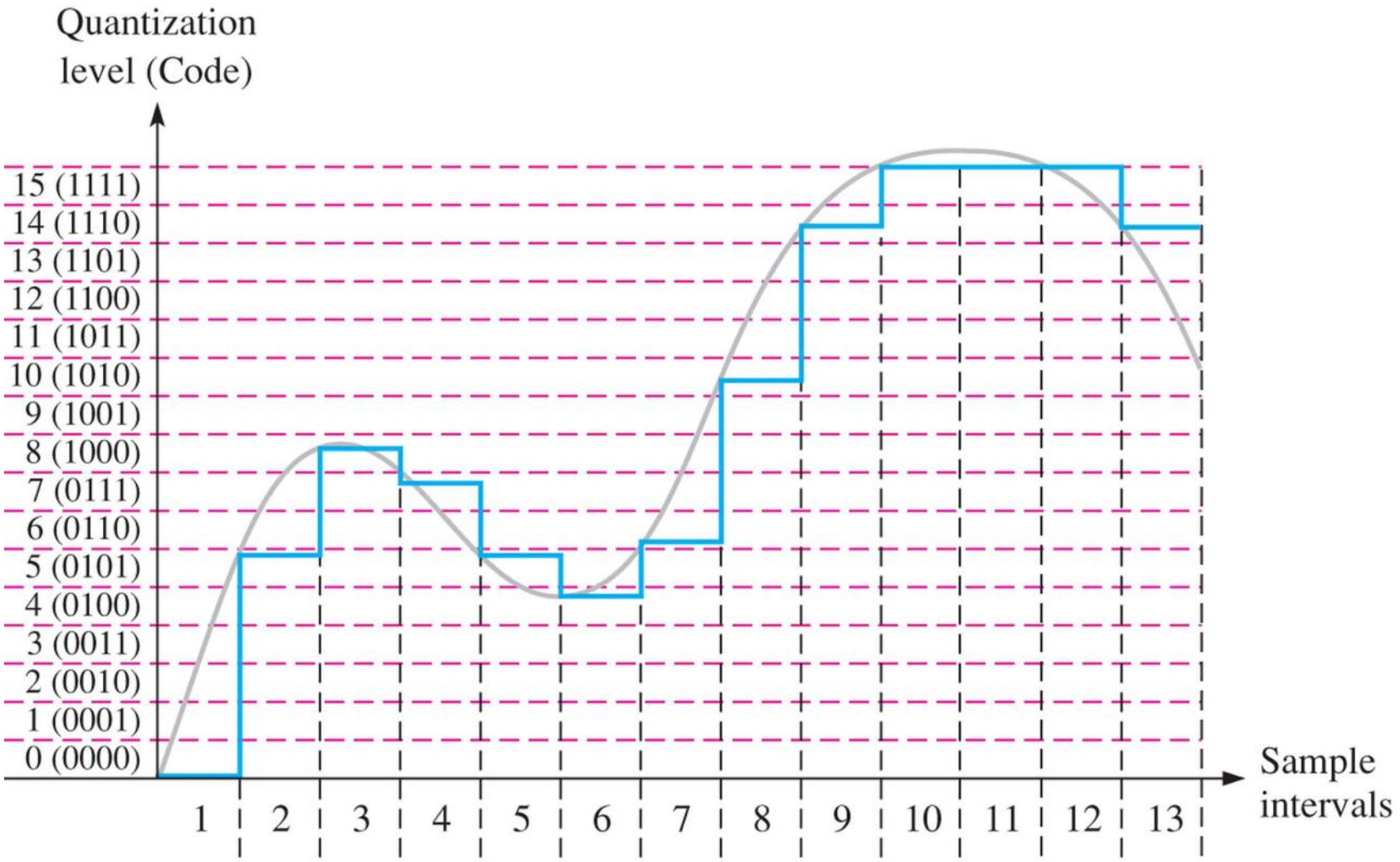
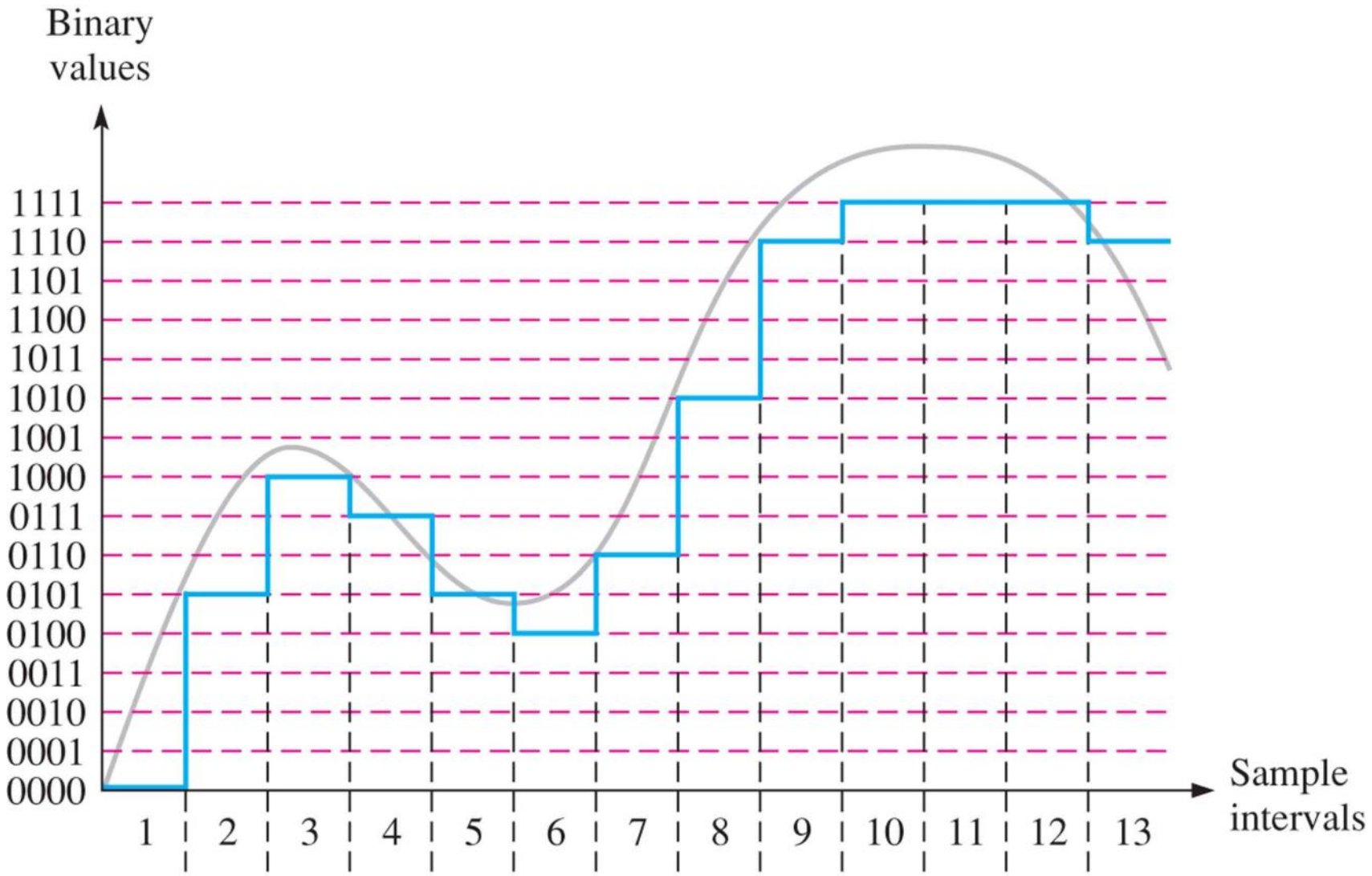


Figure 12.10 Light gray = original waveform. Blue = Reconstructed waveform using sixteen quantization levels (4 bits).



Resolution

- Several common ways of specifying an ADC's resolution:
  - Number of bits, n
  - Number of output codes, $= 2^n$, or number of steps in the output, $= 2^n - 1$
  - **Percentage resolution**, $= 1 / (2^n - 1)$, expressed as a percentage
  - Step size, $= V_{ref} / 2^n$

Resolution: Examples

	Formula	4-bit ADC	10-bit ADC
Number of bits	n	4	
Number of output codes	2^n	16	
Number of steps in the output	$2^n - 1$	15	
Percentage resolution	$1 / (2^n - 1)$	6.67%	
Step size (assuming 5 V reference voltage)	$V_{ref} / 2^n$	312.5 mV	

11-1 Interfacing With the Analog World

- A review of the difference between digital and analog quantities
  - Digital quantities – values can take on one of two possible values. Actual values can be in a specified range so the exact value is not important.

    Example: 0 V to 0.8 V = logic 0
    2 V to 5 V = logic 1

  - Analog quantities – values can take on an infinite number of values, and the exact value is important.

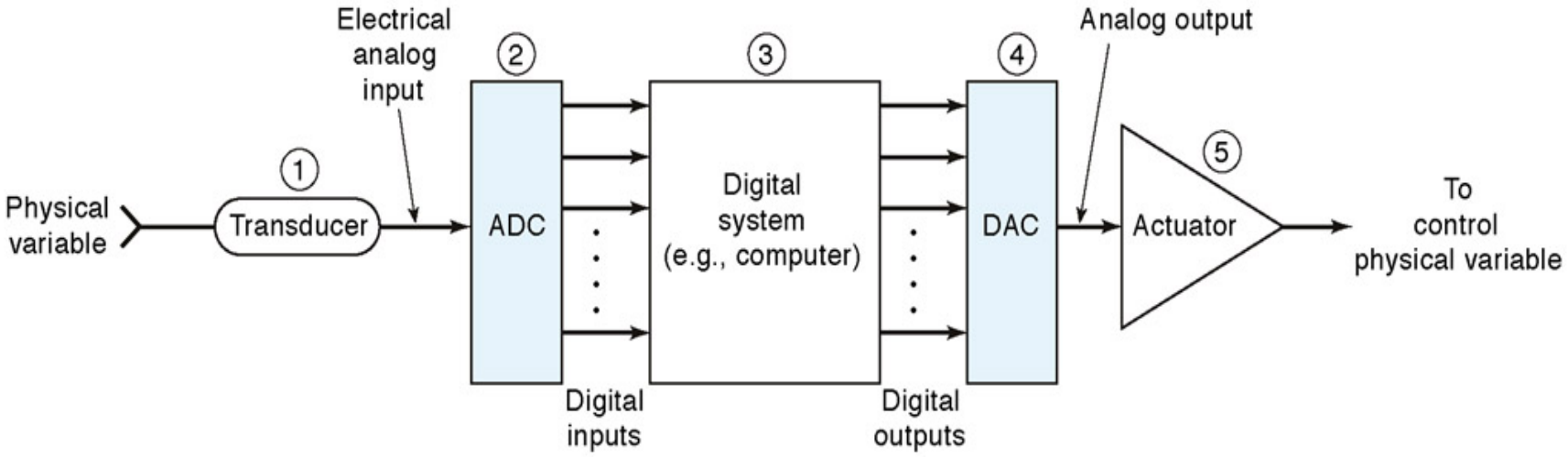
    Example: 2.76 V or 27.6 ^{0}C

11-1 Interfacing With the Analog World

ADC and DAC are used to interface a computer to the analog world so that the computer can monitor and control a physical variable.

There are FIVE elements involved:

- Transducer: convert physical qty to elect. Qty (thermistor, flow meters, tachometers)
- ADC: convert analog value to binary
- Computer: stores digital value and process according to program instruction
- DAC: convert binary value to analog
- Actuator: control physical variables based on the signal from DAC

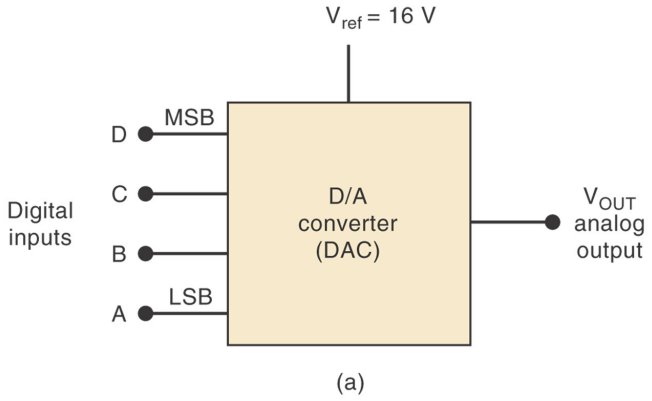


11-2 Digital to Analog Conversion

- The conversion process:
  - Digital code (binary or BCD) is converted to a proportional voltage or current
  - V_{ref}, Reference voltage determines the max output DAC can output
- Analog (pseudo analog) output

Analog output = K x digital input

- Input weights; weighted according to their position in the binary number
- Resolution (step size)
  - What resolution means; smallest change that can occur in the analog output



(a)

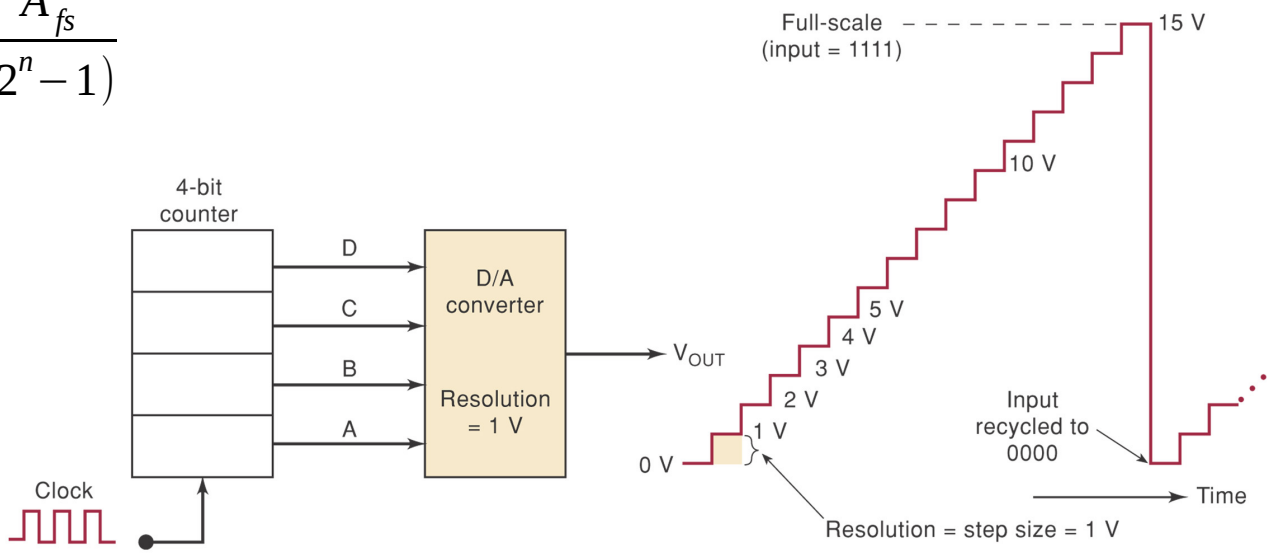
D	C	B	A	V_{OUT}	
0	0	0	0	0	Volts
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	6	
0	1	1	1	7	
1	0	0	0	8	
1	0	0	1	9	
1	0	1	0	10	
1	0	1	1	11	
1	1	0	0	12	
1	1	0	1	13	
1	1	1	0	14	
1	1	1	1	15	Volts

(b)

11-2 Digital to Analog Conversion

- The output from 4-bit binary counter provide input to DAC, the DAC output is a staircase waveform that goes up 1V per step.
- When counter is at 1111, the DAC output is maximum value of 15V.
- When counter is recycles to 0000, the DAC returns to 0V.
- *The resolution or step size is the size of jumps in the staircase waveform, in this case, each step is 1V.*

$$resolution = K = \frac{A_{fs}}{\left(2^n - 1\right)}$$



11-2 Digital to Analog Conversion

EXAMPLE:

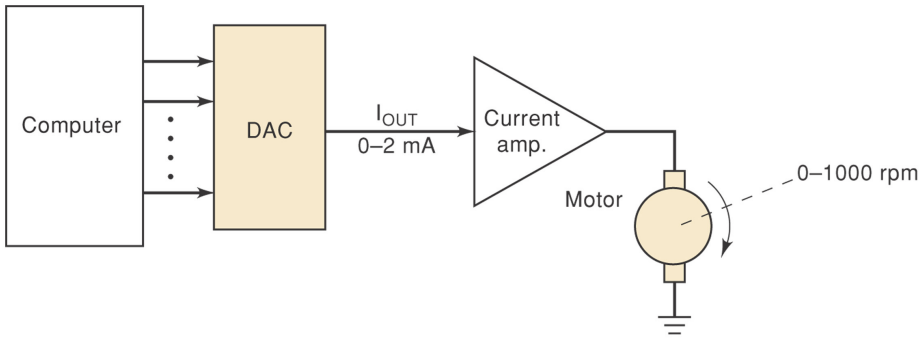
Figure shows a computer controlling the speed of a motor. The 0 to 2-mA analog current from the DAC is amplified to produce motor speeds from 0 to 1000 rpm. How many bits should be used if the computer is to be able to produce a motor speed that is within 5 rpm of the desired speed?

The motor seed, 0-1000rpm, goes from 0 to full-scale. Each step in DAC output produce a step in motor speed. We want the step size not greater than 5 rpm. Thus, at least we need 200 steps (1000/5).

Number of steps: $2N - 1 \geq 200$ or $2N \geq 201$, since $2^8=256$, therefore 8 bits.

Using 8 bits, how close to 366 rpm can the motor speed be adjusted?

With 8 bits, 255 steps, the motor speed1000/255=3.921 rpm. The number of steps is 366/3.921=93.34 or 93. So the actual speed 93 x 3.921=364.65 rpm or 365 rpm.

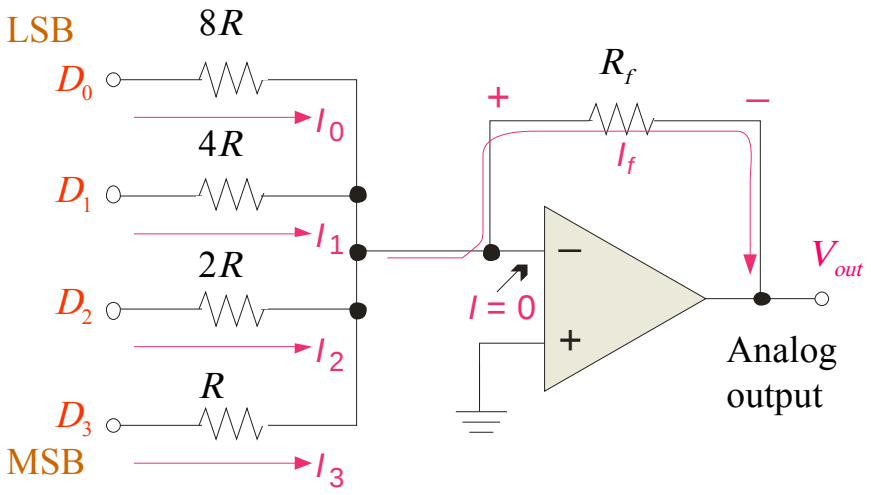


Digital-to-Analog Conversion Methods

Binary-weighted-input DAC:

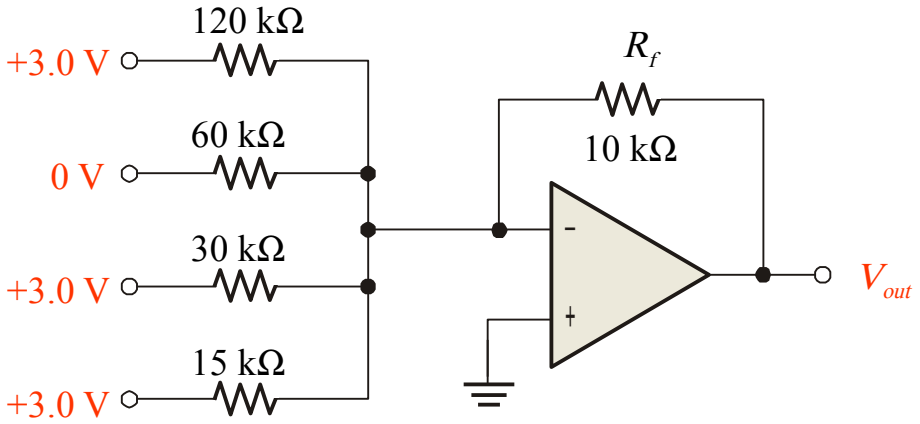
The binary-weighted-input DAC is a basic DAC in which the input current in each resistor is proportional to the column weight in the binary numbering system. It requires very accurate resistors and identical HIGH level voltages for accuracy.

The MSB is represented by the largest current, so it has the smallest resistor. To simplify analysis, assume all current goes through R_f and none into the op-amp.



Digital-to-Analog Conversion Methods

Example A certain binary-weighted-input DAC has a binary input of 1101. If a HIGH = +3.0 V and a LOW = 0 V, what is V_{out}?



Solution

$$I_{out} = -(I_0 + I_1 + I_2 + I_3)$$

$$= -\left(\frac{3.0\text{ V}}{120\text{ k}\Omega} + 0\text{ V} + \frac{3.0\text{ V}}{30\text{ k}\Omega} + \frac{3.0\text{ V}}{15\text{ k}\Omega}\right) = -0.325\text{ mA}$$

$$V_{out} = I_{out} R_f = (-0.325\text{ mA})(10\text{ k}\Omega) = -3.25\text{ V}$$

Determine the output of the DAC in Figure 12–27(a) if the waveforms representing a sequence of 4-bit numbers in Figure 12–27(b) are applied to the inputs. Input D_0 is the least significant bit (LSB).

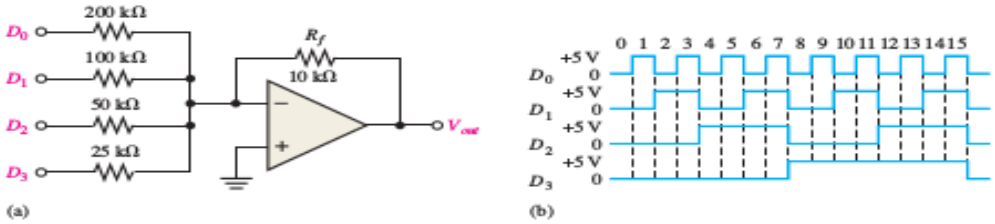


FIGURE 12–27

Solution

First, determine the current for each of the weighted inputs. Since the inverting (−) input of the op-amp is at 0 V (virtual ground) and a binary 1 corresponds to +5 V, the current through any of the input resistors is 5 V divided by the resistance value.

$$I_0 = \frac{5\text{ V}}{200\text{ k}\Omega} = 0.025\text{ mA}$$

$$I_1 = \frac{5\text{ V}}{100\text{ k}\Omega} = 0.05\text{ mA}$$

$$I_2 = \frac{5\text{ V}}{50\text{ k}\Omega} = 0.1\text{ mA}$$

$$I_3 = \frac{5\text{ V}}{25\text{ k}\Omega} = 0.2\text{ mA}$$

Almost no current goes into the inverting op-amp input because of its extremely high impedance. Therefore, assume that all of the current goes through the feedback resistor R_f. Since one end of R_f is at 0 V (virtual ground), the drop across R_f equals the output voltage, which is negative with respect to virtual ground.

$$V_{out(D0)} = (10\text{ k}\Omega)(-0.025\text{ mA}) = -0.25\text{ V}$$
$$V_{out(D1)} = (10\text{ k}\Omega)(-0.05\text{ mA}) = -0.5\text{ V}$$
$$V_{out(D2)} = (10\text{ k}\Omega)(-0.1\text{ mA}) = -1\text{ V}$$
$$V_{out(D3)} = (10\text{ k}\Omega)(-0.2\text{ mA}) = -2\text{ V}$$

From Figure 12–27(b), the first binary input code is 0000, which produces an output voltage of 0 V. The next input code is 0001, which produces an output voltage of −0.25 V. The next code is 0010, which produces an output voltage of −0.5 V. The next code is 0011, which produces an output voltage of −0.25 V + −0.5 V = −0.75 V. Each successive binary code increases the output voltage by −0.25 V, so for this particular straight binary sequence on the inputs, the output is a stairstep waveform going from 0 V to −3.75 V in −0.25 V steps. This is shown in Figure 12–28.

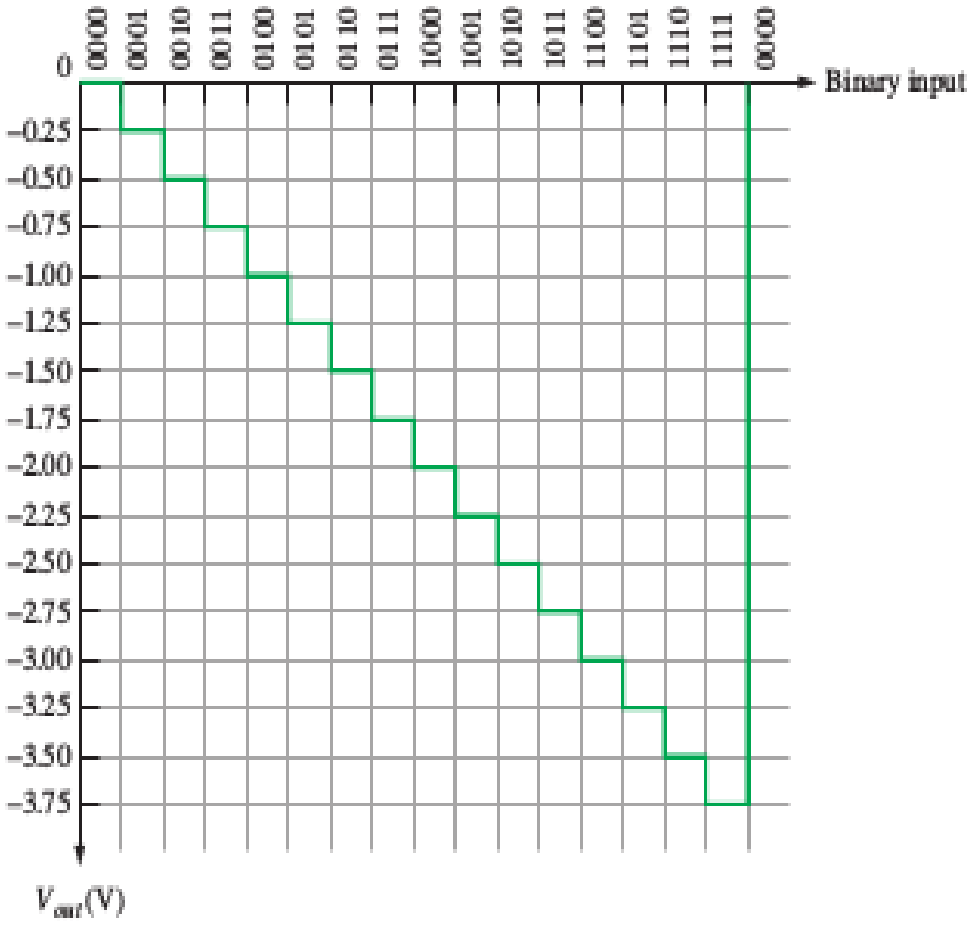


FIGURE 12–28 Output of the DAC in Figure 12–27.

Digital-to-Analog Conversion Methods

R-2R ladder:

The *R-2R* ladder requires only two values of resistors. By calculating a Thevenin equivalent circuit for each input, you can show that the output is proportional to the binary weight of inputs that are HIGH.

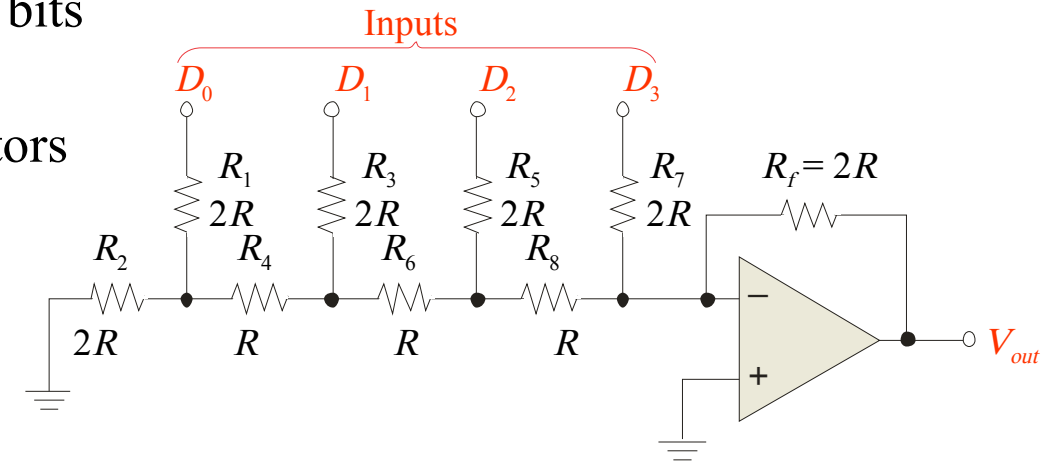
Each input that is HIGH contributes to the output: $V_{out} = -\dfrac{V_S}{2^{n-i}}$

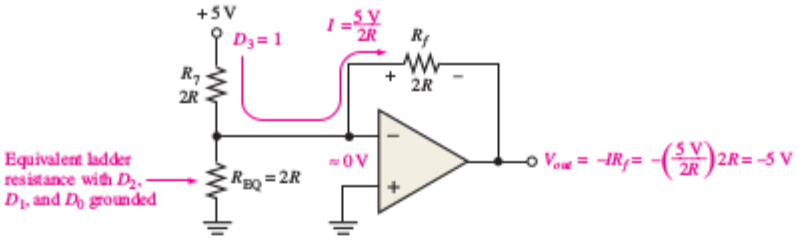
where V_S = input HIGH level voltage

n = number of bits

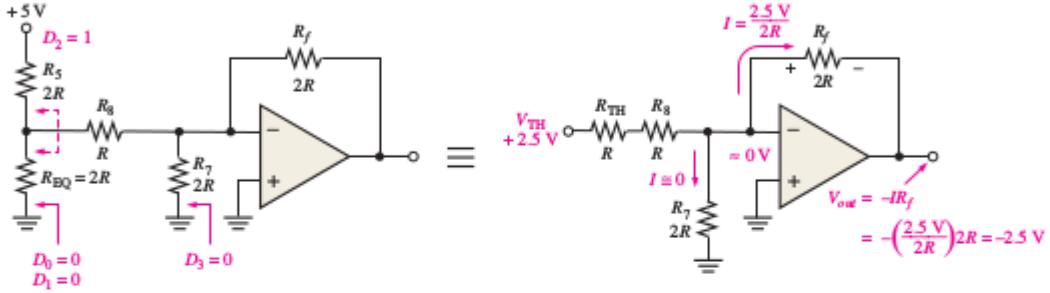
i = bit number

For accuracy, the resistors must be precise ratios, which is easily done in integrated circuits.

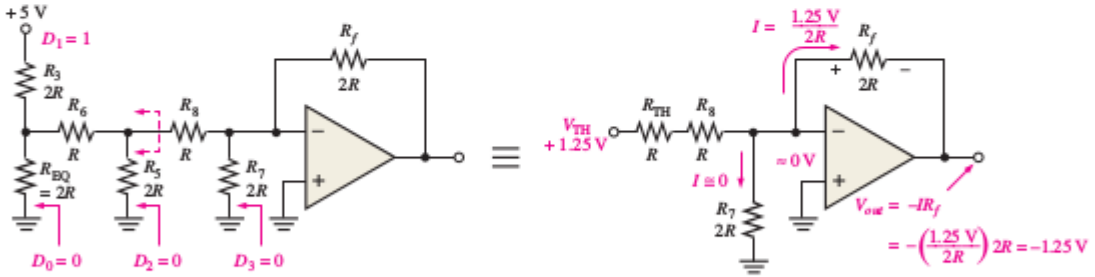




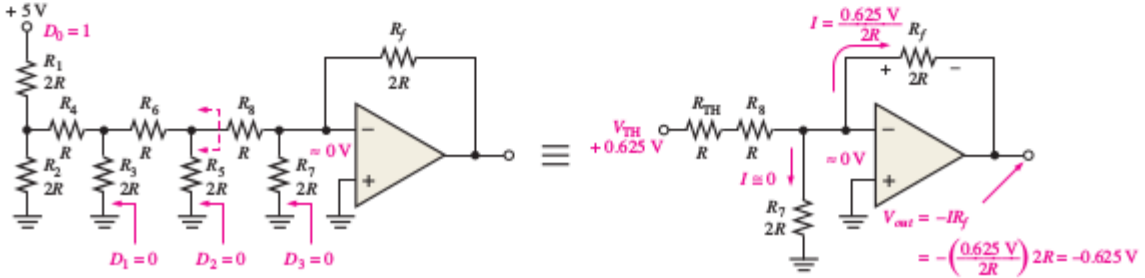
(a) Equivalent circuit for $D_3 = 1, D_2 = 0, D_1 = 0, D_0 = 0$



(b) Equivalent circuit for $D_3 = 0, D_2 = 1, D_1 = 0, D_0 = 0$



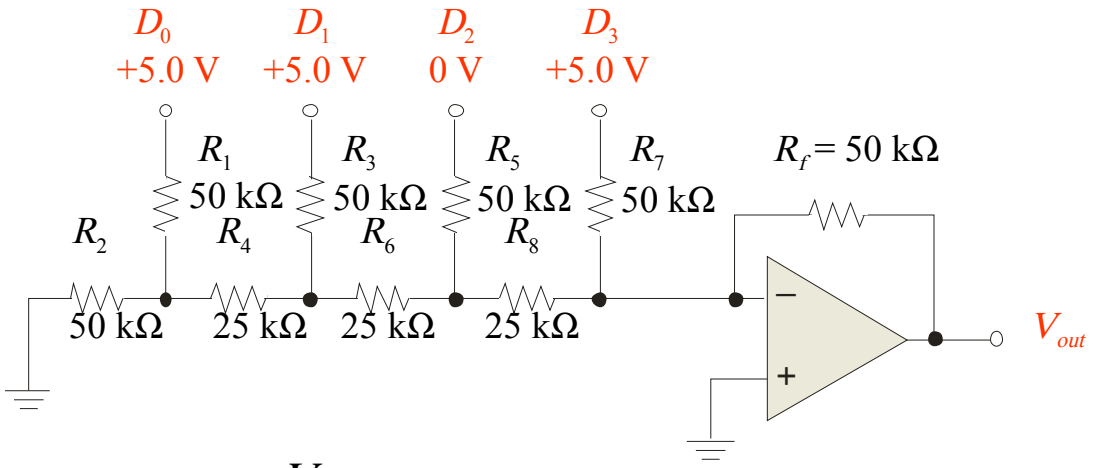
(c) Equivalent circuit for $D_3 = 0, D_2 = 0, D_1 = 1, D_0 = 0$



(d) Equivalent circuit for $D_3 = 0, D_2 = 0, D_1 = 0, D_0 = 1$

Digital-to-Analog Conversion Methods

Example An *R-2R* ladder has a binary input of 1011. If a HIGH = +5.0 V and a LOW = 0 V, what is V_{out}?



Solution Apply $V_{out} = -\dfrac{V_S}{2^{n-i}}$ to all inputs that are HIGH, then sum the results.

$$V_{out}(D_0) = -\frac{5\text{ V}}{2^{4-0}} = -0.3125\text{ V} \qquad V_{out}(D_1) = -\frac{5\text{ V}}{2^{4-1}} = -0.625\text{ V}$$

$$V_{out}(D_3) = -\frac{5\text{ V}}{2^{4-3}} = -2.5\text{ V}$$

Applying superposition, $V_{out} = -3.43\text{ V}$

Resolution and Accuracy of DACs

The *R-2R* ladder is relatively easy to manufacturer and is available in IC packages. DACs based on the *R-2R* network are available in 8, 10, and 12-bit versions. The **resolution** is an important specification, defined as the reciprocal of the number of steps in the output.

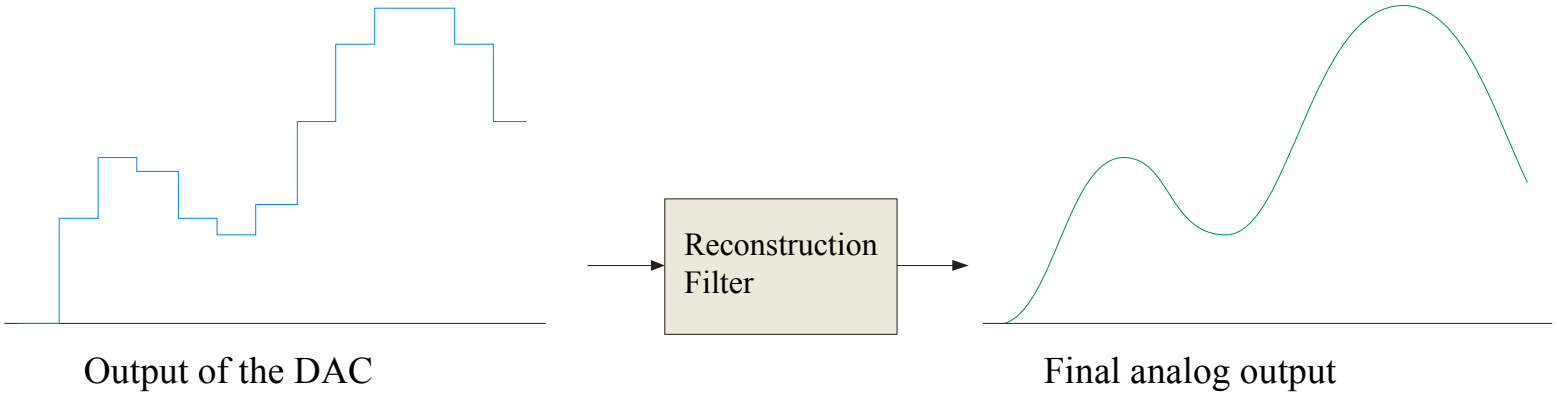
Question What is the resolution of the BCN31 *R-2R* ladder network, which has 8-bits?

Answer $2^8 - 1 = 255 \quad 1/255 = 0.39\%$

The **accuracy** is another important specification and is derived from a comparison of the actual output to the expected output. For the BCN31, the accuracy is specified as ±½ LSB = 0.2%.

Reconstruction Filter

After converting a digital signal to analog, it is passed through a low-pass "reconstruction filter" to smooth the stair steps in the output. The cutoff frequency of the reconstruction filter is often set to the same limit as the anti-aliasing filter, to block higher harmonics due to the digitizing process.



11-3 DAC Specifications

- Many DACs are available as ICs or self contained packages. Key specifications are:
  - Resolution
  - Accuracy: Full scale error and linearity error
  - Offset error: small output voltage
  - Settling time
  - Monotonicity: no downward steps

11-4 DAC Applications

- Used when a digital circuit output must provide an analog voltage or current
  - Control
    - Use a digital computer output to adjust motor speed or furnace temperature
  - Automatic testing
    - Computer generated signals to test analog circuitry
  - Signal reconstruction
    - Restoring an analog signal after it has been converted to digital. Audio CD systems, and audio/video recording
  - A/D conversion
  - Serial DACs

11-6 Analog to digital Conversion

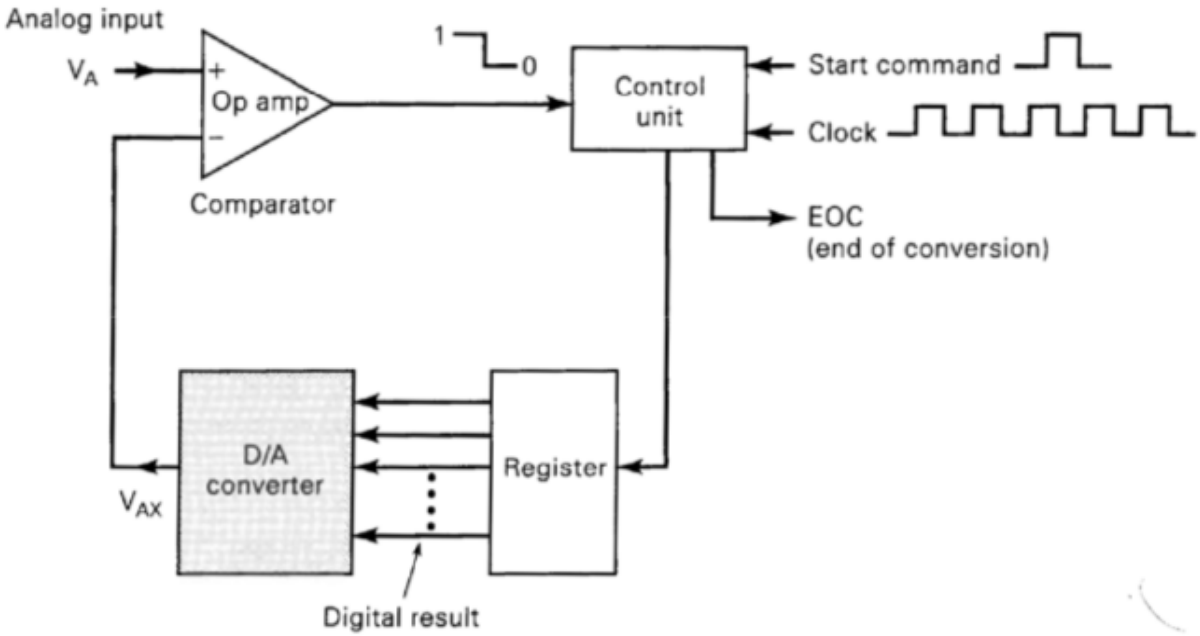
- ADC – digital code represents the analog input
- Generally more complex and time consuming than DAC
- Several types of ADC use DAC circuits
- The Op amp comparator ADC
  - Variations differ in how the control section continually modifies numbers in the register

Analog-to-Digital Conversion

- **Analog-to-Digital converter** (ADC) takes an analog input voltage and after a certain amount of time produces a digital output code that represents the analog input
- More complex
- Time-consuming

11-6 Analog to digital Conversion

- Several types of ADCs utilize a DAC as part of their circuitry
  - The timing for the operation is provided by the input clock signal
  - START COMMAND: initiate the conversion process

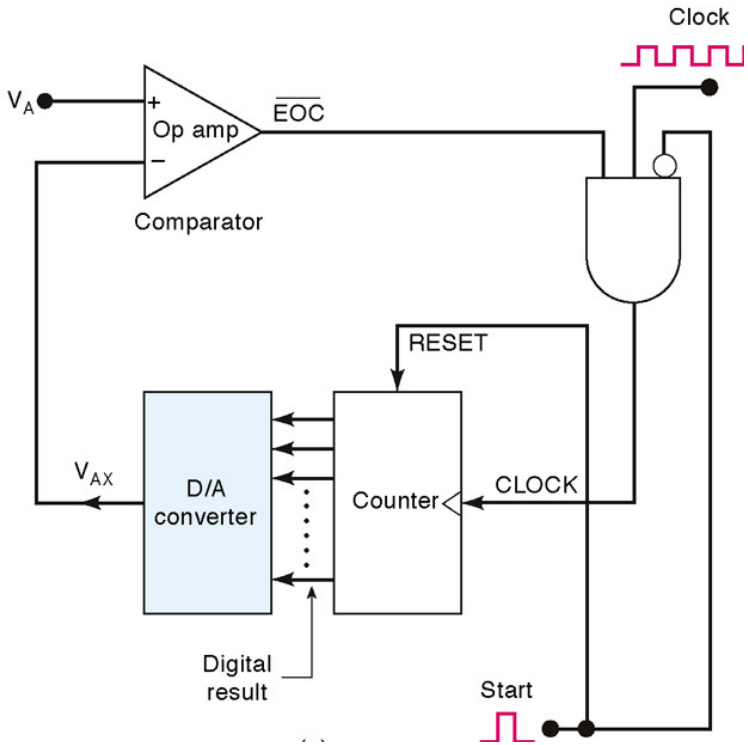


Basic Operation of ADCs

- The START COMMAND pulse initiates the operation
- Control unit continually modifies the binary number that is stored in the register
- The binary number is converted to an analog voltage by the DAC (V_{AX})
- The comparator compares V_{AX} with the analog input V_A
  - If $V_{AX} < V_A$: the comparator output stays HIGH
  - If V_{AX} exceeds V_A at least V_T (threshold voltage): the comparator output goes LOW → stop the process
    - V_{AX} is a close approximation to V_A
- Activate the end-of-conversion signal ($\overline{EOC}$) when the conversion is complete

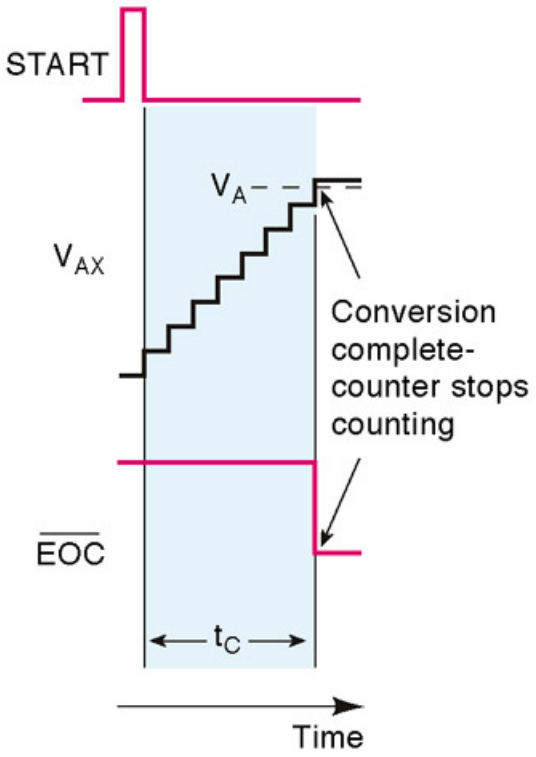
11-7 Digital Ramp ADC

- A binary counter is used as the register and allows clock to increment the counter a step at a time until $V_{AX} \geq V_A$



11-8 Digital Ramp ADC

- A/D resolution and accuracy
  - Measurement error is unavoidable
  - Reducing the step size can reduce but not eliminate potential error
  - This is called quantization error



Digital-Ramp ADC – Example (1)

- ADC with the following values
  - Clock frequency = 1 MHz
  - V_T = 0.1 (mV) = 0.0001 (V)
  - DAC has F.S. output = 10.23 V and a 10-bit input

1. V_A = 3.728 V → Digital value = ?
2. Conversion time = ?
3. The resolution = ?

Digital-Ramp ADC – Example (2)

- DAC has 10-bit input and a 10.23-V F.S. output
  - → Number of possible steps = $2^{10} - 1 = 1023$
  - → Step size = 10.23 / 1023 = 10 mV
- V_{AX} must reach $V_A + V_T = 3.7281$ (V) or more before the comparator goes LOW
  - → Number of steps

    $3.7281 \text{ V} / 10 \text{ mV} = 372.81 \approx 373$
  - → Binary equivalent = 0101110101
- The conversion requires 373 clock pulses
  - → Conversion time = 373 x (1 / 1 MHz) = 373 μs
- Resolution = step size = 10 mV (0.1% F.S.)

A/D Resolution and Accuracy

- An unavoidable source of error in the digital-ramp method: step size (resolution) of internal DAC is the smallest unit of measure
  - Reduce the potential error by making the step size smaller
  - Quantization error: a difference between the actual (analog) quantity and the digital value assigned to it
- Accuracy
  - Depend on the accuracy of the circuit components (comparator, resistor, reference supplies, v.v...)
  - This error is in addition to the quantization error due to resolution

Conversion Time

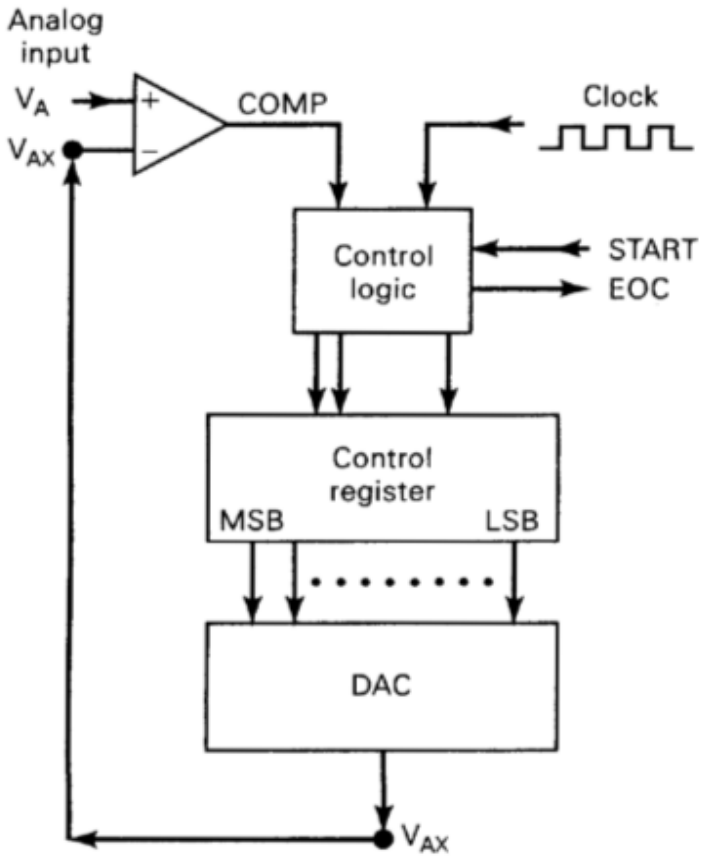
- Conversion time (t_C) is the time interval between the end of the START pulse and the activation of the $\overline{\text{EOC}}$ output
  - Maximum conversion time: V_A is just below full scale

    $t_C(\text{max}) = (2^N - 1)$ clock cycles
  - Average conversion time: half of the maximum conversion time

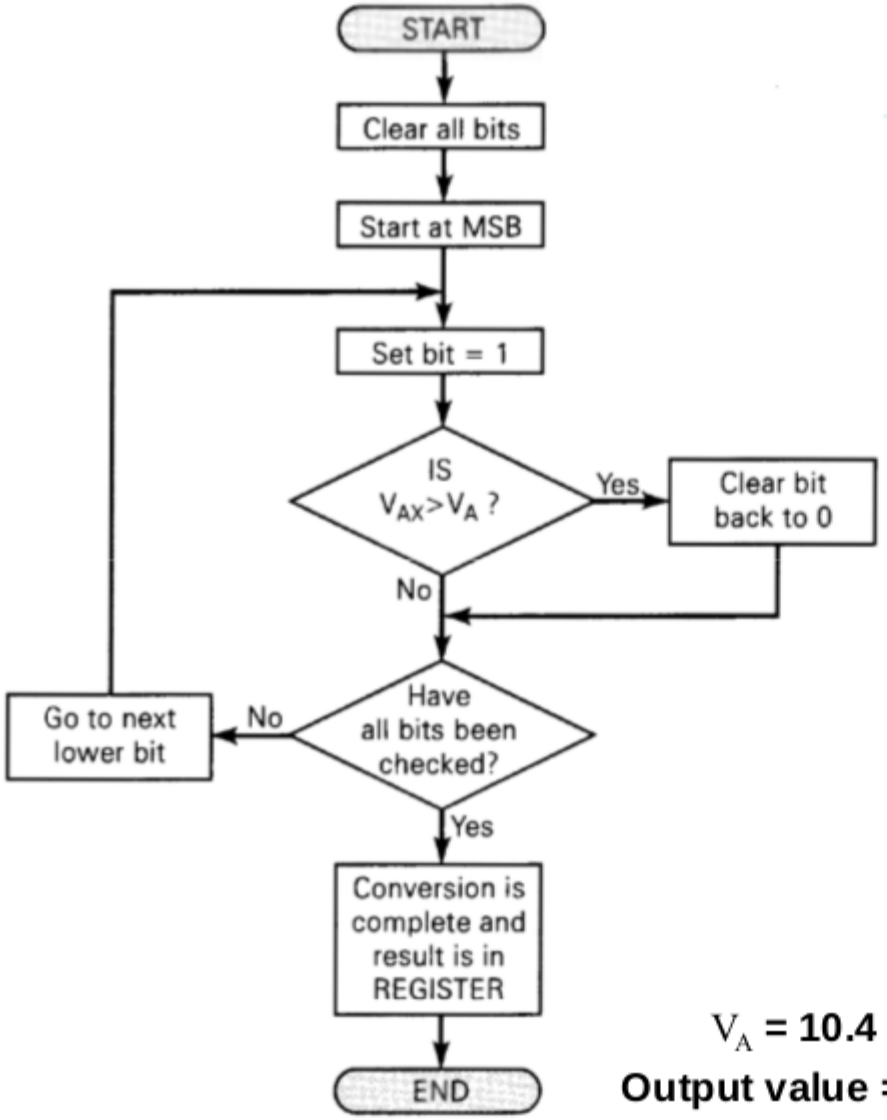
    $t_C(\text{avg}) = t_C(\text{max}) / 2 = 2^{N-1}$ clock cycles
  - Conversion time doubles for each bit that is added to the counter
  - Improve resolution → longer t_C
  - Unsuitable for high-speed A/D conversions

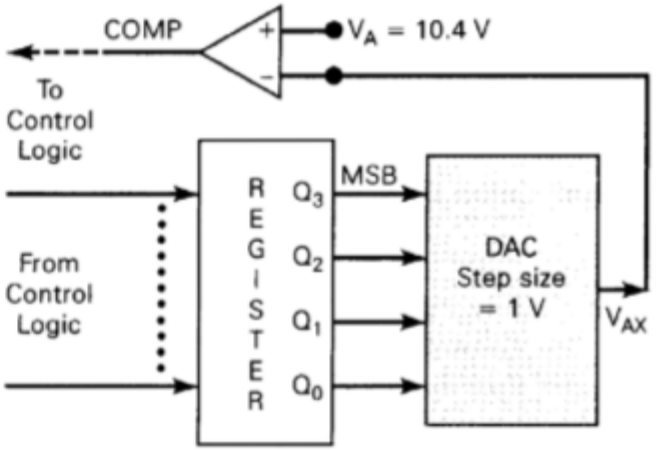
Successive-Approximation ADC (SAC)

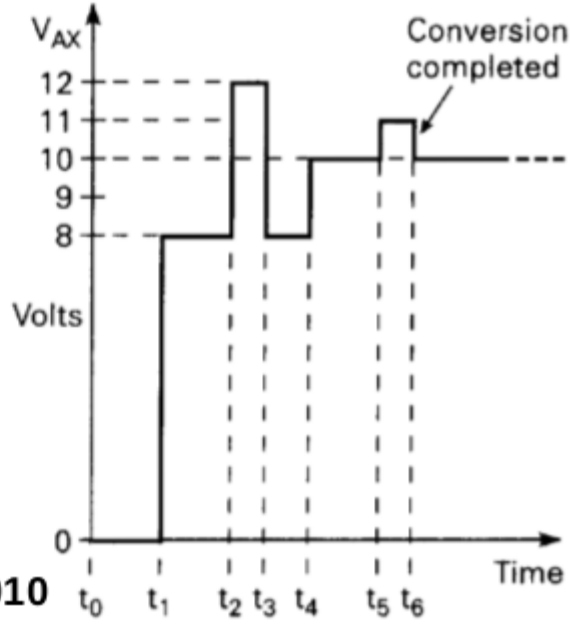
- More complex circuitry than the digital-ramp ADC
- Use register to provide the input to the DAC block
- The digital output is equivalent to a voltage that is less than the analog input V_A



1







V_A = 10.4 V

Output value = 1010

SAC – Conversion time

- Much shorter conversion time
  - Fixed value conversion time
  - Not dependent on the value of the analog input
- Total conversion time for an N-bit SAC: N clock cycles

$$t_C \text{ for SAC} = N \times 1 \text{ clock cycle}$$

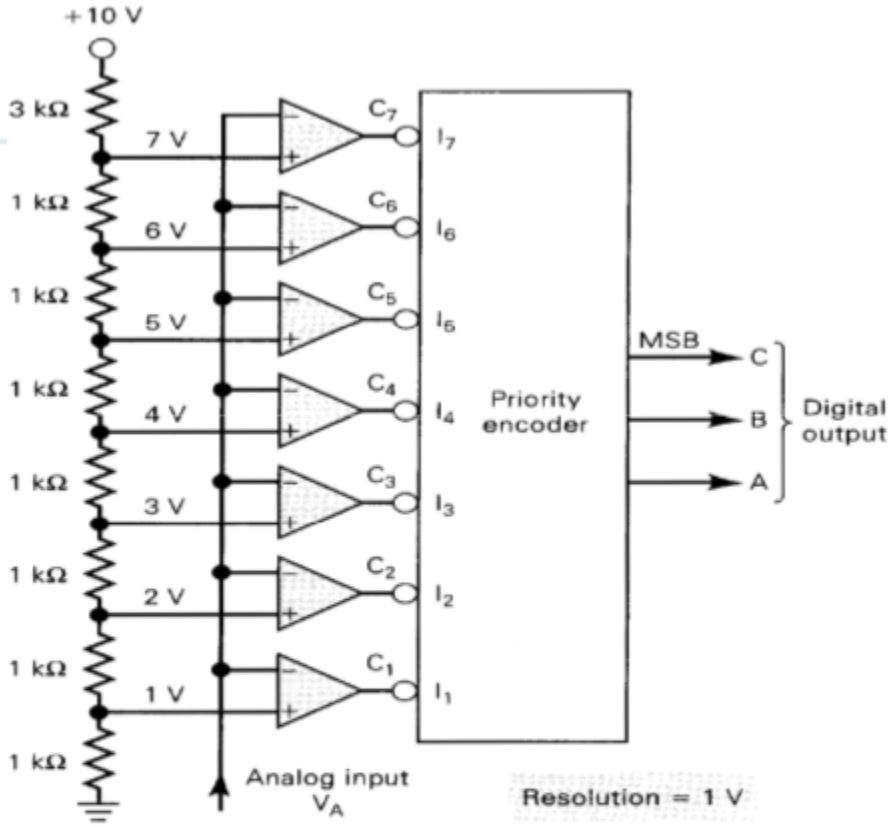
  - Example: two ADCs utilize a 500-kHz clock frequency
    - 10-bit digital-ramp ADC: $t_C = (2^{10} - 1) \times 2\ \mu s = 2046\ \mu s$
    - 10-bit SAC: $t_C = 10 \times 2\ \mu s = 20\ \mu s$
- In data acquisition: permit more data values to be acquired in a given time interval

Flash ADCs

- The highest-speed ADC
- Require much more circuitry, the large number of comparator limits the size of flash converters
- N-bit flash converter require $2^N - 1$ comparators, 2^N resistors, and the necessary encoder logic
- Conversion time: depend only on the propagation delays of the comparators and encoder logic

Flash ADCs

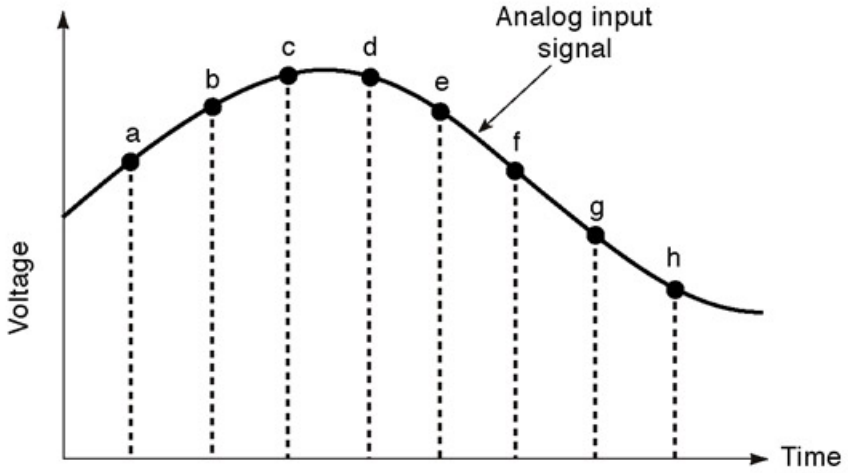
- Use the voltage-divider resistors
- Priority encoder

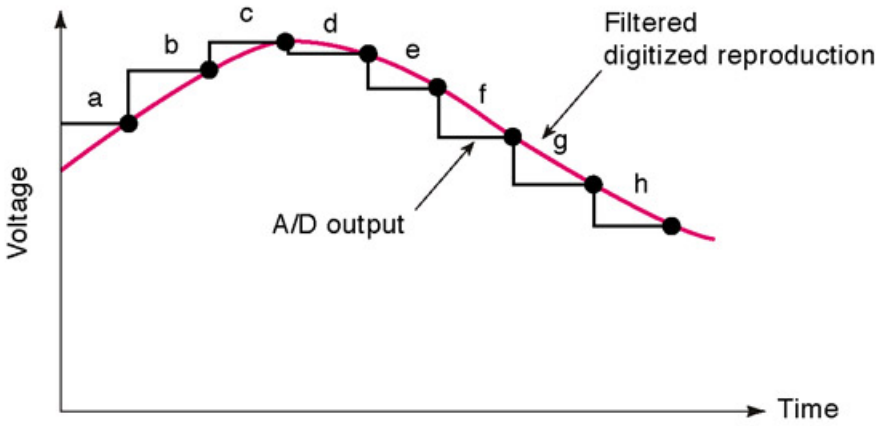


Analog in	Comparator outputs							Digital outputs		
V_A	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C	B	A
0-1 V	1	1	1	1	1	1	1	0	0	0
1-2 V	0	1	1	1	1	1	1	0	0	1
2-3 V	0	0	1	1	1	1	1	0	1	0
3-4 V	0	0	0	1	1	1	1	0	1	1
4-5 V	0	0	0	0	1	1	1	1	0	0
5-6 V	0	0	0	0	0	1	1	1	0	1
6-7 V	0	0	0	0	0	0	1	1	1	0
> 7 V	0	0	0	0	0	0	0	1	1	1

11-9 Data Acquisition

- Digitizing analog data and transferring to memory is data acquisition
- Acquiring a single data point value is sampling
- Reconstructing a digitized signal





11-10 Data Acquisition

- Aliasing
  - To make the signal reconstruction nearly identical to original analog signal.
  - Caused by under sampling
  - Harry Nyquist
    - The sampling frequency must be at least twice the highest input frequency
    - Sampling at a frequency less than twice the input frequency results in under sampling and incorrect reproduction

11-11 Successive Approximation ADC

- Widely used ADC
- More complex than digital ramp but has a shorter conversion time
- Conversion time is fixed and not dependent on the analog input
- Many SACs are available as ICs.

11-12 Flash ADCs

- High speed conversion
- Much more complex circuitry
  - 6 bit flash ADC requires 63 analog comparators
  - 8 bit flash ADC requires 255 comparators
  - 10 bit flash ADC requires 1023 comparators
- A 3 bit flash converter is described in figure 11-22
- Conversion time – No clock signal is used, so the conversion is continuous. This makes for very short conversion times, typically under 17 ns.