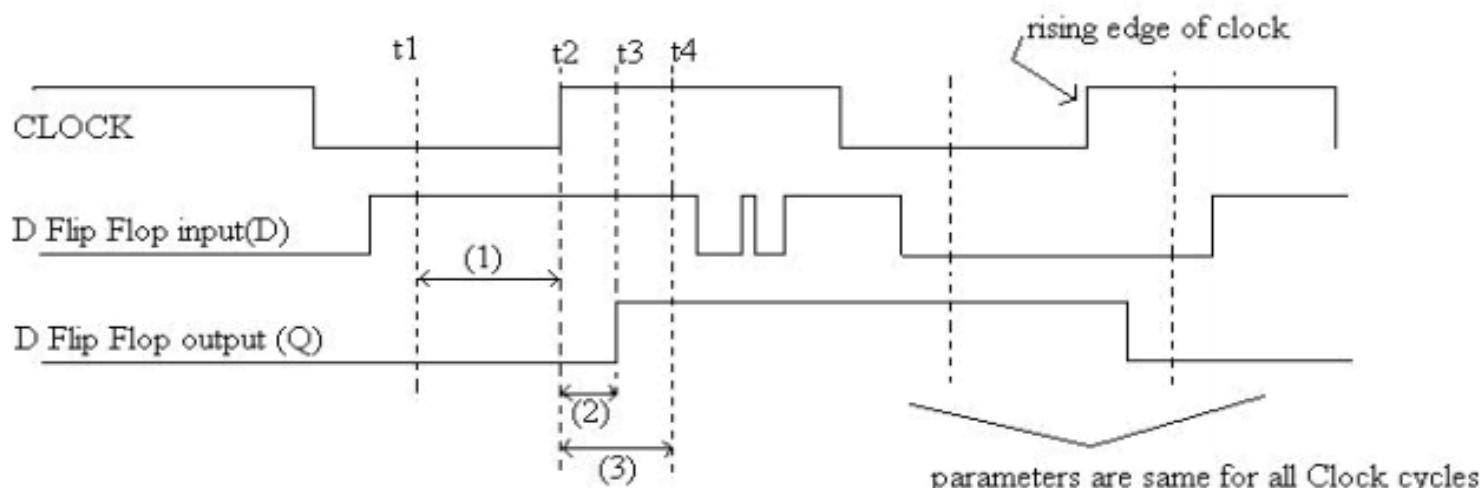


# Setup and Hold Time



The timing diagram above illustrates three signals: the Clock, the Flip Flop Input (D) and the Flip Flop output (Q).

(1) is the Setup Time [ $t_2 - t_1$ ]: the minimum amount of time Input must be held constant BEFORE the clock tick. Note that D is actually held constant for somewhat longer than the minimum amount. The extra “constant” time is sometimes called the setup margin.

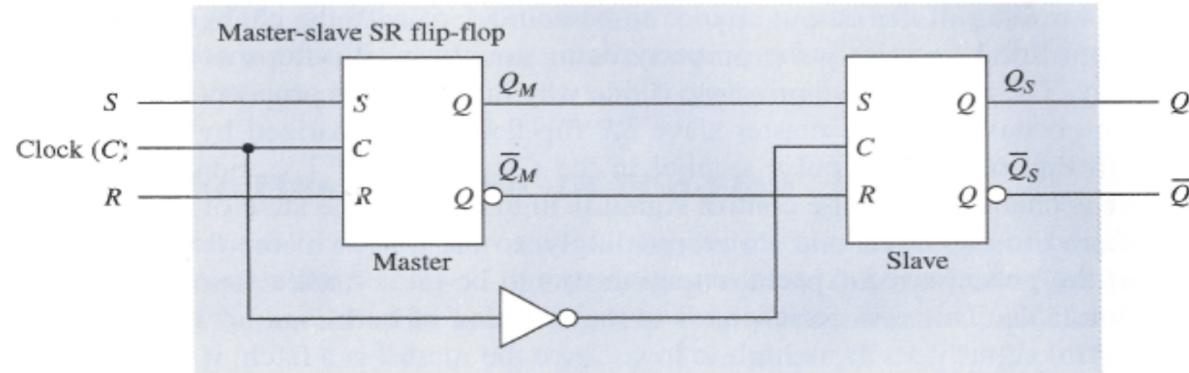
(2) is the Propagation delay of the Flip Flop [ $t_3 - t_2$ ]: this is the time that it takes for the new input to be to propagate and influence the output.

(3) is the Hold time [ $t_4 - t_2$ ]: the minimum amount of time the Input is held constant AFTER the clock tick. Note that Q is actually held constant for somewhat longer than the minimum amount. The extra “constant” time is sometimes called the hold margin.

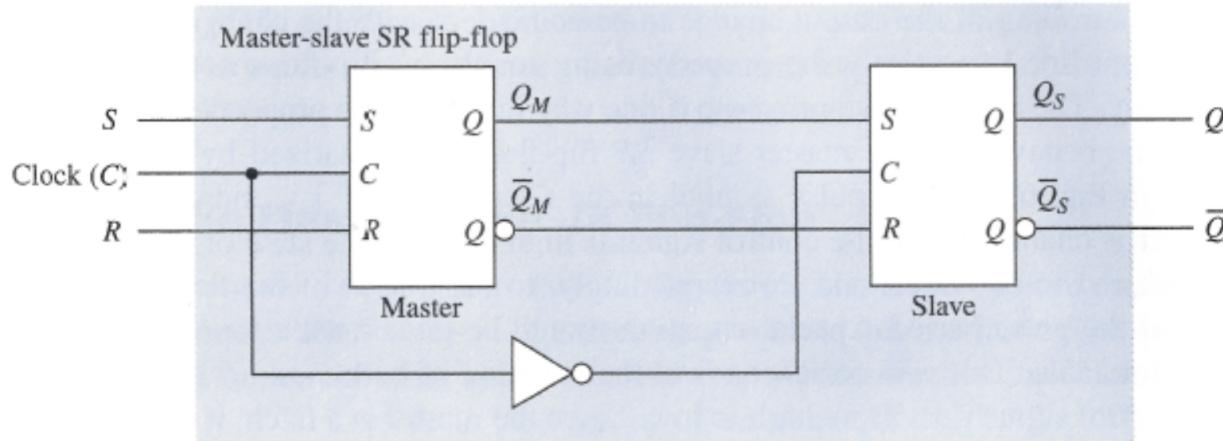
(The above timing diagram has 2 clock cycles; the timing parameters for the second cycle will also be similar to that of the first cycle)

# Master-Slave SR Flip-Flop

- Two sections, each capable of storing a binary symbol.
- First section is referred to as the master and the second section as the slave.
- Information is entered into the master on one edge or level of a control signal and is transferred to the slave on the next edge or level of the control signal.
- Each section is a latch.

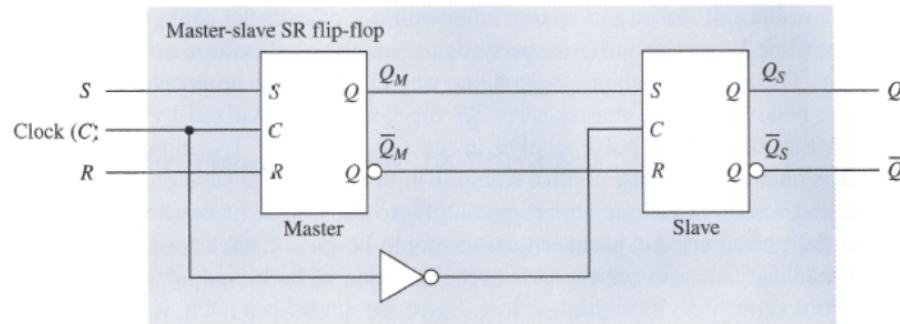


# Master-Slave SR Flip-Flop

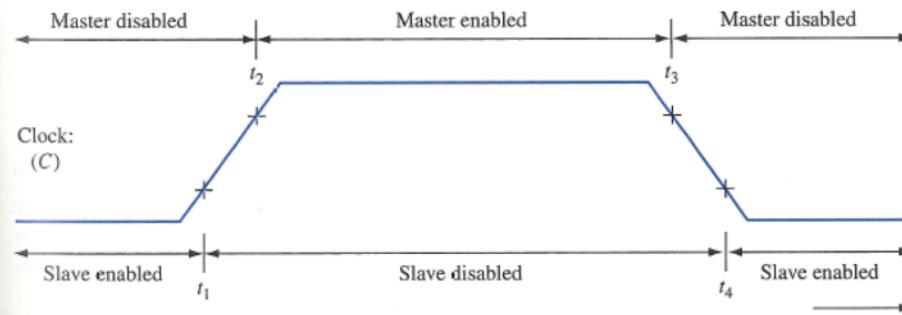


- C = 0:
  - Master is disabled. Any changes to S,R ignored.
  - Slave is enabled. Is in the same state as the master.
- C = 1:
  - Slave is disabled (retains state of master)
  - Master is enabled, responds to inputs. Changes in state of master are not reflected in disabled slave.
- C = 0:
  - Master is disabled.
  - Slave is enabled and takes on new state of the master.
- Important: For short periods during rising and falling edges, both master and slave are disabled.

# Master-Slave SR Flip-Flop



(a)



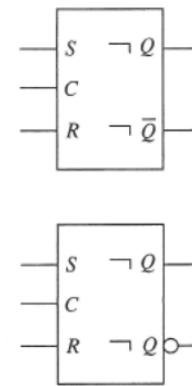
Slave only takes on state of the master at  $t_4$ .

Postponed output indicator: output change postponed until end of pulse

symbol indicates master enabled when  $C = 1$  and state of master transferred to slave at the end of the pulse

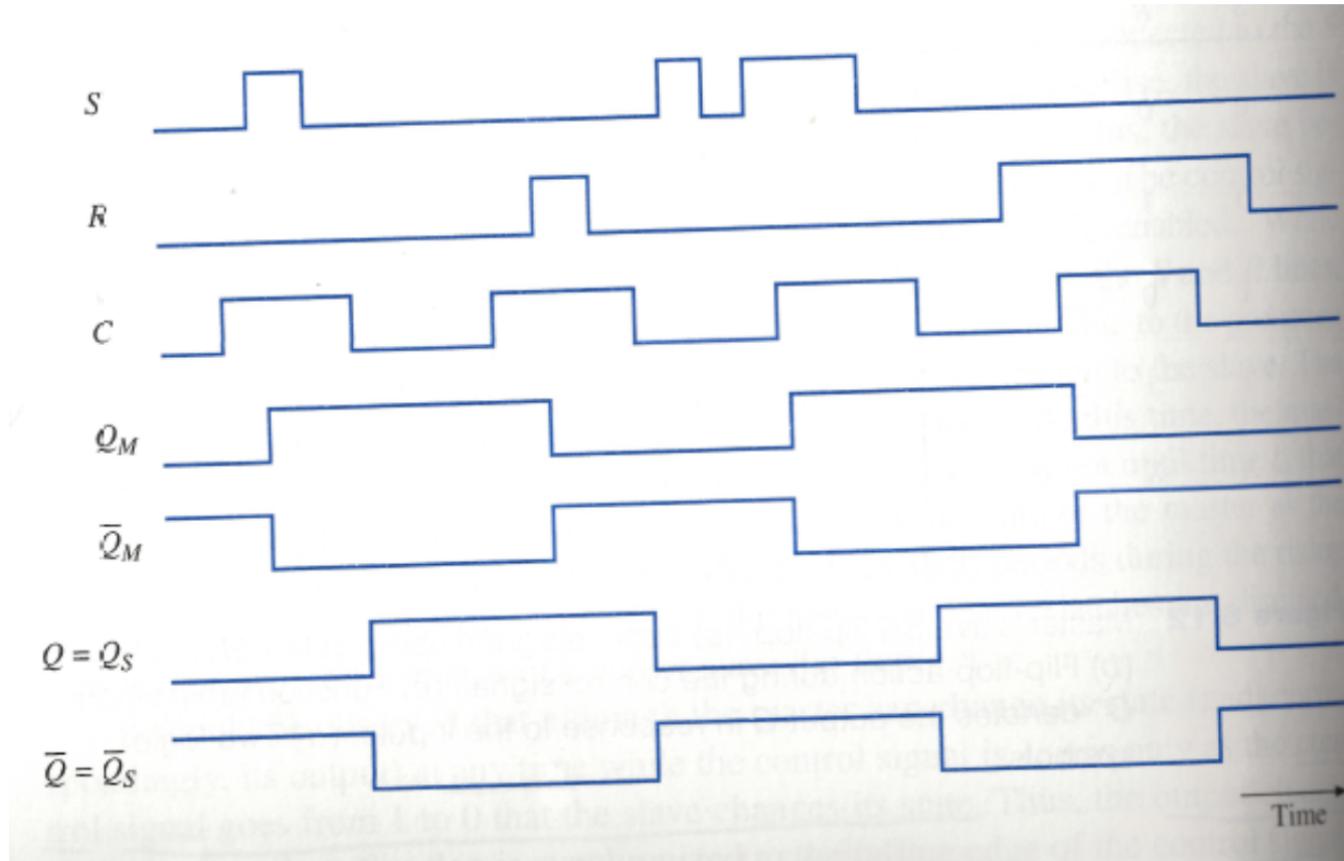
Inputs			Outputs	
S	R	C	$Q^+$	$\bar{Q}^+$
0		High (Master enabled)	$Q$	$\bar{Q}$
1		Low (Master disabled)	0	1
1	0	High (Master enabled)	1	0
1	1	High (Master enabled)	Undefined	Undefined
X	X	0	$Q$	$\bar{Q}$

(c)



(d)

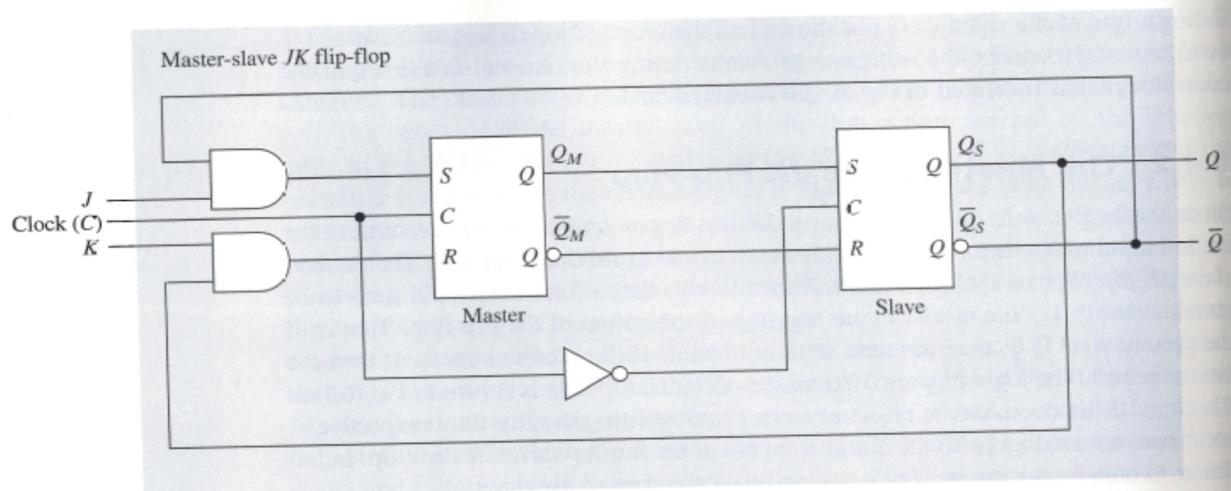
# Timing Diagram for Master-Slave SR flip-flop



# Master-Slave JK Flip-Flop

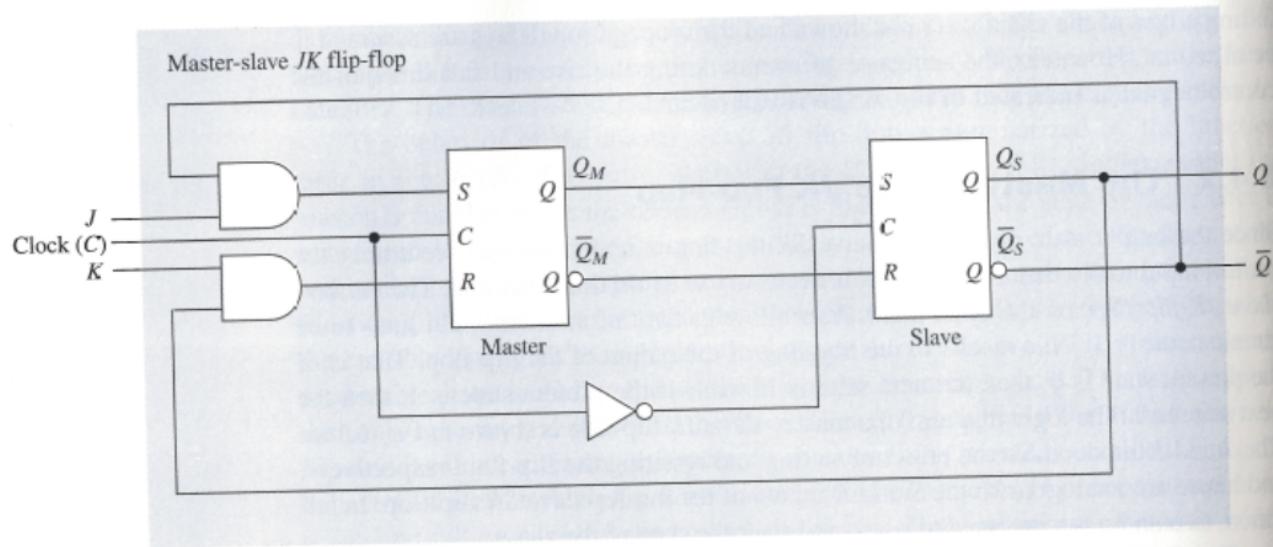
- The output state of a master-slave SR flip-flop is undefined upon returning the control input to 0 when  $S = R = 1$ .
  - Necessary to avoid this condition.
- Master-slave JK flip-flop allows its two information input lines to be simultaneously 1.
  - Results in toggling the output of the flip flop.

# Master-Slave JK Flip-Flop



- Assume in 1-state,  $C = 0$ ,  $J = K = 1$ .
  - Due to feedback, the output of the J-gate is 0, output of K-gate is 1.
  - If clock is changed to  $C = 1$  then master is reset.
- Assume in 0-state,  $C = 0$ ,  $J = K = 1$ .
  - Due to feedback, the output of the J-gate is 1, output of K-gate is 0.
  - If clock is changed to  $C = 1$  then master is set.
- 1 on J input line, 0 on K input line sets the flip-flop.
  - If in 1-state, unchanged b/c S,R set to 0.
  - If in 0-state, S set to 1, R set to 0.
- 0 on J input, 1 on K input line resets the flip-flop. Why?

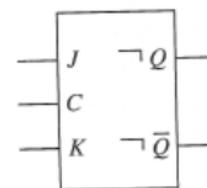
# Master-Slave JK Flip-Flop



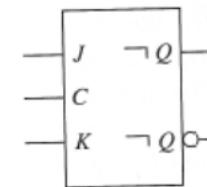
(a)

Inputs			Outputs	
J	K	C	$Q^+$	$\bar{Q}^+$
0	0	High	Q	$\bar{Q}$
0	1	High	0	1
1	0	High	1	0
1	1	High	$\bar{Q}$	Q
X	X	0	Q	$\bar{Q}$

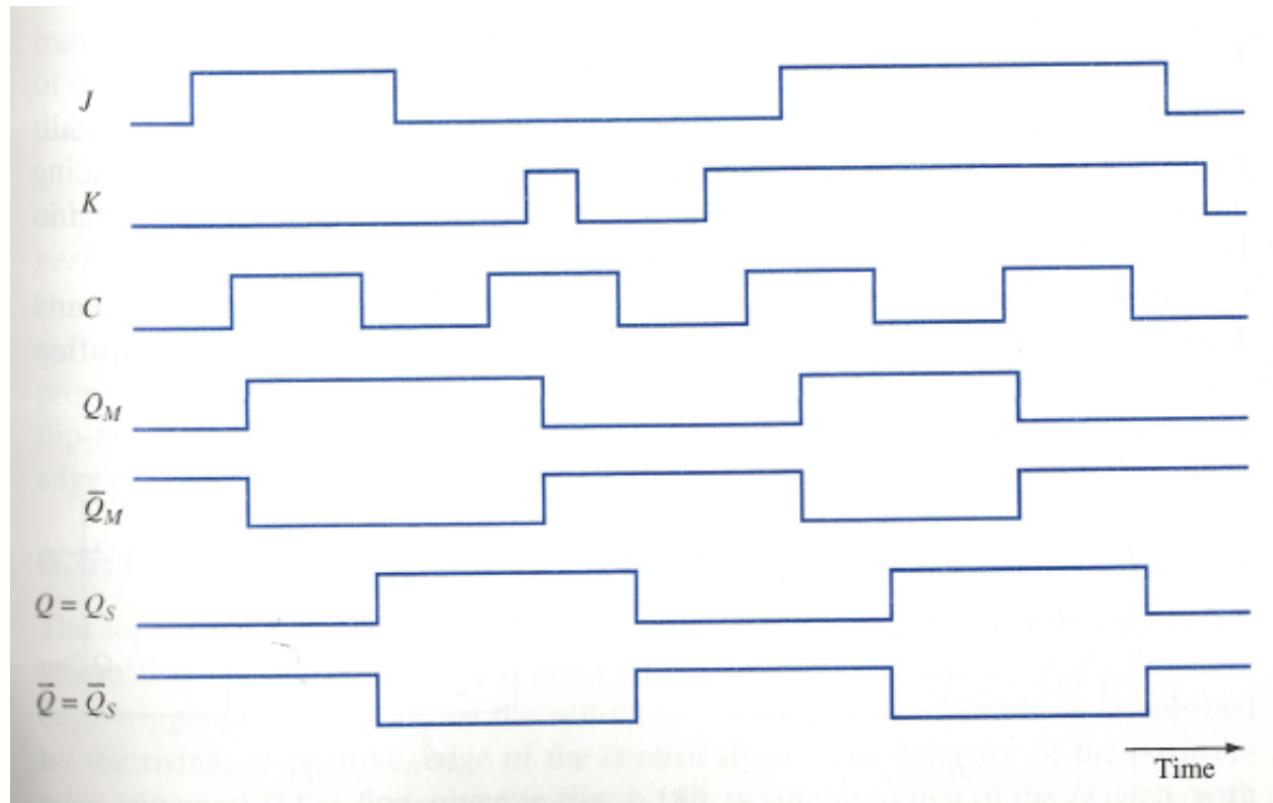
(b)



(c)



# Timing Diagram for Master-Slave JK Flip-Flop



# Characteristic Equations

		SR	
		00	01
Q	0	0	0
	1	1	0
		$Q^+ = S + \bar{R}Q$	( $SR = 0$ )
		(a)	

Flip-flop type	Characteristic equation
SR	$Q^+ = S + \bar{R}Q$ ( $SR = 0$ )
JK	$Q^+ = J\bar{Q} + \bar{K}Q$
D	$Q^+ = D$
T	$Q^+ = T\bar{Q} + \bar{T}Q = T \oplus Q$ (b)

**Figure 6.25** Characteristic equations. (a) Derivation of characteristic equation for an SR flip-flop. (b) Summary of characteristic equations.

# Registers

- A collection of flip-flops taken as an entity.
- Function: Hold information within a digital system so that it is available to the logic elements during the computing process.
- Each combination of stored information is known as the state or content of the register.
- Shift register: Registers that are capable of moving information upon the occurrence of a clock-signal.
  - Unidirectional
  - bidirectional

# Registers

- Two basic ways in which information can be entered/outputted
  - Parallel: All 0/1 symbols handled simultaneously.  
Require as many lines as symbols being transferred.
  - Serial: Involves the symbol-by-symbol availability of information in a time sequence.
- Four possible ways registers can transfer information:
  - Serial-in/serial-out
  - Serial-in/parallel-out
  - Parallel-in/parallel-out
  - Parallel-in/serial-out