IC Logic Families

- Introduction
  - Digital IC technology has advanced rapidly

Complexity	Number of Gates
Small- scale integration(SSI)	Fewer
Medium- scale integration(MSI)	12 to 99(10^2 - 10^3)
Large- scale integration(LSI)	100 to 9,999(10^3 - 10^5)
Very large- scale integration(VLSI)	10,000 to 99,999(10^5 - 10^7)
Ultra large- scale integration(ULSI)	100,000 to 999,999(10^7 - 10^9)
Giga- scale integration(GSI)	1,000,000 or more(10^9 - 10^{11})
Tera- scale integration(TSI)	(10^{12} or more)

    - Moore's Law
      - The number of components that can be packed on a computer chip doubles every 18 months while price stays the same.
  - Most of the reasons that modern digital systems use integrated circuits
    - Integrated circuits pack a lot more circuitry in a small package
      - the overall size of any digital system is reduced
        - the cost is dramatically reduced because of the economies of mass-producing large volumes of similar devices
    - Integrated circuits have made digital systems more reliable by reducing the number of external interconnections
      - Discrete components(transistor, diode, resistor, etc.) are protected from poor soldering, breaks or shorts in connecting paths on a circuit board

- Integrated circuits have drastically reduced the amount of electrical power needed to perform a given function
  - Integrated circuitry typically requires less power than their discrete counterparts
    - the saving in power supply costs

- There are some things that Integrated circuits cannot do
  - Integrated circuits can not handle very large currents or voltages (*because the heat generated in such small spaces would cause temperatures to rise beyond acceptable limits*)
  - Integrated circuits can not easily implement certain electrical devices such as inductors, transformers, and large capacitors
- For these reason
  - Integrated circuits are principally used to perform low-power circuit operations that are commonly called *information processing*
  - The operations *that require high power levels or devices that can not be integrated* are still handled by discrete components
- Various Logic Families
  - Bipolar transistors : TTL and ECL
  - Unipolar MOSFET transistors : NMOS, PMOS, and CMOS

Logic Families Vocabulary

TTL (Transistor Transistor Logic) Integrated-circuit technology that uses the bipolar transistor as the principal circuit element.

CMOS (Complimentary Metal Oxide Semiconductor) Integrated-circuit technology that uses the field-effect transistor as the principal circuit element.

ECL (Emitter Coupled Logic) Integrated-circuit technology that uses the bipolar transistors configured as a differential amplifier. This eliminates saturation and improves speed but uses more power than other families.

Digital IC Terminology

- Voltage Parameters:
  - V_{IH}(min): high-level input voltage, the minimum voltage level required for a logic 1 at an *input*.
  - V_{IL}(max): low-level input voltage
  - V_{OH}(min): high-level output voltage
  - V_{OL}(max): low-level output voltage

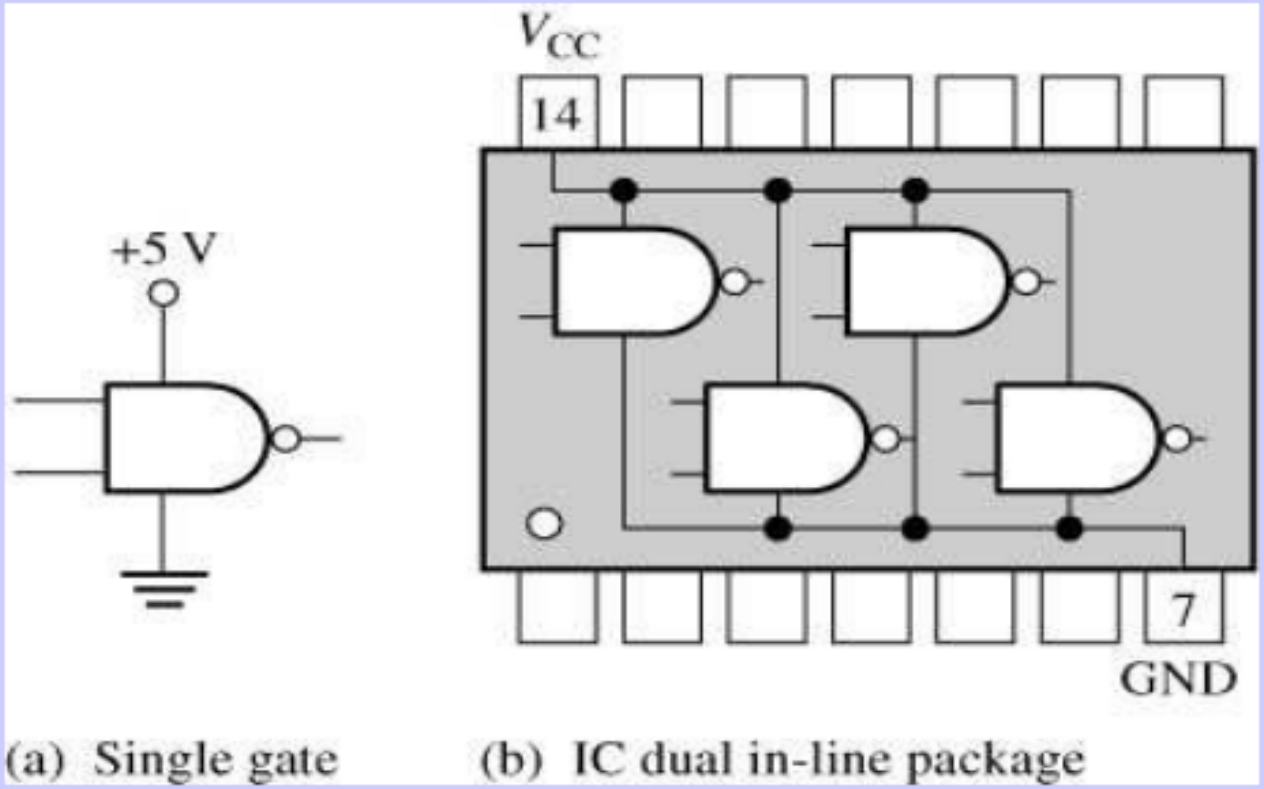

+5 V
V_{CC}
14
7
GND
(a) Single gate
(b) IC dual in-line package

Figure 15--2
Input and output logic levels for CMOS.

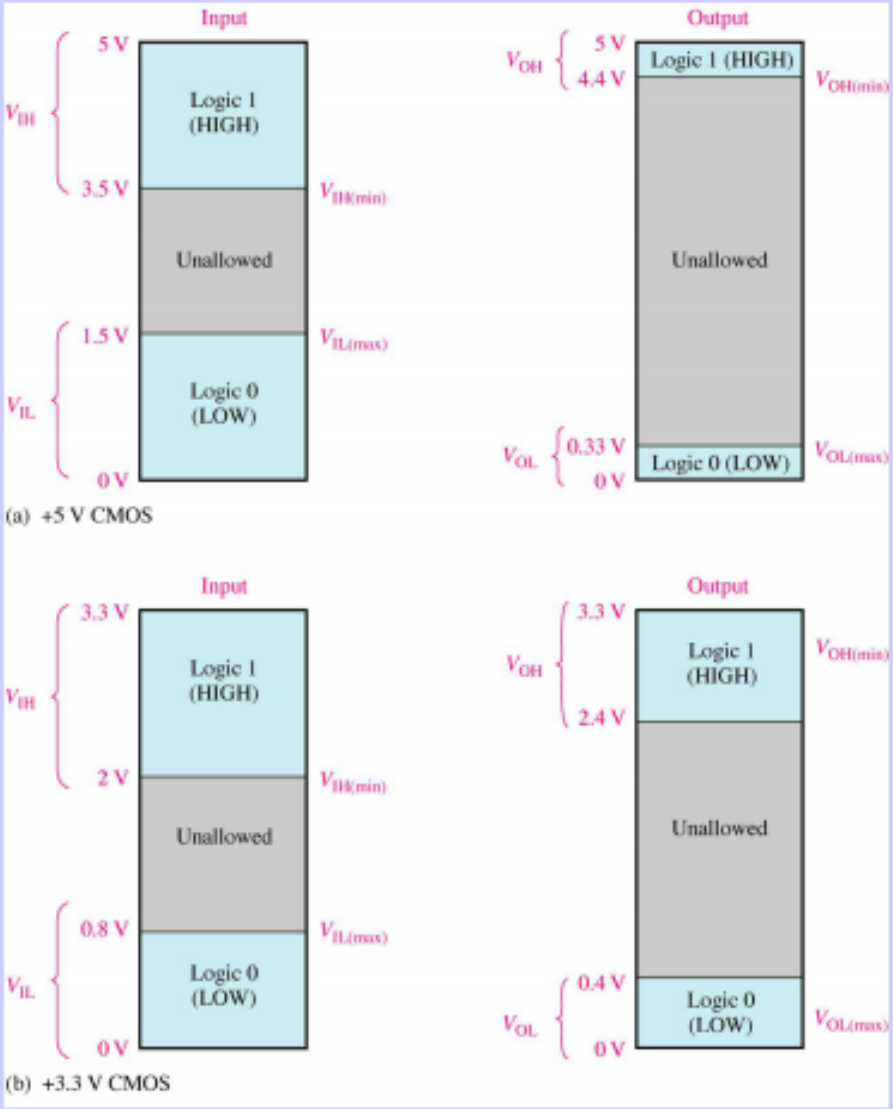
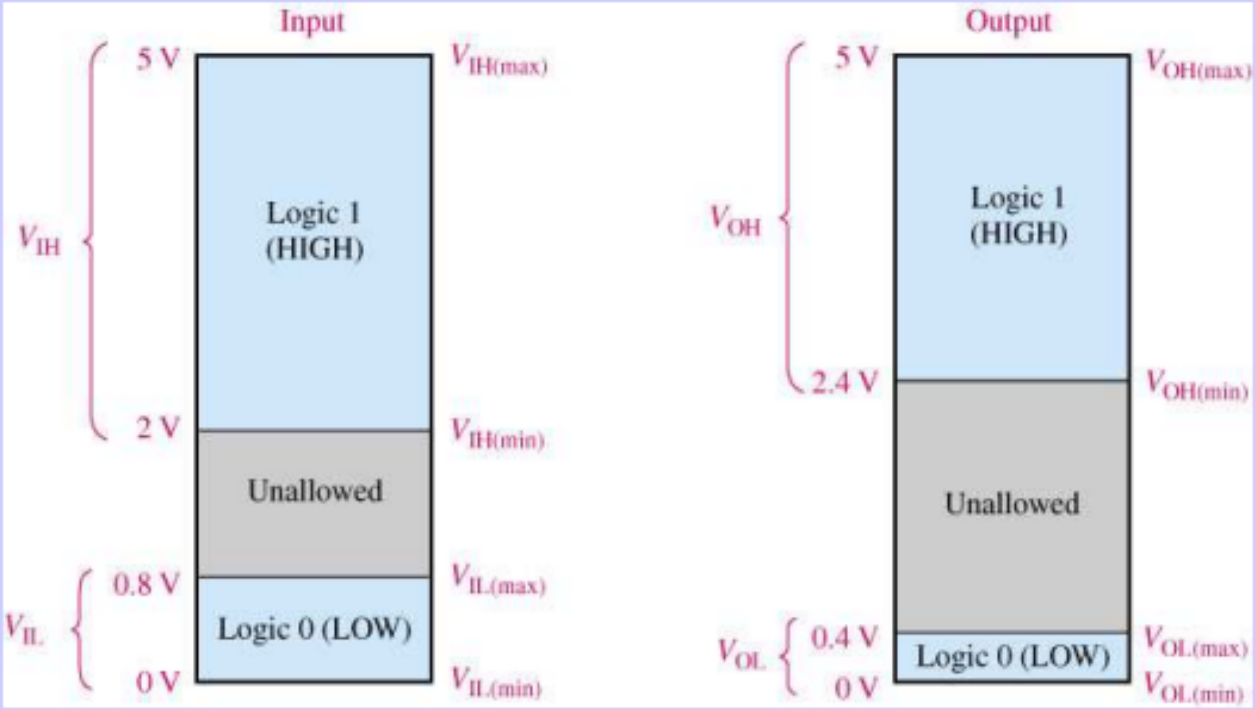


Figure 15--3 Input and output logic levels for TTL.



Current Parameters

- I_{IH}(min): high-level input current, the current that flows into an input when a specified high-level voltage is applied to that input.
- I_{IL}(max): low-level input current
- I_{OH}(min): high-level output current
- I_{OL}(max): low-level output current

Figure 8-1

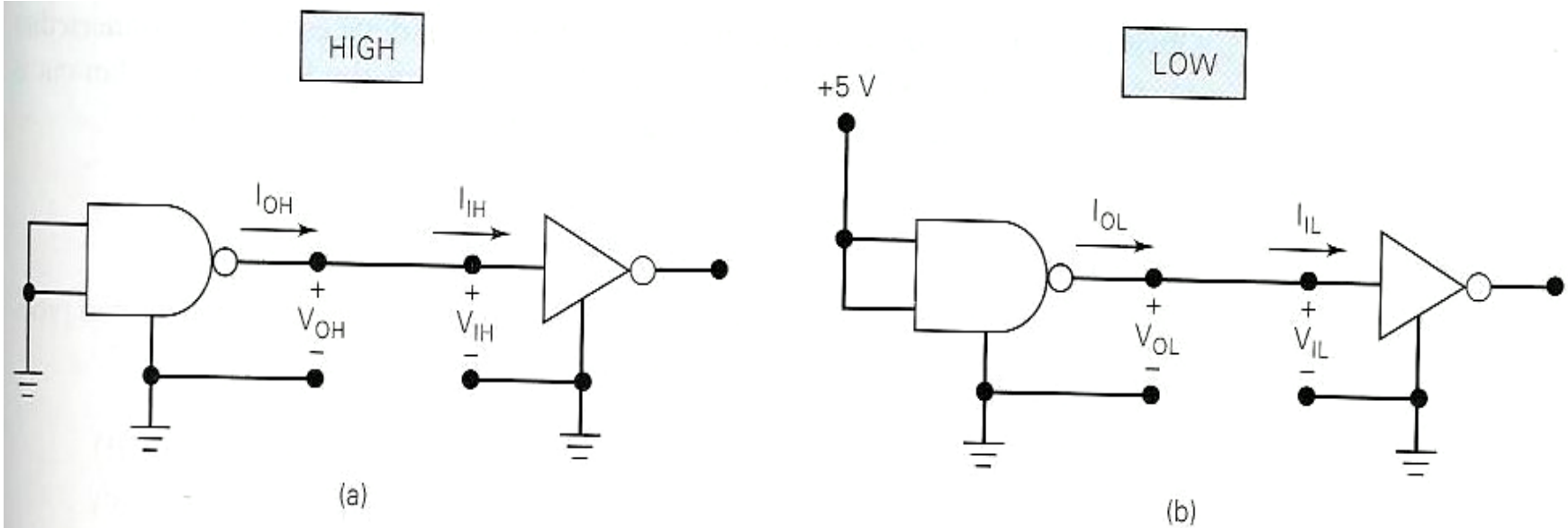
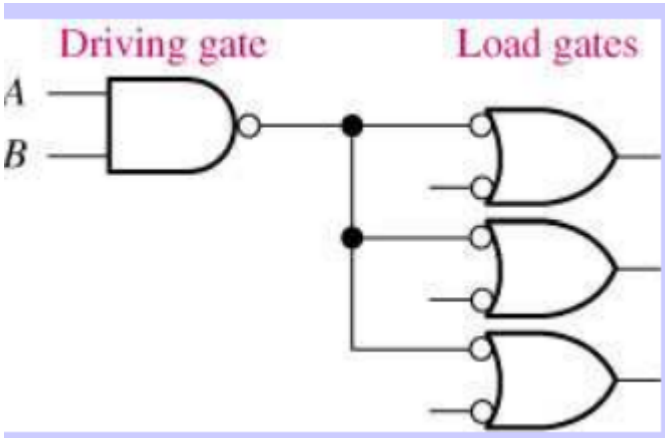


FIGURE 8-1 Currents and voltages in the two logic states.

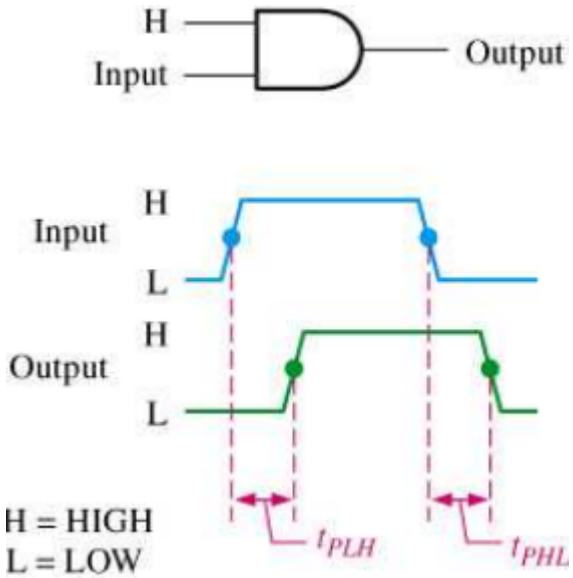
Fan-Out

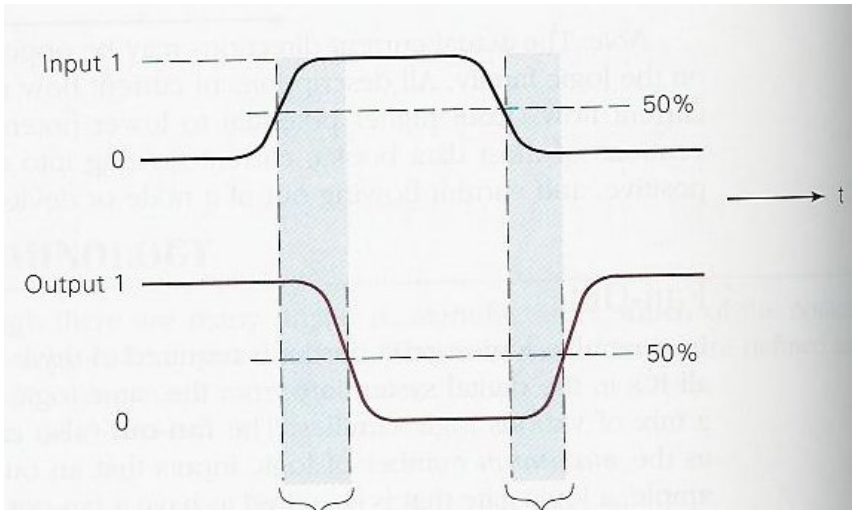
- The maximum number of standard logic inputs that an output can drive reliably.
- Also known as the *loading factor*.
- Related to the current parameters (both in high and low states.)



Propagation Delays

- t_{pLH}: delay time in going from logical 0 to logical 1 state (LOW to HIGH)
- t_{pHL}: delay time in going from logical 1 to logical 0 state (HIGH to LOW)
- Measured at 50% points.





Power Requirements

- Every IC needs a certain amount of electrical power to operate.
- V_{cc} (TTL)
- V_{DD}(MOS)
- Power dissipation determined by I_{cc} and V_{cc}.
- Average $I_{cc}(avg) = (I_{CCH} + I_{CCL})/2$
- $P_D(avg) = I_{cc}(avg) \times V_{cc}$

Figure 8-3

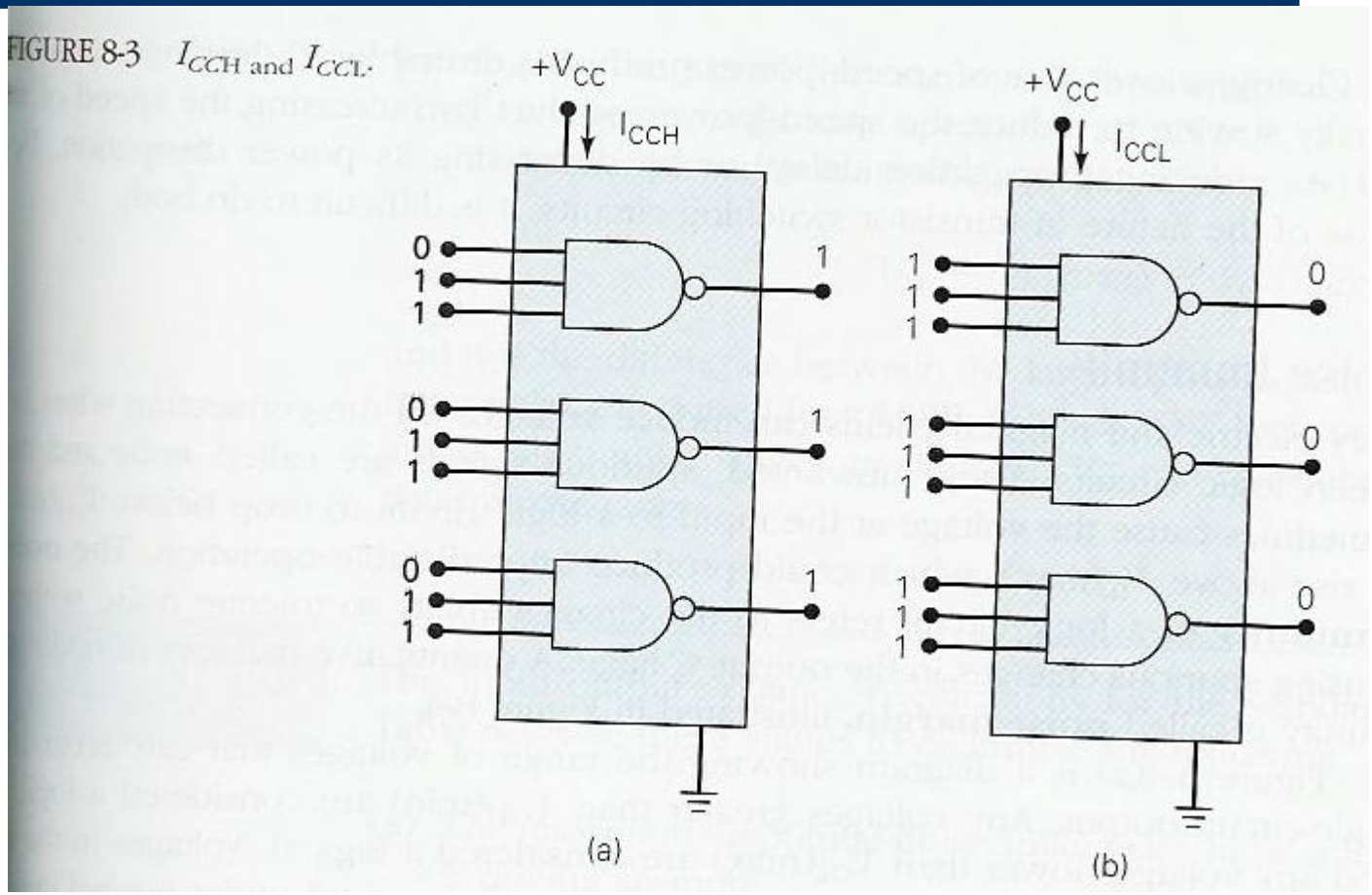


FIGURE 8-3 I_{CCH} and I_{CCL}.
+V_{CC}
I_{CCH}
0
1
1
1
0
1
1
1
0
1
1
1
(a)
+V_{CC}
I_{CCL}
1
1
1
0
1
1
1
0
1
1
1
0
(b)

Speed-Power Product

- Desirable properties:
  - Short propagation delays (high speed)
  - Low power dissipation
- Speed-power product measures the combined effect.

Noise Immunity

- What happens if noise causes the input voltage to drop below V_{IH}(min) or rise above V_{IL}(max)?
- The noise immunity of a logic circuit refers to the circuit's ability to tolerate noise without causing spurious changes in the output voltage.
- Noise margin: Figure 8-4.
- $V_{NH}=V_{OH}(min)-V_{IH}(min)$
- $V_{NL}=V_{IL}(max)-V_{OL}(max)$
- Example 8-1.

Figure 15--4 Illustration of the effects of **input noise** on gate operation.

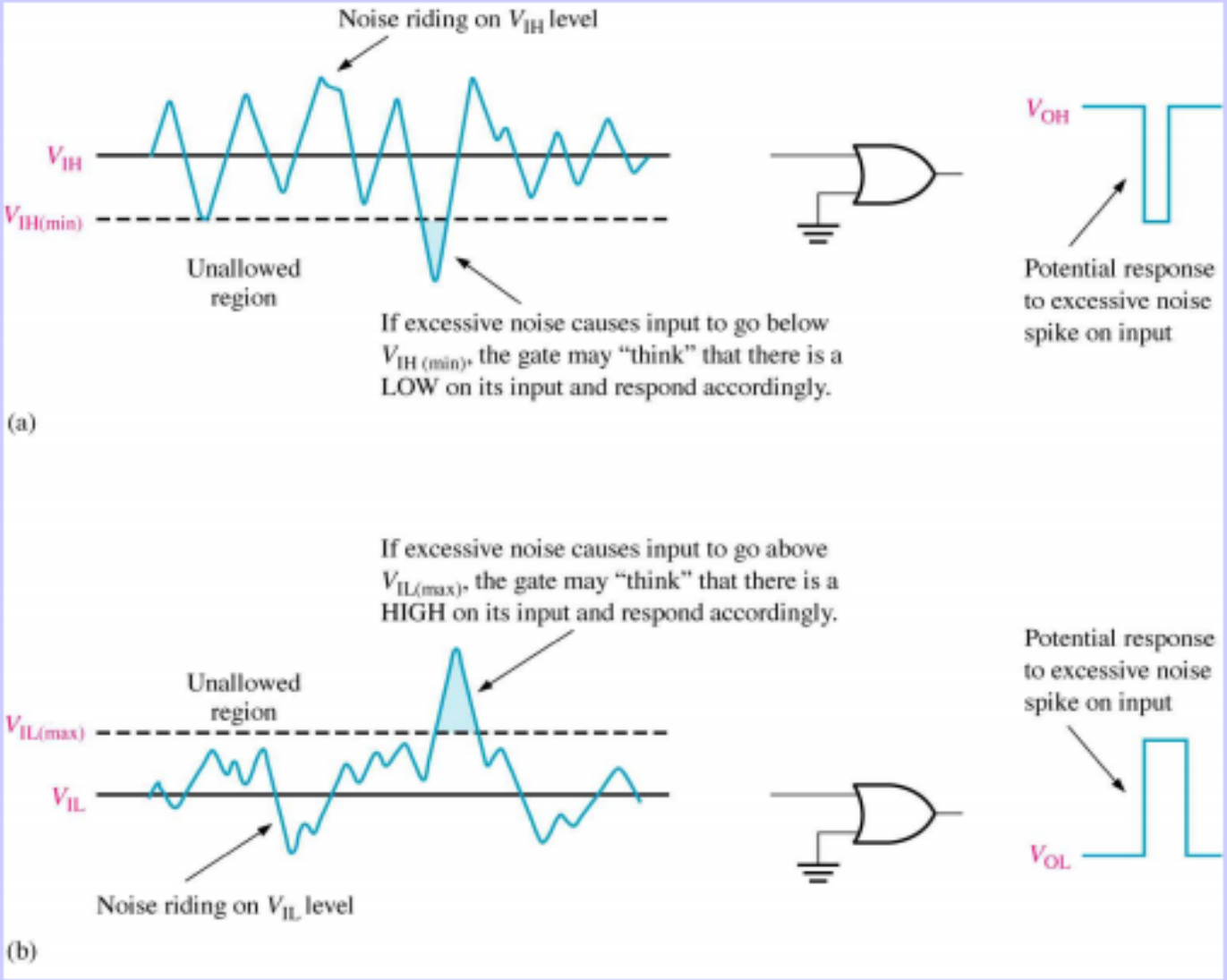


Figure 15--5 Illustration of noise margins. Values are for 5 V CMOS, but the principle applies to any logic family.

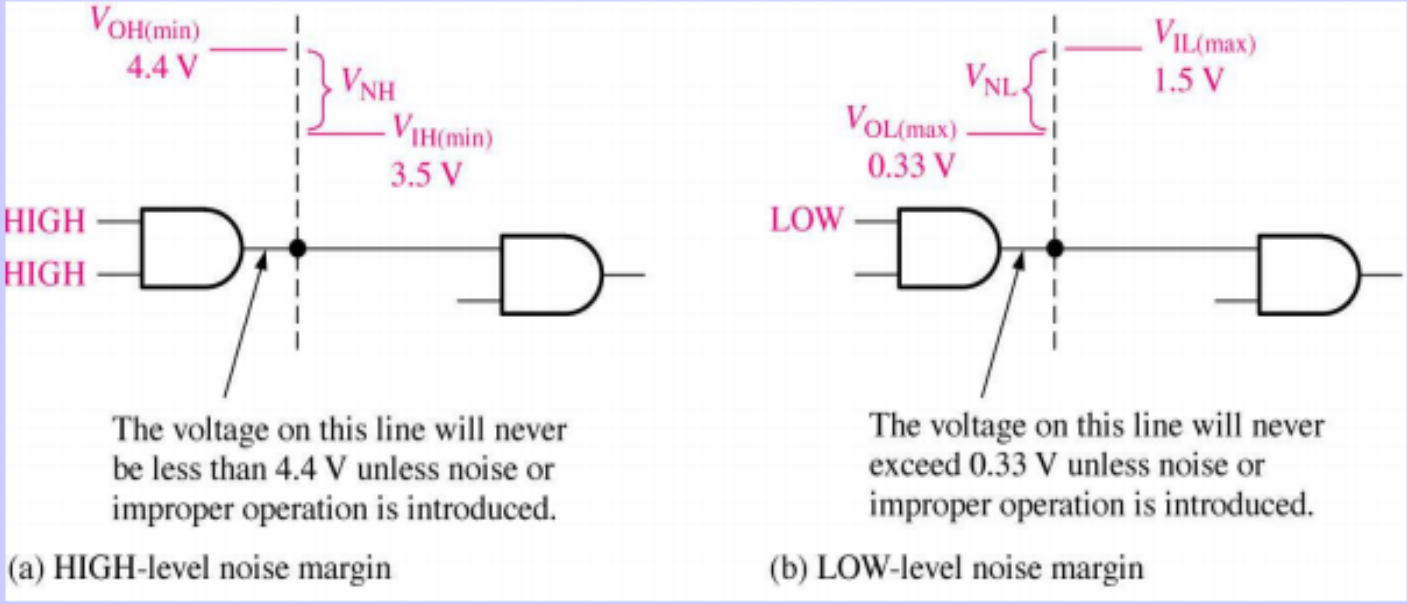


Figure 8-4: Noise Margin

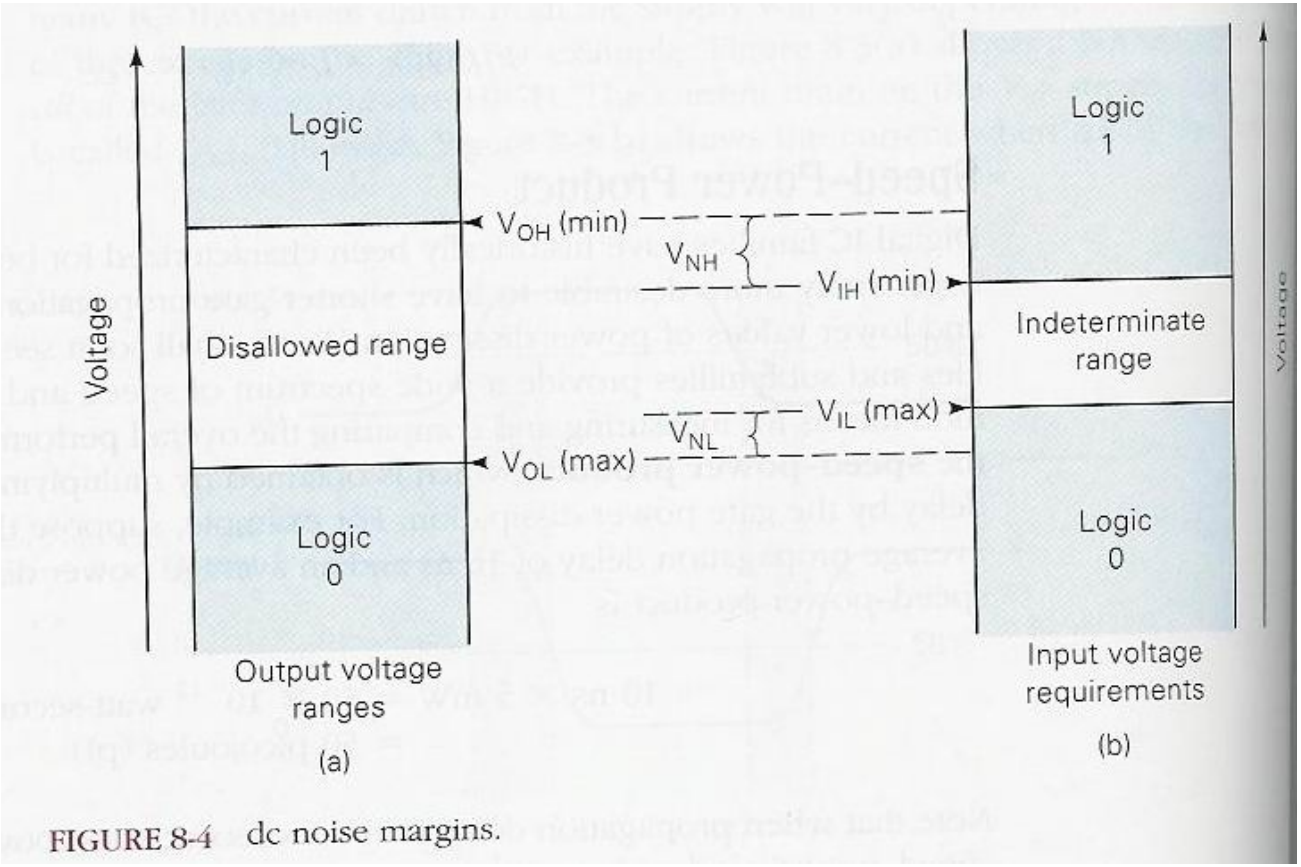
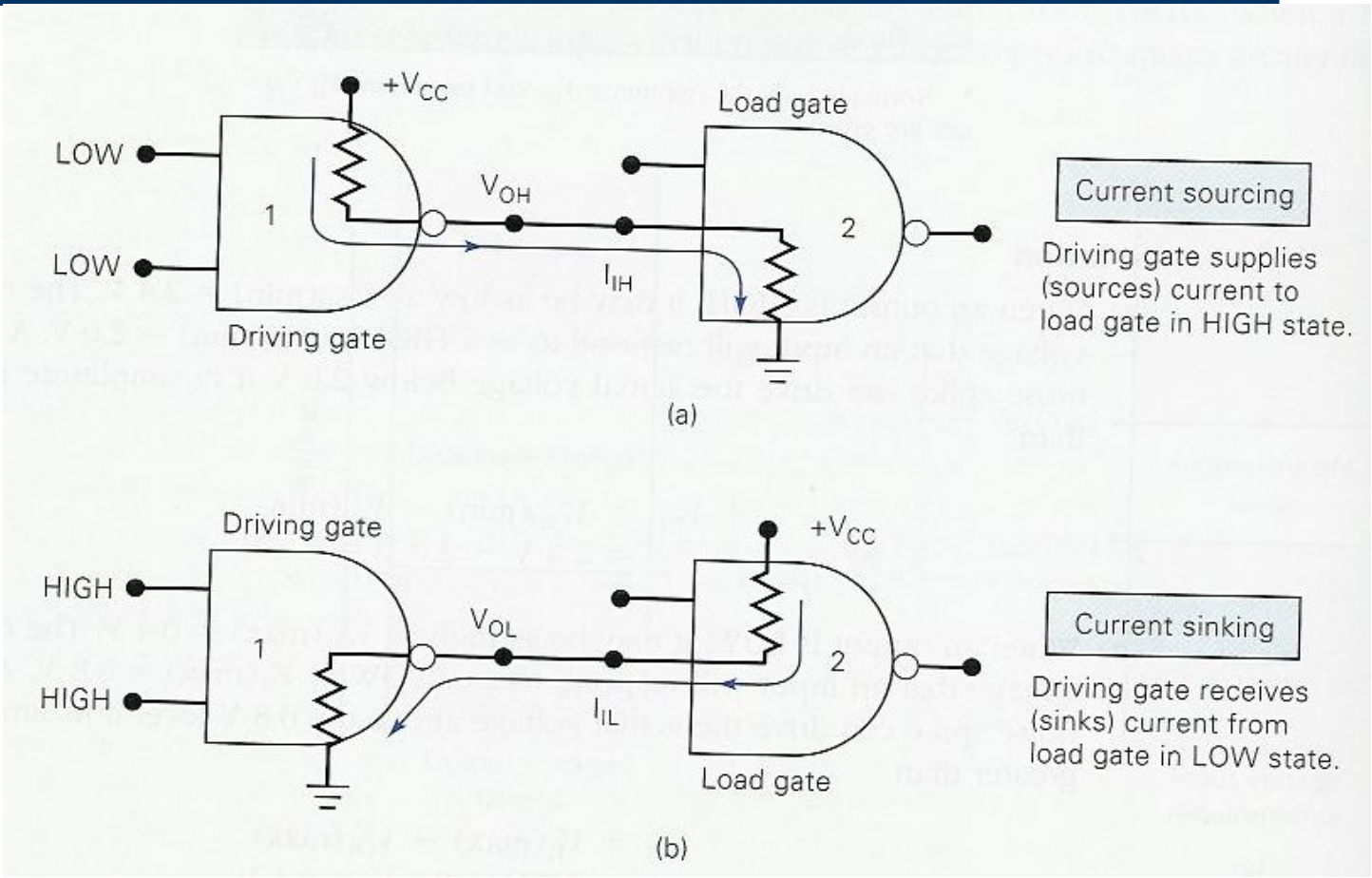


FIGURE 8-4 dc noise margins.

Invalid Voltage Levels

- For proper operation the input voltage levels to a logic must be kept outside the indeterminate range.
- Lower than V_{IL}(max) and higher than V_{IH}(min).

Current-Sourcing and Sinking



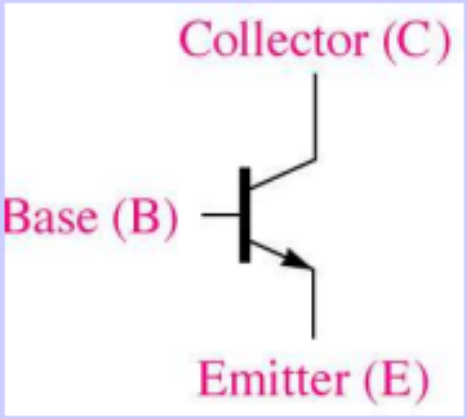
IC Packages

- DIP
- J-Lead
- Gull-wing
- Table 8-2 for a complete list.

The TTL Logic Family

- Transistor-transistor logic
- Figure 8-7: NAND gate.
- Circuit operation: LOW state, current-sinking
- Circuit operation: HIGH state, current-sourcing.

Figure 15--25 The symbol for a BJT.



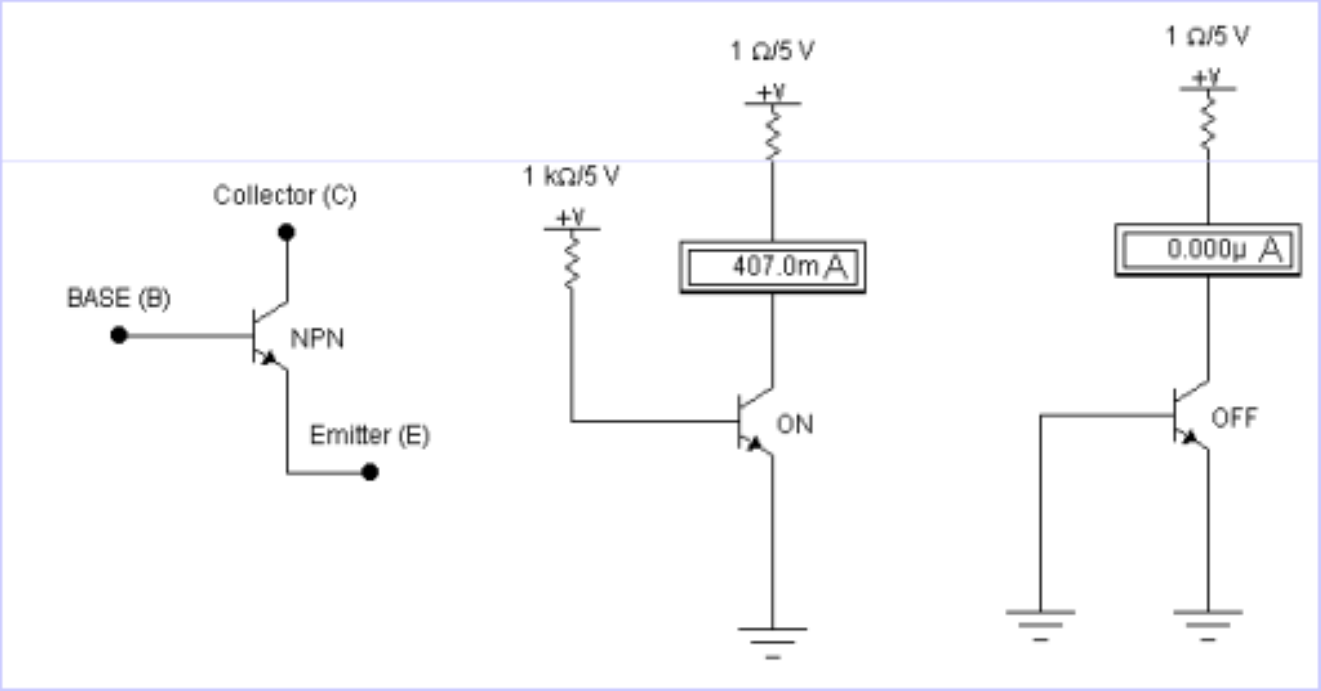
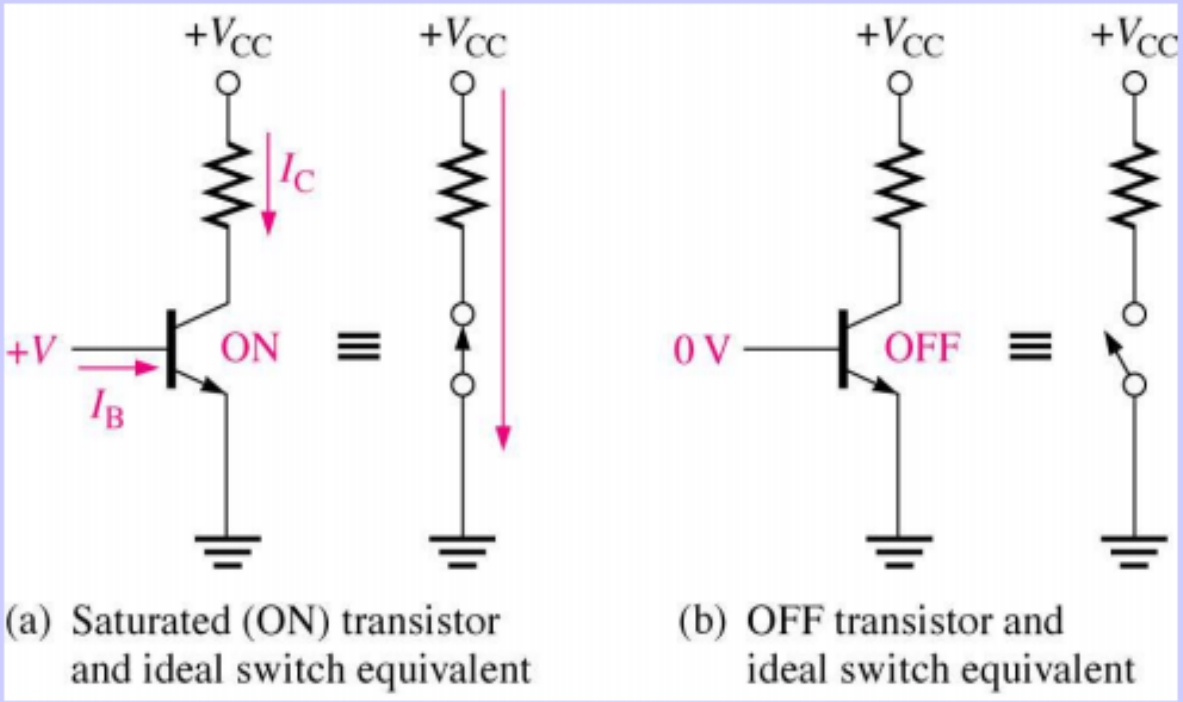


Figure 15--26 The ideal switching action of the BJT.



(a) Saturated (ON) transistor and ideal switch equivalent

(b) OFF transistor and ideal switch equivalent

Figure 15--27 A standard TTL inverter circuit.

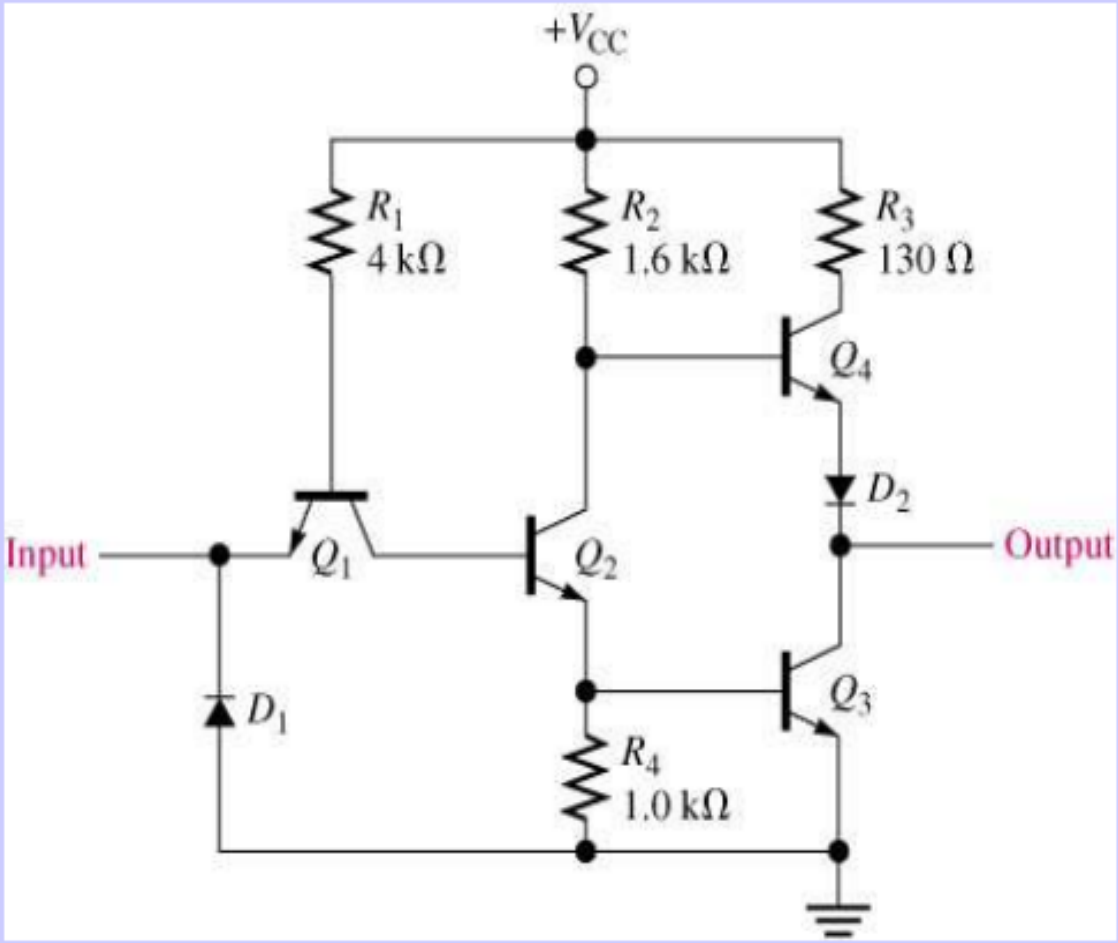
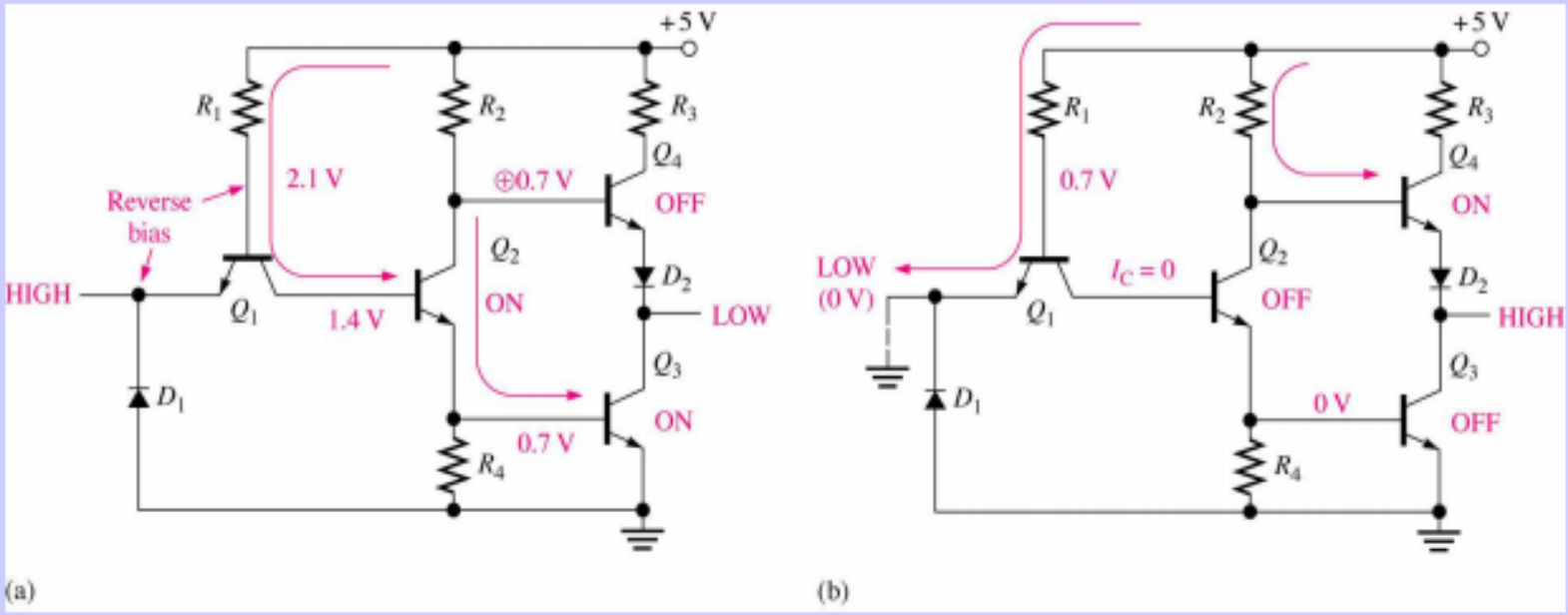


Figure 15--28 Operation of a TTL inverter.



TTL NAND Gate

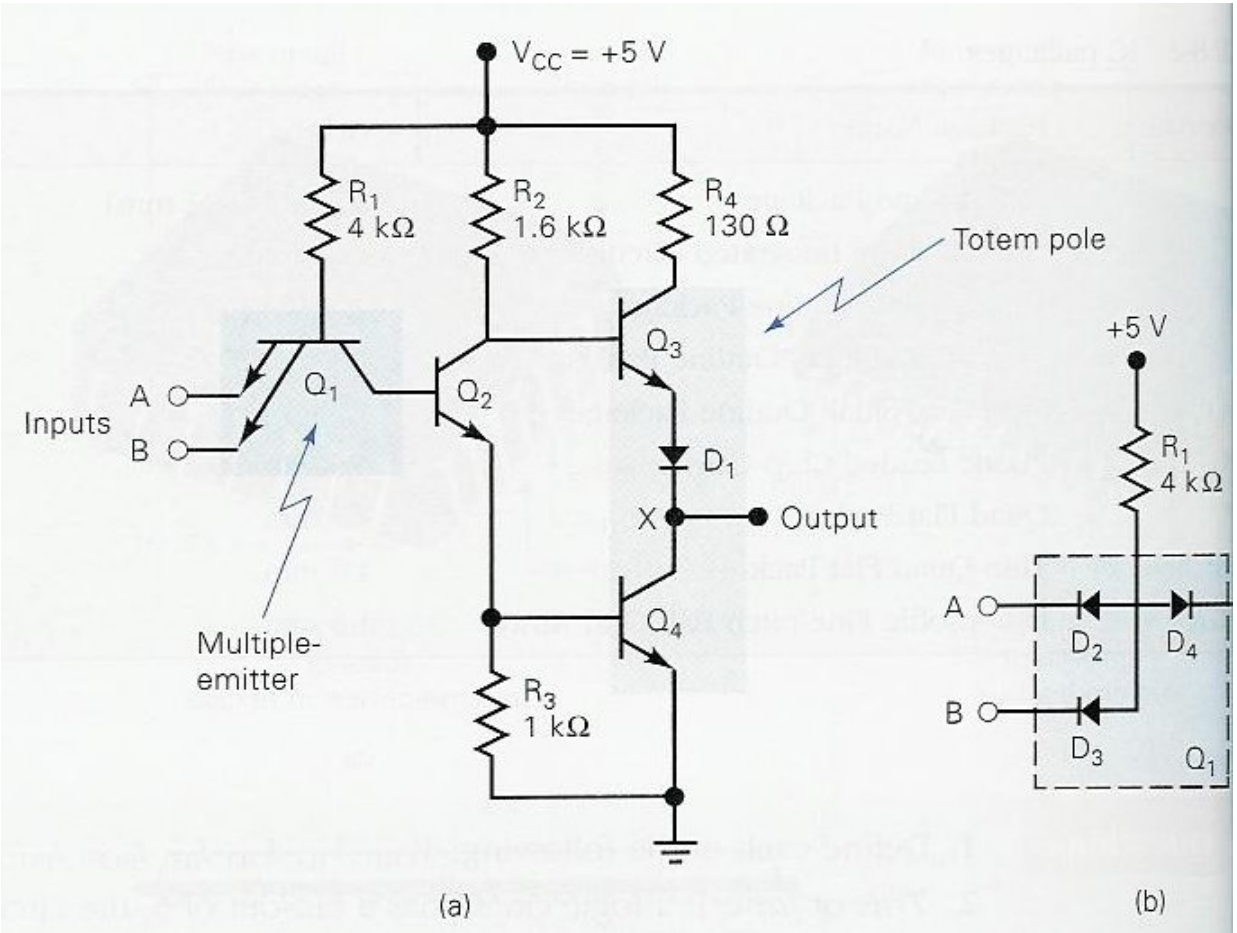
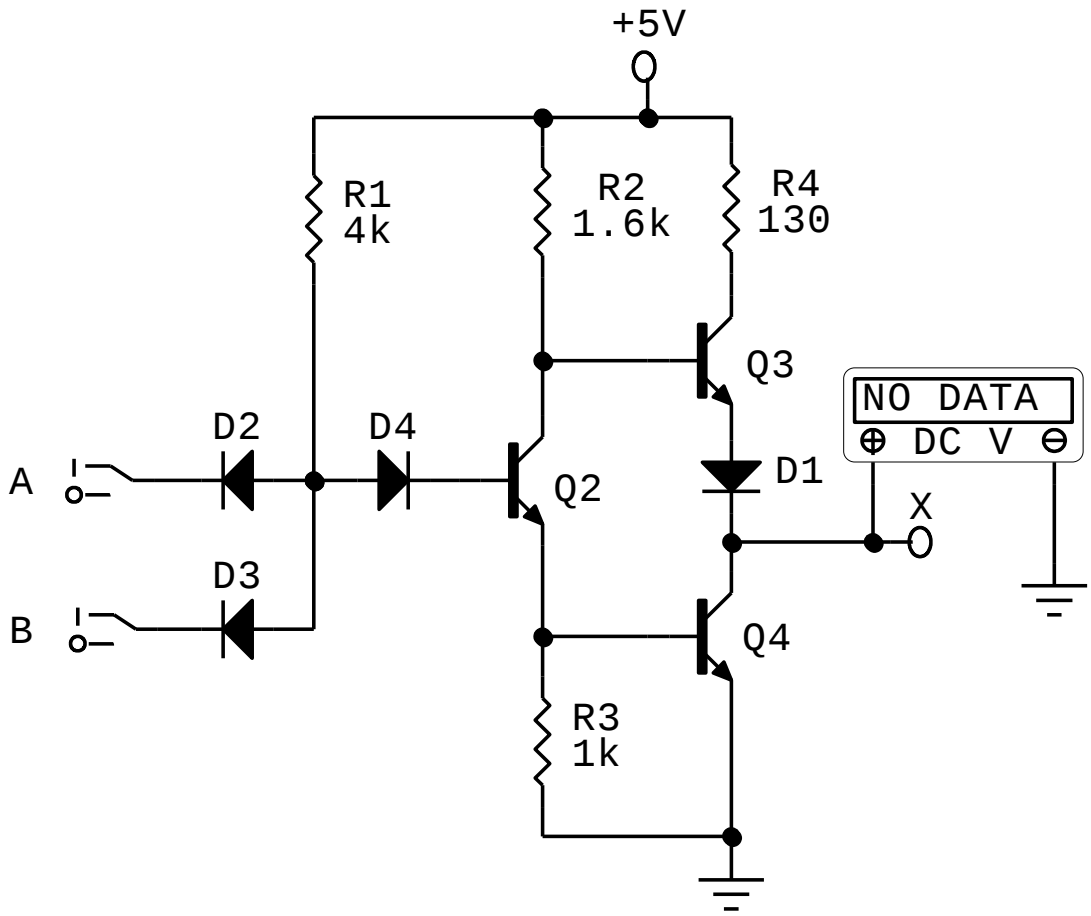
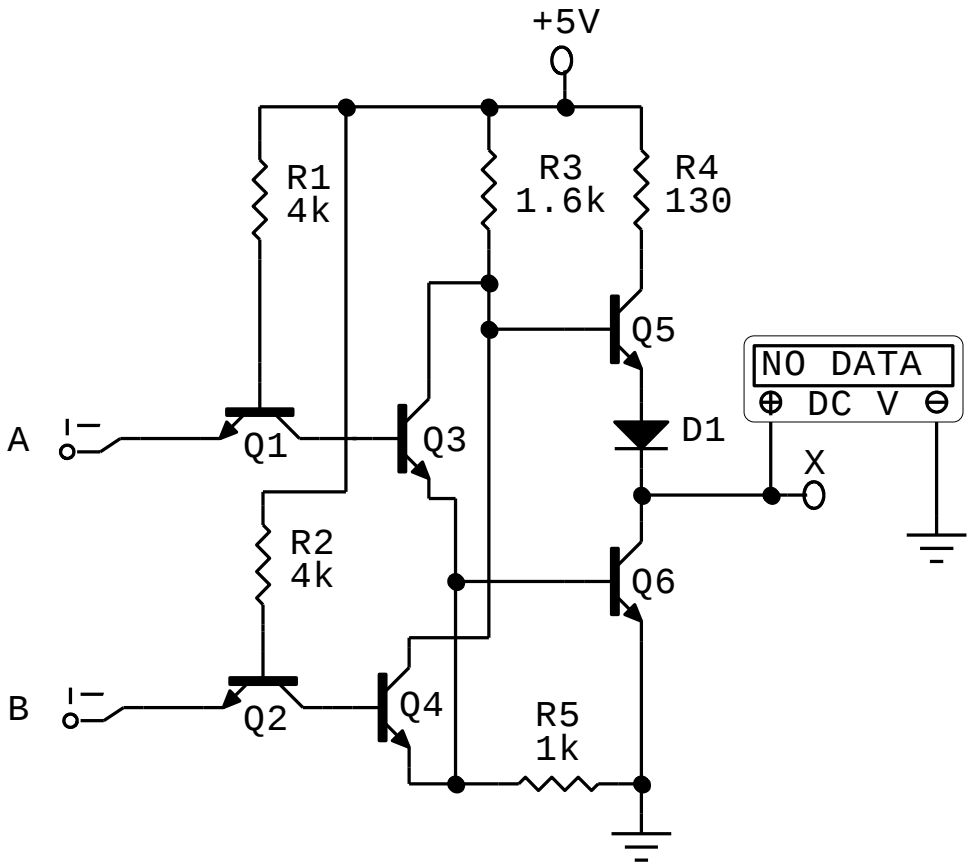


Figure 8-8: TTL NAND Gate



TTL NOR Gate Circuit



Standard TTL Series Characteristics

- TI introduced first line of standard TTL: 54/74 series (1964)
- Manufacturers' data sheets (Figure 8-11)
  - Supply voltage and temperature range
  - Voltage levels
  - Maximum voltage ratings
  - Power dissipation
  - Propagation delays
  - Fan-out
- Example 8-2

Improved TTL Series

- 74 Series
- Schottky TTL, 74S Series: higher speed
- Low-Power Schottky TTL, 74LS series
- Advanced Schottky TTL, 74AS Series
- Advanced Low-Power Schottky TTL, 74ALS Series
- 74F-Fast TTL

Comparison of TTL Series

TABLE 8-6 Typical TTL series characteristics.

	74	74S	74LS	74AS	74ALS	74F
Performance ratings						
Propagation delay (ns)	9	3	9.5	1.7	4	3
Power dissipation (mW)	10	20	2	8	1.2	6
Speed–power product (pJ)	90	60	19	13.6	4.8	18
Max. clock rate (MHz)	35	125	45	200	70	100
Fan-out (same series)	10	20	20	40	20	33
Voltage parameters						
V_{OH}(min)	2.4	2.7	2.7	2.5	2.5	2.5
V_{OL}(max)	0.4	0.5	0.5	0.5	0.5	0.5
V_{IH}(min)	2.0	2.0	2.0	2.0	2.0	2.0
V_{IL}(max)	0.8	0.8	0.8	0.8	0.8	0.8

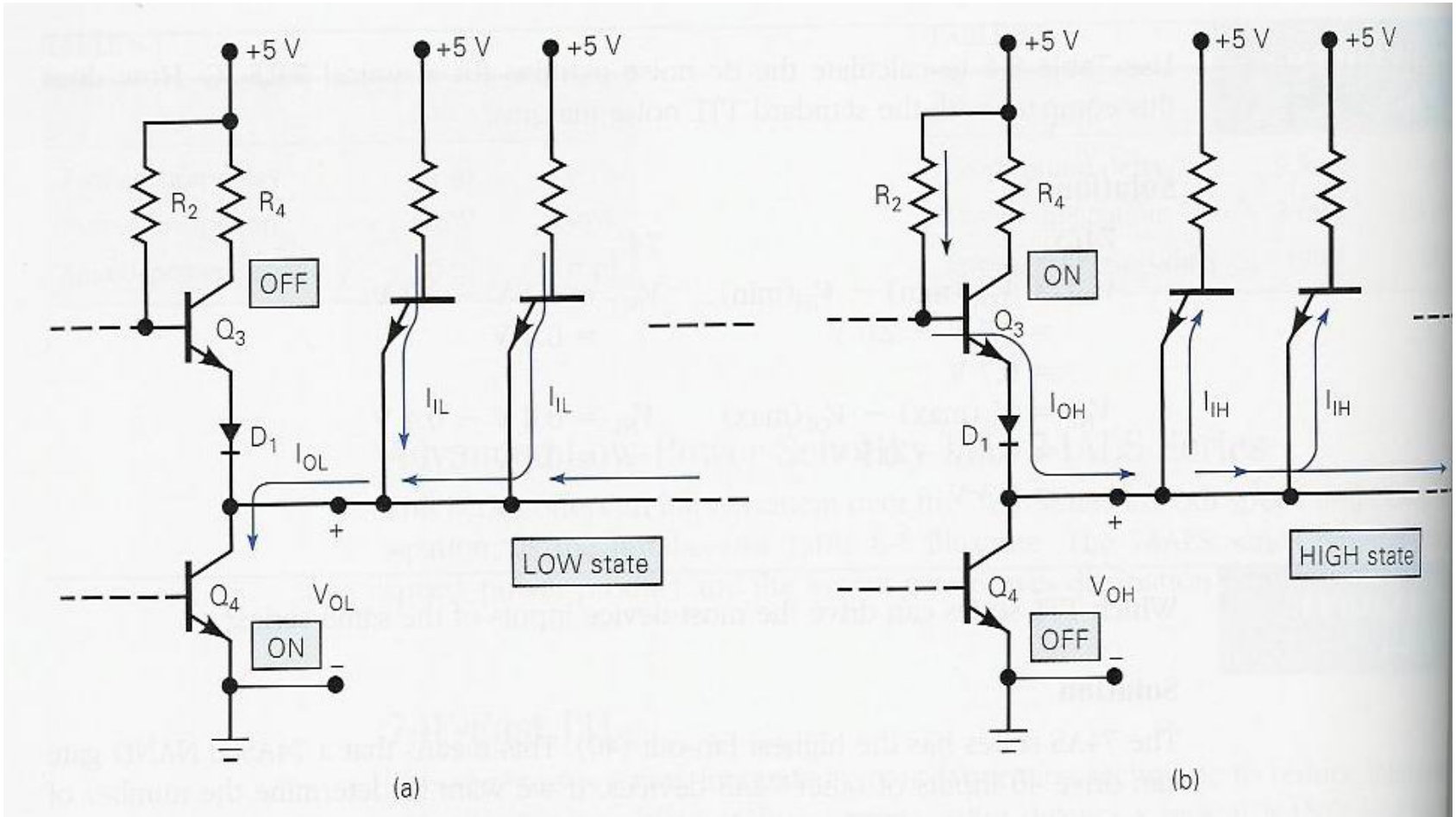
Examples

- Example 8-3: Noise margin of 74 and 74LS
- Example 8-4: TTL series with max number of fan-out

TTL Loading and Fan-Out

- Figure 8-13: currents when a TTL output is driving several inputs.
- TTL output has a limit, I_{OL}(max), on how much current it can sink in the LOW state.
- It also has a limit, I_{OH}(max), on how much current it can source in the HIGH state.

Figure 8-13


+5 V
+5 V
+5 V
R2
R4
OFF
Q3
D1
IOL
IIL
IIL
+
LOW state
Q4
VOL
ON
(a)
+5 V
+5 V
+5 V
R2
R4
ON
Q3
IOH
IIH
IIH
D1
+
HIGH state
Q4
VOH
OFF
(b)

Determining the fan-out

- Same IC family.
- Find fan-out (LOW):$I_{OL}(max)/I_{IL}(max)$
- Find fan-out (HIGH):$I_{OH}(max)/I_{IH}(max)$
- Fan-out: smaller of the above
- Example 8-6: Fan-out of 74AS20 NAND gates

Determining the fan-out

- Different IC families
- Step 1: add up the I_{IH} for all inputs connected to an output. The sum must be less than the output's I_{OH} specification.
- Step 2: add up the I_{IL} for all inputs connected to an output. The sum must be less than the output's I_{OL} specification.
- Examples 8-7 to 8-9.

Other TTL Characteristics

- Unconnected inputs (floating): acts like a logic 1.
- Unused inputs: three different ways to handle.
- Tie-together inputs: common input generally represent a load that is the sum of the load current rating of each individual input. Exception: for AND and NAND gates, the LOW state input load will be the same as a single input no matter how many inputs are tied together.
- Example 8-10.

Other TTL Characteristics (cont'd)

- Current transients (Figure 8-18)
- Connecting TTL outputs together
  - Totem-pole outputs should no be tied together

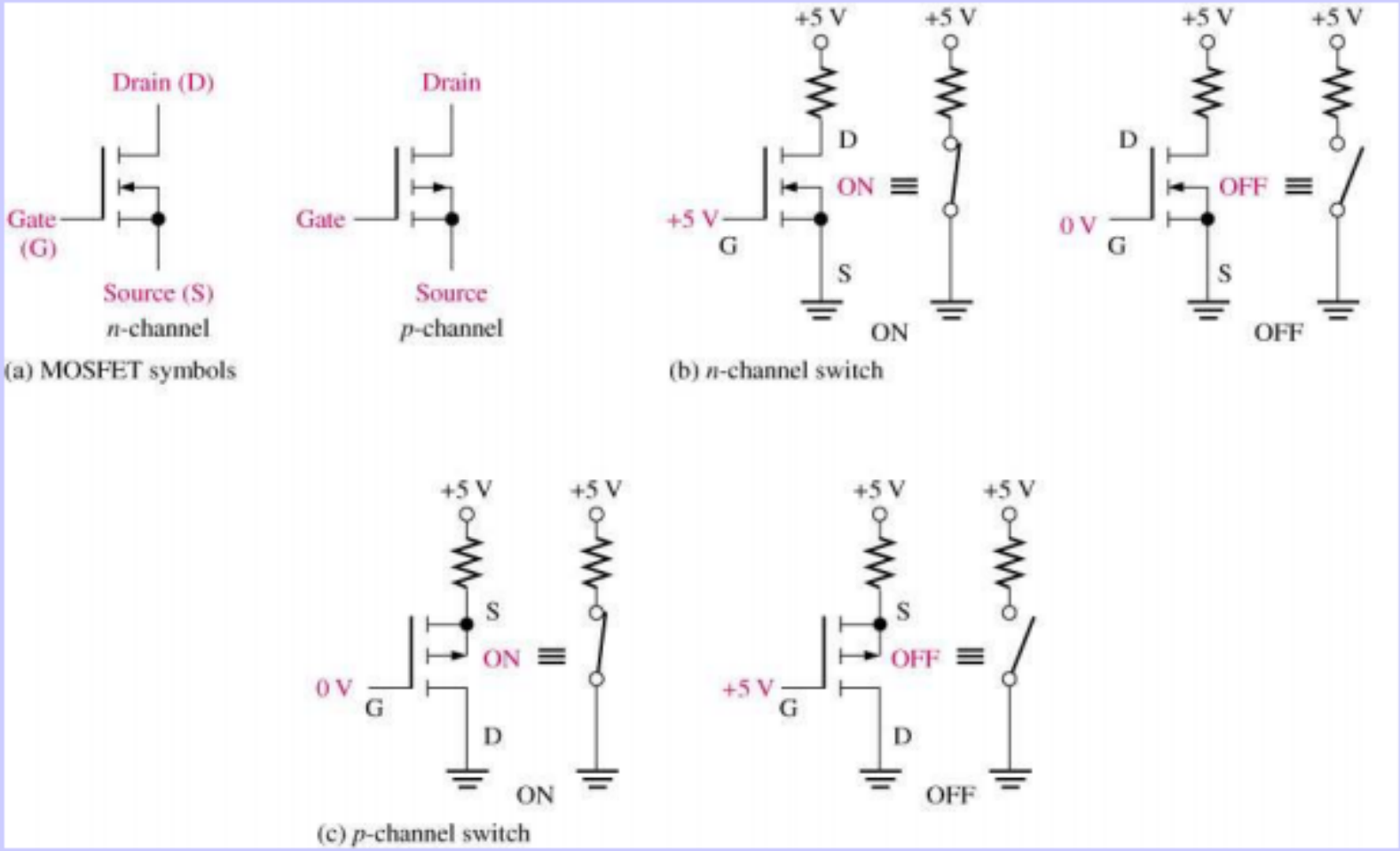
MOS Digital ICs

- MOS: metal-oxide-semiconductor
- MOSFET: MOS field-effect transistors.
- The Good:
  - Simple
  - Inexpensive to fabricate
  - Small
  - Consumes little power
- The bad:
  - Static-electricity damage.
  - Slower than TTL

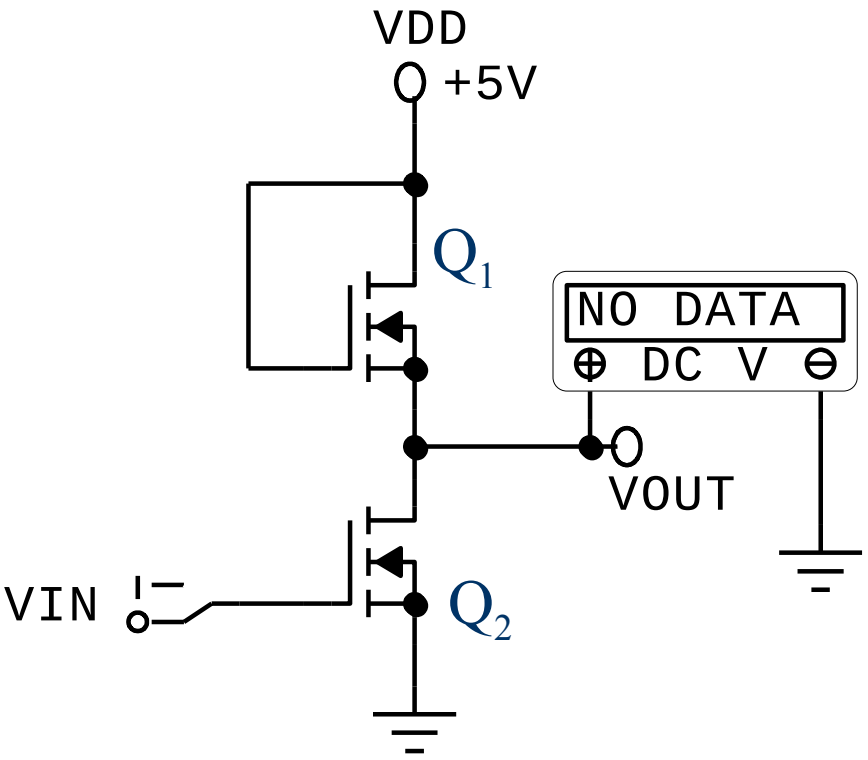
The MOSFET

- P-MOS: P-channel MOS
- N-MOS: N-channel MOS, fastest
- CMOS: complementary MOS, higher speed, lower power dissipation.
- Figure 8-20: how N-channel MOSFET works:
  - V_{GS}=0V OFF State, R_{off}= 10^{10} ohms
  - V_{GS}=5V ON State,R_{on}=1000 ohms

Figure 15--15 Basic symbols and switching action of MOSFETs.



N-MOS INVERTER

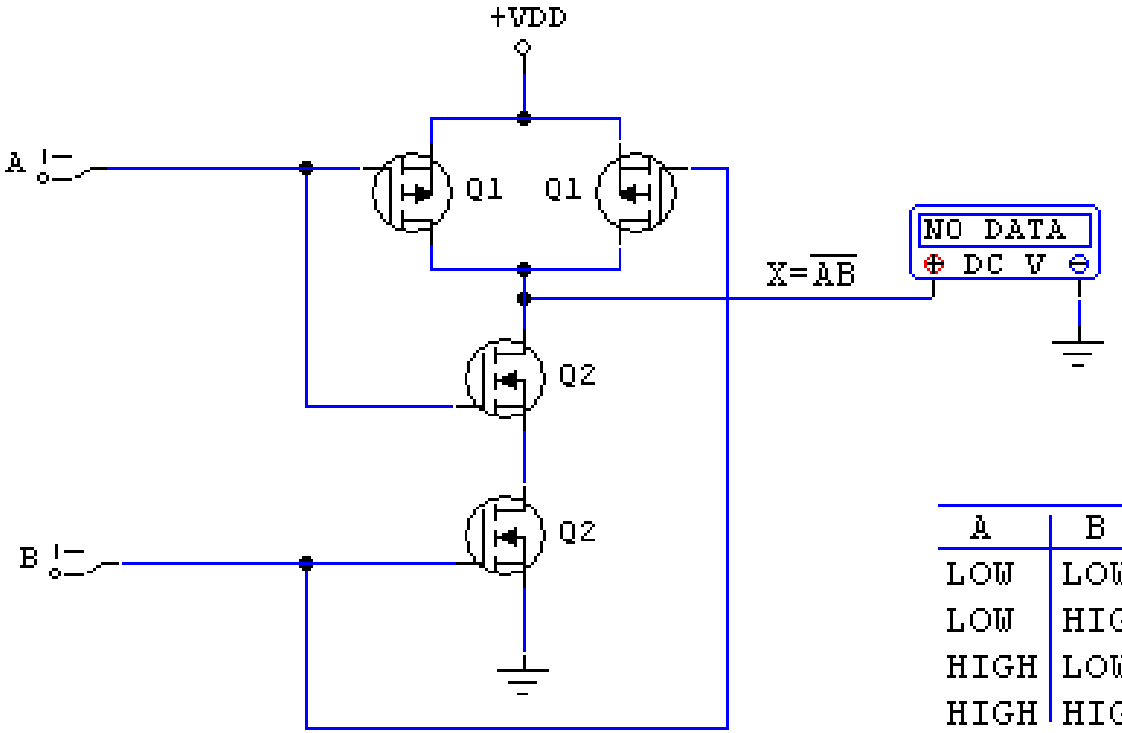


V_{in}	Q_1	Q_2	V_{out}
0V	R_{on}= 100K	R_{off}= 10^{10}K	5V
5V	R_{on}= 100K	R_{on}= 1K	0.05 V

CMOS

- Uses both P- and N-channel MOSFETs in the same circuit to realize several advantages over the P-MOS and N-MOS families.
- CMOS INVERTER (Figure 8-22)
- CMOS NAND (Figure 8-23)
- CMOS NOR (Figure 8-24)

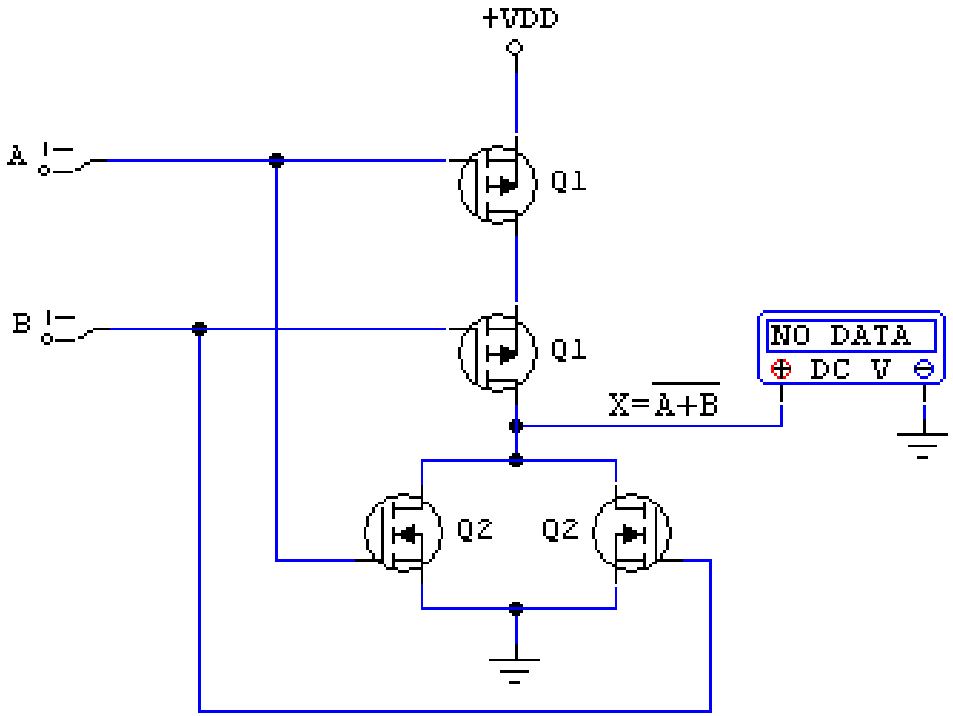
CMOS NAND Gate



A	B	X
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	HIGH

CMOS NAND gate.

CMOS NOR Gate



A	B	X
LOW	LOW	HIGH
LOW	HIGH	LOW
HIGH	LOW	LOW
HIGH	HIGH	LOW

CMOS NOR gate.

CMOS Series Characteristics

- Pin-compatible
- Functionally equivalent
- Electrically compatible
- 4000/14000 Series
- 74C, 74HC/HCT, 74AC/ACT, 74AHC,
- BiCMOS (Bipolar + CMOS)
- Table 8-10: low-voltage series characteristics
- Table 8-11, comparison of ECL, CMOS and TTL Series

Low-Voltage Technology

- 5V → 3.3V
- Reduces power dissipation
- 74LVC, 74ALVC, 74LV, 74LVT

Other CMOS Issues

- Conventional CMOS outputs should not be connected together.
- Bilateral switch (Figure 8-43,44)

IC Interfacing

- Connecting the output(s) of one circuit to the input(s) of another circuit that has different electrical characteristics.
- Occurs often in complex digital systems, where designers utilize different logic families for different parts of system.
- TTL driving CMOS
- CMOS driving TTL

TTL driving CMOS

- No problem with the current requirements (See Table 8-12)
- V_{OH}(min) of TTL is low compared to V_{IH}(min) of some CMOS series (Table 8-9), use pull-up resistor to raise TTL output voltage (Figure 8-46)
- TTL driving high-voltage CMOS (V_{DD} of CMOS is greater than 5V)
  - Use 7407 buffer
  - Use voltage level-translator (such as 4504B)

CMOS driving TTL

- HIGH state:Table 8-9 and 8-12 indicate no special consideration the HIGH state.
- LOW state: depends on the series used.