

(1) Convert  $(934.685)_{10}$  to base 2, 8 and 16.

$$\begin{array}{r}
 2 \overline{)934} \\
 2 \overline{)467} \quad 0 \\
 2 \overline{)233} \quad 1 \\
 2 \overline{)116} \quad 1 \\
 2 \overline{)58} \quad 0 \\
 2 \overline{)29} \quad 0 \\
 2 \overline{)14} \quad 1 \\
 2 \overline{)7} \quad 0 \\
 2 \overline{)3} \quad 1 \\
 2 \overline{)1} \quad 1 \\
 2 \overline{)0} \quad 1
 \end{array}$$

LSB ↑ MSB

$$\begin{array}{r}
 0.685 \\
 \times 2 \\
 \hline
 1.37 \\
 \times 2 \\
 \hline
 0.74 \\
 \times 2 \\
 \hline
 1.48 \\
 \times 2 \\
 \hline
 0.96 \\
 \times 2 \\
 \hline
 0.92
 \end{array}$$

$$(934.685)_{10} = (1110100110.101010)_2$$

∴ (converted binary)

Now,

$$\begin{array}{r}
 0 \ 0 \ 1 \ 1 \ 1 \ 0 \ 1 \ 0 \ 0 \ 1 \ 1 \ 0 \\
 \hline
 1 \ 6 \ 4 \ 6 \ 5 \ 0 \ 6 \ 4 \ 0 \ 6 \ 5 \ 0
 \end{array}$$

$$(934.685)_{10} = (1646.52)_8 \quad (\text{converted octal})$$

$$\begin{array}{r}
 0 \ 0 \ 1 \ 1 \ 1 \ 0 \ 1 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0 \\
 \hline
 3 \ A \ 6 \ 4 \ 0 \ 8
 \end{array}$$

$$(934.685)_{10} = (3A6.A8) \quad (\text{converted Hexadecimal})$$

(1) Represent  $(-469)_{10}$  to sign-magnitude 1's complement and 2's complement for.

Ans.

$$(-469)_{10} = \underbrace{1}_{\text{sign bit}} \underbrace{111010101}_{\text{magnitude}} \quad (\text{signed magnitude})$$

1's complement: 000101010

$$\text{1's complement : } \underbrace{1}_{\text{sign bit}} \underbrace{000101010}_{\text{magnitude}} \quad (\text{signed 1's complement})$$

2's complement :

$$\begin{array}{r} 1000101010 \\ +1 \\ \hline \underbrace{1000101011}_{\text{sign bit magnitude}} \end{array} \rightarrow (\text{signed 2's complement})$$

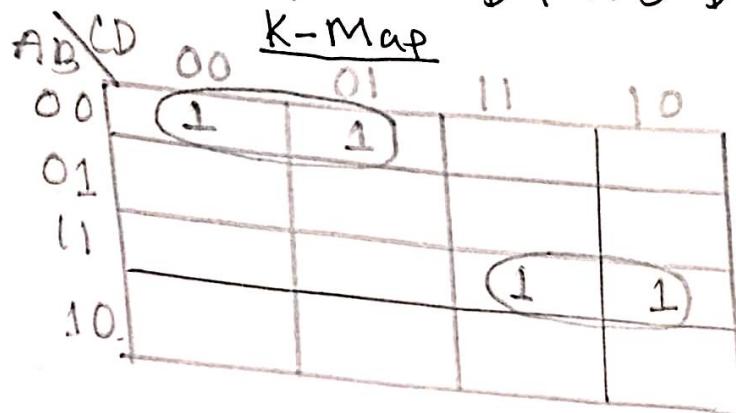
(3) Convert the following expression to sum-of-product (SOP) forms.

$$\begin{aligned} (a) \quad & BC(C'D' + CE) \\ & = BC C'D' + BC CE \\ & = 0 + BC E \\ & = BCE \end{aligned}$$

$$\begin{aligned} (b) \quad & B + C(BD + (C + D')E) \\ & = B + CBD + (C + D')CE \\ & = B + CEC + CED \\ & = B + CE + CED \\ & = B + CE \end{aligned}$$

(4.) Use the a Karnaugh map to reduce each expression to a minimum SOP form:

$$(a) A'B'C'D' + A'B'C'D + ABCD + ABCD'$$

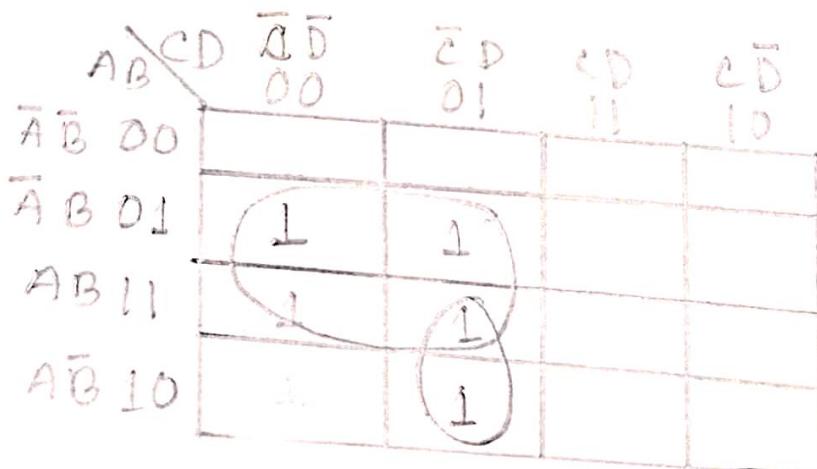


$$= \bar{A}\bar{B}\bar{C} + ABC$$

$$(b) A'B(C'D' + C'D) + AB(C'D' + C'D) + AB'C'D$$

$$= A'B'C'D' + A'B'C'D + AB'C'D' + ABC'D + AB'C'D$$

K-Map



$$= B\bar{C} + A\bar{C}D$$

(5)

First Comparison:

Group	Match pairs	Binary representation	check
1	0, 1	0 0 0 -	
2	(1, 5) (1, 9)	0 - 0 1 - 0 0 1	

Prime implicants:

$$(0, 1) = 0 0 0 -$$

$$(1, 5) = 0 - 0 1$$

$$(1, 9) = - 0 0 1$$

$$6 = 0 1 1 0$$

$$10 = 1 0 1 0$$

$$12 = 1 \cdot 1 0 0$$

Petries method:

P.I	Minterm involved	0	1	5	6	9	10	12
$\bar{A} \bar{B} \bar{C}$	0, 1	(X)	X					
	1, 5		X	(X)				
	1, 9			X		(X)		
	6				(X)			
	10						(X)	
	12							(X)

Essential prime implicants are

$$x = \bar{A} \bar{B} \bar{C} + \bar{A} \bar{C} D + \bar{B} \bar{C} D + \bar{A} B C \bar{D} + A \bar{B} C \bar{D}$$

$$+ A B \bar{C} \bar{D}$$

(5)

Prime implicants:

$$(1, 3, 5, 7) = (- - \perp)$$

$$(6, 7) = \perp \perp -$$

Now, Petriek Method

P-I	Minterm involved	1	3	5	6	7
c	1, 3, 5, 7	✗	✗	✗		✗
AB	6, 7				✗	✗

Essential prime implicant,  $X = AB + C$

$$\begin{aligned}
 5(b) \quad X &= A' B' C' D' + A' B' C D + A' B C' D + A B C' D' \\
 &\quad + A B' C D' + A' B C D' + A B' C' D \\
 &= (0000)_2 + (0001)_2 + (0102)_2 + (1100)_2 \\
 &\quad + (1010)_2 + (0110)_2 + (1001)_2
 \end{aligned}$$

Group	Minterm	Binary representation	check
1	0	0 0 0 0	✓
2	1	0 0 0 1	✓
	5	0 1 0 1	✓
	6	0 1 1 0	
3	9	1 0 0 1	✓
	10	1 0 1 0	
	12	1 1 0 0	

5(a)

$$X = ABC + A'B'C + ABC' + AB'C + A'BC$$

Input

Group	Minterm	Binary representation	check
1	1	0 0 1	✓
2	3	0 1 1	✓
	5	1 0 1	✗
	6	1 1 0	✓
3	7	1 1 1	✓

First Comparison

Group	Match pairs	Binary Representation	check
1	0, 3	0 - 1	✓
	1, 5	- 0 1	✓
2	3, 7	- 1 1	✓
	5, 7	1 - 1	✓
	6, 7	1 1 -	

Second Comparison

Group	Match pairs	Binary Representation	check
1	1, 3, 5, 7 1, 5, 3, 7	- - 1 - - 1	

## Question - 6 :

### Assumptions:

Let the variable 'A' represents switch at back door.

Let the variable 'B' represents switch at front door.

Let high output denoted by '1' represent the ON condition.

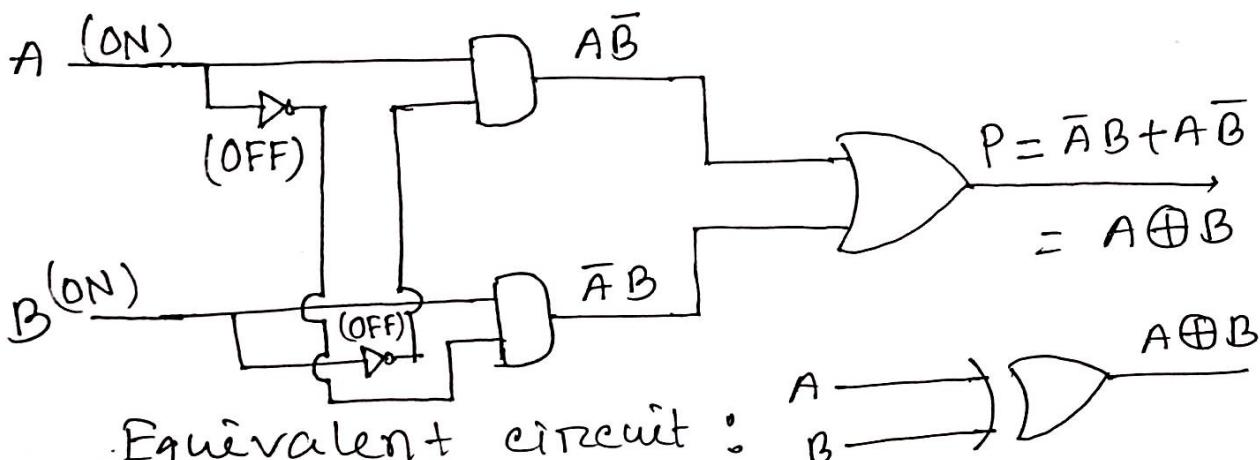
Let low output denoted by '0' represent the OFF condition.

### Constructing truth table

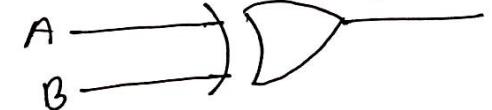
A	B	Output (P)
0	0	0
0	1	1
1	0	1
1	1	0

$$\Rightarrow P = \bar{A}B + A\bar{B} = A \oplus B$$

### Logic circuit



Equivalent circuit :



7. Design and discuss a 3 bit adder/subtractor circuit.

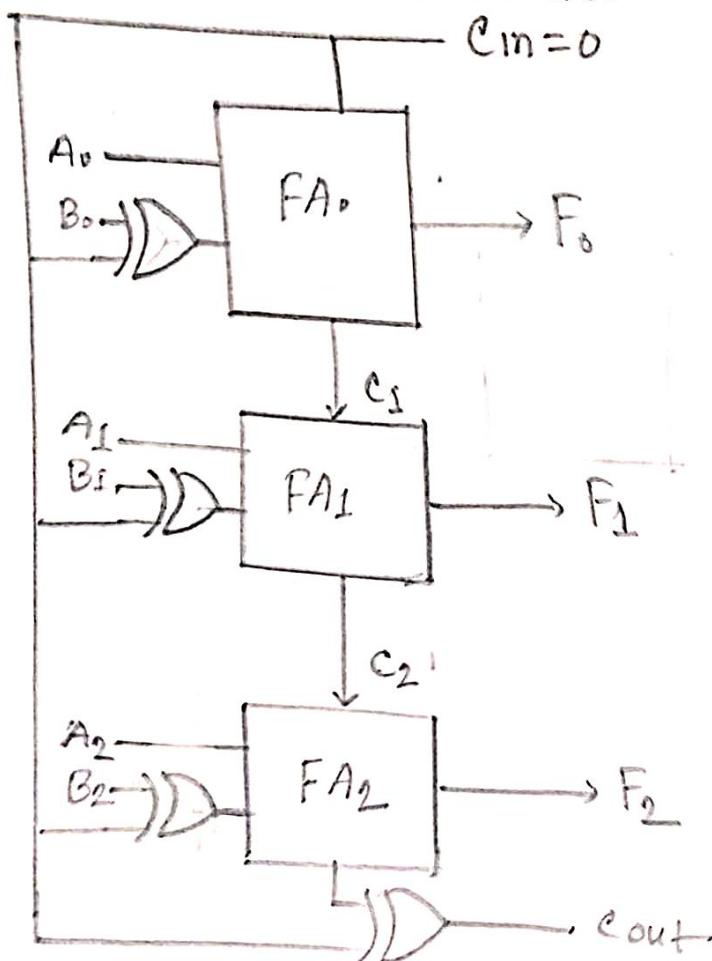


Fig: 3 bit Adder/Subtractor circuit.

When  $C_{in}=1$ , the circuit is a subtractor and when  $C_{in}=0$ , the circuit becomes adder. The X-OR gate consists of two input to which one is connected to the B and other to input  $C_{in}$ .

When  $C_{in}=0$ , B X-OR of 0 produce B. Then full adders add the B with A with carrying input zero and hence an addition operation is performed.

8. Design a combinational circuit with inputs ABCD and output w, x, y, z. Assume that the inputs A, B, C, D represent a 4-bit signed number. The output is also a signed number, which is 2's complemented of the input.

(8)

## 2's complement

Input				Output				
a	b	c	d	w	x	y	z	g
0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	1
0	0	1	0	1	1	1	0	0
0	0	1	1	1	1	0	1	1
0	1	0	0	1	1	0	0	0
0	1	0	1	1	0	1	0	0
0	1	1	0	1	0	1	1	0
0	1	1	1	1	0	0	1	0
1	0	0	0	1	0	0	1	1
1	0	0	1	0	1	0	0	0
1	0	1	0	0	1	1	1	1
1	0	1	1	0	0	1	0	0
1	1	0	0	0	1	0	1	1
1	1	0	1	0	0	0	1	0
1	1	1	0	0	0	1	1	0
1	1	1	1	1	0	0	1	1

For w

		cd	00	01	11	10
		ab	00	01	11	10
00	00	1	1	1	1	1
01	01	1	1	1	1	1
11	11					
10	10	1				

$$W = \bar{a}\bar{d} + \bar{a}\bar{c} + \bar{a}\bar{b} + a\bar{b}\bar{c}\bar{d}$$

For x

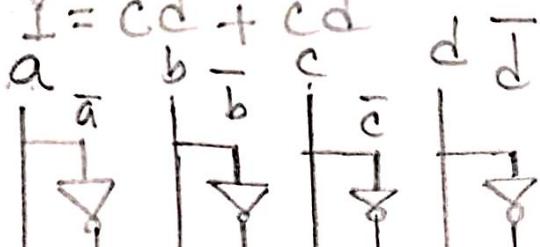
		cd	00	01	11	10
		ab	00	01	11	10
00	00	1	1	1	1	1
01	01	1	1	1	1	1
11	11	1				
10	10	1	1	1	1	1

$$X = b\bar{c}\bar{d} + \bar{a}\bar{d} + \bar{a}\bar{c}$$

For Y:

ab	00	01	11	10
cd	00	1	1	
ab	01	1	1	
cd	11	1	1	
ab	10	1	1	

$$Y = \bar{c}d + c\bar{d}$$



For Z:

ab	00	01	11	10
cd	00	1	1	
ab	01	1	1	
cd	11	1	1	
ab	10	1	1	

$$Z = d$$

$$W = \bar{a}\bar{b}\bar{c}d + ab + \bar{a}c\bar{d}a$$

$$X = b\bar{c}\bar{d} + \bar{b}d + \bar{b}\bar{c}$$

$$Y = \bar{c}d + c\bar{d}$$

$$Z = d$$

9.

Input			Output			
X	Y	Z	A	B	C	
0	0	0	0	0	1	1
1	0	1	0	1	0	2
2	0	1	0	1	1	3
3	0	1	1	1	0	4
4	1	0	0	0	1	3
5	1	0	1	1	0	4
6	1	1	0	1	0	5
7	1	1	1	1	0	6

Output for C :

Y <sup>2</sup>		00	01	11	10
X	Z	0	1	1	0
X	Z	1	1	0	1

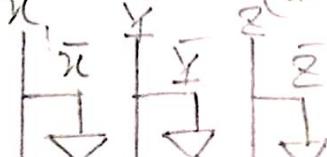
$C = \bar{Z}$

Output for A :

Y <sup>2</sup>		00	01	11	10
X	Z	0	1	1	0
X	Z	1	1	0	1

$$A = XZ + YZ + X'Y$$

$$= X(Y+Z) + YZ$$



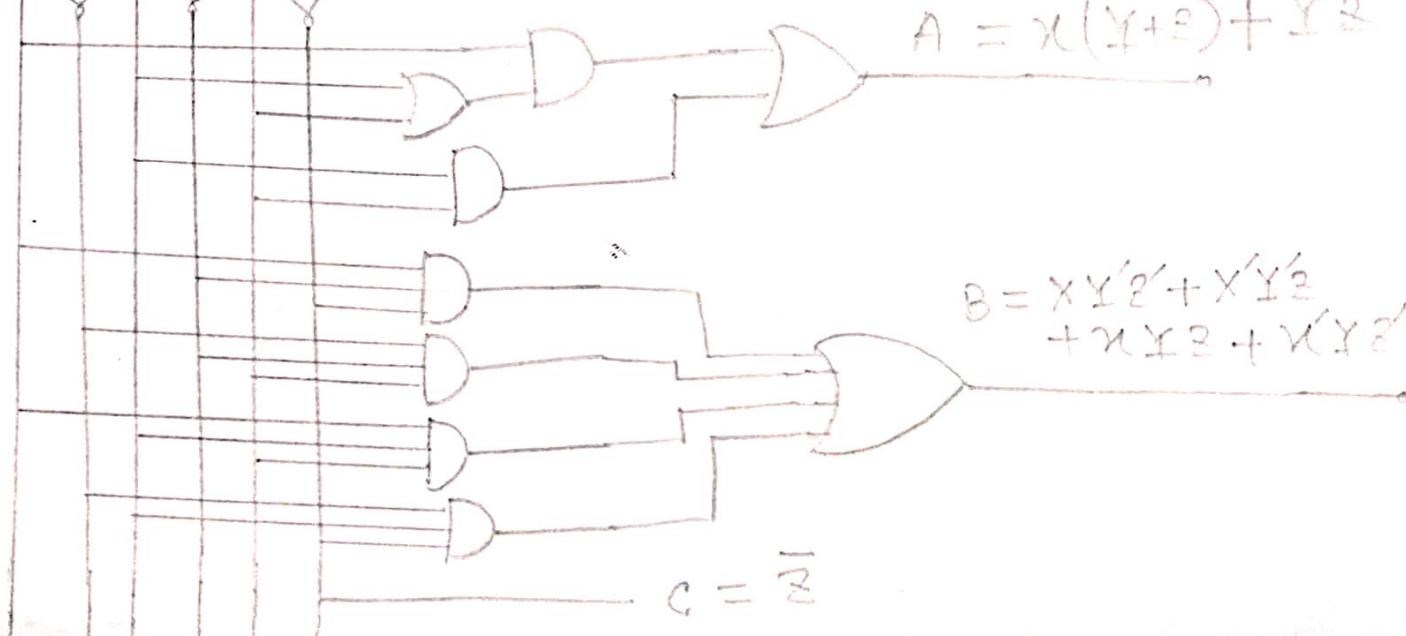
Output for B :

Y <sup>2</sup>		00	01	11	10
X	Z	0	1	1	0
X	Z	1	1	0	1

$$B = X'Y'Z' + X'Y'Z + X'YZ + X'YZ'$$

$$A = X(Y+Z) + YZ$$

$$B = X'Y'Z' + X'Y'Z + X'YZ + X'YZ'$$



$$C = \bar{Z}$$

10.

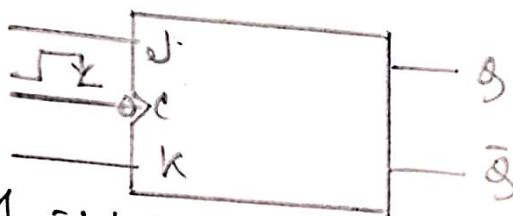
The difference between the given two J-K flip-flop is one is negative edge trigger J-K flip-flop and the other is positive edge trigger J-K flip-flop.

Truth Table of J-K flip-flop:

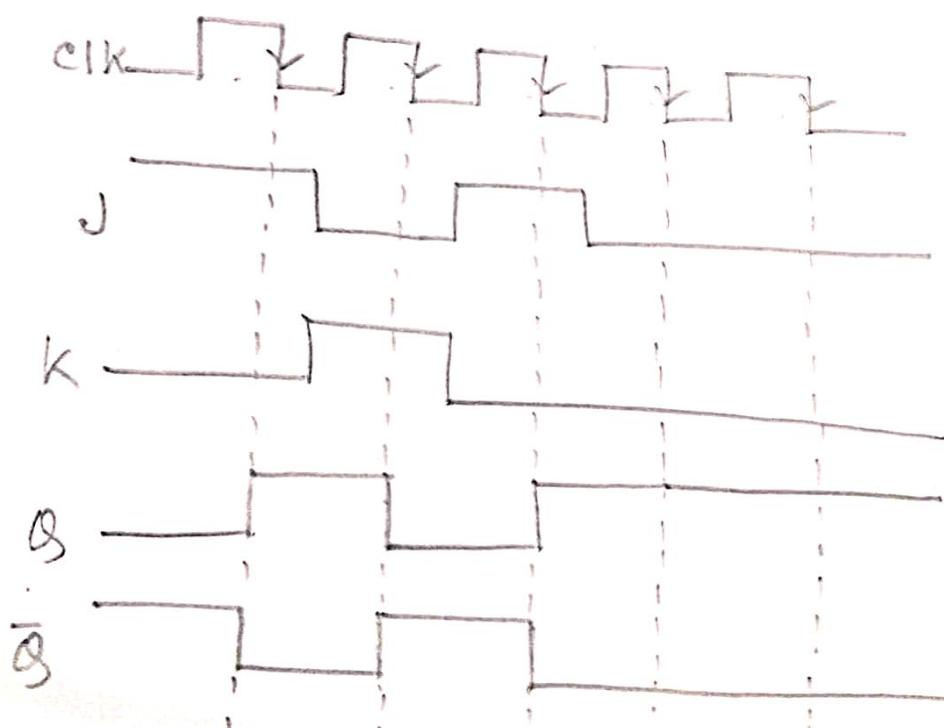
J	K	Q	Description
0	0	0	No change.
0	1	0	Reset
1	0	1	Set
1	1	0	Toggle

Case-1:

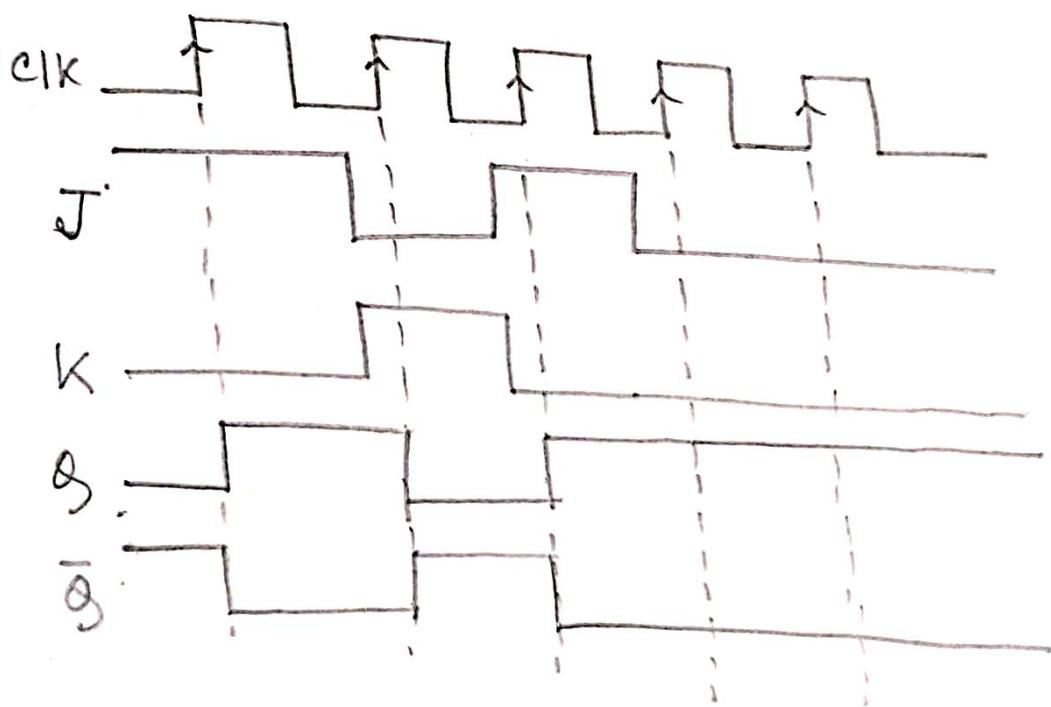
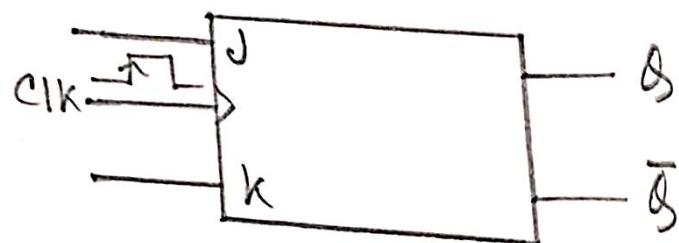
Negative edge triggering.



→ Initial state of each flip-flop is Reset(0).



## Case-2: Positive edge triggering.



The difference between the given two flip-flop is flip-flop-1 is negatively edge triggered whereas flip-flop-2 is positively edge triggered.

Negatively edge trigger  $\rightarrow$  output change their state when there is negative edge trigger at the clock pulse.

Positively edge trigger  $\rightarrow$  output change their state when there is positive edge at the clock pulse (shown in waveform)

11.

## Master slave SR flip-flop:

Master slave SR flip-flop is designed utilizing 2 SR flip-flop, in that each complementary flip-flop is connected to CLK pulse first flip-flop is the master flip-flop which works when the clock pulse is high state and at that time the slave flip-flop is in the hold state and if the clock pulse is in low state, the slave flip-flop works and the master slave flip-flop stays in the hold state.

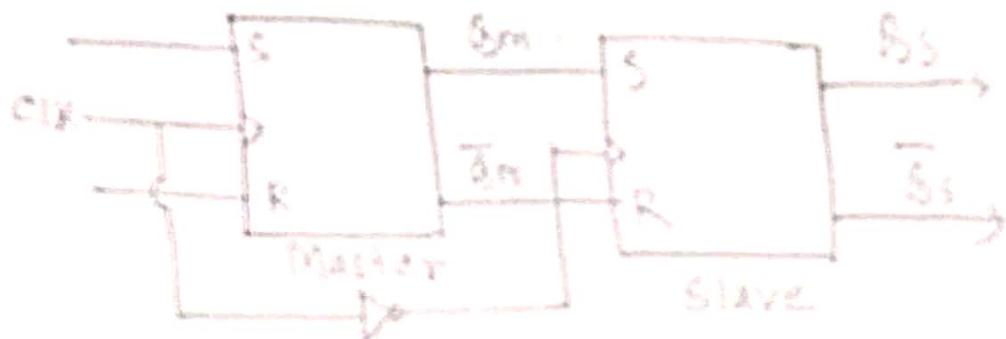
### Working :

1. When  $S=0, R=0$ , there will be no change in the output with or without CLK pulse.
2. When  $S=1, R=0$  and clock pulse is high,  $Q_m=1$  and  $\bar{Q}_m=0$  and when the clock pulse is in low state  $Q_s=1$  and  $\bar{Q}_s=0$
3. When  $S=0, R=1$  and clock pulse is in high state,  $Q_m=0$ , and  $\bar{Q}_m=1$  and when the negative edge of the clock pulse is arrives,

the master flip-flop is in off-state and slave flip-flop is in on-state. As a result

As a result,  $B_S = 0$ ,  $\bar{B}_S = 1$

4. When  $S=1, R=1$ , the output of SR master slave SR flip-flop is undefined



Pg: Jk master slave block circuit diagram

## Master slave JK flip-flop:

Master slave JK flip-flop is designed using 2 JK flip-flop in that each flip-flop is connected to CLK pulse complementary to each other and the first flip-flop is the master flip-flop which works when the clock pulse is high state and at that time the slave flip-flop is in the hold state and if the CLK pulse is in low state, then the slave flip-flop works and the master flip-flop stays in the hold state.

### Working :

The master slave JK flip-flop works as like the master slave SR flip-flop. But when  $J=1, K=1$ , Both master and slave flip-flop toggles when the clock pulse is in high state, the master flip-flop toggles and when the clock pulse is in low state, the slave flip-flop toggles.

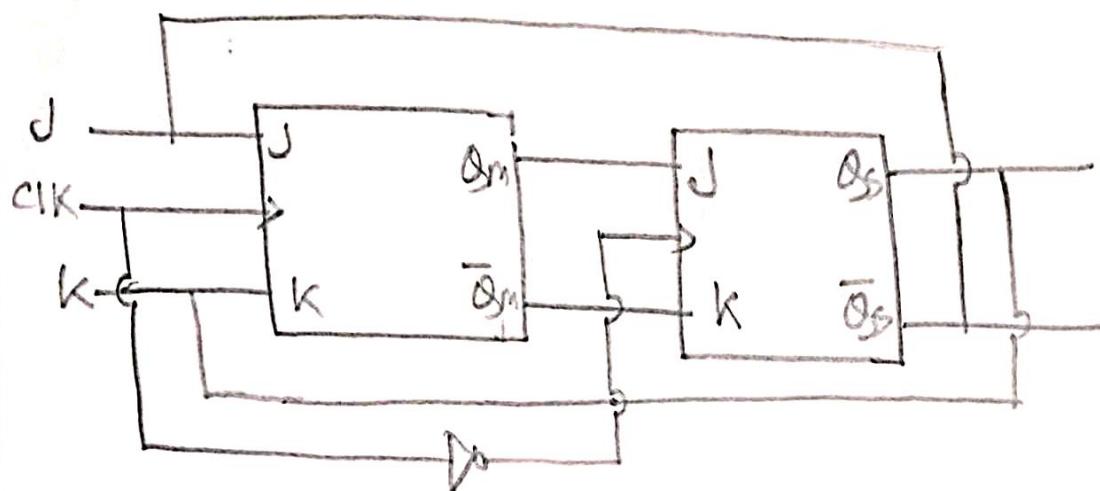


Fig: JK master slave block circuit diagram.

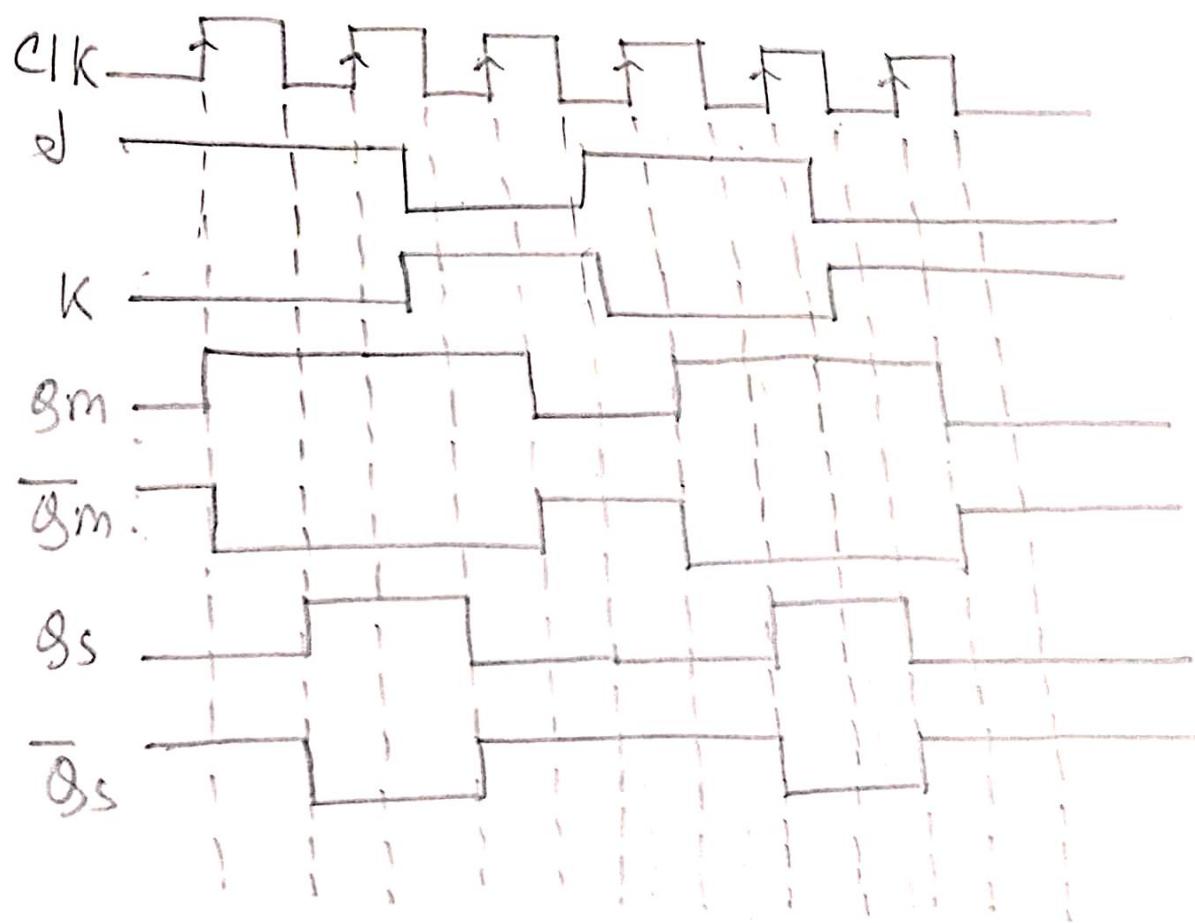


Fig: Timing diagram of master slave JK flip-flop.

12.

$$\text{Frequency, } f = \frac{1.44}{(R_A + 2R_B) \times C}$$

$$\text{2. } f = \frac{1.44}{(2 + 4.3 \times 2) \times 10^3 \times 0.1 \times 10^{-6}}$$

$$= 1.358 \text{ kHz}$$

Here,

$$R_1 = 2.0 \text{ k}\Omega$$

$$R_2 = 4.3 \text{ k}\Omega$$

$$C = 0.1 \mu\text{F}$$

$$T = 0.69 (R_A + 2R_B) \times C$$

13.

$$\begin{aligned} T &= \frac{1}{f} \\ &= \frac{1}{10 \times 10^3 \text{ Hz}} \\ &= 0.1 \text{ ms} \end{aligned}$$

Here

$$f = 10 \text{ kHz}$$

$$C = 0.004 \mu\text{F}$$

$$\text{Duty cycle} = 80\% = 0.8$$

$$\text{Duty cycle} = \frac{R_1 + R_2}{R_1 + 2R_2}$$

$$\Rightarrow 0.80 = \frac{R_1 + R_2}{R_1 + 2R_2}$$

$$\Rightarrow 0.80(R_1 + 2R_2) = (R_1 + R_2)$$

$$\Rightarrow 0.8R_1 + 1.6R_2 = R_1 + R_2$$

$$\Rightarrow 0.2R_1 = 0.6R_2$$

$$\Rightarrow R_1 = 3R_2$$

$$T = 0.693 (R_1 + 2R_2) \times C$$

$$\Rightarrow 0.1 \times 10^{-3} = 0.693 \times 5 \times R_2 \times 0.004 \times 10^{-3}$$

$$\Rightarrow R_2 = 7.215 \Omega$$

$$\therefore R_1 = 3R_2 = 3 \times 7.215 = 21.645 \Omega \quad \underline{\text{Ans}}$$

14.

$$\begin{aligned}P_L &= VI_L \\&= 5 \times 2 \times 10^{-3} \\&= 10 \text{ mWatt}\end{aligned}$$

$$\begin{aligned}P_H &= VI_H \\&= 5 \times (3.5 \text{ mA}) \\&= 5 \times 3.5 \times 10^{-3} \\&= 17.5 \text{ mWatt}\end{aligned}$$

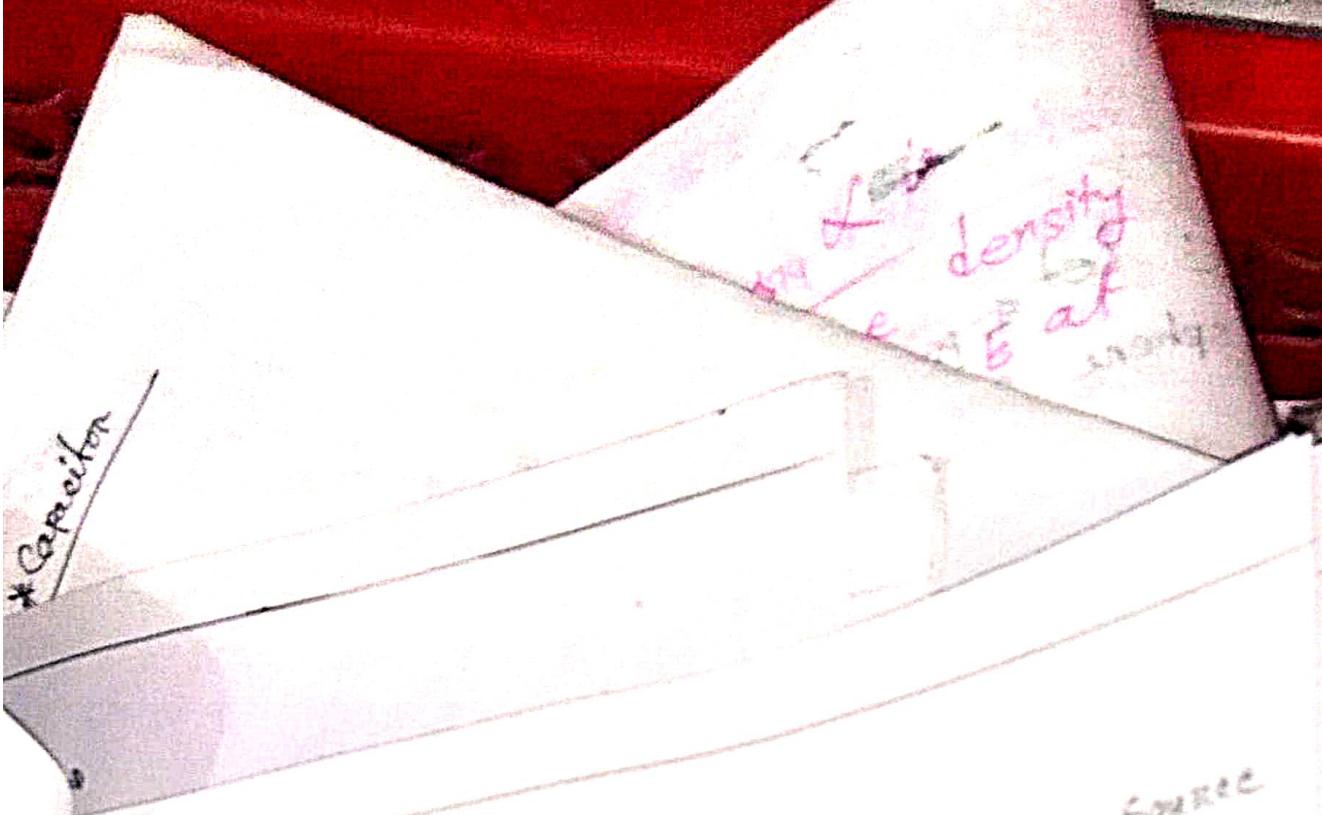
Here

$$\begin{aligned}V &= 5 \text{ V} \\I_L &= 2 \text{ mA} \\I_H &= 3.5 \text{ mA}\end{aligned}$$

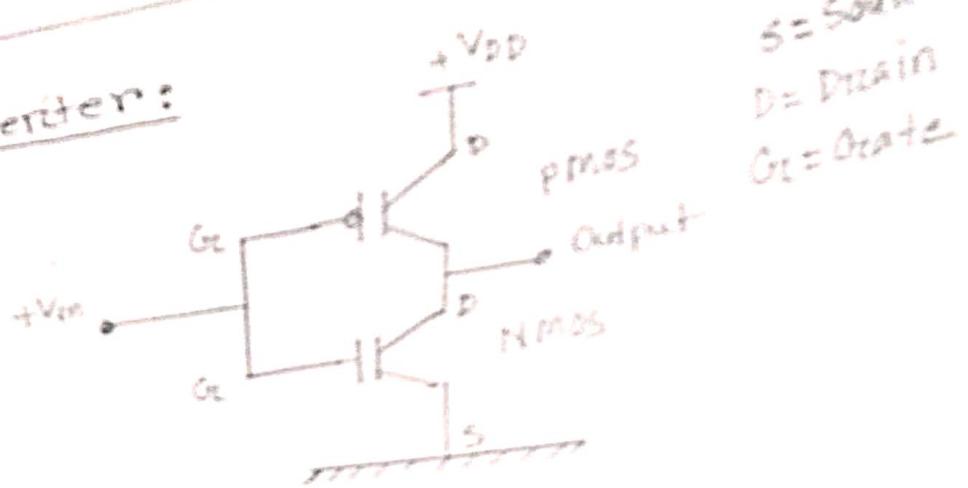
with 50% duty cycle

$$\begin{aligned}P_L &= (10 \times 0.5) \text{ mWatt} \\&= 5 \text{ mWatt}\end{aligned} \quad \begin{aligned}P_H &= (17.5 \times 0.5) \text{ mWatt} \\&= 8.75 \text{ mWatt}\end{aligned}$$

$$\begin{aligned}\text{Average power dissipation} &\equiv \frac{P_L + P_H}{2} \\&= \frac{5 + 8.75}{2} \\&= 6.875 \text{ mWatt}.\end{aligned}$$



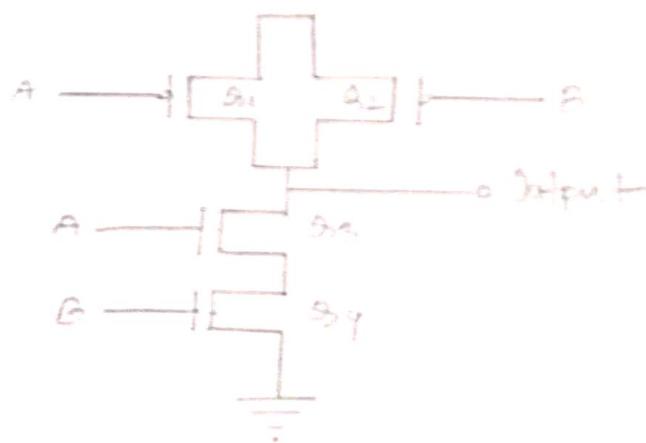
### 16: CMOS Inverter:



#### Operation :

When  $V_{in}$  is low, pMOS switch is on and nMOS switch is off. When  $V_{in}$  is HIGH, pMOS switch is off and nMOS switch is ON.

### CMOS NAND Gate:



PMOS = Parallel connection

NMOS = Series connection

CMOS NAND gate consists of two p-channel mosfets,  $Q_1$  and  $Q_2$  connected in parallel and two n-channel mosfets

$Q_3$  and  $Q_4$  connected in series.

A	B	$Q_1$	$Q_2$	$Q_3$	$Q_4$	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Operations: When both inputs A and B are logic 0,  $Q_1$  and  $Q_2$  transistor are "ON" and  $Q_3$  and  $Q_4$  transistor are "OFF". Producing a logic 1 output. This is consistent with the first row of the truth table.

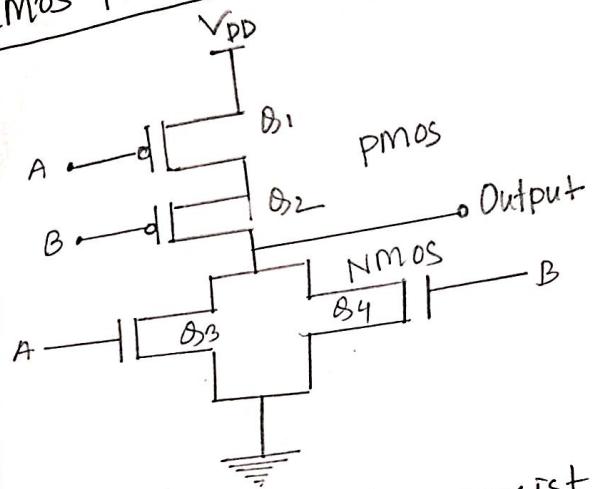
When one of the inputs is a logic "1" and the other one is logic "0", Then either  $Q_1$  is ON,  $Q_4$  is OFF or  $Q_2$  is "ON" and  $Q_3$  is "OFF". The output is both cases logic "1". Validating the second and the rows of the truth table.

With logic 1 input A and B,  $Q_3$  and  $Q_4$  transistors are "ON" and  $Q_1$  and  $Q_2$  transistors are off. producing a logic "0" output. This is consistent with the lowest row in the above truth table.

\*Capacitor

V<sub>DD</sub>

CMOS NOR gate:



Truth Table

A	B	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	B <sub>4</sub>	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

CMOS NOR gate consists of two P-channel  $B_1$  and  $B_2$  MOSFET connected in series and two n-channel  $B_3$  and  $B_4$  connected in parallel

Operation:

When both inputs A and B are logic "0",  $B_1$  and  $B_2$  are ON and  $B_3$  and  $B_4$  are OFF and the output is logic 1. This confirms the first row of the truth table above.

With both inputs logic "1",  $B_3$  and  $B_4$  are "ON" and  $B_1$  and  $B_2$  are "OFF", producing a logic 0 output that confirms the last row of the truth table.

For the two remaining input combinations, either  $B_1$  is "OFF" and  $B_3$  is ON or  $B_2$  is "OFF" and  $B_4$  is "ON". In these cases, the output is logic "0" which is consistent with the above truth table.

17. What is the resolution in volts of a 10 bit DAC whose F.S output is  $5V$ ?

Here,  $n=10$

$$\text{Resolution} = \frac{\text{Full scale output}}{2^n}$$
$$= \frac{5V}{2^{10}}$$
$$= 4.883 \times 10^{-3} = 4.883 \text{ mV}$$

Ans

18. How many bits are required for a DAC so that its F.S output is  $10mA$  and its resolution is less than  $4mA$ .

$$\text{Resolution, } K = \frac{\text{F.S.O}}{2^n}$$

$$\therefore K < 40$$
$$\Rightarrow \frac{10}{2^n} < 40$$
$$\Rightarrow \frac{2^n}{10} > \frac{1}{40}$$
$$\Rightarrow 2^n > 2^{-2}$$
$$\Rightarrow n > -2$$

19. The 8 bits of 10bit DAC to be connected are LSB(2) to MSB(10) because the full scale of the 10 bit DAC is 10 volt.

$$K_{10\text{bit}} = \frac{10V}{2^{10}} = 9.77 \text{ mV}$$

If we neglect MSB it would give Fullscale of F.S.O =  $K \times 2^8 = 9.77 \text{ mV} \times 2^8$   
 $\approx 2.50 \text{ V}$

Because the weight of MSB is higher than that of LSB. So if we reject the first 2 LSB it would lesser than the MSB's. Because these 2 bits LSB would causes  $(9.77 + 2 \times 9.77) = 29.31 \text{ mV}$  which much less to avoid.

~~20. F.S.O = 12V,  $K = 20 \text{ mV}$  or less~~

~~20. F.S.O = 12V  
 $K = 20 \text{ mV}$  or less  
 $K \leq 20 \text{ mV}$~~

$$\Rightarrow \frac{12}{2^n} \leq 20 \text{ mV} \quad \boxed{\frac{\text{F.S.O.}}{2^n} = K}$$

$$\Rightarrow 2^n \geq \frac{12}{20} \times 10^3$$

$$\Rightarrow \log 2^n \geq \log 600$$

$$\begin{aligned} &\Rightarrow n \geq \frac{\log 600}{\log 2} \\ &\Rightarrow n \geq 9.23 \\ &\Rightarrow n \geq 9 \end{aligned}$$

Ans

(21)

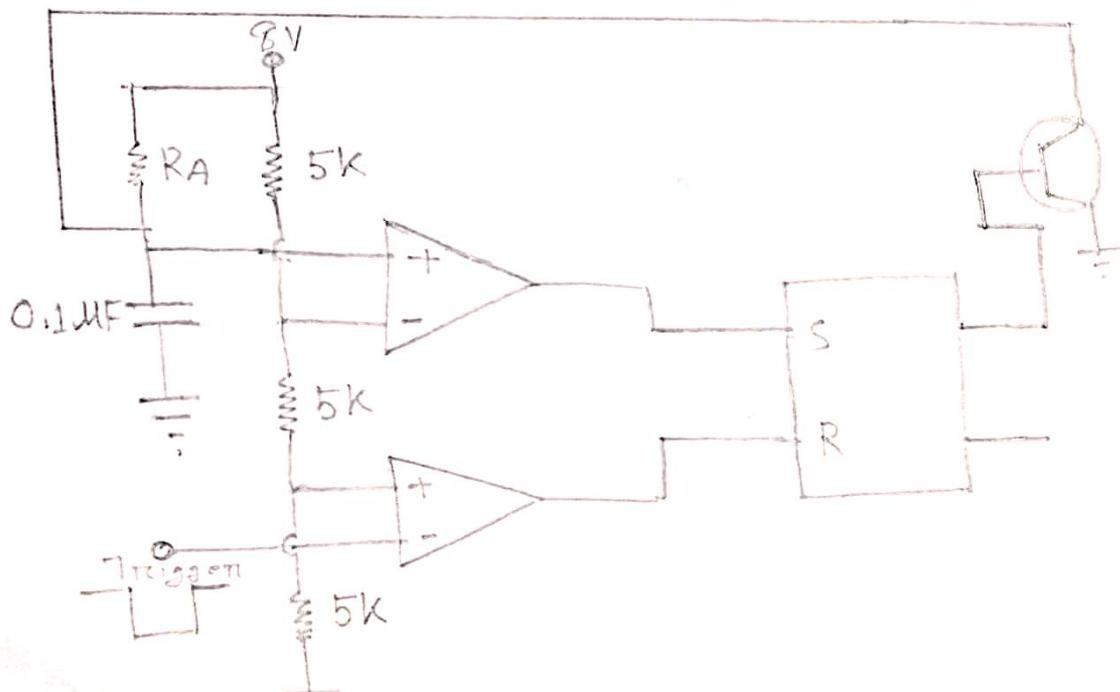
21. A certain eight-bit successive approximation converter has  $2.55V$  full-scale. The conversion time for  $V_A = 1V$  is  $80\text{ ms}$ . What will be the conversion for  $V_A = 1.5V$ ?

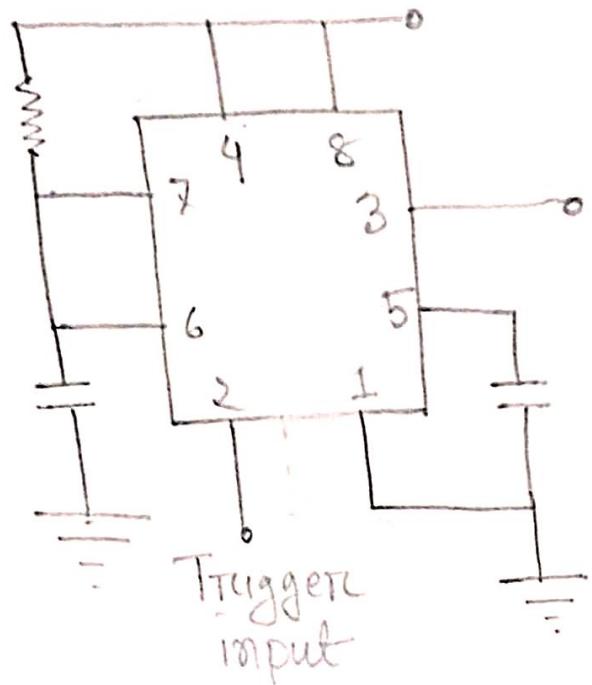
Solution:

Conversion time of successive approximation ADC depends upon the number of bits only and not on the value of analog input voltage. As the number of bits don't change and it is 8bit So the conversion time for  $1.5V$  don't change and remains  $80\text{ ms}$ .

22. Draw a monostable multivibrator circuit using 555 timer and discuss its operation.

Solution:





### Operation :

- (i) The monostable multivibrator will be in its stable state (output low) until it is triggered.
- (ii) When a negative trigger is applied to trigger pin of 555 timer, output of lower comparator will become high and output of upper comparator will be low. Since the comparator voltage is zero, this makes the output high.
- (iii) The discharge transistor turns off and the capacitor starts charges through resistor R to Vcc.
- (iv) After the negative trigger, output of lower comparator becomes low and that off upper comparator remains low. Since both inputs of the SR flip-flop are low, output will not change. So the output is HIGH.

(22)

(v) When the capacitor voltage will become greater than  $\frac{2}{3} V_{cc}$ , output of upper comparator becomes HIGH and that of lower comparator remains low, so the output becomes low.

(vi) This turns on the discharge transistor and the capacitor discharge.

(vii) The circuit remains in its stable state (output low) until next trigger occurs.

23.

Here, bits  $n = 8$

resolution,  $K = 40 \text{ mV}$

frequency clock =  $2.5 \text{ mHz}$

comparator  $V_T = 1 \text{ mV}$

Number of possible steps =  $2^n - 1$

$$= 2^8 - 1$$

$$= 255$$

$V_{max}$  must reach  $V_A + V_T$  or more before comparator goes low.

(a) Here  $V_A = 6 \text{ V}$

$$V_A + V_T = 6000 \text{ mV} + 1 \text{ mV} = 6001 \text{ mV}$$

$$\text{digital equivalent decimal output} = \frac{V_A + V_T}{K}$$
$$= \frac{6001 \text{ mV}}{40 \text{ mV}}$$

$$\text{digital output} = (10010110)_2 = 150.025 \approx 150$$

(2)

$$(b) V_A = 6.035 \text{ V}$$

$$V_A + V_T = 6.035 \times 10^3 + 1 \text{ mV} = 6036 \text{ mV}$$

digital equivalent decimal output,  
 $= \frac{V_A + V_T}{K} = \frac{6036 \text{ mV}}{40 \text{ mV}}$   
 $= 150.9 \approx 151$

$$\text{digital output} = (10010111)_2$$

(c) The maximum value and average conversion times for this ADC.

Maximum time is calculated for the maximum possible value of the analog input which is 10.2 V (F.S.O.). To convert this value to digital, the ADC needs  $255/2^8 = 1$  steps. The time is calculated using  $T = \frac{1}{f}$  which is the inverted value of the frequency to obtain the full scale output (F.S.O) voltage.

$$T_{\text{clock}} = \frac{1}{f} = \frac{1}{2.5 \text{ MHz}} = 0.4 \text{ } \mu\text{s}$$

$$T_{\text{max}} = T_{\text{clock}} \times \text{no of step} = 0.4 \text{ } \mu\text{s} \times 255$$

$$= 102 \text{ } \mu\text{s}$$

The average time is the mean time between fastest and slowest conversion.

Fastest conversion time = 0  $\mu\text{s}$

Slowest conversion time = 102  $\mu\text{s}$

$$\text{Average conversion time} = \frac{0 + 102}{2} = 51 \text{ } \mu\text{s}$$

24.

$$(01100100)_2 = (100)_10$$
$$(10110011)_2 = (179)_10$$

Output voltage  $\propto$  (decimal equivalent of input binary)

Let  $V_{02} = x$

$$\therefore \frac{x}{179} = \frac{2}{100}$$

$$\Rightarrow x = \frac{2 \times 179}{100} = 3.58 \text{ V (Ans)}$$

OR,

$$V_{01} = k \times \text{Signed No of input}$$

$$\Rightarrow k = \frac{2}{100} = 0.02 \text{ V}$$

$$V_{02} = k \times \text{Signed no of input}$$

$$= 0.02 \text{ V} \times 179 = 3.58 \text{ V (Ans)}$$