

Lab Report

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Dept: CSE

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course Title: Introduction to Digital Electronics
Lab

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1.

Name of the experiment:

Design and implement combinational logic circuit.

objective:

To investigate the properties of combinational logic circuits. as illustrated by X-OR gate. half adder full adder.

Theory: combinational logic circuit are interconnections of logic elements in which the output at any time reflects the condition of the input at that time. Combinational circuit do not retain information as do sequential circuits. And their outputs change with any input. one example of the combinational circuit is the binary adder.

Half Adder:

The half adder is the simpler of two types of adders. As it does not use a carry input from a previous stage. The input consists only of the two binary bits to be added. The output are the sum of the two bits and the carry if any. resulting from the addition. As there is no carry input, the half adder may be used only as the

as least significant adder of an array of adders.

Full adder: The full adder differs from the half adder in that it has an additional input for the carry-in term from a previous stage as shown in figure. The full adder requires two half adders and an OR-gate. The first half adder performs the addition of the input bits, while the second half adder sum the result of the addition and the carry input to produce the sum output. The OR gate produces the carry output. ~~the OR gate~~ from the carries of the two half adder.

Apparatus:

- i) Bread Board
- ii) Trainer Board
- iii) 5 V dc power supply.
- iv) 7408 - AND gate (2-inputs)
- v) 7486 - X-OR gate (2-inputs)

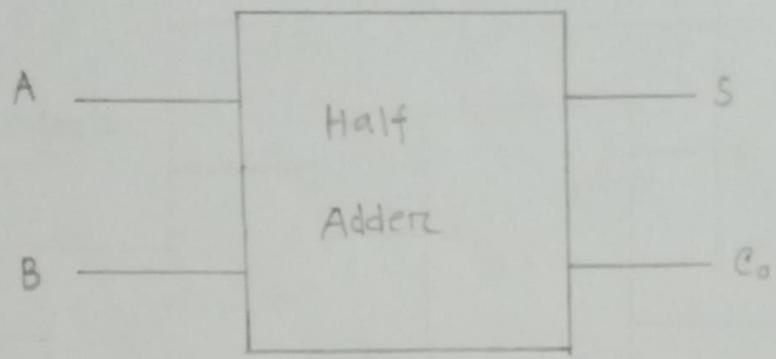


Fig : Box Diagram

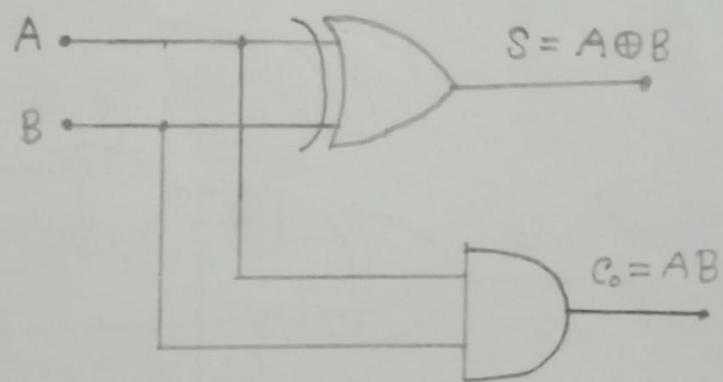


Fig: Half adder circuit diagram

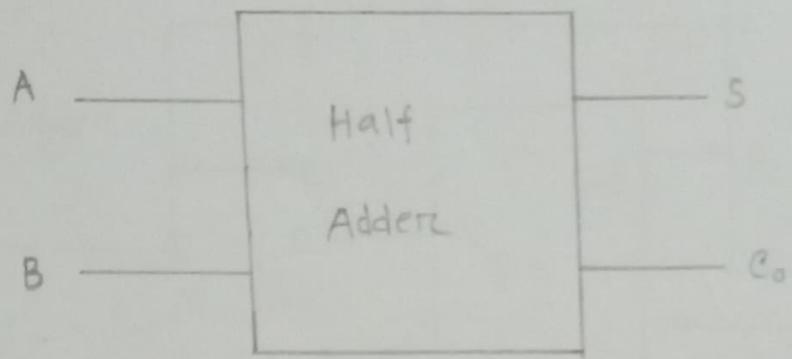


Fig : Box Diagram

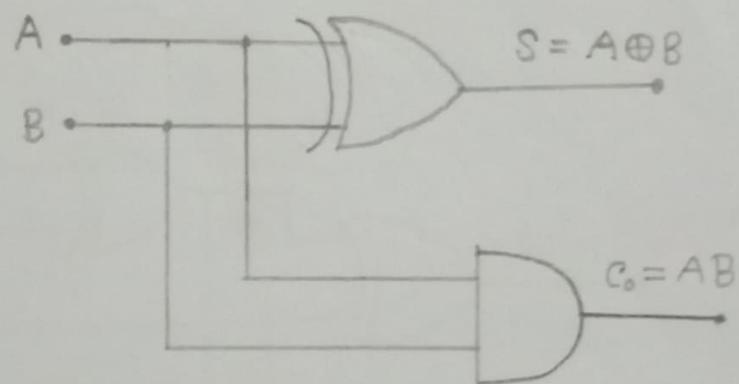
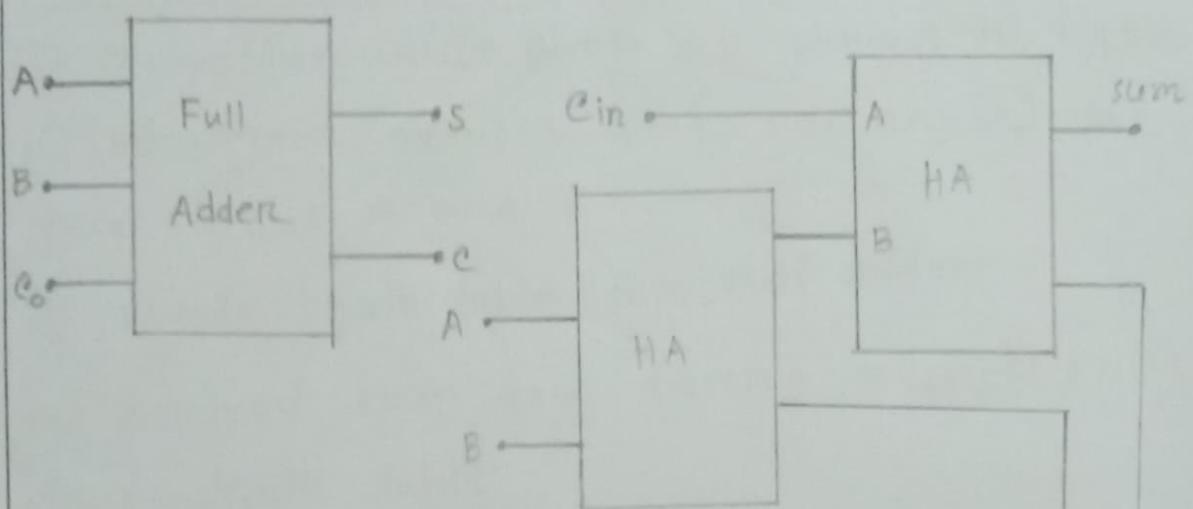
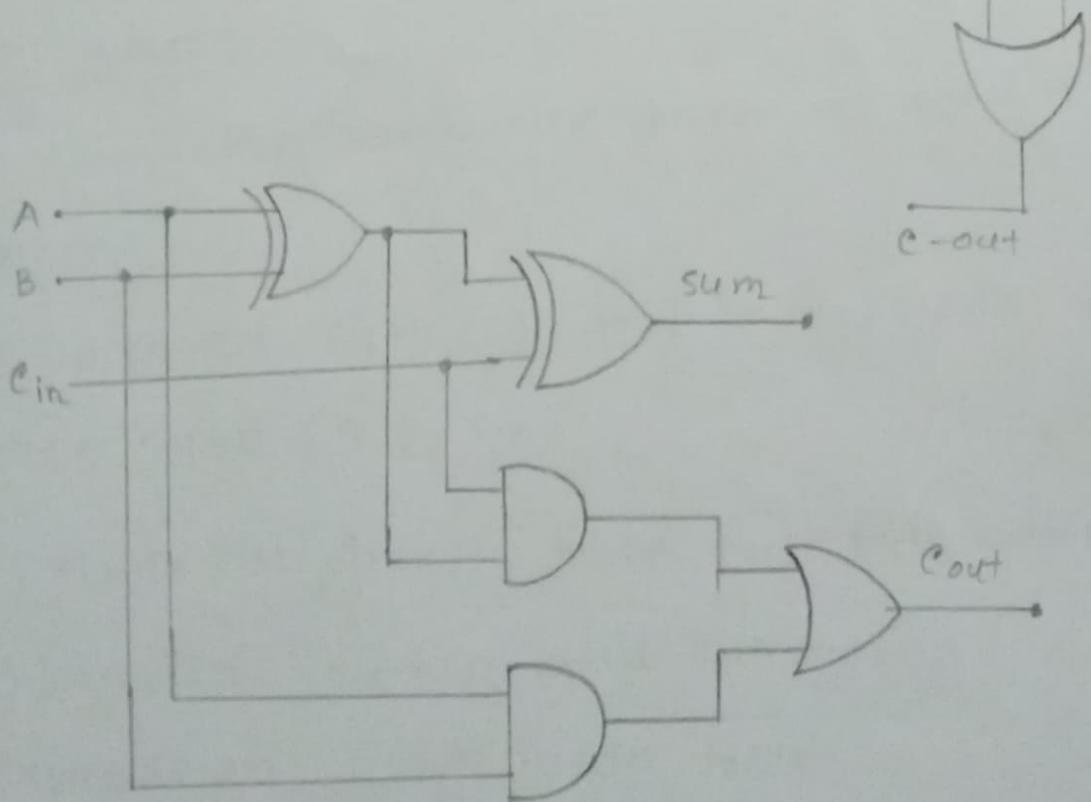


Fig: Half adder circuit diagram



Block diagram Full Adder



Full Adder circuit

Working Procedure: (Half Adder)

- i) connection will be given as shown in fig (b).
- ii) Determined sum(s) and carry(c_o) for two input A and B.
- iii) made truth table for half adder.
- iv) Derived sum and carry expression from truth table.

Full adder:

- i) connection will be given as shown in figure.
- ii) observed sum(s) and carry (c_o) for three input (A, B, e_{in}) .
- iii) made the truth table for full adder.
- iv) Derived sum(s) and carry (c_o) expression from truth table.

Result and discussion:

A	B	S	C _o
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table for half Adder

$$S = A \oplus B$$

$$S = \bar{A}B + A\bar{B} = A \oplus B$$

$$C = AB$$

A	B	C _{in}	S	C _o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
1	0	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\therefore S = \bar{A}\bar{B}C_{in} + A\bar{B}\bar{C}_{in} + A\bar{B}C_{in} + ABC = A \oplus B \oplus C_{in}$$

$$\therefore C_o = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

The sum and carry output expression are based on the truth table of both half adders and full adders. For half adder sum is the X-OR gate and carry is only And gate of two input. For full adder sum is three input X-OR gate and carry is the sum of cin and Cout.

Precaution:

- i) connection were given carefully.
- ii) ~~checked~~ checked the ie before starting the experiment.
- iii) power supply was turned off when there is need to change the circuit.

2.

■ Name of experiment: To design and implement SR flip-flop.

■ Objective: To learn about the operation of SR flip-flop.

■ Task:

- i) To design a circuit to observe the output of a SR flip-flop.
- ii) To implement the original designed circuit on the breadboard.
- iii) To observe the output.

■ Theory: SR- flip-flop is an edge triggered flip-flop. It is triggered by the positive going edge of the clock signal. This means that the FF can change state only when a signal applied to its clock input makes a transition from 0 to 1. The S and R input control the state of the FF in the same manner of a SR Latch. The figure of a SR flip-flop is given at the next page.

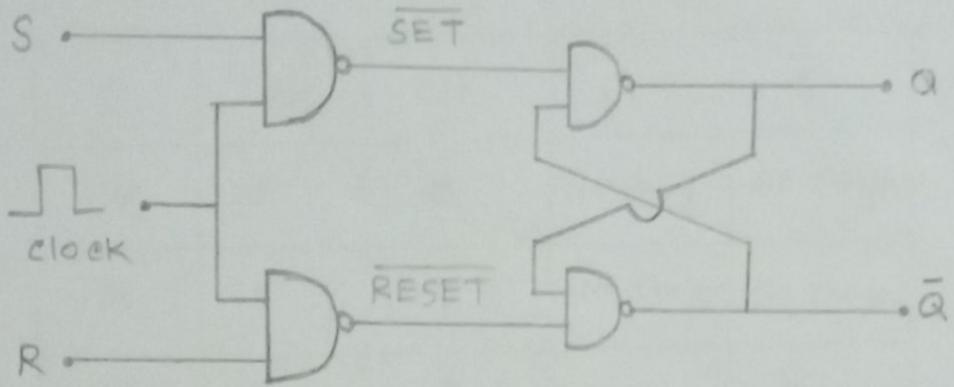


Figure: SR flip-flop

■ Equipment:

- i) Breadboard and wires
- ii) 7400 or 74LS00

■ working procedure:

- i) At first all the necessary equipment had been taken and made a circuit according to the circuit drawn figure.
- ii) Two LED's were connected to the SET and RESET output to observe the output.
- iii) SET and RESET inputs were connected to 5V voltage supply through switch.

Truth Table:

S	R	CLK	Q	\bar{Q}
0	0	0	No change	No change
0	0	↑	No change	No change
1	0	↑	1	0
0	1	↑	0	1
1	1	↑	1*	1*

Result and Discussion:- Initially there was no clock pulse and the output was remained same. When there was a clock pulse, output change their state according to SR control input. But, when SET and RESET input both are HIGH, the both output were HIGH. As we know, outputs are complement to each other. It's an invalid state

Precaution:

- 1) The NAND IC was placed properly on the breadboard.

- ii) Connections were made carefully.
- iii) Supply voltage was 5V for safety.
- iv) Power supply was turned OFF whenever there was a need to make a circuit change.

3.

Name of experiment: To design and implement JK flip-flop.

Objective: To learn about the operation of JK flip-flop.

Task:

- i) To design a circuit to observe the output of a JK flip-flop.
- ii) To implement the designed circuit on the breadboard.
- iii) To observe the output.

Theory: JK flip flop is triggered by the positive going edge of the clock signal. The J and K input control the state of the state of the FF in the same ways as the S and R

inputs for the clocked SR flip-flop except for one major difference: the $J=K=1$ condition does not result in an ambiguous output. For this J,K condition, the FF will always go to its opposite state upon the PGT of the clock signal. This is called the toggle mode of operation. In this mode, if both J and K are left HIGH the FF will change state (toggle) for each PGT of the clock.

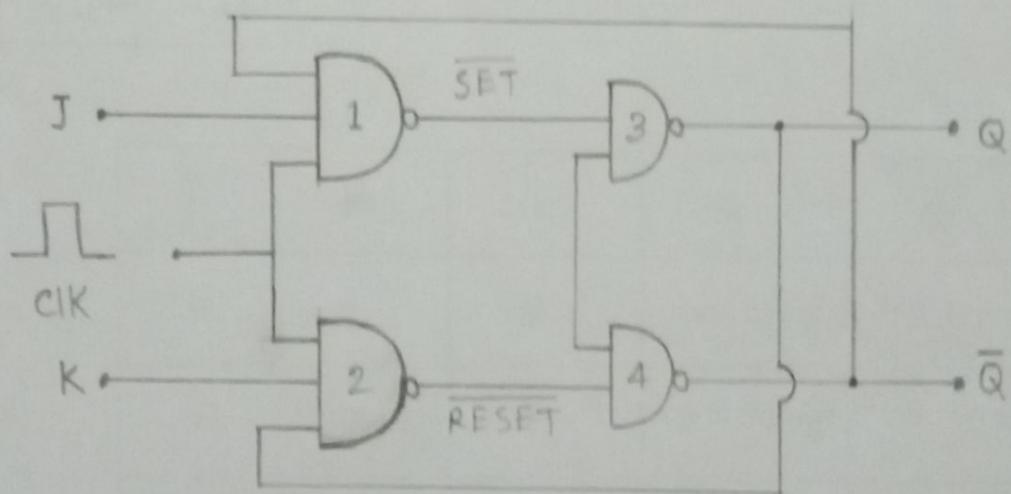


Figure: JK flip-flop

Equipment:

- i) Breadboard and wires.
- ii) 7410 or 74LS10 and 7400 or 74LS00 IC.
- iii) LED(s).
- iv) Resistors.

Working procedure:

- i) At first all necessary equipment had been taken and made a circuit according to the circuit drawn above.
- ii) 5v supply was given to J and K through switch.
- iii) RESET and SET output was connected to the LED's to observe the output.
- iv) The SET and RESET was given back to three input NAND gate as one of the input.

Truth Table:

J	K	Clk	Q	\bar{Q}
0	0	0	No change	No change
0	0	\uparrow	No change	No change
0	1	\uparrow	0	1
1	0	\uparrow	1	0
1	1	\uparrow	0	1

Result and Discussion:

Initially there was no clock pulse and output remained same, when the clock pulse is applied, output was changed according to input. When J and K are both were HIGH, the output was reversed from the previous state. This shows the toggle mode of JK FF.

Precaution:

- i) The 74LS10 IC was placed properly on the breadboard.
- ii) Connection were made carefully.
- iii) Power supply was turned off whenever there was a need to make a circuit change.

4.

Name of experiment: To design and implement T flip-flop.

Observe: To learn about the operation of T (toggle) flip-flop.

Task:

- i) To design a circuit for T flip-flop.

ii) To implement the designed circuit on the breadboard.

iii) To observe the output.

Theory: T flip-flop is a single input version of JK flip-flop, in which the input J and K are connected together and is provided as a single input labeled as T. When the clock is absent, the flip-flop is disabled as usual and previous output is maintained at output. When the clock is present and $T=0$, even though flip-flop is enabled the output does not switch its state. When $T=1$ during $Clk=1$, it causes $J=K=1$ and as earlier discussed it will toggle the output state.

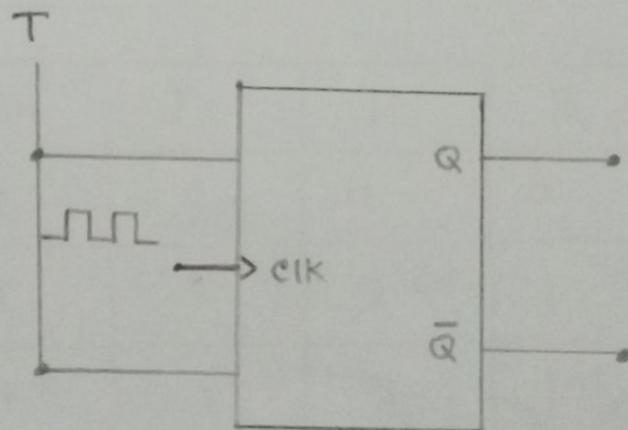


Figure: T flip-flop

Equipment:

- i) Breadboard and wires.
- ii) 7410 or 74LS10 and 7400 or 74LS00 IC.
- iii) LED's (2)
- iv) Resistors

Working procedure:

- i) At first all the necessary equipment had been taken and a circuit was made for T flip-flop.
- ii) 5v supply was connected to the T input through switch.
- iii) The SET and RESET output was connected to the LEDs.

Truth-Table:

Clk	T	J	K	Q	\bar{Q}
↑	0	0	0	No change	No change
↑	1	1	1	0	1
↑	1	1	1	1	0
↑	1	1	1	0	1

Result and Discussion: When there was no clock pulse, output remained unchanged. When there was a clock, but $T=0$, output still remain same. When $T=1$, both J and K is HIGH, it drives the output to toggle. This toggle continues until the clock pulse stop.

Precaution:

- i) The NAND IC was placed properly on the breadboard.
- ii) Connection were given carefully.
- iii) 5V power supply was given for safety.
- iv) Power supply was turned OFF whenever there was a need to make a circuit change.

5.

Name of Experiment: To design and implement of Astable multivibrator using 555 timer.

Objective:

- i) To learn to use the oscilloscope for troubleshooting digital circuit.
- ii) To learn the function generator as a source of digital signals.

Task:

- i) To design a circuit using 555 timer to study astable multivibrator.
- ii) To implement the designed circuit on the breadboard.
- iii) To observe the output signal,

Theory: Astable multivibrator operates as a free running oscillator. Its output is a repetitive rectangular waveform that switch between two logic level. The heart of the 555 timer is made up of two voltage comparators are device that produce a HIGH output ~~between~~ whenever the voltage on the + input is greater than the voltage on the - input. The external capacitor ~~c~~ charge up until its voltage

exceed $\frac{2}{3} V_{cc}$ as determined by the upper voltage comparator monitoring V_{t+} when this comparator's output goes high, it resets the SR Latch, causing the output pin(3) to go low. At the same time, \bar{Q} goes HIGH, closing the discharge switch and causing the capacitor to begin to discharge through R_B . It will continue to discharge until the capacitor voltage drops between $\frac{1}{3} V_{cc}$, as determined by the lower voltage comparator monitoring V_{t-} . When this comparator's output goes high, it sets the SR Latch, causing the output pin(3) to go HIGH, opening the discharge switch, and allowing the capacitor to start charging again as the cycle repeats. The figure is given at the next page.

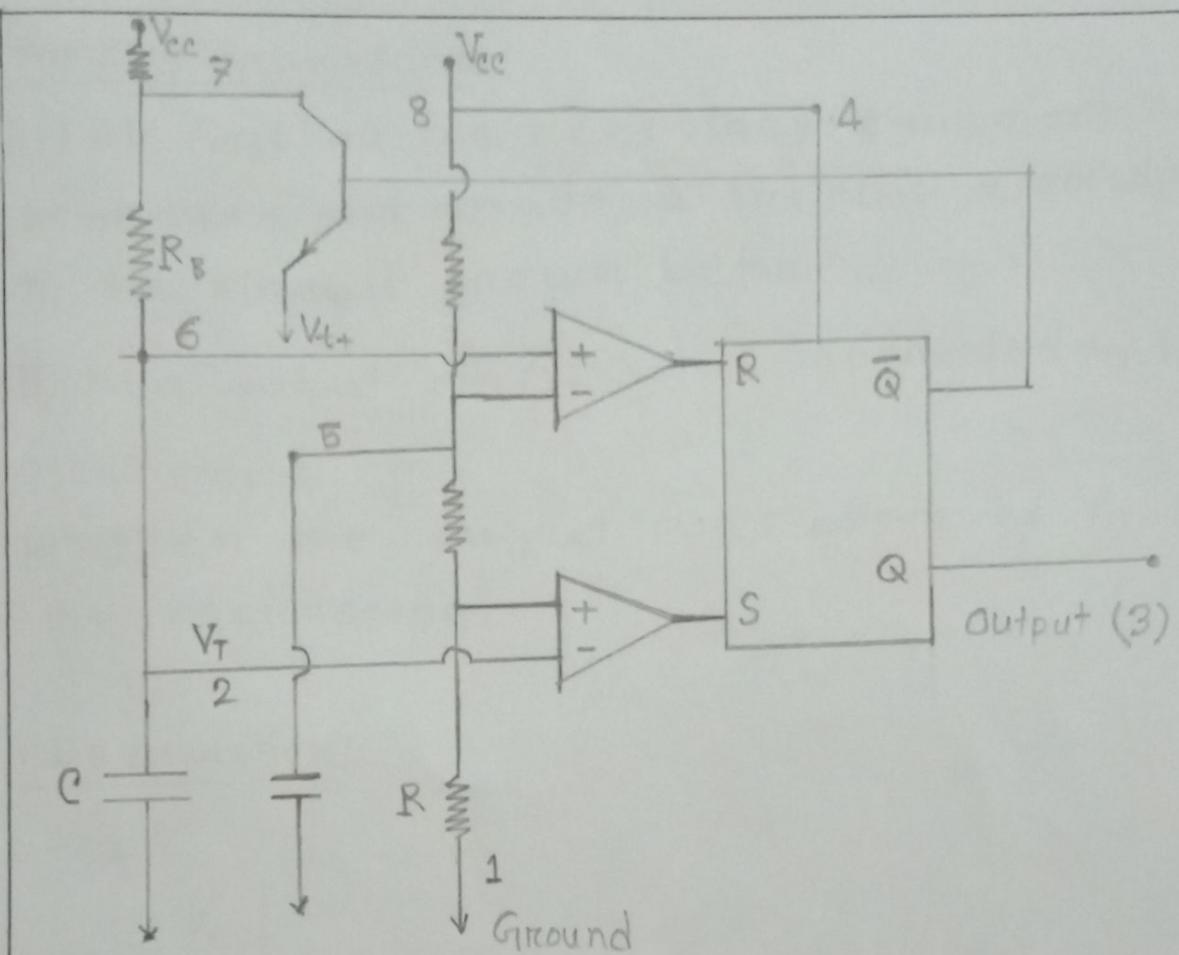


Figure: Astable multivibrator using 555 timer.

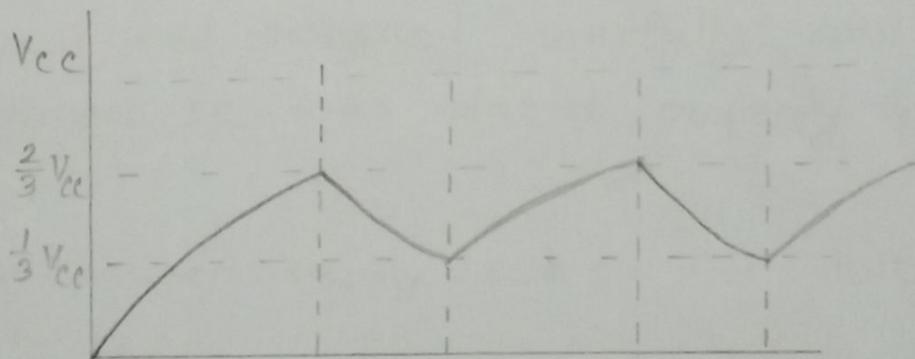
Equipment:

- i) Oscilloscope
- ii) Breadboard and wire
- iii) 555 timer
- iv) Resistors
- v) Capacitors

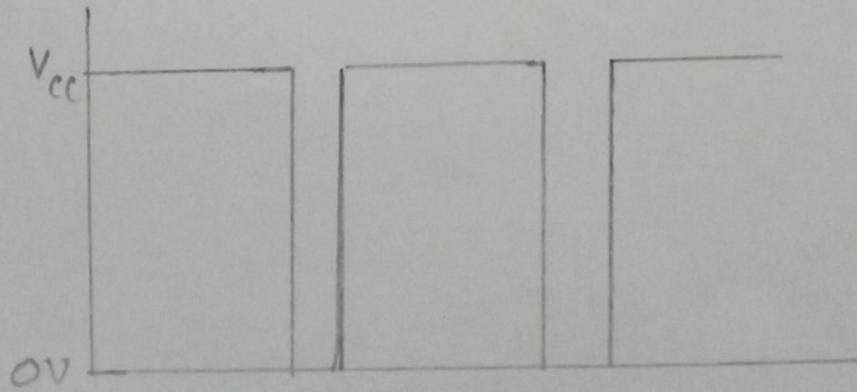
Working procedure:

- i) At first all the necessary equipment had been taken and made a circuit according to the circuit drawn before.
- ii) The output pin (3) was connected to the oscilloscope.
- iii) Then the output was observed from the oscilloscope.

Observation:



Analog output



Digital output

Result and Discussion: when the power supply switch was closed the output was HIGH at the oscilloscope. But after some time the output goes low. And Again after certain amount of time the output was HIGH. This continued until the power is on. Hence the both HIGH and Low state are unstable, it's a astable multivibrator. If we apply $R_B \gg R_A$, the duty cycle will be closed to 50% (i.e., $t_L \approx t_H$).

Precaution:

- i) circuit was designed carefully and the 555 timer IC was placed properly on the board.
- ii) The power supply was 5V for safety.
- iii) Power supply was turned OFF whenever there was a need to make a circuit change.

6.

Name of experiment: To design and implement of Monostable multivibrator using 555 timer.

Objective:

- i) To learn to use the oscilloscope for troubleshooting digital circuits.
- ii) To learn to use the function generators as a source of digital signal.

Task:

- i) To design a circuit using 555 timer to study monostable multivibrator.
- ii) To implement the designed circuit on the breadboard.
- iii) To observe the input and output signal.

Theory: The monostable multivibrator is also called 'one-shot' pulse generator. The sequence of event starts when a negative going trigger pulse is applied to the trigger comparator. When this trigger comparator sense the short

negative going trigger pulse to be just below the reference voltage ($\frac{1}{3}V_{cc}$), the device triggers and the output goes ~~fl~~ HIGH. The HIGH o/p pulse ends when the charge of the capacitor reaches $\frac{2}{3}V_{cc}$

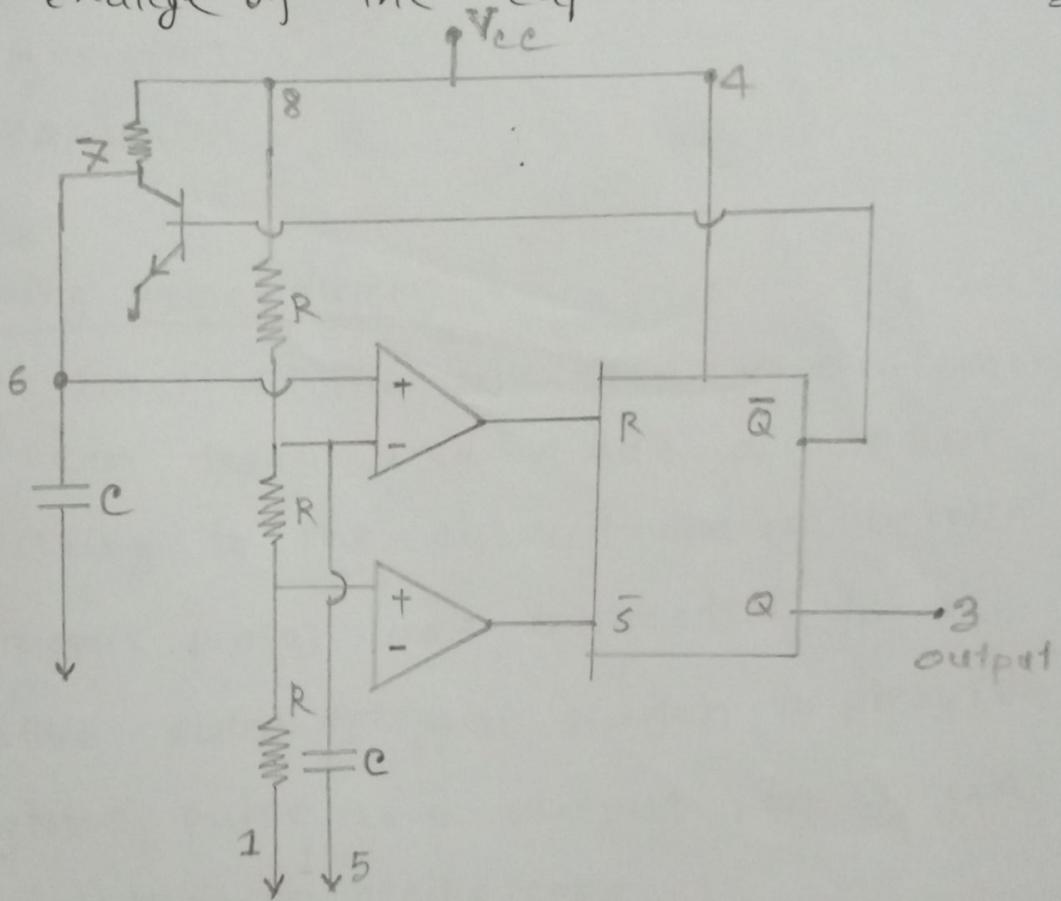


Figure: Monostable multivibrator using 555 timer

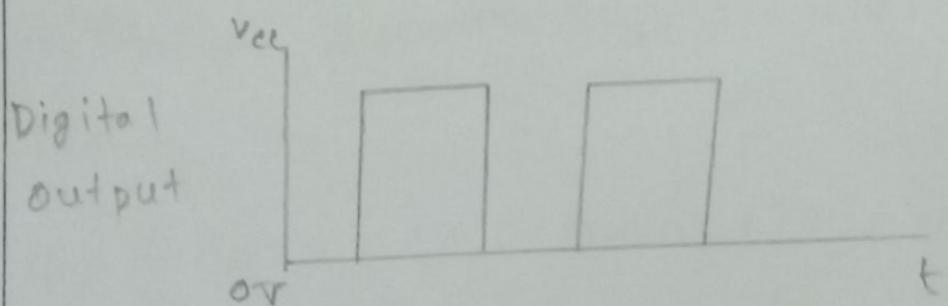
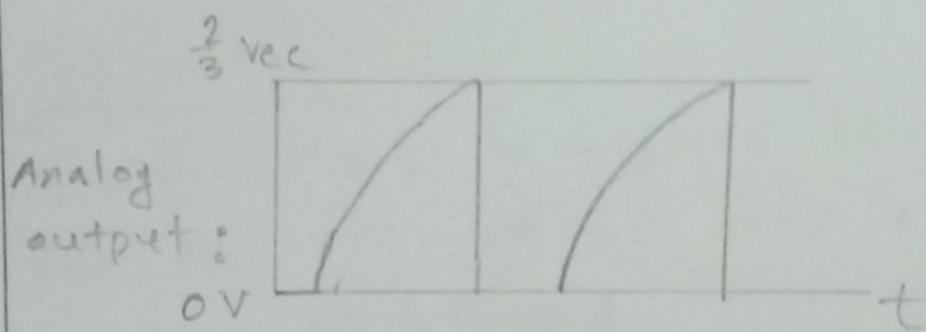
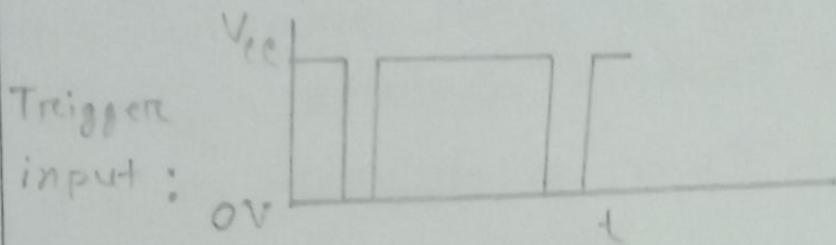
Equipment:

- i) Oscilloscope
- ii) Function generator with analog and digital outputs.
- iii) Breadboard and wires.
- iv) 555 timer
- v) Resistors
- vi) Capacitor

Working procedure:

- i) At first all the necessary equipment had been taken and made a circuit according to the circuit drawn before.
- ii) Trigger pin(2) was connected to a negative pulse trigger switch to provide negative pulse and output pin (3) was connected to oscilloscope.
- iii) Then the output signal was observed several times when the switch was pressed.

Observation:



Result and discussion: Initially the output was at Low (stable state). When the trigger pulse switch was pressed, the output goes High (unstable state). After a certain amount of time the output returned to Low (stable state).

This observation indicates that

The circuit has one stable and one unstable state. The unstable state disappears after a certain amount of time. Hence it's a monostable multivibrator.

Precautions:

- i) Circuit was designed carefully and the 555 timer IC was placed properly on the breadboard.
- ii) The power supply was 5V for safety.
- iii) Power was turned OFF whenever there was a need to make a circuit change.