ANDREAS PRODROMOU

10545 Ponder Way
San Diego, CA, 92126

prodromou.andreas@gmail.com
tel: (858) 263-5813

Research Interests

- Heterogeneous and heterogeneous-ISA computer architectures
- Heterogeneous memory architectures and emerging memory technologies
- Applications of Machine Learning algorithms in computer architecture

---

Education

University of California, San Diego, San Diego, CA
Ph.D. Student in Computer Science and Engineering
September 2013 – Present
Advisor: Dr. Dean Tullsen
GPA: 3.6/4
Powell Fellow (2013-2016)

University of Cyprus, Nicosia, Cyprus
Master of Science in Computer Engineering, June 2013
Advisor: Dr. Chrysostomos Nicopoulos
Co-Advisor: Dr. Yiannakis Sazeides
GPA: 8.57/10

University of Cyprus, Nicosia, Cyprus
Bachelor of Science in Computer Engineering, June 2011
Advisor: Dr. Chrysostomos Nicopoulos
GPA: 7.81/10

Research Experience

Graduate Student Researcher, June 2013 – Present
Department of Computer Science and Engineering, UCSD, San Diego, CA

- **Dynamic memory management for Heterogeneous Memory Architectures.**

  - Exploited a "Majority Element Algorithm", originally proposed for big data analytics, to achieve greater prediction accuracy on future memory accesses.
  - Combined MEA algorithm with a "Divide-and-Conquer" hardware mechanism for more efficient and scalable memory management than state-of-the-art proposals.
  - Work published in HPCA'17 conference.
- **Machine-Learning-based scheduling for heterogeneous(-ISA) architectures**
  - Trained and evaluated thousands of different ML models over large collection of data collected via simulations (43200 cycle-accurate simulations - 72 workloads on 600 different cores). These models were trained to predict dynamic performance given an application and core characterization.
  - Developed techniques to reverse-engineer trained ML models and understand how important each input feature is towards the prediction goal. Insights were later used to minimize amount of on-chip counters necessary and overall reduce overheads.
  - Proposed a "scheduler efficiency" metric to bridge the gap between ML metrics and system performance.
  - Proposed a "system scheduling difficulty" metric that quantifies how hard scheduling is for a given collection of cores in a processor. We find that scheduling difficulty is a reasonable architectural trade-off.

Co-op Intern, June 2018 – Sept. 2018
NVidia, Santa Clara, California

- Competition analysis and projections team
  - In-depth characterization of the training phase of various neural network architectures. Compared NVidia's products (GPUs) against competitora products (othe GPUs, as well as various accelerators such as Google's TPU.)

Co-op Intern, June 2016 – Sept. 2016
Advanced Micro Devices (AMD), Austin, Texas

- Implementation of a statistical memory simulator.
  - Implemented a tool capable of extrapolating the behavior of large memories after simulating tiny memories.

Co-op Intern, June 2015 – Sept. 2015
Advanced Micro Devices (AMD), Austin, Texas

- Research in dynamic memory management in hybrid configurations.
  - Developed dynamic memory management mechanism focusing mainly on scalability to very large memory capacities.

– Utilizing a "Majority Element Algorithm" heuristic for extremely efficient activity tracking

Special Scientist, June 2011 – June 2013
Department of Electrical and Computer Engineering, University of Cyprus, Nicosia, Cyprus
Ξ Lab (https://www2.cs.ucy.ac.cy/carch/xi/)

- Part of Eurocloud FP7 Project (http://www.eurocloudserver.com/) – European research and development program for building a 3D server-on-chip concept integrating low power cores.
- Research in Network-on-Chip Reliability.
- Designed and evaluated circuit-level modules to detect hardware faults. (Published in MICRO'45 conference)

Special Scientist, June 2010 – August 2010
Department of Electrical and Computer Engineering, University of Cyprus, Nicosia, Cyprus
multiCAL (multicore Computer Architecture Laboratory) (`www.multical.ece.ucy.ac.cy`)

- Implementation of a parameterized cycle-accurate Network-on-Chip simulator as part of a Full-System simulator (extensive programming and simulations)
- Later awarded as Best Senior Design Project

Undergraduate Research Intern, June 2009 – August 2009
Department of Electrical and Computer Engineering, University of Cyprus, Nicosia, Cyprus
KIOS Research Center (`www.kios.ucy.ac.cy`)

- Studied the infrastructure of a Network-on-Chip module
- Implemented and assessed (simulations) routing algorithms for such networks

---

Skills

Operating Systems
Extensive knowledge of Windows, Linux and Mac OS

Programming/Scripting Languages
Excellent knowledge of C, C++
Excellent knowledge of scripting languages (Perl, Python and Bash)
Good knowledge of MATLAB programming environment
Familiarized with Verilog HDL, Javascript and ActionScript

CAD Software
Synopsis Design Compiler
Autodesk AutoCAD

Languages

Greek	Native speaker
English	Verbal and written fluency at an advanced level

Professional Activities

Military Service, *Greek Cypriot National Guard*, June 2005 – July 2007
Reserve Officer in the Telecommunications Division of the Cyprus Military

- Attended a military academy for reserve officers in Athens, Greece, specializing in military telecommunications, June 2005 – Sept 2005
- Served a 25-month military service as an officer
- Currently a reserve officer ranked as Second Lieutenant

– Webchair for the Design For Reliability (DFR) workshop, held in conjunction with *The 8th International Conference on High Performance and Embedded Architectures and Compiles* (HiPEAC), 2013.

– Assisted in reviewing manuscripts for conferences such as:

- ACM Computing Surveys Journal, 2012
- DATE 2013
- MICRO 2011, 2012

– IEEE Student Member 2010 – Present

Recognition

2013	Powell Fellowship for academic years 2013–2016, UCSD Computer Science and Engineering.
2011	Best Senior Design Project award in the Department of Electrical and Computer Engineering, University of Cyprus for academic year 2010-2011.
2008	Award for excellent performance from the Department of Electrical and Computer Engineering of University of Cyprus for the academic year 2007-2008.

Publications

2018 M. Gupta, V. Sridharan, D. Roberts, **Prodromou, Andreas**, A. Venkat, D.. Tullsen, M., and R. Gupta. Reliability-aware data placement for heterogeneous memory architectures. In *2018 IEEE International Symposium on High Performance Computer Architecture (HPCA)*, Feb 2018

2017 **Prodromou, A.**, M. Meswani, N. Jayasena, G. Loh, and D. Tullsen. Mempod: A clustered architecture for efficient and scalable migration in flat address space multi-level memories. In *2017 IEEE International Symposium on High Performance Computer Architecture (HPCA)*, Feb 2017

J. H. Ryoo, M. Meswani, **Prodromou, Andreas**, and Lizy John, K. Silcfm: Subblocked interleaved cache-like flat memory organization. In *2017 IEEE International Symposium on High Performance Computer Architecture (HPCA)*, Feb 2017

2016 Kypros Chrysanthou, Panayiotis Englezakis, **Andreas Prodromou**, Andreas Panteli, Chrysostomos Nicopoulos, Yiannakis Sazeides, and Giorgos Dimitrakopoulos. An online and real-time fault detection and localization mechanism for network-on-chip architectures. *ACM Trans. Archit. Code Optim.*

2012 **Prodromou, A.**, A. Panteli, C. Nicopoulos, and Y. Sazeides. Nocalert: An on-line and real-time fault detection mechanism for network-on-chip architectures. In *Microarchitecture (MICRO), 2012 45th Annual IEEE/ACM International Symposium on*, Dec 2012

2011 D. Milojevic, S. Idgunji, D. Jevdjic, E. Ozer, P. Lotfi-Kamran, A. Panteli, **Prodromou, A.**, C. Nicopoulos, D. Hardy, B. Falsari, and Y. Sazeides. Thermal characterization of cloud workloads on a power-efficient server-on-chip. In *Computer Design (ICCD), 2012 IEEE 30th International Conference on*, Sept 2012

Patents

2016 **(Pending) Prodromou A.**, M. Meswani, A. Basu, N. Jayasena, and G. Loh. Cluster-based migration in a multi-level memory hierarchy, 2016

Theses

2013 A. Prodromou. Detection and localization of transient, permanent and intermittent faults in network-on-chip routers via invariance checking. M.Sc. Thesis (Advisor: C. Nicopoulos), June 2013

2011 A. Prodromou. Interconnx: A cycle-accurate network-on-chip (noc) simulator with a graphical user interface (gui). Undergraduate Thesis (Advisor: C. Nicopoulos), June 2011