ANDREAS PRODROMOU

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EDUCATION

Ph.D., Computer Science **June 2013 – Present**
Department of Computer Science and Engineering
University of California, San Diego

M.Sc., Computer Engineering **2011 – 2013**
Department of Electrical and Computer Engineering
University of Cyprus

B.Sc., Computer Engineering **2007 – 2011**
Department of Electrical and Computer Engineering
University of Cyprus

EXPERIENCE

Advanced Micro Devices (AMD) June 2015 – Sept. 2015
Co-op Intern *Austin, TX*

· Implemented a dynamic memory management mechanism for hybrid memory configurations.
· Focused mainly on the mechanism's scalability to very large memory capacities.
· Utilized novel algorithms and clustered micro-architecture to maintain scalability.
· Implemented from scratch in cycle-accurate simulator and compared against state-of-the-art proposals.

University of California San Diego, CSE Department August 2013 – Present
Graduate Student Researcher *San Diego, CA*

· Exploring the capabilities of dynamic dead code elimination.
· Evaluating memory controller scheduling policies under emerging technological trends.

University of Cyprus, CS Department June 2011 – June 2013
Special Scientist *Nicosia, Cyprus*

· Part of Eurocloud FP7 Project (http://www.eurocloudserver.com/) – European research and development program for building a 3D server-on-chip concept integrating low power cores.
· Research in Network-on-Chip Reliability.
· Designed and evaluated circuit-level modules to detect hardware faults. (Published in MICRO'45 conference)
· Participated in assessing the impact design changes have at the datacenter level.

University of Cyprus, ECE Department June 2010 – September 2010
Special Scientist *Nicosia, Cyprus*

· Implementation of a parameterized cycle-accurate Network-on-Chip simulator as part of a Full-System simulator (extensive programming and simulations)
· Later awarded as Best Senior Design Project

KIOS Research Center for Intelligent Systems & Networks June 2009 – September 2009
Undergraduate Research Scientist *Nicosia, Cyprus*

· Studied the infrastructure of a Network-on-Chip module
· Implemented and assessed routing algorithms for such networks

RESEARCH INTERESTS

Memory scheduling policies, dynamic dead code elimination, multicore architectures, 3D microprocessor design, Network-on-Chip architectures.

SKILLS

Programming & Scripting	C, C++, Java, VHDL, Haskell, Javascript, Perl, Python
Debugging	GDB
Simulators	Gem5 & Simics full-system simulators, Garnet NoC simulator, QEMU
Architectural Analysis	SPEC & PARSEC benchmarks, Pin, Simpoint
Version Control	Git, SVN
Languages	Greek, English

PUBLICATIONS

2012 NoCAlert: An on-line and real-time fault detection mechanism for network-on-chip architectures, **A. Prodromou**, A.Panteli, C. Nicopoulos and Y. Sazeides

2011 Thermal characterization of cloud workloads on a power-efficient server-on-chip, D. Milojevic, S. Idgunji, D. Jevdjic, E. Ozer, P. Lotfi-Kamran, A. Panteli, **A. Prodromou**, C. Nicopoulos, D. Hardy, B. Falsafi and Y. Sazeides

AWARDS AND ACCOMPLISHMENTS

2013 **Powell Fellowship** for academic years 2013–2016, UCSD Computer Science and Engineering.

2012 **HiPEAC Paper Award** for the paper titled "NoCAlert: An on-line and real-time fault detection mechanism for network-on-chip architectures".

2011 **Best Senior Design Project Award** in the Department of Electrical and Computer Engineering, University of Cyprus for academic year 2010-2011.