Processor	
Cores	8 @ 3.2GHz
Width	4 wide out-of-order

Caches	
L1 I-Cache(private)	64KB, 2 way, 4 cycles
L1 D-Cache (private)	16KB, 4 way, 4 cycles
L2 Cache (shared)	8MB, 16 way, 11 cycles

HBM2	
Bus Frequency	1 GHz (DDR 2 GHz)
Bus Width	128 bits
Channels	8
Ranks	1 per Channel
Banks	16 per Rank
Row Buffer Size	8KB (open-page policy)
tCAS-tRCD-tRP-tRAS	7-7-7-17 (mem. cycles)

DDR4	
Bus Frequency	800 MHz (DDR 1.6 GHz)
Bus Width	64 bits
Channels	4
Ranks	1 per Channel
Banks	16 per Rank
Row Buffer Size	8KB (open-page policy)
tCAS-tRCD-tRP-tRAS	11-11-11-28 (mem. cycles)