Available online at www.sciencedirect.com
ScienceDirect
Solid-State Electronics 51 (2007) 806–811
SOLID-STATE ELECTRONICS
www.elsevier.com/locate/sse

Modeling of retention characteristics for metal and semiconductor nanocrystal memories

Weihua Guan, Shibing Long, Ming Liu *, Qi Liu, Yuan Hu, Zhigang Li, Rui Jia

Laboratory of Nanofabrication and Novel Device Integration, Institute of Microelectronics, Chinese Academy of Sciences, No. 3, West Road of BeiTuCheng, ChaoYang District, Beijing 100029, China

Received 25 December 2006; received in revised form 22 March 2007; accepted 27 March 2007
Available online 15 May 2007

The review of this paper was arranged by Prof. A. Zaslavsky

Abstract

The charge retention characteristics of metal nanocrystal (MNC) and semiconductor nanocrystal (SNC) memory devices are comparatively studied in this paper. A charge retention model is proposed, taking into account the quantum confinement effect, to account for the better retention characteristics of metal nanocrystal memory observed in the experiment. Simulation results are in good agreement with experimental data, which confirms the validity of this model. The impact of the nanocrystal size, tunneling dielectric materials (especially high-κ dielectrics), and tunneling dielectric thickness on the retention characteristics are all investigated for both the metal nanocrystals and the semiconductor nanocrystals.

PACS: 72.20.Jv; 73.63.Kv; 85.30.De

Keywords: Device modeling; Nanocrystal memory; Quantum confinement; Retention characteristic

1. Introduction

Flash memory based on silicon nanocrystals (NC-Si) was proposed to meet the challenge of the scaling limits of traditional floating gate non-volatile memory (NVM) by Tiwari et al. [1]. The overall performance of such devices is improved due to discrete charge storage. However, there is an inherent contradiction between the program/erase (P/E) time and charge retention time. To enable fast P/E operation, a thinner tunneling dielectric is needed. But at the same time, a thicker tunneling oxide is favorable to achieve an acceptable retention time (e.g., 10 years). In order to overcome this problem, most of the recent research has focused on various materials and structures of tunneling and control dielectrics [2–6], including the adoption of high-dielectric constant (high-κ) materials. There is, in fact, another way that can also solve the contradiction. By engineering the shape (either the depth or the structure) of the potential well where the charges are stored, an asymmetrical barrier between the storage nodes and the substrate can be created, and thus it is possible to get a small barrier for writing and a large barrier for retention. Ge/Si hetero-nanocrystal can be used to achieve this [7]. Unfortunately, it is difficult to control the formation of this hetero-nanocrystal structure. For metal nanocrystal memory, however, which was introduced by Liu et al. [8], it is not the case. The fabrication process is not complex and the nanocrystals are formed by self-assembly. The availability of various metal work functions makes it easy to tune the depth of the potential well.

Recent research has shown that metal nanocrystals (MNC) have better performance than semiconductor

* Corresponding author. Tel.: +86 10 62007699; fax: +86 10 62055666.
E-mail address: liuming@ime.ac.cn (M. Liu).

0038-1101/$ - see front matter © 2007 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2007.03.017

nanocrystals (SNC), such as a longer retention time [9]. Previous works have presented several theoretical models concerning write, erase, and retention characteristics for SNC memory [10–12], but there is no detailed theoretical model of MNC memory by far. In this work, we present a charge retention model, which compares the difference between MNC and SNC, taking into account the quantum confinement effect on the energy level of the nanocrystal. The effect of nanocrystal size and tunneling oxide thickness, as well as the tunneling materials on charge retention characteristics are investigated and discussed for both MNC and SNC.

2. Charge retention modeling

The schematic cross-sectional structure of nanocrystal memory device discussed in this paper is shown in Fig. 1. Here we define some physical parameters that will be used in the following discussion: ε_{tun} and ε_{con} are the permittivity of tunneling and control dielectric; t_{tun} and t_{con} are the thickness of tunneling dielectric and control dielectric; ε_{nc} and d_{nc} are the permittivity and diameter of the nanocrystal, respectively.

2.1. Quantum confinement effect

When the size of the nanocrystals comes into the range of a few nanometers, the Coulomb blockade effect [13] and the quantum confinement effect becomes a significant phenomenon. The Coulomb blockade effect raises the electrostatic potential of the nanocrystal while the quantum confinement effect shifts the nanocrystal energy band edge upward and as a result, the energy band offset between the nanocrystal and the surrounding dielectric is reduced [10]. In this study, we have focused our attention on the quantum confinement effect which impacts MNC and SNC differently. Since there are several physical differences betweens MNC and SNC such as the energy band structure, we should separately investigate the impact of quantum confinement effect on the effective barrier height for both kinds of nanocrystals.

For MNC, according to Kubo theory [14], the quantum confinement effect makes the continuous energy band of MNC split into separated energy levels. The average energy spacing δ can be calculated as:

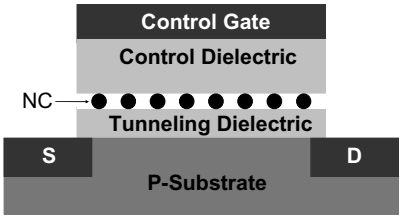

Fig. 1. Schematic cross-sectional structure of p-substrate memory device using nanocrystals as floating gate. All nanocrystals are assumed to be in the same plane and have the same size.

$$\delta = 4E_F/(3N) \tag{1}$$

Here, E_F is the Fermi potential of the bulk metal. N is the total number of conductive electrons in the nanocrystal. The relationship between energy E and charge density n is given by:

$$E(n) = \frac{\hbar^2}{2m^*}(3\pi^2 n)^{2/3} \tag{2}$$

From Eqs. (1) and (2), we can calculate the splitting energy spacing δ for any given metal nanocrystal. Taking NC-Ni and NC-Au for example, using the parameters as follows: $E_{FNi} = 11.7$ eV, $E_{FAu} = 5.53$ eV [15] and $m^* = m_0$ (m_0 is the free electron mass: 9.1×10^{-31} kg), we can get the relation between δ (in eV) and the diameter d (in nm) for NC-Ni and NC-Au as follows (d is the diameter of MNC):

$$\delta_{Ni} = \frac{0.1639}{d_{Ni}^3} \tag{3}$$

$$\delta_{Au} = \frac{0.2388}{d_{Au}^3} \tag{4}$$

For SNC, the quantum confinement effect will result in widening of band gap and the upward shift of the conduction band minimum (CBM). Niquet et al. studied the electronic structure of Ge nanocrystals, using sp^3 tight binding method and the analytical law for the CBM, valid over the whole range of sizes, is derived as [16]:

$$E_C(d_{Ge}) = E_C(\infty) + \frac{11.8637}{d_{Ge}^2 + 2.391 d_{Ge} + 4.252} \tag{5}$$

Here, the energies are in eV, $E_C(\infty)$ is the conduction band minimum for bulk Ge, d_{Ge} is the diameter of NC-Ge in nm. Using the same form of Eq. (5), we fit the experimental data on the conduction band edge up-shift of NC-Si reported by van Buuren et al. [17] as follows:

$$E_C(d_{Si}) = E_C(\infty) + \frac{1.39}{d_{Si}^2 + 1.788 d_{Si} + 0.668} \tag{6}$$

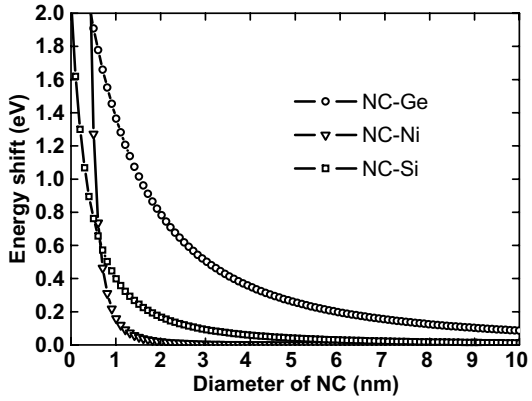

Fig. 2. The conduction band minimum up-shift of SNC and Fermi level up-shift of MNC as a function of nanocrystal size.

As shown in Fig. 2, the CBM up-shift of NC-Ge is larger than that of NC-Si, which indicates that the quantum confinement effect affects NC-Ge more than NC-Si. The Fermi level up-shift of NC-Ni is also demonstrated in Fig. 2. For nanocrystals of the same size larger than 2 nm, the Fermi level up-shift of MNC is much smaller than the CBM up-shift of SNC. This may be due to the fact that MNC contains a large number of electrons even when the nanocrystal size is small. As a result, the quantum confinement effect will have less impact on the MNC.

2.2. Discharging dynamics

In order to model the charge retention characteristics of the nanocrystal memory device, we should first make clear the charging and discharging mechanism.

During programming, a positive gate bias was applied and electrons were injected from the inverted substrate into the nanocrystals (NCs). In our model, electrons are assumed to be stored in the conduction band minimum for SNC and the Fermi level for MNC, respectively. The charge stored in the NCs will change the threshold voltage of the device, the magnitude of which can be described as [1]:

$$\Delta V_{\mathrm{th}} = \frac{Q}{\varepsilon_{\mathrm{tun}}}\left(t_{\mathrm{con}} + \frac{1}{2}\frac{\varepsilon_{\mathrm{tun}}}{\varepsilon_{\mathrm{nc}}}d_{\mathrm{nc}}\right) \tag{7}$$

In the equations above, Q is the charge density in the nanocrystal layer (C/cm^2). The other parameters are those defined at the beginning of this section.

During retention, a discharging current caused by the hole tunneling is not taken into account because of the relatively large barrier height at the tunneling interface for the hole. For electrons, there are three main discharging paths: discharging from NCs to the control gate, discharging from one NC to the adjacent nanocrystal, and discharging from NCs to the substrate. Since the control dielectric is always thicker than the tunneling dielectric, discharging current via the control dielectric can be neglected. The discharging current from one nanocrystal to the adjacent nanocrystal can also be neglected. This is reasonable due to the strong Coulomb block effect of the nanocrystal and the large spacing between nanocrystals. In our model, the discharging current during retention is dominated by electrons tunneling out from NCs to the substrate. Since the control gate is zero biased during retention and the number of charges stored in the nanocrystals is limited, the electric field in the tunneling dielectric is low. Therefore, the tunneling mechanism is direct tunneling.

Based on the above discussion, a one-dimensional (1D) retention model, considering vertical discharge via direct tunneling, is presented. Fig. 3 shows the schematic energy band diagram of MNC and SNC memory during retention.

According to our discussion above, the density of discharge current dominated by direct tunneling from NC to the substrate can be expressed as [18]:

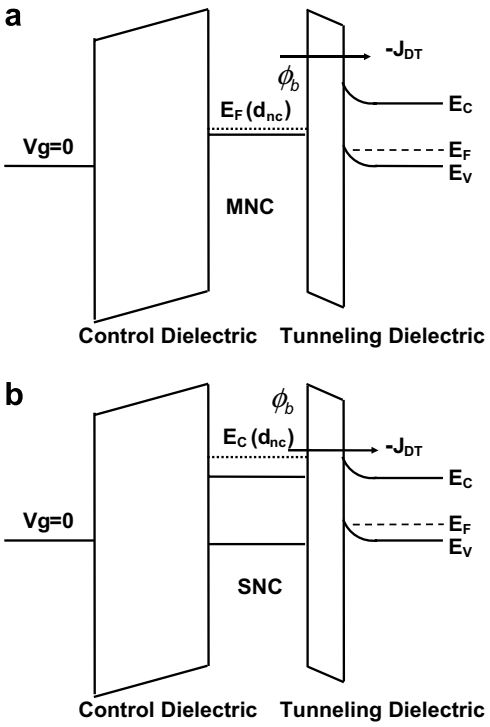

Fig. 3. Schematic energy band diagram of MNC and SNC memory during retention, demonstrating the reduced effective barrier offset caused by quantum confinement effect. (a) The up-shift of Fermi level was little for metal nanocrystals. (b) The up-shift of CBM is significant and the effective barrier offset is reduced notably for semiconductor nanocrystals.

$$J_{\mathrm{DT}} = AE_{\mathrm{tun}}^2 \exp\left\{-\frac{B}{E_{\mathrm{tun}}}\left[\phi_{\mathrm{b}}^{3/2} - (\phi_{\mathrm{b}} - qV_{\mathrm{tun}})^{3/2}\right]\right\} \tag{8}$$

Here, $A = q^3 m_0/(16\pi^2\hbar m_{\mathrm{tun}}^* \phi_{\mathrm{b}})$, $B = 4\sqrt{2m_{\mathrm{tun}}^*}/(3\hbar q)$, q is the charge of a single electron, m_0 the mass of a free electron, $\hbar$ the reduced Planck's constant, m_{tun}^* the effective mass of electron in tunneling dielectric, ϕ_{b} the barrier height from NC to substrate which can be given as: $\phi_{\mathrm{b0}} - \phi_{\mathrm{up}}$, ϕ_{b0} is the barrier offset for bulk material, and ϕ_{up} is the energy band up-shift when considering the quantum confinement effect. V_{tu} is the voltage drop across tunneling dielectric layer which can be written as $E_{\mathrm{tun}}t_{\mathrm{tun}}$. E_{tun} is the electrical field in tunneling dielectric. In our model, we approximately describe each nanocrystal and the substrate area underneath as a plate capacitor and the electric field caused by a neighboring NC is neglected. As a result, the electrical field intensity is expressed as:

$$E_{\mathrm{tun}} = \frac{Q}{\varepsilon_{\mathrm{tun}}R} \tag{9}$$

Here, R is the nanocrystal coverage ratio. With electrons tunneling out of the nanocrystal layer, the charge density Q decreases and we have the following relationship between Q and J_{DT}:

$$\frac{\mathrm{d}Q}{\mathrm{d}t} = -J_{\mathrm{DT}}(t) \tag{10}$$

Notice that Eqs. (9) and (10) provide an intuitive understanding of the charge retention characteristics of nanocrystal memory. When the device programming process was finished at $t = 0$, the programmed charge density in the NCs had its maximum value. According to Eq. (9), the electrical field in the tunneling dielectric is the strongest. As a result, the discharging current in the largest and the charge loss is the fastest at the beginning of the retention period. With electrons tunneling out of NCs, the charge density Q as well as the electrical field decrease. Thus the process of charge loss becomes slower and slower.

3. Results and discussion

The nanocrystal coverage R in Eq. (9) and the initial value of the charge density $Q(0)$ at $t = 0$ as the boundary condition for Eq. (10) can be extracted from the experimental retention data. Using Eqs. (8)–(10), we can numerically calculate the transient charge density Q and thus the threshold voltage shift. Fig. 4 shows the experimental and the simulated ΔV_{th} as a function of time. The experimental data was obtained from the work of Lee and Kwong [19]. As it is shown, the simulated results are in good agreement with the experimental data, which validates the physical retention model described in Section 2.

Fig. 5 shows the retention time versus the size of nanocrystals for various nanocrystal materials. Note that the retention time we derived from the simulation result is defined as the time when 50% of the charges escaped from the nanocrystals. For the same nanocrystal size, NC-Au and NC-Ni show better retention performance than NC-Si and NC-Ge. There are two reasons for this result: one is the higher electron barrier height from MNC to the substrate. Another reason is the weaker quantum confinement effect of MNC, which is ignored by Lee and Kwong [19]. In fact, because of the up-shift of the conduction band, even if the electron barrier was the same for bulk metal and semiconductor materials, the retention performance of MNC can still be better than that of SNC. For metal nanocrystal memory, the longer retention time of NC-Au than NC-Ni is the result of the larger work function and thus the higher barrier height. It is also found that the retention time for both NC-Au and NC-Ni changes a little when nanocrystal size changes from 2 to 10 nm. This is due to the weak quantum confinement effect in this size range for MNC as shown in Fig. 2. For semiconductor nanocrystal memory, when the size of SNC is small (<5 nm), the retention time increase notably with the increase of nanocrystal size. And when the size of SNC is relatively large, the retention time reaches a stable stage. NC-Ge shows a worse retention performance in the small size region and a little better when the size is large. This can be explained by the impact of the quantum confinement effect on the energy band structure shown in Fig. 2. The difference of CBM up-shift between NC-Ge and NC-Si decreases from 0.75 eV for 2 nm nanocrystal down to 0.25 eV for 5 nm nanocrystal. In other words, when the nanocrystal size increases, the difference of conduction band up-shift becomes small. Since ϕ_b for bulk Ge (3.23 eV) is a little larger than bulk Si (3.15 eV), the effective barrier height of NC-Ge is a little larger than NC-Si in the large size range where the quantum confinement effect has little impact. As a result, NC-Ge shows a little better retention performance than NC-Si.

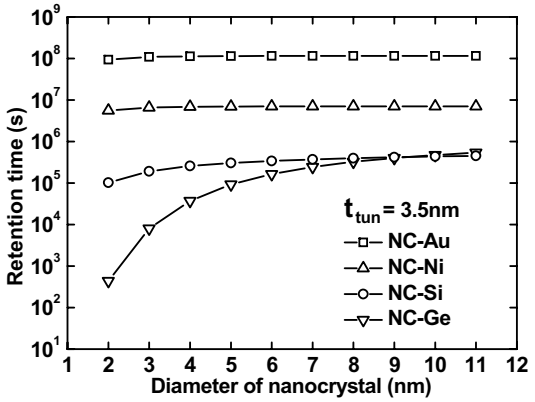

Fig. 5. Retention time for various nanocrystal materials and the impact of the size of nanocrystal on retention performance. The parameters used in simulation are as follows: R=30%, $\Delta V_{th}(0) = 1$ V, $t_{tun} = 3.5$ nm, $t_{con} =$ 15 nm. The tunneling dielectric is SiO_2.

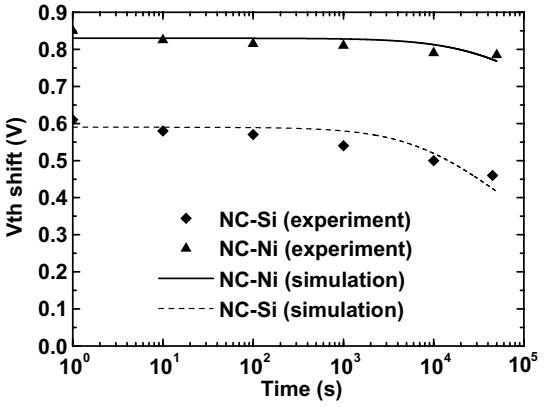

Fig. 4. Experimental and simulated threshold shift as a function of time.

Fig. 6 demonstrates the retention time as a function of tunneling dielectric thickness. As can be seen, for the same tunneling dielectric thickness, metal nanocrystal memory shows better charge retention characteristics. A tunneling oxide of 3.6 nm is thick enough to guarantee the 10 years retention for NC-Au. However, due to the stronger quantum confinement effect, SNC requires a thicker tunneling oxide to achieve this goal. Therefore, memory structure employing metal nanocrystals can provide a greater margin for the tradeoff between fast P/E operation and long retention time.

Recently, high-κ dielectric material has received great research interest for the application of nanocrystal memory [2–4]. For NC memories, the use of high-κ materials as tunneling dielectrics will have two major effects on device retention performance. The first is the different energy bar-

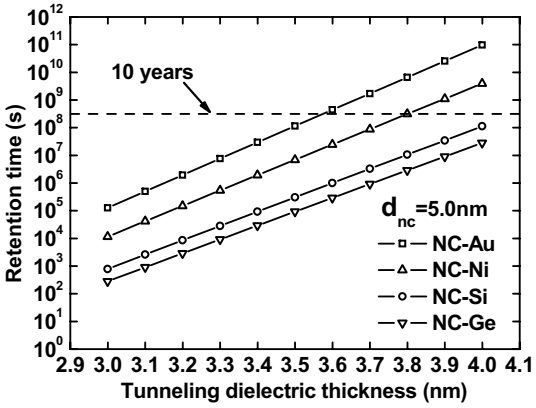

Fig. 6. The dependence of retention time on tunneling dielectric thickness for MNC and SNC. The parameters used in simulation are as follows: $R = 30\%$, $\Delta V_{th}(0) = 1$ V, $d_{nc} = 5.0$ nm, $t_{con} = 15$ nm. The tunneling dielectric is SiO_2.

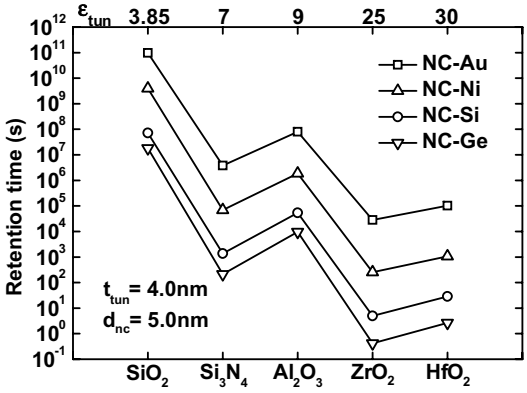

Fig. 7. The impact of tunneling dielectric and nanocrystal material on the device retention characteristic. The parameters used in simulation are as follows: $R = 30\%$, $\Delta V_{th}(0) = 1$ V, $d_{nc} = 5.0$ nm, $t_{tun} = 4.0$ nm, $t_{con} = 15$ nm.

rier height at the interface between nanocrystal and high-κ material. The second effect is caused by the different dielectric constant (ε) with respect to SiO_2, which contributes to the decrease of the electrical field according to Eq. (9). These two impacts are summarized in Table 1. It should be noted that besides the influences of the energy barrier height and dielectric constant, effective mass of electron in tunneling dielectric (m^*) is another important parameter which may have impact on the tunneling current and m^* is dependent on the material. For example, Hou et al. indicates a lower effective mass for HfO_2 dielectric [20]. In this study, we make the assumption that m^* is the same ($0.5m_0$) with various tunneling dielectrics for simplicity.

The impact of tunneling dielectric and nanocrystal material on the device retention characteristic is shown in Fig. 7. For a specific high-κ material, MNC memory shows better retention. However, due to the different energy barrier height at the interface of NC/high-κ materials, there seems to be no obvious relationship between the permittivity of high-κ material and the retention time. The retention time is the collective result of barrier height at the interface of NC/ high-κ materials and the permittivity of high-κ dielectric. However, according to Eq. (9), when all the other parameters are unchanged, a larger ε_{tun} can reduce the electrical field in the tunneling layer during retention and thus improve the device retention performance. As a matter of fact, as shown in Fig. 8, with the same equivalent oxide

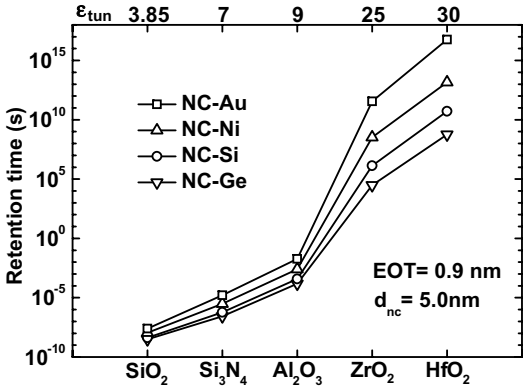

Fig. 8. Improvement of charge retention characteristics by using high-κ tunneling dielectric. Various combination of different nanocrystal and high-κ materials are shown. The parameters used in simulation are as follows: $R = 30\%$, $\Delta V_{th}(0) = 1$ V, $d_{nc} = 5.0$ nm, EOT = 0.9 nm, $t_{con} = 15$ nm.

Table 1
The energy barrier height for electrons at NC/high-κ dielectric interface and the permittivity of tunneling dielectric used in simulation

	SiO_2 ($\varepsilon = 3.85$)	Si_3N_4 ($\varepsilon = 7$)	Al_2O_3 ($\varepsilon = 9$)	ZrO_2 ($\varepsilon = 25$)	HfO_2 ($\varepsilon = 30$)
Si	3.15	2	2.3	1.4	1.5
Ge	3.25	2.1	2.4	1.5	1.6
Ni	3.6	2.35	2.65	1.75	1.85
Au	4.0	2.75	3.05	2.15	2.25

All data are in eV.

thickness (EOT), high-κ tunneling materials can greatly improve the charge retention performance, especially when combined with high work function metal nanocrystals (e.g., NC-Au in our case). This is consistent with the experimental observation [19]. Therefore, MNC memory is a promising candidate for the application of non-volatile memories.

4. Conclusions

A theoretical model and numerical calculations concerning the retention characteristics of metal and semiconductor nanocrystal non-volatile memory are presented, taking into consideration the different impact of the quantum confinement effect on the energy band structure. Simulation results are in good agreement with experimental data. According to the model, due to the less disturbance of the Fermi level caused by quantum confinement, MNC memory devices have a better retention performance than SNC memory. It is also found that when combined

with high-κ tunneling dielectrics, MNC memory can improve the retention performance greatly. As a result, nanocrystal memory devices employing high work function metal nanocrystal and high-κ gate dielectrics are promising for the application of non-volatile memories.

Acknowledgements

The authors would like to thank Mr. Jie Ma for useful discussion. This work is partly supported by National Basic Research Program of China (973 Program) under Grant No.: 2006CB302706 and National Natural Science Foundation of China under Grant Nos.: 90607022, 90401002, and 60506005.

References

[1] Tiwari S, Rana F, Hanafi H, Hartsten A, Crabbe EF, Chan K. Appl Phys Lett 1996;68:1377–9.
[2] Chen JH, Wang YQ, Yoo WJ, Yeo YC, Samudra G, Chan DS, et al. IEEE Trans Electron Devices 2004;51:1840–8.
[3] Punchaipetch P, Uraoka Y, Fuyuki T, Tomyo A, Takahashi E, Hayashi T, et al. Appl Phys Lett 2006;89:093502.
[4] Yuan CL, Darmawan P, Setiawan Y, Lee PS, Ma J. Appl Phys Lett 2006;89:043104.
[5] Baik SJ, Lim KS. Appl Phys Lett 2003;81:5186–8.
[6] Liu Y, Dey S, Tang S, Kelly DQ, Sarkar J, Banerjee SK. IEEE Trans Electron Devices 2006;53:2598–602.
[7] Zhao D, Zhu Y, Li R, Liu J. IEEE Trans Nanotechnol 2006;5:37–41.
[8] Liu Z, Lee C, Narayanan V, Pei G, Kan EC. IEEE Trans Electron Devices 2002;49:1606–13.
[9] Zhao D, Zhu Y, Liu J. Solid State Electron 2006;50:268–71.
[10] She M, King T-J. IEEE Trans Electron Devices 2003;50:1934–40.
[11] Koh BH, Kan EWH, Chim WK, Choi WK, Antoniadis DA, Fitzgerald EA. J Appl Phys 2005;97:124305.
[12] Compagnoni CM, Ielmini D, Spinelli AS, Lacaita AL. IEEE Trans Electron Devices 2005;52:569–76.
[13] Likharev Konstantin K. IEEE Proc 1999;97:606–32.
[14] Kubo Ryogo. J Phys Soc Jpn 1962;17:975–86.
[15] Ashcroft NW, Mermin ND. Solid state physics. Orlando: Saunders College Publishing; 1976.
[16] Niquet YM, Allan G, Delerue C, Lannoo M. Appl Phys Lett 2000;77:1182–4.
[17] van Buuren T, Dinh LN, Chase LL, Siekhaus WJ, Terminello LJ. Phys Rev Lett 1998;80:3803–6.
[18] Schuegraf KF, Hu C. Proc IEEE Int Reliab Phys Symp 1993.
[19] Lee JJ, Kwong DL. IEEE Trans Electron Devices 2005;52:507–11.
[20] Hou YT, Li MF, Yu HY, Kwong D-L. IEEE Electron Devices Lett 2003;24:96–8.